OKI Semiconductor

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ML7037-003

Dual Echo Canceler & Noise Canceler with Dual Codec for Hands-Free

GENERAL DESCRIPTION

The ML7037-003 is an IC device developed for portable, handsfree communication with built-in line echo canceler, acoustic echo canceler, and transmission signal noise canceler. Built-in to the voice signal interface is a PCM CODEC for the analog interface on the acoustic-side, and another PCM CODEC for the analog interface on the line-side. On the line-side, in addition to the analog interface, there is also a μ-law PCM/16-bit linear digital interface.
Equipped with gain and mute controls for data transmission and reception, a μ-law PCM/16-bit linear digital interface for memo recording and message output, and transfer clock and sync clock generators for digital communication, this device is ideally suited for a handsfree system.

FEATURES

• Single 3.3 V Power Supply Operation (3.0 to 3.6 V) [with built-in regulator to generate internal power supply]
• Built-in 2-channel (line and acoustic) echo canceler
  Echo attenuation : 35 dB (typ.) for white noise
  Cancelable echo delay time :
    Single echo canceler mode (only an acoustic echo canceler is enabled)
      Tacoud= 64 ms (max)
    Dual echo canceler mode (both of an acoustic and line echo cancelers are enabled)
      Tacoud = 64 ms Tlined = 20 ms
• Built-in transmission signal noise canceler
  Noise attenuation : 13 dB (typ.) for white noise
• Built-in 2-channel CODEC's
• Analog input gain amp's (Acoustic side = 2 stages; Line-side = 1 stage)
• Analog output configuration: Push-pull drive (can drive a 2.0 kΩ load)
• Receive-side ALC (Auto Level Controler)
• Programmable Gain/Mute
• A slope filter on transmit side
• 16 GPI's and 8 GPO's
• Speech digital interface coding formats : μ-law PCM (G.711 [64kbps]), 16-bit linear (2's complement)
• Speech digital interface sync formats : Long-frame-sync, short-frame-sync
• PCM shift clocks (BCLK)
  Clock slave mode : 64kHz to 2.048MHz (μ-law PCM) / 128kHz to 2.048MHz (16bit Linear PCM)
  Clock master mode : 64kHz (μ-law PCM) / 128kHz (16bit Linear PCM)
• Master clock frequency : 12.288 MHz (crystal unit the ML7037's built-in driving circuit for a crystal unit or a crystal oscillator)
• Transmission signal equalizer
• Package : 64-pin plastic TQFP (TQFP64-P-1010-0.50-K) (ML7037-003TB)

* This is a digest version of the ML7037-003 datasheet. Ask an OKI sales for a full version before you start actual designing activities.

BLOCK DIAGRAM

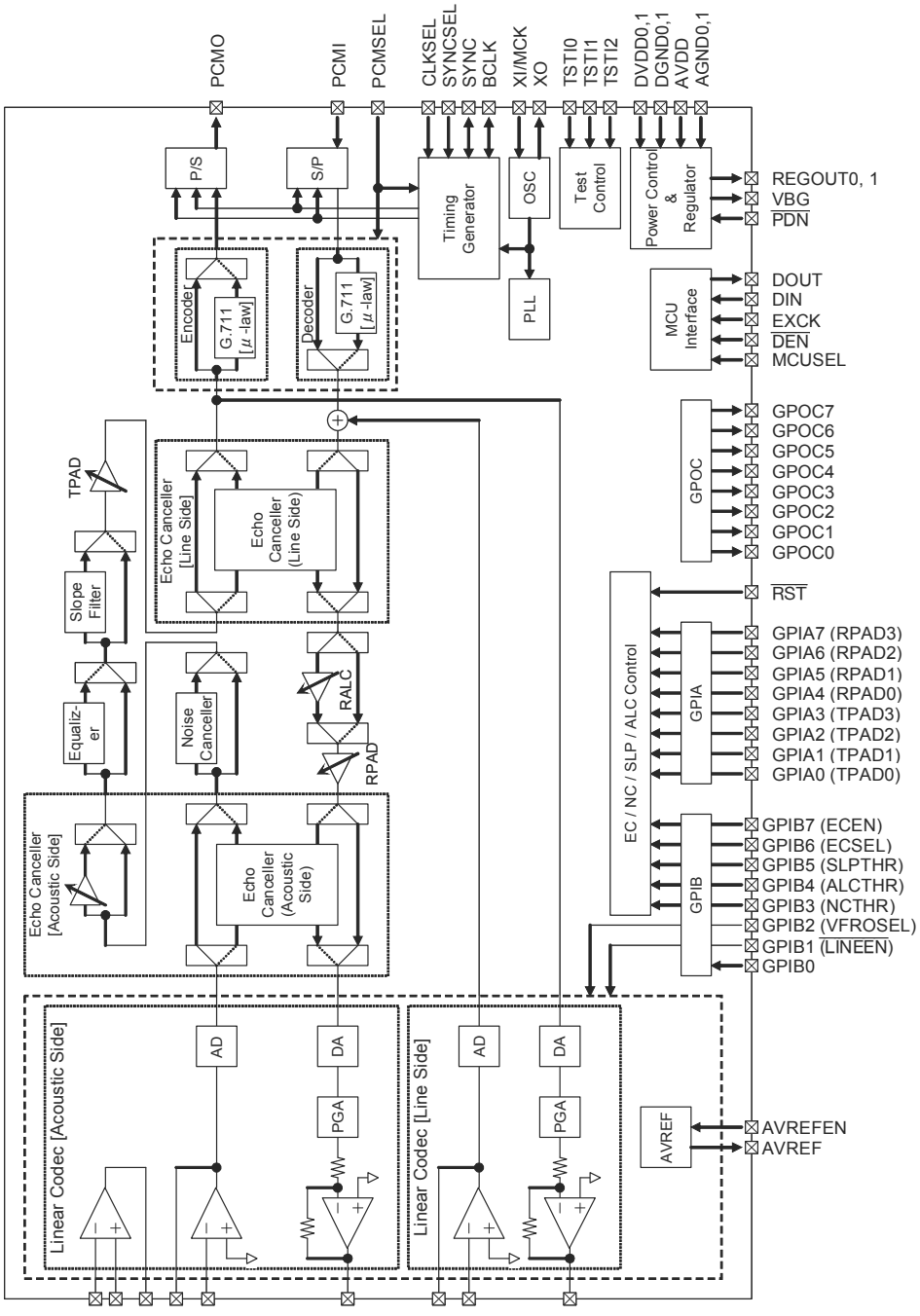


Figure 1

PIN CONFIGURATION (TOP VIEW)

64-Pin Plastic TQFP

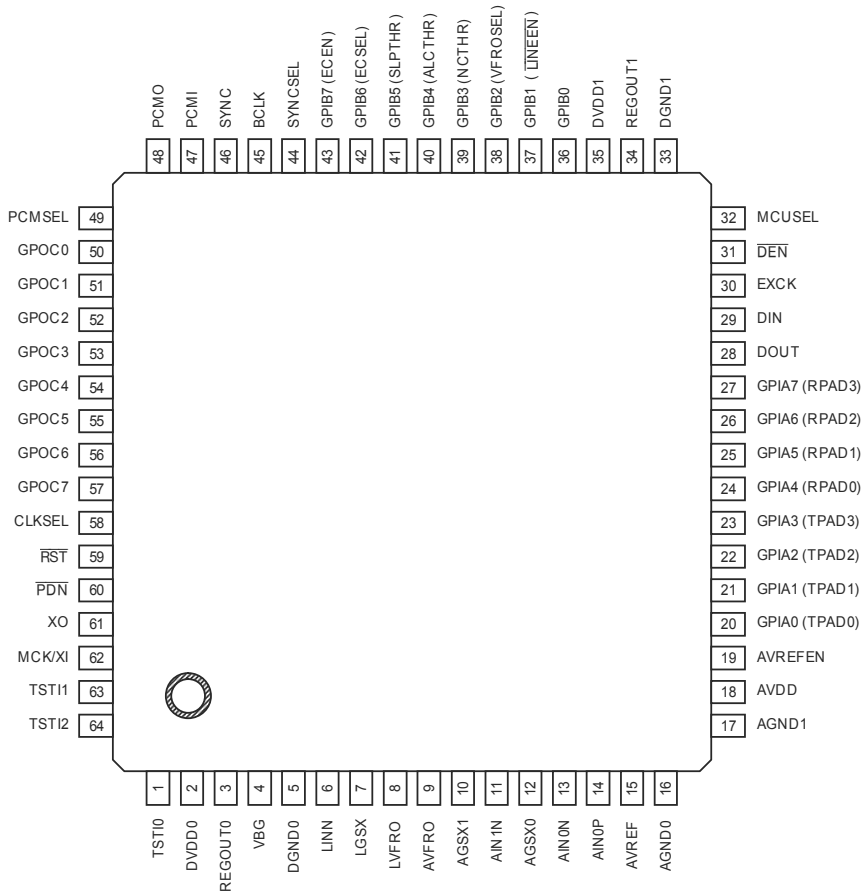


Figure 2

PIN OVERVIEW

Pin Number	Pin Name	I/O	$\overline{PDN}$="0"	Descriptions
1	TSTI0	I	I	Test pin0
2	DVDD0	-	-	Digital power supply pin
3	REGOUT0	-	-	Regulatoroutput pin
4	VBG	-	-	Regulatorreference voltage output pin
5	DGND0	-	-	Digital ground pin
6	LINN	I	I	Line-sideanalog input pin (reversed input pin for an analog input amplifier)
7	LGSX	O	Hi-Z	Line-sideanalog output pin (output pin from an analog input amplifier)
8	LVFRO	O	L (*1) 1.4V apporx(*2)	Line-sideanalog output pin
9	AVFRO	O	L (*1) 1.4V apporx(*2)	Acoustic-sideanalog output pin
10	AGSX1	O	Hi-Z	Acoustic-sideanalog output pin (output pin from an analog input amplifier)
11	AIN1N	I	I	Acoustic-sideanalog input pin (reversed input pin for an analog input amplifier)
12	AGSX0	O	Hi-Z	Acoustic-sideanalog output pin (output pin from an analog input amplifier)
13	AIN0N	I	I	Acoustic-sideanalog input pin (reversed input pin for an analog input amplifier)
14	AIN0P	I	I	Acoustic-sideanalog input pin (reversed input pin for an analog input amplifier)
15	AVREF	O	L (*1) 1.4V apporx(*2)	Output pin for analog signal ground level
16	AGND0	-	-	Analog ground pin
17	AGND1	-	-	Analog ground pin
18	AVDD	-	-	Analog power supply pin
19	AVREFEN	I	I	Input pin to switch enabling/disabling AVREF during power-down
20	GPIA0 (TPAD0)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to tune volume of transmit speech signals
21	GPIA1 (TPAD1)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to tune volume of transmit speech signals
22	GPIA2 (TPAD2)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to tune volume of transmit speech signals

（Note）
(*1):Shows the output state when the AVREFEN pin is logic '0'.
(*2):Shows the output state when the AVREFEN pin is logic '1'.

Pin Number	Pin Name	I/O	$\overline{PDN}$="0"	Descriptions
23	GPIA3 (TPAD3)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to tune volume of transmit speech signals
24	GPIA4 (RPAD0)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to tune volume of receive speech signals
25	GPIA5 (RPAD1)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to tune volume of receive speech signals
26	GPIA6 (RPAD2)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to tune volume of receive speech signals
27	GPIA7 (RPAD3)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to tune volume of receive speech signals
28	DOUT	O	Hi-Z	Data output pin for MCU interface
29	DIN	I	I	Data input pin for MCU interface
30	EXCK	I	I	Clock input pin for MCU interface
31	$\overline{DEN}$	I	I	Data enable input pin for MCU interface
32	MCUSEL	I	I	Input pin to switch between MCU interface enabled and disabled
33	DGND1	-	-	Digital ground pin
34	REGOUT1	-	-	Regulatoroutput pin
35	DVDD1	-	-	Digital power supply pin
36	GPIB0	I	I	General-purpose input port pin
37	GPIB1 ($\overline{LINEEN}$)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to switch between enabling and disabling of line-side analog interface
38	GPIB2 (VFROSEL)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to select output signals from AVFRO/LVFRO
39	GPIB3 (NCTHR)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to select noise canceler mode between normal mode and through mode

Pin Number	Pin Name	I/O	$\overline{PDN}$="0"	Descriptions
40	GPIB4 (ALCTHR)	I	I	General-purpose input port pin <Primary function> General-purpose input port pin <Secondary function> Input pin to select ALC mode between normal mode and through mode
41	GPIB5 (SLPTHR)	I	I	General-purpose input port pin <Primary function> General-purpose input port pin <Secondary function> Input pin to select slope filter mode between normal mode and through mode
42	GPIB6 (ECSEL)	I	I	General-purpose input port pin <Primary function> General-purpose input port pin <Secondary function> Input pin to select echo canceler mode between single echo canceler mode and dual echo canceler mode
43	GPIB7 (ECEN)	I	I	General-purpose input port pin <Primary function> General-purpose input port pin <Secondary function> Input pin to switch between disabling and enabling echo canceler
44	SYNCSEL	I	I	Input pin to select between long frame sync and short frame sync
45	BCLK	I/O	L (*1) I (*2)	Shift clock input pin for PCM interface
46	SYNC	I/O	L (*1) I (*2)	Sync clock input pin for PCM interface
47	PCMI	I	I	line-side PCM data input pin
48	PCMO	O	Hi-Z	line-side PCMdata output pin
49	PCMSEL	I	I	Input pin to select speech digital interface coding format between 16bit Linear PCM and μ-law PCM
50	GPOC0	O	L	General-purpose output port pin
51	GPOC1	O	L	General-purpose output port pin
52	GPOC2	O	L	General-purpose output port pin
53	GPOC3	O	L	General-purpose output port pin

(Note)
(*1):Shows the output state when the CLKSEL-pin is logic '0'.
(*2):Shows the output state when the CLKSEL-pin is logic '1'.

Pin Number	Pin Name	I/O	$\overline{PDN}$="0"	Descriptions
54	GPOC4	O	L	General-purpose output port pin
55	GPOC5	O	L	General-purpose output port pin
56	GPOC6	O	L	General-purpose output port pin
57	GPOC7	O	L	General-purpose output port pin
58	CLKSEL	I	I	Input pin to select between clock slave mode and clock master mode for PCM interface
59	$\overline{RST}$	I	I	Reset pin
60	$\overline{PDN}$	I	I	Power-down pin
61	XO	O	H	Ouput pin to connect a crystal unit for master clock
62	MCK/XI	I	I	Input pin to connect a crystal unit for master clock Master clock input pin
63	TSTI1	I	I	Test pin1
64	TSTI2	I	I	Test pin2

PIN FUNCTIONAL DESCRIPTION

AIN0N, AIN0P, AGSX0, AIN1N, AGSX1

These are the acoustic analog input and level tuning pins. The AIN0N pin and the AIN1N pin are connected to the inverting input of the internal amp (AMP2、AMP1), and the AIN0P pin is connected to the non-inverting input of the internal amp (AMP2). The AGSX0 pin and the AGSX1 pin are connected to the internal amp (AMP2、AMP1). For the way to tune the level, refer to Figure 3 Analog Interface.
During power-down mode ($\overline{PDN}$ pin = logic '0' or SPDN-bit [CR0-B7] = '1'), the AGSX0 pin and the AGSX1 pin go to a high impedance state.

(Note) When the acoustic side LSI-internal amplifier (AMP2) is not used, connect the AIN0P pin and the AVREF pin and short the AIN0N pin and the AGSX0 pin.
(Note) Please refer to the application circuit example when the acoustic side LSI-internal amplifier (AMP2) is used as a single-end input.

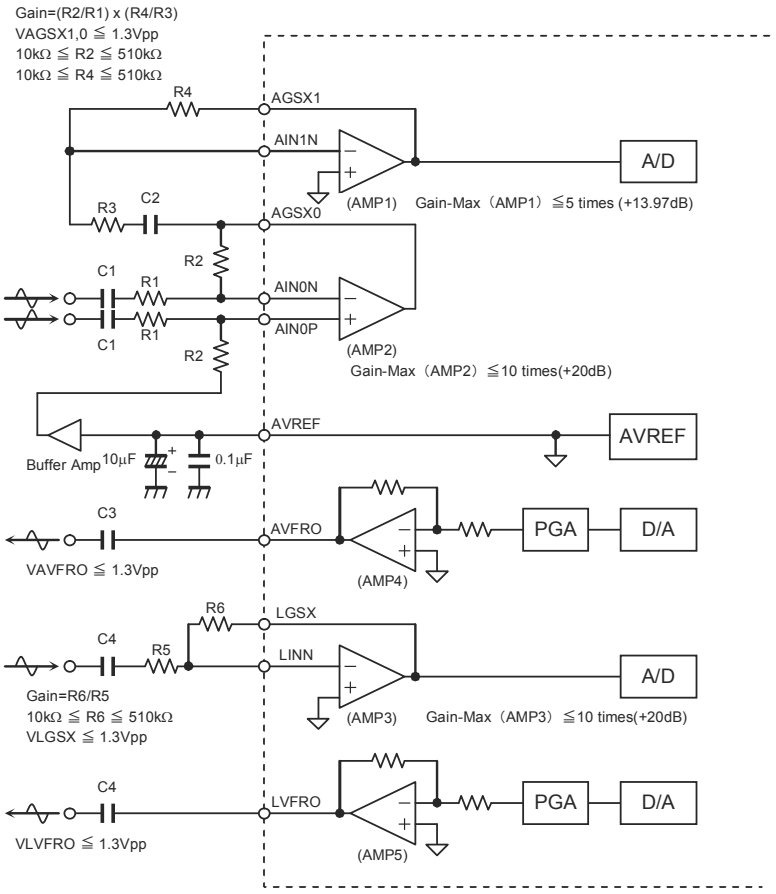


Figure 3 Analog Interface

LINN, LGSX

These are the line analog input and level tuning pins. The LINN pin is connected to the inverting input of the internal amp (AMP3) and the LGSX pin is connected to the output of the amp (AMP3). For level tuning, refer to Figure 3 Analog Interface.

During power-down mode ($\overline{PDN}$ pin = logic '0' or SPDN-bit [CR0-B7] = '1'), the LGSX pin goes to a high impedance state.

(Note) When the line side analog interface is not used, set the secondary function of the GPIB1 pin ($\overline{LINEEN}$) to logic '1' or set the $\overline{LINEEN}$-bit [CR0-B5] to '1', and short the LINN pin and the LGSX pin.

AVFRO, LVFRO

These are analog output pins respectively for acoustic-side and line-side. The AVFRO is connected to the output of the internal amp (AMP4), and the LVFRO is connected to the output of the internal amp (AMP5).

The output state of the AVFRO pin and the LVFRO pin can be selected between speech signal output and the AVREF level output (1.4V approx.) by the VFROSEL pin or by the AVFROSEL-bit [CR16-B1] and the LVFROSEL-bit [CR16-B0]. When the concerned pin or the concerned bit is logic '1', the AVFRO and/or the LVFRO pin outputs speech signals; when the concerned pin and the concerned bit is logic '0', the AVFRO pin and/or the LVFRO pin outputs the AVREF level (1.4V approx.).

During power-down mode ($\overline{PDN}$ pin = logic '0' or SPDN-bit [CR0-B7] = '1'), if the AVREFEN pin and the AVREFEN-bit [CR16-B7] are logic '0', the AVFRO pin and the LVFRO pin go to a high impedance state; and, if the AVREFEN pin or the AVREFEN-bit [CR16-B7] are logic '1', the pins output 1.4V approx..

(Note) If the AVREFEN pin and the AVREFEN-bit [CR16-B7] are logic '0', pop noises may occur on release and execution of power-down. If the AVREFEN pin and the AVREFEN-bit [CR16-B7] need to be logic '0' and still the pop noises have to be eliminated, it has to be fixed outside of this LSI.
To avoid the pop noises, set the AVREFEN pin or the AVREFEN-bit [CR16-B7] to logic '1' and let the AVREF and the analog output amps alive. Furthermore, the power-down should be released and executed having the output state of the AVFRO pin and the LVFRO pin the AVREF level.
In concrete, the power-down should be released while keeping the VFROSEL pin and by the AVFROSEL-bit [CR16-B1] and the LVFROSEL-bit [CR16-B0] to logic '0', and then change the VFROSEL pin or the AVFROSEL-bit [CR16-B1] and the LVFROSEL-bit [CR16-B0] to logic '1'.
And, the VFROSEL pin and the AVFROSEL-bit [CR16-B1] and the LVFROSEL-bit [CR16-B0] should be changed to logic '0' before the power-down execution.
Please note that the power supply current during the power-down would be I_{SS2} compliant (Please refer to the specification under the DC Characteristics to come in a later section.) if the AVREFEN pin or the AVREFEN-bit [CR16-B7] are logic '1'.

AVREF

This is the output pin for the analog signal ground level. The output voltage is approximately 1.4 V.

Insert a 10 µF bypass capacitor (a tantalum capacitor [recommendation] or an aluminum electrolytic capacitor) and a 0.1 µF capacitor (laminating ceramic type) in parallel between this pin and the AGND0 pin.

During power-down mode ($\overline{PDN}$ pin = logic '0' or SPDN-bit [CR0-B7] = '1') with the AVREFEN pin and the AVREFEN-bit [CR16-B7] to be logic '0', the AVREF pin outputs 0.0V.

During power-down mode ($\overline{PDN}$ pin = logic '0' or SPDN-bit [CR0-B7] = '1') with the AVREFEN pin or the AVREFEN-bit [CR16-B7] to be logic '1', the AVREF pin outputs 1.4V approx..

(Note) If you make use of the AVREF pin output externally in your system, it must be via a buffer amp.

AVREFEN

This is to select disabling and enabling the AVREF output during power-down mode ($\overline{PDN}$ pin = logic '0' or SPDN-bit [CR0-B7] = '1').

When this is logic '0', the AVREF pin is disabled (power-down state).

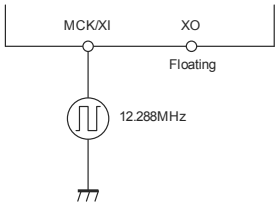
When this is logic '1', the AVREF pin is enabled, and the outputs of the AVREF, the AVFRO and the LVFRO become 1.4V approx..

This pin control is valid only during power-down.

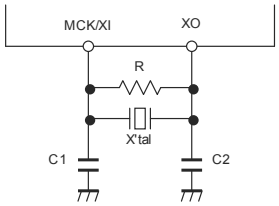
GPIB1 ($\overline{\text{LINEEN}}$)
This is a general-purpose input port pin.
This also works as a power-down control over the line-side analog interface as the secondary function.
When this pin is logic '0', the line-side analog interface is enabled; and, when this pin is logic '1', the line-side analog interface is powered-down (excluding the LVFRO output amp).
During power-down, the LVFRO outputs 1.4V approx..
When the MCUSEL pin is logic '1', this pin is automatically assigned with its secondary function.
When the MCUSEL pin is logic '0', this pin's function assignment follows the state of GPFB1-bit [GPCR1-B1].
(Note) The change of the input state to this pin is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 μs may not be reflected as the LSI behavior.
(Note) In an application where the line-side codec is never enabled, the LINN pin and the LGSX pin must be shorted.
(Note) The change of the enabled/disabled state of the line-side codec must be made during power-down state ($\overline{\text{PDN}}$ pin = logic '0' or SPDN-bit [CR0-B7] = '1') or during initial mode.

GPIB2 (VFROSEL)
This is a general-purpose input port pin.
This also works as the output state control over the AVFRO pin and the LVFRO pin as the secondary function.
When this pin is logic '0', they output the AVREF level (1.4V apporx.); and, when this pin is logic '1', they output speech signals.
When the MCUSEL pin is logic '1', this pin is automatically assigned with its secondary function.
When the MCUSEL pin is logic '0', this pin's function assignment follows the state of GPFB2-bit [GPCR1-B2].
(Note) When, during a call, the output state is changed or the reset is made, minor noises could happen due to an interruption at an arbitrary point in a sequence of PCM codes so that this output state selection and the reset are recommended to be made before a call as long as it is application-wise allowed.
(Note) The power-down execution and its release are recommended to be made when the AVFRO pin and the LVFRO pin are selected to output the AVREF level.
(Note) When this pin is not used, set this pin to logic '0'.

MCK/X1, XO
These are pins to connect a crystal unit, and the former is used as the master clock input pin as well. The clock frequency is 12.288 MHz.
During power-down mode ($\overline{\text{PDN}}$ pin = logic '0' or SPDN-bit [CR0-B7] = '1'), oscillation of the connected crystal unit is stopped.
After the release of the power-down, the connected crystal unit starts being oscillated, but the master clocks start being utilized within this LSI only after the steady oscillation waiting time (28ms approx.).
Refer to Figure 4 for an example application with an external clock and that with a crystal unit.



ex) External Clock



ex) Crystal Unit

X'tal (12.288MHz)	R	C1	C2
HC-49/U-S	1MΩ	10pF	10pF

Figure 4 Examples of external clock and crystal unit as a master clock

(Note) When a crystal unit is used, connect the unit and a feedback resistor of 1MΩ (R) between the MCK/XI and the XO. The appropriate values of capacitors (C1, C2) to be connected between the MCK/XI and GND and between the XO and GND are influenced by load capacitance of a crystal unit and PCB patterns so that they are recommended to be determined by asking a crystal unit vendor for a matching test.

SYNC
This is the 8 kHz sync clcok I/O pin for PCM interface. When the internal clock mode is selected by the CLKSEL pin = logic '0', this pin outputs 8kHz sync clocks synchronizing with the BCLK. When the external clock mode is selected by the CLKSEL pin = logic '1', input 8kHz clocks to this pin in synchronization with the BCLK.
When the SYNCSEL pin is logic '0', this pin outputs/expects to have sync clocks in a long frame sync timing; whereas, when the SYNCSEL pin is logic '1', this pin outputs/expects to have sync clocks in a short frame sync timing.

BCLK
This is the shift clock I/O pin for PCM interface. When the internal clock mode is selected by the CLKSEL pin = logic '0', this pin outputs 64kHz in μ-law PCM mode or 128kHz in 16-bit linear PCM mode. When the external clock mode is selected by the CLKSEL pin = logic '1', input shift clocks to this pin in synchronization with the SYNC. The input frequency must be between 64 kHz and 2048 kHz in μ-law PCM mode and 128 kHz and 2048 kHz in 16-bit linear PCM mode.

CLKSEL
This pin selects internal or external clock modes for PCM interface.
A logic '0' selects the internal clock mode where the SYNC pin and the BCLK pin output clocks so that this LSI could works as a clock master device in your system.
A logic '1' selects the external clock mode where this LSI needs the SYNC and the BCLK externally so that this LSI could works as a clock slave device in your system.
If PCM digital interface is not used, set this pin to a logic '0' to select internal clock mode.
(Note) The change of the input state of this pin must be made during power-down state ($\overline{PDN}$ pin = logic '0' or SPDN-bit [CR0-B7] = '1') or during initial mode.

SYNCSEL
This is the frame sync timing selection pin for PCM interface.
A logic "0" selects long frame sync timing, and a logic "1" selects short frame sync timing.
Refer Figure 5 to Figure8 for the timing.
(Note) The change of the input state of this pin must be made during power-down state ($\overline{PDN}$ pin = logic '0' or SPDN-bit [CR0-B7] = '1') or during initial mode.

PCMSEL
This is the coding format selection pin for PCM interface for the PCMO-pin output and the PCMI-pin input signal.
A logic '0' selects 16-bit linear PCM (2's complement) coding format, and a logic '1' selects μ-law PCM coding format.
The full scale table for both formats are shown below;

16bit Linear PCM (2's complement) Full Scale Table

Level	MSB															LSB
+ Full Scale	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
+1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
- Full Scale	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

μ-law PCM Full Scale Table

Level	MSB							LSB
+ Full Scale	1	0	0	0	0	0	0	0
+0	1	1	1	1	1	1	1	1
-0	0	1	1	1	1	1	1	1
- Full Scale	0	0	0	0	0	0	0	0

(Note) If PCM interface is not used, set this pin to a logic '0'.
(Note) The change of the input state of this pin must be made during power-down state ($\overline{PDN}$ pin = logic '0' or SPDN-bit [CR0-B7] = '1') or during initial mode.

PCMI

This is the receive PCM data input pin on the line-side. This input data is shifted at the falling edge of the BCLK. The PCM coding format can be selected between 16-bit linear PCM (2's complement) coding format and μ-law PCM coding format with the PCMSEL pin or the PCMSEL-bit [CR0-B4].

The PCM frame sync timing can be selected between a long frame sync and a short frame sync with the SYNCSEL pin.

Refer Figure 5 to Figure8 for the timing.

(Note) If this pin is not used, set this pin to a logic '0'.

(Note) The change of the input state of this pin must be made during power-down state ($\overline{PDN}$ pin = logic '0' or SPDN-bit [CR0-B7] = '1') or during initial mode.

PCMO

This is the receive PCM data output pin on the line-side. This output data is shifted at the rising edge of the BCLK. During power-down mode ($\overline{PDN}$ pin = logic '0' or SPDN-bit [CR0-B7] = '1') and initial mode or while effective PCM data bits are not being output, this pin goes to a high impedance state.

The PCM coding format can be selected between 16-bit linear PCM (2's complement) coding format and μ-law PCM coding format with the PCMSEL pin or the PCMSEL-bit [CR0-B4].

The PCM frame sync timing can be selected between a long frame sync and a short frame sync with the SYNCSEL pin.

Refer Figure 5 to Figure8 for the timing.

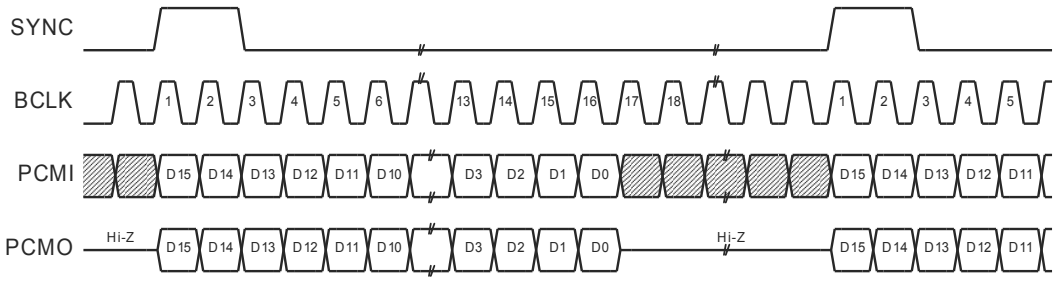


Figure 5 16-bit linear PCM timing chart (long frame sync)

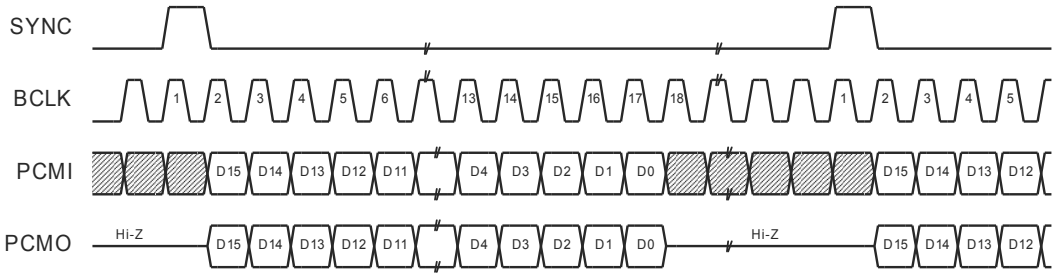


Figure 6 16-bit linear PCM timing chart (short frame sync)

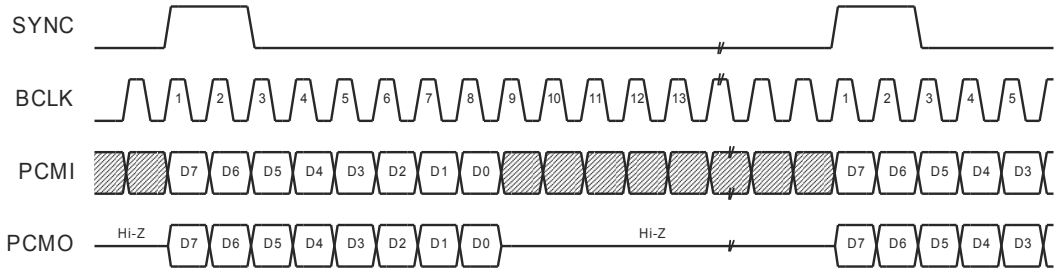


Figure 7 μ-law PCM timing chart (long frame sync)

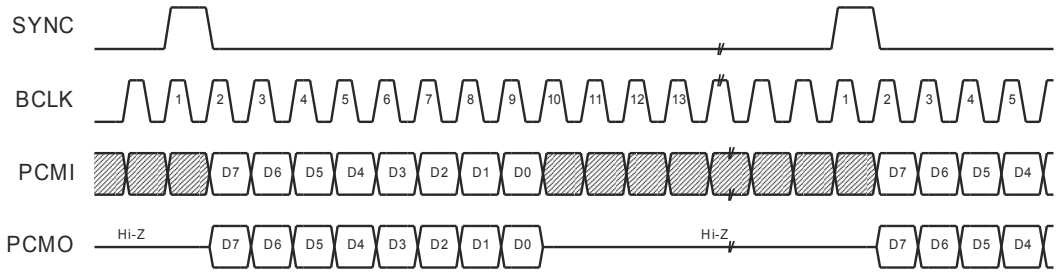


Figure 8 μ-law PCM timing chart (short frame sync)

GPIB3 (NCTHR)
This is a general-purpose input port pin.
This also works as a through-mode control pin over the noise canceller as the secondary function.
A logic '0' enables the noise canceller, and a logic '1' disables the noise canceller and the speech data by-passes the noise canceller.
When the MCUSEL pin is logic '1', this pin is automatically assigned with its secondary function.
When the MCUSEL pin is logic '0', this pin's function assignment follows the state of GPFB3-bit [GPCR1-B3].
(Note) The change of the input state to this pin is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 μs may not be reflected as the LSI behavior.
(Note) For 24ms approx. after the state change from a noise canceller enabling mode to a through-mode, the speech signals may not be ordinarily processed and be got mute or attenuated. The state change, if needed, is recommended to be made before a call.
(Note) If this pin is not used, set this pin to a logic '0'.

GPIB4 (ALCTHR)
This is a general-purpose input port pin.
This also works as a through-mode control pin over the automatic level controller (ALC) as the secondary function.
A logic '0' enables the ALC, and a logic '1' disables the ALC and the speech data by-passes the ALC.
The ALC is a function to mainly aim to absorb the difference in speech volume with handsets to connect to a hands-free. For the functional details, please refer to descriptions under the RALCTHR-bit [CR2-B4].
When the MCUSEL pin is logic '1', this pin is automatically assigned with its secondary function.
When the MCUSEL pin is logic '0', this pin's function assignment follows the state of GPFB4-bit [GPCR1-B4].
(Note) The change of the input state to this pin is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 μs may not be reflected as the LSI behavior.
(Note) If this pin is not used, set this pin to a logic '0'.

GPIB5 (SLPTHR)
This is a general-purpose input port pin.
This also works as a through-mode control pin over the slope filter as the secondary function.
A logic '0' enables the slope filter, and a logic '1' disables the slope filter and the speech data by-passes the slope filter.
The slope filter has frequency characteristics to suppress low frequency range and gain high frequency range so that it helps to relax near-end ambient noises usually dominant in low frequency range and to emphasize speech consonants mostly dominant in high frequency range. For the functional details, please refer to the slope filter characteristics under Reference Data.
When the MCUSEL pin is logic '1', this pin is automatically assigned with its secondary function.
When the MCUSEL pin is logic '0', this pin's function assignment follows the state of GPFB5-bit [GPCR1-B5].
(Note) The change of the input state to this pin is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 μs may not be reflected as the LSI behavior.
(Note) If this pin is not used, set this pin to a logic '0'.

GPIB6 (ECSEL)
This is a general-purpose input port pin.
This also works as an echo canceller selection as the secondary function.
A logic '0' selects single echo canceller mode (enables only acoustic echo canceller), and a logic '1' selects dual echo canceller mode (enables both of acoustic and line echo cancellers).
When the MCUSEL pin is logic '1', this pin is automatically assigned with its secondary function.
When the MCUSEL pin is logic '0', this pin's function assignment follows the state of GPFB6-bit [GPCR1-B6].
(Note) The change of the input state to this pin is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 μs may not be reflected as the LSI behavior.
(Note) The single echo canceller mode should be selected in an environment where no line echoes exist.
(Note) The change of the input state of this pin must be made during power-down state ($\overline{\text{PDN}}$ pin = logic '0' or SPDN-bit [CR0-B7] = '1') or during initial mode.
(Note) If this pin is not used, set this pin to a logic '0'.

GPIB7 (ECEN)
This is a general-purpose input port pin.
This also works as an enabling/disabling selection for echo cancellers as the secondary function.
A logic '0' disables echo cancellers and their auxiliary functions (ATTrA/ATTrL, ASIPAD/LPAL, ASOPAD/LSOPAD, ATTsA/ATTrA, Center Clip), and a logic '1' enables them.
When the MCUSEL pin is logic '1', this pin is automatically assigned with its secondary function.
When the MCUSEL pin is logic '0', this pin's function assignment follows the state of GPFB7-bit [GPCR1-B7].
(Note) The change of the input state to this pin is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 µs may not be reflected as the LSI behavior.
(Note) If this pin is not used, set this pin to a logic '0'.

GPIA0 (TPAD0), GPIA1 (TPAD1), GPIA2 (TPAD2), GPIA3 (TPAD3)
These are general-purpose input port pins.
These also work as transmit-side volume control as the secondary function.
For the setting, please refer to Table 1.
When the MCUSEL pin is logic '1', these pins are automatically assigned with their secondary function.
When the MCUSEL pin is logic '0', these pins' function assignment follows the state of GPFA3-0-bits [GPCR0-B3,2,1,0].
(Note) The change of the input state these pins is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 µs may not be reflected as the LSI behavior.
(Note) If these pins are not used, set them to a logic '0'.

GPIA4(RPAD0), GPIA5(RPAD1), GPIA6(RPAD2), GPIA7(RPAD3)
These are general-purpose input port pins.
These also work as receive-side volume control as the secondary function.
For the setting, please refer to Table 1.
When the MCUSEL pin is logic '1', these pins are automatically assigned with their secondary function.
When the MCUSEL pin is logic '0', these pins' function assignment follows the state of GPFA7-4-bits [GPCR0-B7,6,5,4].
(Note) The change of the input state to these pins is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 µs may not be reflected as the LSI behavior.
(Note) If these pins are not used, set them to a logic '0'.

Table 1 Receive-/Transmit-Side Volume Control

GPIA7 (RPAD3)	GPIA6 (RPAD2)	GPIA5 (RPAD1)	GPIA4 (RPAD0)	GPIA3 (TPAD3)	GPIA2 (TPAD2)	GPIA1 (TPAD1)	GPIA0 (TPAD0)	Level
0	1	1	1	0	1	1	1	+21dB
0	1	1	0	0	1	1	0	+18dB
0	1	0	1	0	1	0	1	+15dB
0	1	0	0	0	1	0	0	+12dB
0	0	1	1	0	0	1	1	+9dB
0	0	1	0	0	0	1	0	+6dB
0	0	0	1	0	0	0	1	+3dB
0	0	0	0	0	0	0	0	0dB
1	1	1	1	1	1	1	1	-3dB
1	1	1	0	1	1	1	0	-6dB
1	1	0	1	1	1	0	1	-9dB
1	1	0	0	1	1	0	0	-12dB
1	0	1	1	1	0	1	1	-15dB
1	0	1	0	1	0	1	0	-18dB
1	0	0	1	1	0	0	1	-21dB
1	0	0	0	1	0	0	0	MUTE

MCUSEL
This pin selects whether the microcontroller interface is used or unused.
When the microcontroller interface is used, set this pin to a logic '0'.
When the microcontroller interface is not used, set this pin to a logic "1".
A logic '1' with this pin automatically determines general-purpose input port pins to work as their secondary functions.
This pin is OR'ed with OPE_STAT-bit [CR0-B0].
Refer to NOTE ON USE.

$\overline{\text{DEN}}$, EXCK, DIN, DOUT
These are serial control ports for the microcontroller interface.
This LSI has 32 bytes control registers, and the data read and write between the registers and the microcontroller are made via these pins.
The $\overline{\text{DEN}}$ pin is a data read/write enabling signal input pin, the EXCK pin is a clock signal input pin for data shifting, the DIN pin is an address and data input pin, the DOUT pin is a data output pin. If the mirrocontroller interface is not used, set the $\overline{\text{DEN}}$ pin to a logic "1", the EXCK pin and DIN pins to a logic "0", and the MCUSEL pin to logic '1'.
Figure 9-12 shows the input/output timing.

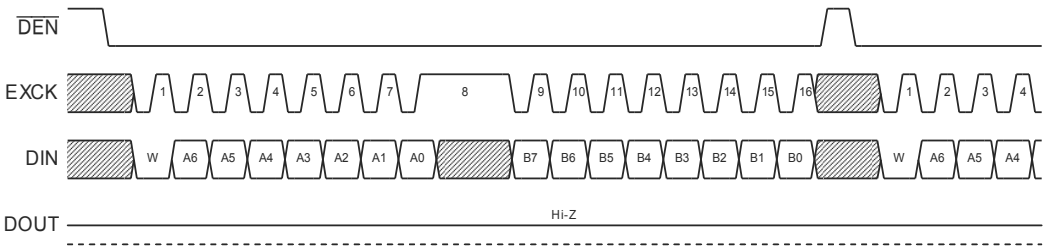


Figure 9 MCU Interface Input/Output Timing (Data Write with 8-bit MCU)

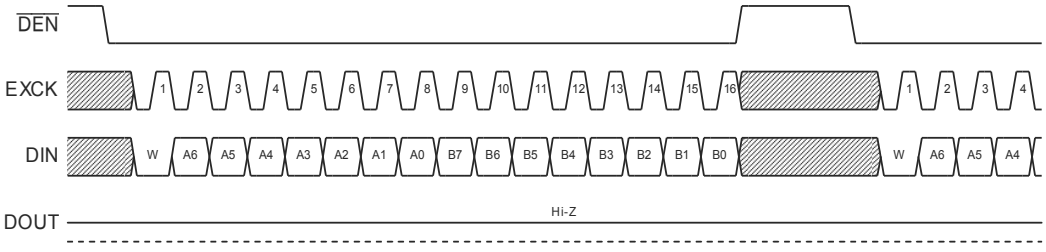


Figure 10 MCU Interface Input/Output Timing (Data Write with 16-bit MCU)

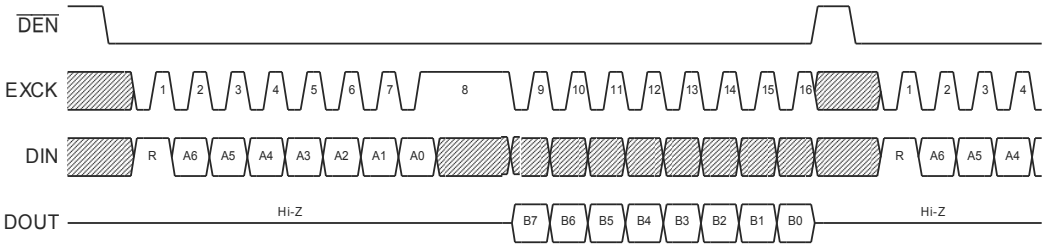


Figure 11 MCU Interface Input/Output Timing (Data Read with 8-bit MCU)

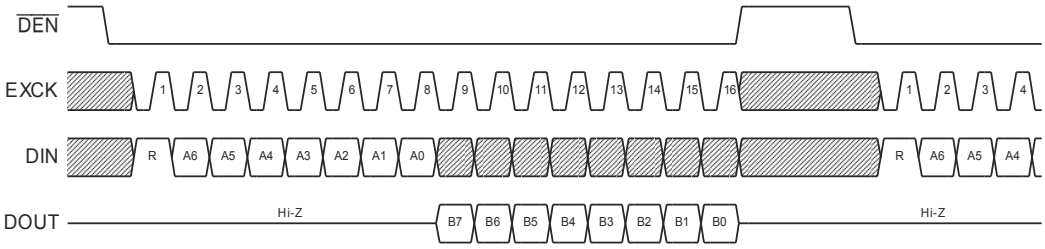


Figure 12 MCU Interface Input/Output Timing (Data Read with 16-bit MCU)

GPIB0
This is a general-purpose input port pin.
(Note) If this pin is not used, set this pin to a logic '0'.

GPOC0, GPOC1, GPOC2, GPOC3, GPOC4, GPOC5, GPOC6, GPOC7
These are general-purpose output port pins.
(Note) If these pins are not used, leave these pins floating.

DVDD0, DVDD1, AVDD
These are power supply pins. The DVDD0 and the DVDD1 are connected to digital circuits and the AVDD is connected to analog circuits in this LSI via the built-in regulator.
Connect them common in the shortest distance, and insert a 10 µF bypass capacitor (a tantalum capacitor [recommendation] or an aluminum electrolytic capacitor) and a 0.1 µF capacitor (laminating ceramic type) in parallel between these pins and the DGND0, 1 pins and the AGND0, 1 pins respectively.

DGND0, DGND1, AGND0, AGND1
These are ground pins. The DGND0 pin and the DGND1 pin are connected to the ground of digital circuits in this LSI. The AGND0 pin and the AGND1 pin are connected to the ground of analog circuits in this LSI. Connect them common in the shortest distance

REGOUT0, REGOUT 1
These are the built-in regulator output pins (2.6V approx.).
Insert a 10 µF capacitor (a tantalum capacitor [recommendation] or an aluminum electrolytic capacitor) and a 0.1 µF capacitor (laminating ceramic type) in parallel between the REGOUT0 pin and the DGND0 pin.
Insert a 0.1 µF capacitor (laminating ceramic type) in parallel between the REGOUT1 pin and the DGND1 pin.

VBG
This is an output pin for a reference voltage of the built-in regulator (1.2V approx.).
Insert a 150 pF (approx.) laminating ceramic capacitor between the this pin and the DGND0.

$\overline{\text{PDN}}$
This is the power-down reset control input pin.
A logic '0' executes the power-down reset.
When a logic '1' is input to this pin, this LSI is in a normal operation.
This execution also initializes all of this LSI including the control registers, the internal data memories, the filter coefficients of the echo cancellers and those of the noise cancellers.
(Note) The negative logic of this pin is ORed with the SPDN-bit [CR0-B7].
(Note) To avoid unstable operations, right after the power-up, execute the power-down rest with this pin (not with the SPDN-bit [CR0-B7]). The master clock input to the XI pin and the REGOUT output higher than 90% of the normal state are prerequisite to secure the power-down reset.
(Note) When an ORed logic of the AVREFEN pin and the AVREFEN-bit [CR16-B7] are logic '1', the AVREF and analog output amps keep powered up even during the power-down state.

$\overline{\text{RST}}$
This is an input pin to initialize the filter coefficients of the echo cancellers and the noise canceller and the ALC acquired gain.
A logic '0' executes the initialization. For a normal operation, give this pin a logic '1'.
During the reset state, no speech signals are output. Control registers are preserved.
Execute the initialization in cases where the echo path changes (due to line switching during a telephone conversation, etc.), or for another call.
(Note) The negative logic of this pin is ORed with the RST-bit [CR0-B6].
(Note) The change of the input state to these pins is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 µs may not be reflected as the LSI behavior.
(Note) The execution of this reset during a call may cause minor noises due to interruption at an arbitrary point in a sequence of PCM codes so that an execution of the reset is recommended to be made in a silent state.

TSTI0, TSTI1, TSTI2
These are LSI manufacturer's test input pins. Set these pins to a logic "0".

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Analog power supply voltage	AV_{DD}	—	–0.3 to +4.6	V
Digital power supply voltage	DV_{DD}	—	–0.3 to +4.6	V
Input voltage	V_{AIN}	Analog pins	–0.3 to AV_{DD}+0.3	V
	V_{DIN}	Digital pins	–0.3 to DV_{DD}+0.3	V
Short-circuit output current	I_{OS}	—	–20 to +20	mA
Power dissipation	P_D	Ta = 85 °C, per package	350	mW
Storage Temperature	T_{STG}	—	–65 to +150	°C

RECOMMENDED OPERATING CONDITION (1)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog power supply voltage (*1)	AV_{DD}	AVDD	3.0	3.3	3.6	V
Digital power supply voltage (*1)	DV_{DD}	DVDD0, DVDD1	3.0	3.3	3.6	V
Operating temperature	T_a	—	-40	—	85	°C
High-level input voltage	V_{IH1}	MCK/XI	DVDD x 0.75	—	DVDD + 0.3	V
	V_{IH2}	Normal digital pins	DVDD x 0.75	—	DVDD + 0.3	V
Low-level input voltage	V_{IL1}	MCK/XI	0.0	—	DVDD x 0.19	V
	V_{IL2}	Normal digital pins	0.0	—	DVDD x 0.19	V
Digital input rise time	t_{IR}	Digital pins	-	2	20	ns
Digital input fall time	t_{IF}	Digital pins	-	2	20	ns
Master clock frequency	f_{MCK}	MCK/XI	12.2867712 (-0.01%)	12.288	12.2892288 (+0.01%)	MHz
Master Clock Duty Ratio	d_{MCK}	MCK/XI	40	50	60	%

Note

*1 Turn on and off the analog power supply and digital power supply simultaneously, or turn on digital power supply prior to analog power supply and turn off analog power supply prior to digital power supply.

RECOMMENDED OPERATING CONDITION (2)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Bit clock frequency	f_{BCLK1}	BCLK (*1) μ-law PCM	64	—-	2048	kHz
	f_{BCLK2}	BCLK (*1) 16bit Linear PCM	128	—	2048	KHz
Bit clock duty ratio	d_{BCLK}	BCLK (*1)	40	50	60	%
Synchronous Signal Frequency	f_{SYNC}	SYNC (*1)	7.992 (-0.1%)	8.0	8.008 (+0.1%)	kHz
Synchronous Signal Width	f_{WS}	SYNC (*1)	1BCLK	—	100	μs
Transmit/Receive Sync Signal Setting Time	t_{BS}	BCLK to SYNC (*1)	100	—	—	ns
	t_{SB}	SYNC to BCLK (*1)	100	—	—-	ns
Digital output load resistance	C_{DL}	Digital pins	—	—	50	pF
Bypass capacitor for AVREF	C_{AVREF}	AVREF - AGND0	—	10+0.1	—	μF
Bypass capacitor for VBG	C_{VBG}	VBG-DGND0	—	150	—	pF
Bypass capacitor for REGOUT	$C_{REGOUT1}$	REGOUT0-DGND0	—	10+0.1	—	μF
	$C_{REGOUT2}$	REGOUT1-DGND1	—	0.1	—	μF

Note
*1 In external clock mode (CLKSEL = logic “1’)

ELECTRICAL CHARACTERISTICS

DC Characteristics

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{SS1}	Stand-by state (1) $\overline{PDN}$="0", AVREFEN="0", AVDD=DVDD0,1=3.30V	—	100	500	µA
	I_{SS2}	Stand-by state (2) $\overline{PDN}$="0", AVREFEN="1", AVDD=DVDD0,1=3.30V	—	3.5	7.0	mA
	I_{DD1}	Operating state MCK/XI, XO 12.288MHz crystal connected Inpu signal : none AVDD=DVDD0,1=3.30V, T_a=25°C	—	50	60	mA
Digital input pin input leak current	I_{IH1}	V_{IN}=DVDD	—	0.02	10	µA
	I_{IL1}	V_{IN}=0.0V	-10	-0.02	—	µA
Digital I/O pin input leak current	I_{OZH}	V_{IN}=DVDD	—	0.02	10	µA
	I_{OZL}	V_{IN}=0.0V	-10	-0.02	—	µA
High-level output voltage	V_{OH1}	Digital output pins Digital I/O pins I_{OH}=4.0mA	0.78 x DVDD	—	—	V
	V_{OH2}	XO pin I_{OH}=0.5mA	0.78 x DVDD	—	—	V
Low-level output voltage	V_{OL1}	Digital output pins Digital I/O pins I_{OL}=-4.0mA	—	—	0.4	V
	V_{OL2}	XO pin I_{OL}=-0.5mA	—	—	0.4	V
Input capacitance	C_{IN}	Input pins, I/O pins	—	6.0	—	pF

Analog Interface

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input resistance	R_{IN}	Analog input pins (*2)	10	—	—	MΩ
Output load resistance	R_{L1}	AGSX0, AGSX1, LGSX	10	—	—	kΩ
	R_{L2}	AVFRO, LVFRO	2	—	—	kΩ
Output load capacitance	C_L	Analog output pins (*3)	—	—	50	pF
Offset voltage	V_{OF}	Analog output pins (*3)	-40	—	40	mV
Output voltage level (*1)	V_O	LVFRO, AVFRO RL=10kΩ, Input=+3dBm0	1.158	1.3	1.458	V_{PP}

Note

*1 -7.7dBm(600Ω)=0dBm0, +3dBm0=1.3Vpp

*2 Analog input pins (AIN0P, AIN0N, AIN1N, LINN)

*3 Analog output pins (AGSX0, AGSX1, LGSX, AVFRO, LVFRO)

$\overline{\text{PDN}}$, XO, AVREF Timing

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AVDD supply start delay time	t_{AVDDS}	AVDD	0	—	—	ns
DVDD supply cease delay time	t_{DVDDE}	DVDD0,1	0	—	—	ns
Power-down reset start latency	t_{RSTS}	$\overline{\text{PDN}}$	—	—	100	ns
Power-dwon reset signal pulse width	t_{RSTW}		1.0	—	—	µs
Power-down reset release latency	t_{RSTE}		—	—	250	ms
Oscillation activation time	t_{SXO}	crystal unit (*1)	—	—	28	ms

Note

*1 Crystal unit (HC-49/U-S), R=1MΩ, C1=C2=10pF

Timing Chart ($\overline{\text{PDN}}$, XO, AVREF timing)

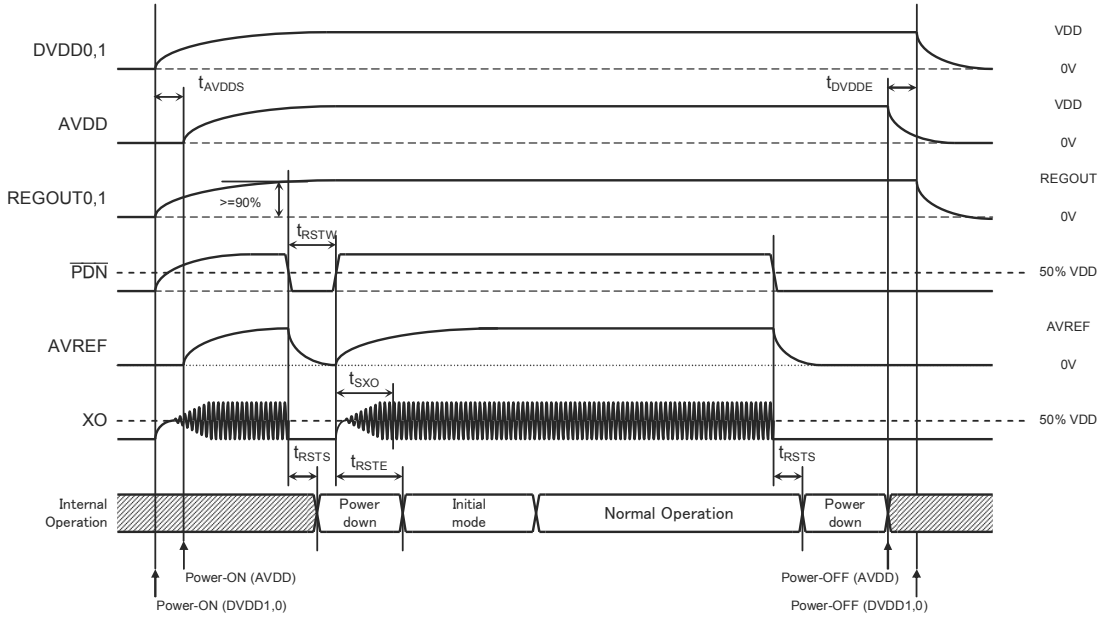


Figure 13 $\overline{\text{PDN}}$, XO, AVREF Timing

Digital Interface (Pin control, general port timing)

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Pin control latency (Low to High)	t_{PARD}	*1	—	—	250	µs
Pin control pulse width	t_{PARW}		250	—	—	µs
Pin control latency (High to Low)	t_{PARH}		—	—	250	µs
General purpose output port output delay time	t_{GPOD}	*2	—	—	100	ns
General output port hold time	t_{GPOH}		—	—	100	ns

Note

*1 GPIA7-4 (RPAD3-0), GPIA3-0 (TPAD3-0), GPIB7 (ECEN), GPIB6 (ECSEL), GPIB5 (SLPTHR), GPIB4 (ALCTHR), GPIB3 (NCTHR), GPIB2 (VFROSEL), GPIB1 ($\overline{\text{LINEEN}}$), GPIB0, $\overline{\text{RST}}$, PCMSEL, CLKSEL

*2 GPOC7-0

Timing Chart (Pin Control, General Ports)

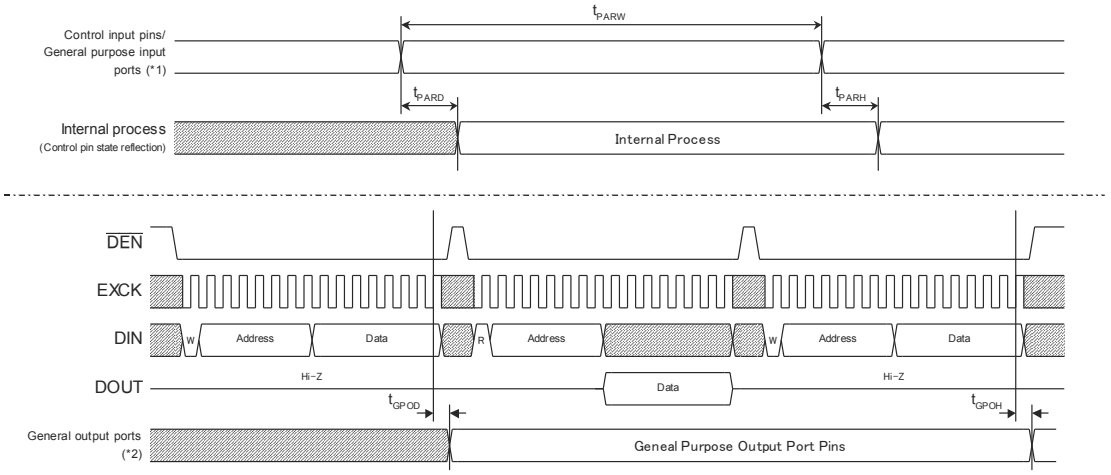


Figure 14 Control Input Pin and General Purpose Output Port Pin Timing

PCM Interface

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Bit clock frequency	f_{BCLK1}	μ-law PCM mode (*1, *2, *3)	63.36	64	64.64	kHz
	f_{BCLK2}	16bit Linear PCM mode (*1, *2, *3)	126.72	128	129.28	kHz
Bit clock duty ratio	d_{BCLK}	(*1, *2, *3)	40	50	60	%
Sync signal frequency	f_{SYNC}	(*1, *2, *3)	7.92	8.0	8.08	kHz
Sync signal duty ratio	d_{SYNC1}	μ-law PCM mode (*1, *2, *3) Long frame sync mode (*1, *2, *3)	24.85	25	25.15	%
	d_{SYNC2}	16bit Linear PCM mode Long frame sync mode (*1, *2, *3)	12.35	12.5	12.65	%
	d_{SYNC3}	μ-law PCM mode (*1, *2, *3) Short frame sync mode (*1, *2, *3)	12.35	12.5	12.65	%
	d_{SYNC4}	16bit Linear PCM mode Short frame sync mode (*1, *2, *3)	6.10	6.25	6.40	%
Transmit/Receive Sync signal timing	t_{SB}	SYNC to BCLK (*3)	100	—	—	ns
	t_{BS}	BCLK to SYNC (*3)	100	—	—	ns
Input setup time	t_{DS}	—	100	—	—	ns
Input hold time	t_{DH}	—	100	—	—	ns
Digital output delay time	t_{SDX}	C_{DL}=50pF	—	—	100	ns
	t_{XD1}	C_{DL}=50pF	—	—	100	ns
Digital output hold time	t_{XD2}	C_{DL}=50pF	—	—	100	ns
	t_{XD3}	C_{DL}=50pF	—	—	100	ns

Note
*1 C_{DL}=20pF
*2 MCK/XI=12.288MHz
*3 In internal clock mode (CLKSEL = logic “0’)

Timing Chart (PCM Interface)

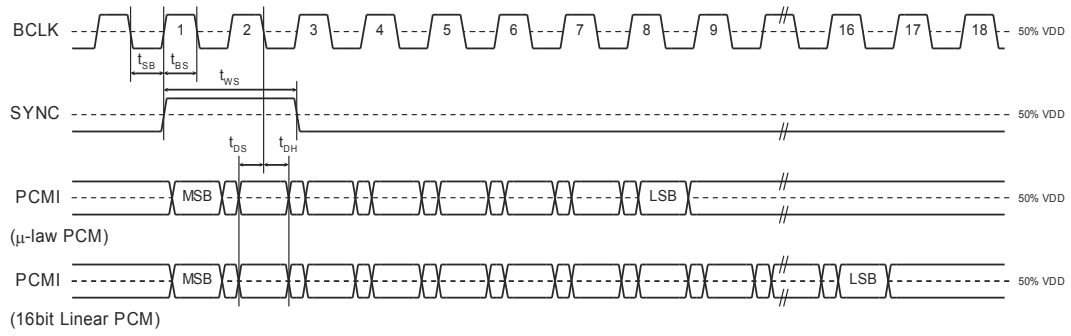


Figure 15 PCM Input Timing (Long Frame Sync)

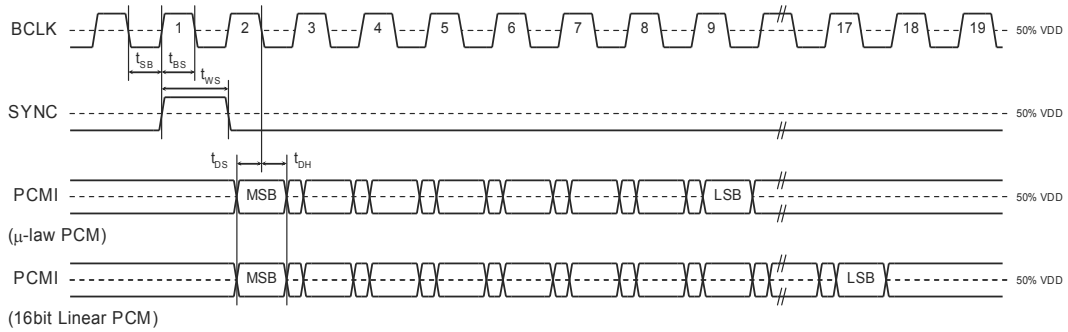


Figure 16 PCM Input Timing (Short Frame Sync)

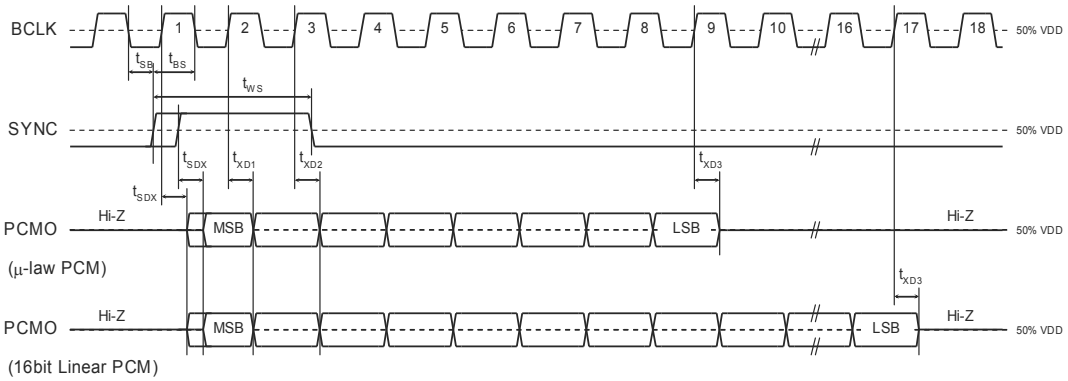


Figure 17 PCM Output Timing (Long Frame Sync)

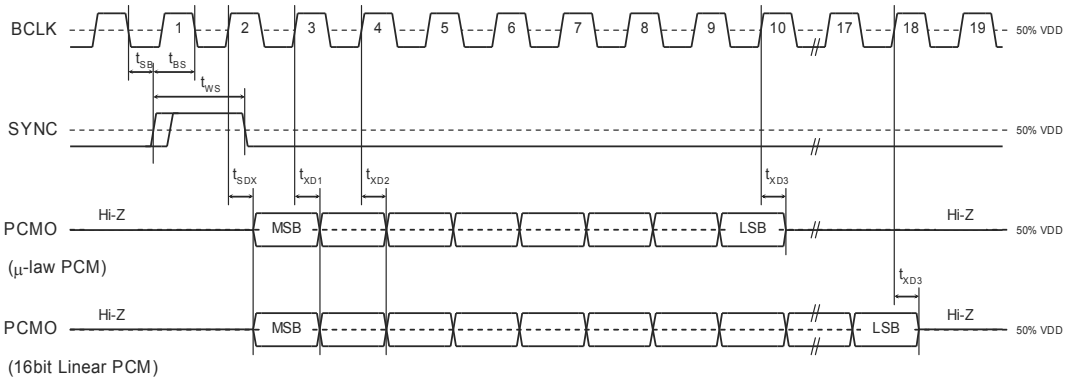


Figure 18 PCM Output Timing (Short Frame Sync)

Microcontroller Interface (Serial Interface)

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital input/output timing	t_{M1}	C_{DL}=50pF	20	—	—	ns
	t_{M2}		20	—	—	ns
	t_{M3}		50	—	—	ns
	t_{M4}		100	—	—	ns
	t_{M5}		50	—	—	ns
	t_{M6}		50	—	—	ns
	t_{M7}		—	—	30	ns
	t_{M8}		0	—	—	ns
	t_{M9}		50	—	—	ns
	t_{M10}		—	—	30	ns
	t_{M11}		100	—	—	ns
EXCK clock frequency	f_{EXCK}	—	—	—	10	MHz

Timing Chart (Microcontroller Serial Interface)

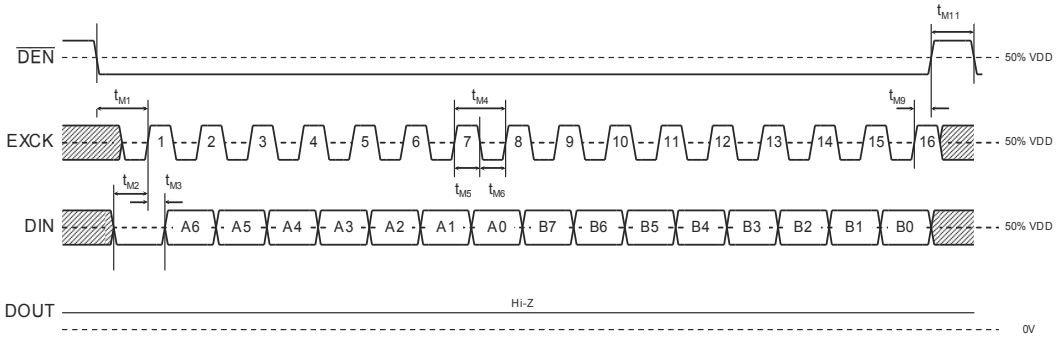


Figure 19 Write Timing

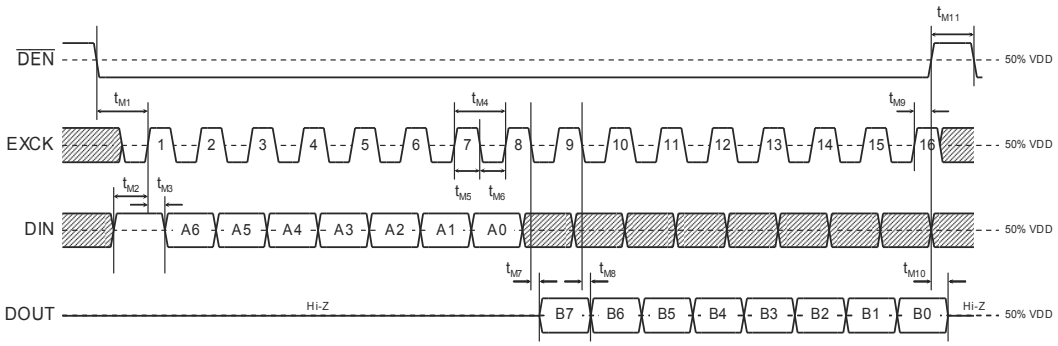


Figure 20 Read Timing

Microcontroller Interface (Serial Interface)

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Frequency (Hz)	Level (dBm0)	Others				
Transmit frequency response	LossT1	0 to 60	0	*1, *2	25	—	—	dB
	LossT2	300 to 3000			-0.15	—	0.25	dB
	LossT3	1020			Reference			—
	LossT4	3300			-0.15	—	0.8	dB
	LossT5	3400			0	—	0.8	dB
	LossT6	3968.75			13	—	-	dB
Receive frequency response	LossR1	0 to 3000	0	*1, *2	-0.15	—	0.2	dB
	LossR2	1020			Reference			—
	LossR3	3300			-0.15	—	0.8	dB
	LossR4	3400			-0.15	—	0.8	dB
	LossR5	3968.75			13	—	—	dB
Transmit signal to distortion ratio	SDT1	1020	+3	*1, *2, *3	35	—	—	dB
	SDT2		0		35	—	—	dB
	SDT3		-30		35	—	—	dB
	SDT4		-40		28	—	—	dB
	SDT5		-45		23	—	—	dB
Receive signal to distortion ratio	SDR1	1020	+3	*1, *2, *3	35	—	—	dB
	SDR2		0		35	—	—	dB
	SDR3		-30		35	—	—	dB
	SDR4		-40		28	—	—	dB
	SDR5		-45		23	—	—	dB
Transmit gain tracking	GTT1	1020	+3	*1, *2, *3	-0.2	—	0.2	dB
	GTT2		-10		Reference			—
	GTT3		-40		-0.2	—	0.2	dB
	GTT4		-50		-0.5	—	0.5	dB
	GTT5		-55		-1.2	—	1.2	dB
Receive gain tracking	GTR1	1020	+3	*1, *2, *3	-0.2	—	0.2	dB
	GTR2		-10		Reference			—
	GTR3		-40		-0.2	—	0.2	dB
	GTR4		-50		-0.5	—	0.5	dB
	GTR5		-55		-1.2	—	1.2	dB
Idle channel noise	$N_{IDL}T$	—	—	*1, *2, *3 *5	—	—	-68	dBm0p
	$N_{IDL}R$	—	—		—	—	-72	dBm0p
Absolute signal level (*4)	AVT	1020	0	*1, *2	0.285	0.32	0.359	Vrms
	AVR		0		0.285	0.32	0.359	Vrms

Note
*1 Echo cancellers, Noise canceller, slope filter, ALC = off
Programmable gain = 0dB
*2 Analog and digital gain = 1
*3 with a psophometric filter
*4 0.32Vrms = 0dBm0 = -7.7dBm (600Ω)
*5 Input signals = Idle pattern

AC Characteristics (Programmable Gain Characteristics)

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit/Receive gain accuracy	G_{AC1}	against a set gain (*1)	-1.0	—	+1.0	dB
	G_{AC2}	against an adjacent gain step (*2)	-1.0	—	+1.0	dB

Note *1 TPAD, RPAD
*2 Acoustic-side PGA's (Programmable Gain Amp's), Line-side PGA

Noise Canceller Characteristics

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Noise attenuation	N_{RES}	with white noise for voice band noise attenuation setting = default	—	13	—	dB

[Measurement System Block Diagram]

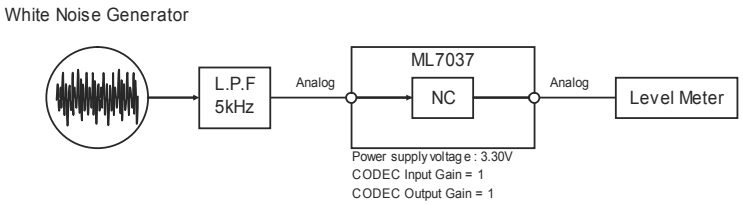


Figure 21 Measurements (Noise Attenuation)

Echo Canceller Characteristics

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Echo attenuation	E_{RES}	Acoustic-side, Line-side *3 (Analog interface or 16bit Linear PCM mode)	—	35	—	dB
		Line-side (μ-law PCM mode)	—	30	—	dB
Cancellable echo delay time	T_{ACOUD}	Acoustic-side	—	—	100	ms
	T_{LINED}	Line-side *3	—	—	20	ms

Note *3 Only in dual echo canceller mode

[Measurement System Block Diagram]

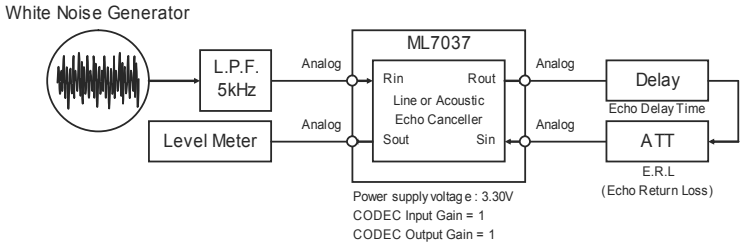


Figure 22 Measurements (Echo Attenuation)

FUNCTIONAL DESCRIPTION

Control Register

The control register map and the general-purpose port control register map are shown as Table 2 and Table3 respectively.

Table 2-1 Control Register Map

Register Name	Address	Data								R/W
		B7	B6	B5	B4	B3	B2	B1	B0	
CR0	00h	SPDN	RST	$\overline{\text{LINEEN}}$	PCMSEL	$\overline{\text{CLKEN}}$	PCMEN	ECSEL	OPE_STAT (MCUSEL)	R/W
		/E	/E	I/	I/	I/	I/	I/	I/	
CR1	01h	DMWR	#	#	#	#	#	#	#	R/W
		I/E	-	-	-	-	-	-	-	
CR2	02h	#	#	#	RALCTHR	RPAD3	RPAD2	RPAD1	RPAD0	R/W
		-	-	-	I/E	I/E	I/E	I/E	I/E	
CR3	03h	#	#	#	#	TPAD3	TPAD2	TPAD1	TPAD0	R/W
		-	-	-	-	I/E	I/E	I/E	I/E	
CR4	04h	#	#	#	APGA4	APGA3	APGA2	APGA1	APGA0	R/W
		-	-	-	I/E	I/E	I/E	I/E	I/E	
CR5	05h	#	#	#	LPGA4	LPGA3	LPGA2	LPGA1	LPGA0	R/W
		-	-	-	I/E	I/E	I/E	I/E	I/E	
CR6	06h	A15	A14	A13	A12	A11	A10	A9	A8	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR7	07h	A7	A6	A5	A4	A3	A2	A1	A0	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR8	08h	D15	D14	D13	D12	D11	D10	D9	D8	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR9	09h	D7	D6	D5	D4	D3	D2	D1	D0	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR10	0Ah	READY	#	#	#	#	#	#	#	R/
		-	-	-	-	-	-	-	-	
CR11	0Bh	LTHR	LECEN	LHLD	#	LCLP	LSLC	LATT	#	R/W
		I/E	I/E	I/E	-	I/E	I/	I/E	-	
CR12	0Ch	ATHR	AECEN	AHLD	#	ACLP	ASLC	AATT	#	R/W
		I/E	I/E	I/E	-	I/E	I/	I/E	-	
CR13	0Dh	ASOPAD1	ASOPAD0	ASIPAD1	ASIPAD0	LSOPAD1	LSOPAD0	LSIPAD1	LSIPAD0	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR14	0Eh	SLPTHR	#	#	#	NCTHR	#	#	#	R/W
		I/E	-	-	-	I/E	-	-	-	

Table 2-2 Control Register Map

Register Name	Address	Data								R/W
		B7	B6	B5	B4	B3	B2	B1	B0	
CR15	0Fh	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR16	10h	AVREFEN	#	#	#	#	#	AVFROSEL	LVFROSEL	R/W
		I/E	-	-	-	-	-	I/E	I/E	
CR17	11h	#	#	#	#	#	#	AATTMODE1	AATTMODE0	R/W
		-	-	-	-	-	-	I/E	I/E	
CR18	12h	#	#	#	#	#	#	LATTMODE1	LATTMODE0	R/W
		-	-	-	-	-	-	I/E	I/E	
CR19	13h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR20	14h	#	#	#	#	EQL_EN	EQL_2	EQL_1	EQL_0	R/W
		-	-	-	-	I/E	I/E	I/E	I/E	
CR21	15h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR22	16h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR23	17h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR24	18h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR25	19h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR26	1Ah	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR27	1Bh	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR28	1Ch	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR29	1Dh	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR30	1Eh	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR31	1Fh	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	

Table 3 General-Purpose Port Control Register Map

Register Name	Address	Data								R/W
		B7	B6	B5	B4	B3	B2	B1	B0	
GPCR0	20h	GPFA7	GPFA6	GPFA5	GPFA4	GPFA3	GPFA2	GPFA1	GPFA0	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
GPCR1	21h	GPFB7	GPFB6	GPFB5	GPFB4	GPFB3	GPFB2	GPFB1	#	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	-	
GPCR2	22h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
GPCR3	23h	GPDA7	GPDA6	GPDA5	GPDA4	GPDA3	GPDA2	GPDA1	GPDA0	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
GPCR4	24h	GPDB7	GPDB6	GPDB5	GPDB4	GPDB3	GPDB2	GPDB1	GPDB0	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
GPCR5	25h	GPDC7	GPDC6	GPDC5	GPDC4	GPDC3	GPDC2	GPDC1	GPDC0	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
GPCR6	26h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
GPCR7	27h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
GPCR8	28h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	

Symbols for register name
- # : Reserved bits
- $: Don't read nor write

Symbols to show when it can be altered (When to alter)
- I/E : both in the initial mode and in normal operation
- I/ : only in the initial mode
- /E : only in normal operation
- - : Don't change

Symbols to show Read or Write
- R/W : Both for Read and Write
- R/ : Read only
- /W : Write only
- / : Both read and write prohibited

(Note) The change of control registers (including the control registers for general-purpose ports) is detected with SYNC signals (8kHz) so that the change of the control registers less than 250 ms may not be reflected as the LSI behavior.

(Note) When you write a control register in any other mode than the initial mode, SYNC signals (8kHz) must be supplied unless the ML7037-003 is in the internal clock mode (the CLKSEL pin = logic 0').

(Note) Refer to descriptions under Internal Data Memory Access for a way to set CR6, CR7, CR8 and CR9.

MICRO CONTROLLER INTERFACE

A way to use the micro controller interface is shown herebelow;

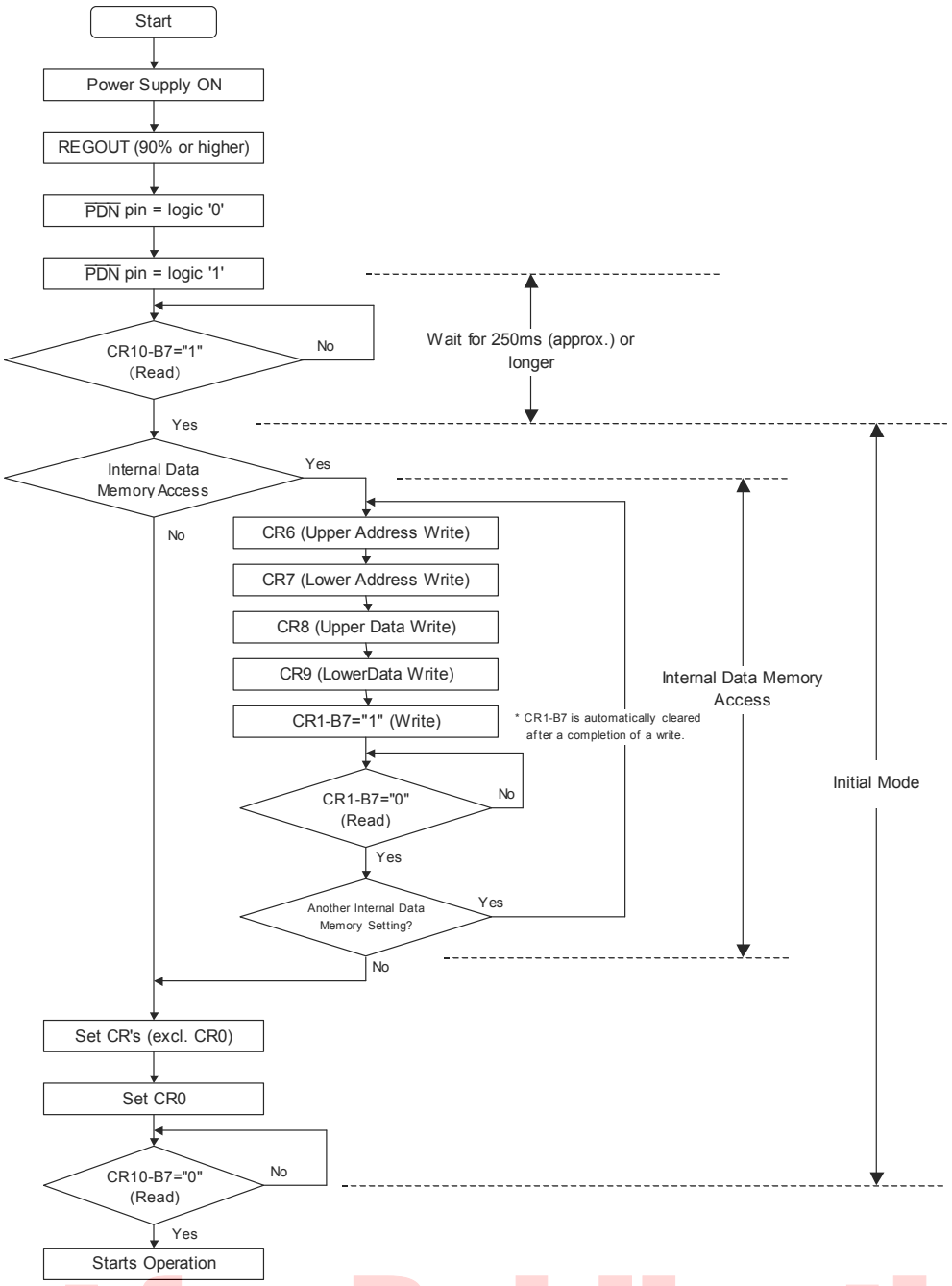


Figure 25 Micro Controller Interface Flow Chart

INTERNAL DATA MEMORY ACCESS

The ML7037-003 has an area called the internal data memories (16-bit wide address and 16-bit wide data), and operates reading variables such as coefficients and thresholds retained therein. By alternating the data in the given memory addresses, the default state could be customized.

How to Write into the Internal Data Memory

The CR6 (A15-A8) and the CR7 (A7-A0) are registers to specify the address of the internal data memory to alter. The CR8 (D15-D8) and the CR9 (D7-D0) are registers to store the data to write into the internal data memory to alter.
When the MCUSEL pin is given a logic '0', the ML7037-003 automatically transits into the initial mode 250ms (approx.) after a release of power-down reset by the $\overline{\text{PDN}}$ pin or the SPDN-bit [CR0-B7], and the READY-bit [CR10-B7] turns to be a logic '1' which shows the ML7037-003 has got ready for the control register access.
During this initial mode, specify both the 16-bit wide address by the CR6-CR7 and the 16-bit wide data by the CR8-CR9 first, and then write a logic '1' into the DMWR-bit [CR1-B7], which executes alternation of the internal data memory in the given address. After the internal data memory alternation, the DMWR-bit [CR1-B7] automatically is cleared to be a logic '0'. The flow of this internal data memory access is shown in Figure 26.
When more than an internal data memory, repeat the procedure above. A change of the OPE_STAT-bit [CR0-B0] to a logic '1' let the ML7037-003 out of the initial mode, and it starts normal operation.

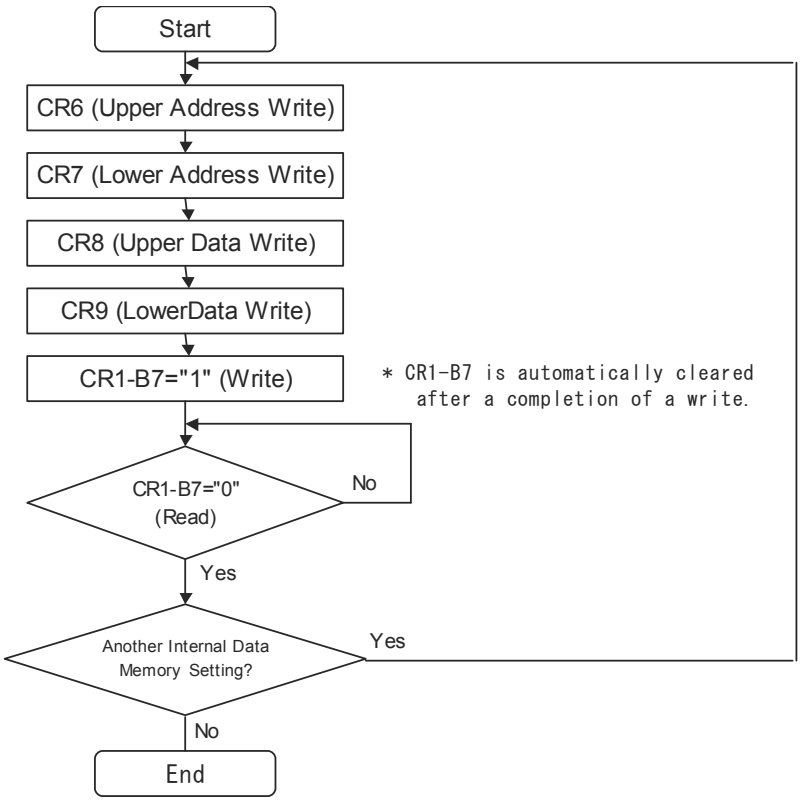


Figure 26 Internal Data Memory Access Flow Chart

PIN CONTROL AND CONTROL REGISTERS

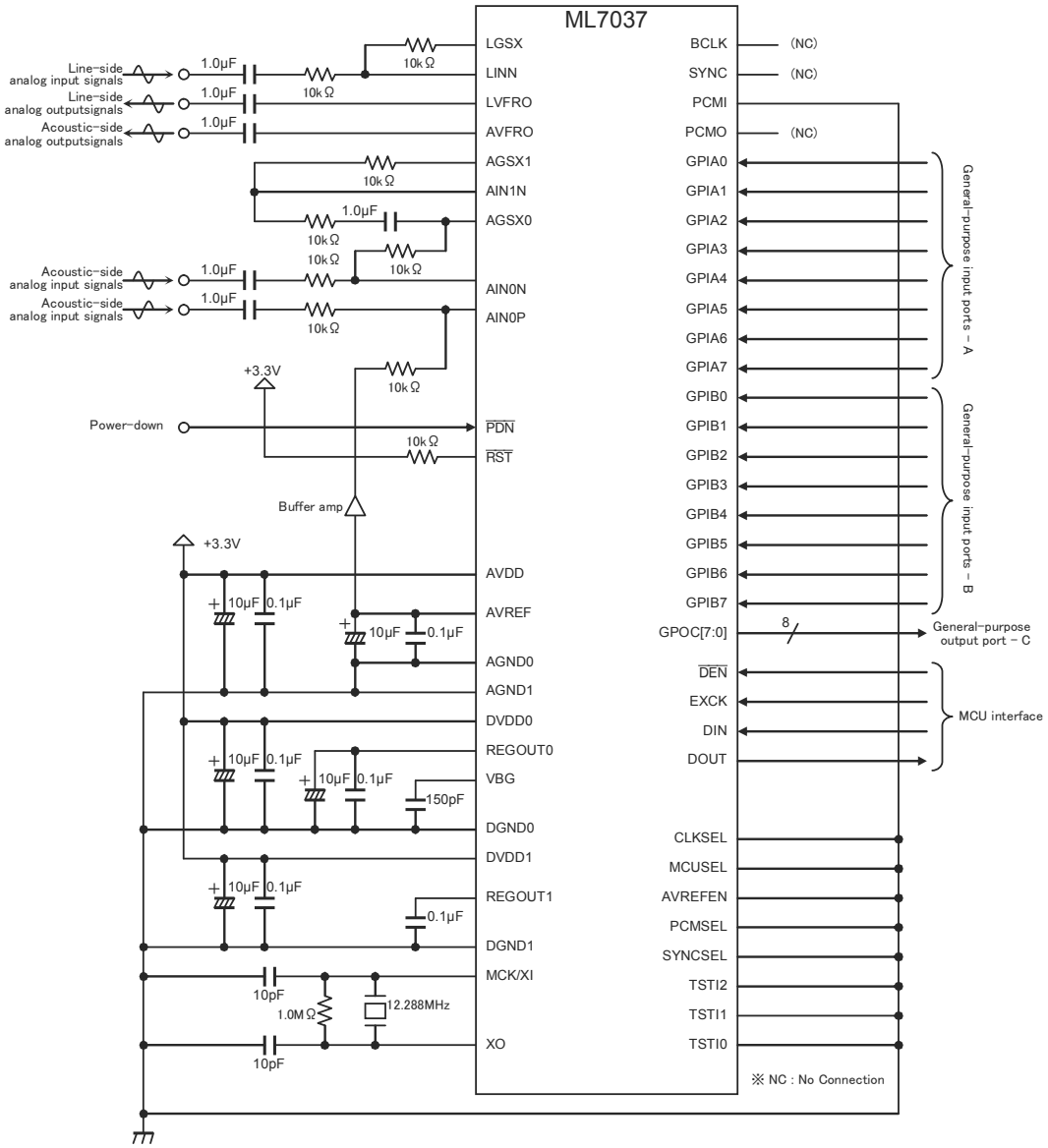
Some of functions and states with the ML7037-003 could be determined either by input state of certain pins (their secondary functions, if the pins are general-purpose input port pins) and/or the control registers. In such cases, the functions and states are determined by ORed logics between them. Hence, when a function or a state is determined (called as "State Control") by the concerned pin input, it is required to be careful with the concerned register setting; and visa versa.
Table 13 shows such pins and the relevant control registers.
All the values to be set in the relevant control registers are the initial values set on a release of power-down reset by the $\overline{\text{PDN}}$ pin or the SPDN-bit [CR0-B7].

Function	Pin input to make when State Control is made by the control register	Pin	Control register value to set when State Control is made by the pin	Control Register
Power-down reset	logic '1'	$\overline{\text{PDN}}$	logic '0'	SPDN
Reset	logic '1'	$\overline{\text{RST}}$	logic '0'	RST
PCM Coding Format Selection	logic '0'	PCMSEL	logic '0'	PCMSEL
Micro Control Interface Enable/Disable Selection	logic '0'	MCUSEL	logic '0'	OPE_STAT
Transmit-Side Volume Control	logic '0'	GPIA[3-0] (TPAD[3-0]) *1	logic '0'	TPAD[3-0]
Receive-Side Volume Control	logic '0'	GPIA[4-7] (RPAD[3-0]) *1	logic '0'	RPAD[3-0]
Line-Side Analog Interface Power-Down Control	logic '0'	GPIB1 ($\overline{\text{LINEEN}}$) *1	logic '0'	$\overline{\text{LINEEN}}$
Analog Output Selection	logic '0'	GPIB2 (VFROSEL) *1	logic '0'	AVFROSEL LVFROSEL
Noise Canceller Through Mode Selection	logic '0'	GPIB3 (NCTHR) *1	logic '0'	NCTHR
Receive-Side ALC Through Mode Selection	logic '0'	GPIB4 (ALCTHR) *1	logic '0'	RALCTHR
Slope Filter Through Mode Selection	logic '0'	GPIB5 (SLPTHR) *1	logic '0'	SLPTHR
Echo Canceller Mode Selection Register	logic '0'	GPIB6 (ECSEL) *1	logic '0'	ECSEL
Acoustic Echo Canceller Enable Control	logic '0'	GPIB7 (ECEN) *1	logic '0'	LECEN AECEN

*1 : A name in (bracket) shows the pin name when the secondary function is assigned.

Table 13 Relevant Input Pins And Control Registers

APPLICATION CIRCUIT (1)

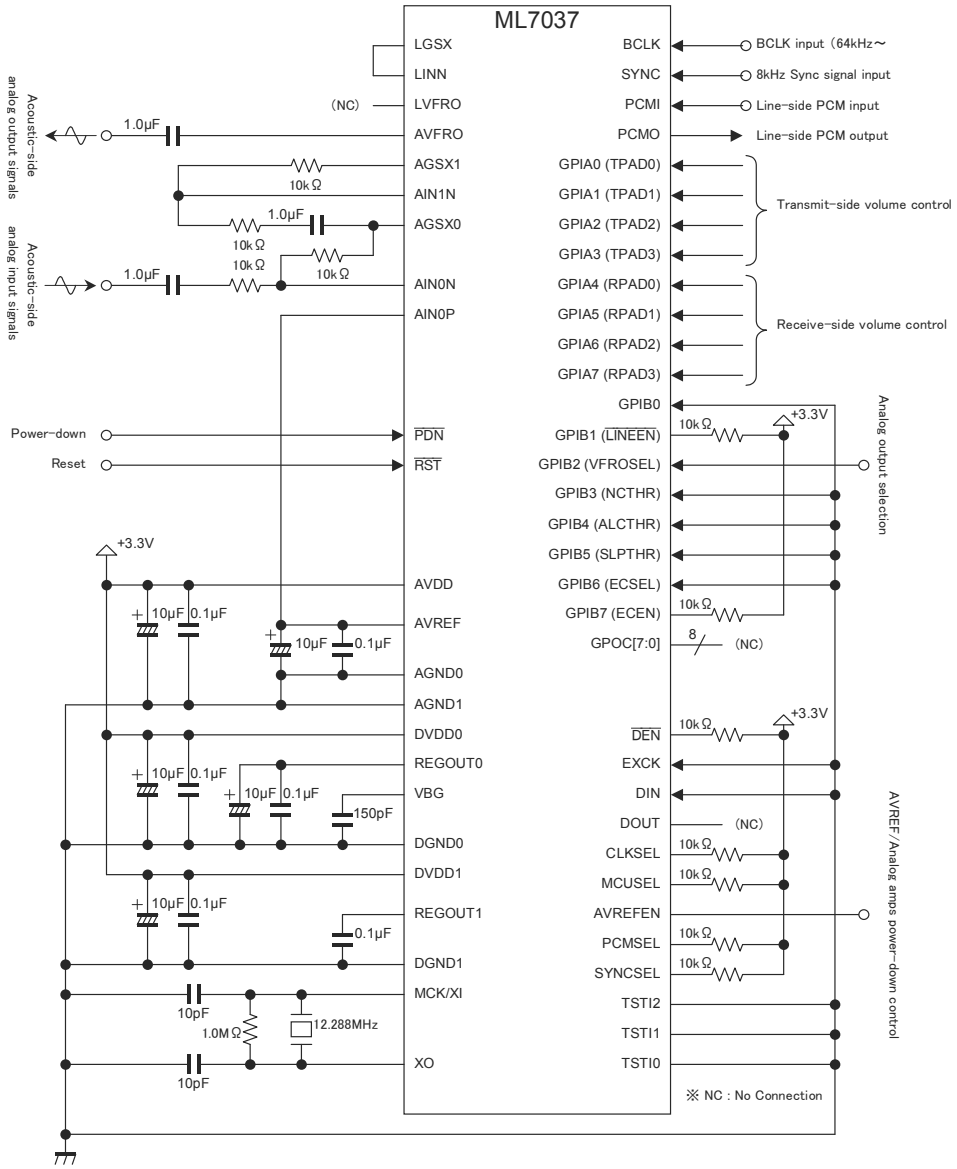


(Conditions)

Speech signal interface on line-side	:	Analog
Speech signal input on acoustic side	:	Differential
PCM coding format	:	16bit Linear PCM
PCM frame sync timing	:	Long frame sync
PCM clock mode	:	Internal clock mode (Clock master)
MCU interface	:	used

Figure 27

APPLICATION CIRCUIT (2)



(Conditions)

Speech signal interface on line-side	:	Digital (PCM)
Speech signal input on acoustic side	:	Single
PCM coding format	:	μ-law PCM
PCM frame sync timing	:	Short frame sync
PCM clock mode	:	External clock mode (Clock slave)
MCU interface	:	used

Figure 28

NOTE ON USE

1. Use a stabilized power supply with a low level of noises (especially spike noises and pulse noises of high frequencies) in order to prevent this device from malfunction or degradation in characteristics.

2. Place bypass-capacitors with a good high frequency characteristics for the power supply near the pins of this device in order to assure its electrical characteristics.

3. Place bypass-capacitors with a good high frequency characteristics for the analog signal ground (AVREF pin) near the pins of this device in order to assure its electrical characteristics.

4. Place bypass-capacitors with a good high frequency characteristics for the regulator's reference voltage output (VBG pin) and for the regulator outputs (REGOUT0,1 pins) near the pins of this device in order to assure its electrical characteristics.

5. Connect the AGND0, AGND1, DGND0 and DGND 2 to the system ground at a shortest distance and in a low impedance state.

6. Turn on and off the analog power supply and digital power supply simultaneously, or turn on digital power supply prior to analog power supply and turn off analog power supply prior to digital power supply.

7. After turning on the power, be sure to reset the device with the $\overline{\text{PDN}}$ pin while the master clocks are being supplied.

8. Set a system level diagram so that a value of the Echo Return Loss (E.R.L. = [Power of echo-originating signals at RoutA/RoutL] – [Power of echo signals at SinA/SinL]) is negative and the ASLC function is recommended to be enabled. When the E.R.L. cannot be negative all the time, the GLPAD function is recommended to be enabled with the ASLC function disabled. Refer to a reference data for the E.R.L level vs. echo attenuation of an echo canceller.

9. The input level should be –10 to –20 dBm0. Refer to a reference data for Rin input level vs. echo attenuation.

10. Application-level volume control on use is recommended to be made outside of the echo path such as by the RALC, the RPAD and the TPAD (not between the RoutA and the SinA in the single echo canceller mode; or not between the RoutA and the SinA nor not between the RoutL and the SinL).

    in Dual Echo Canceler mode : to be controlled with the TPAD, the RPAD, and/or the RALC.

    in Signal Echo Canceler mode : to be controlled with the TPAD, the RPAD, the RALC, and/or with the analog input (LINN) that is set at less than 1.3 VPP.

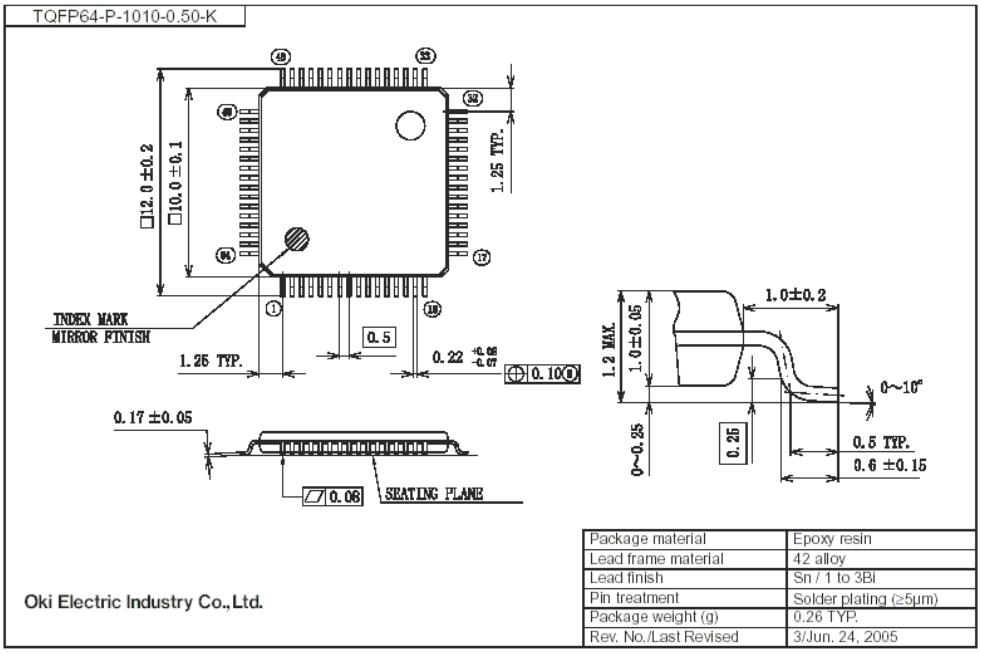
11. Turn off an echo canceller in an environment where no echoes exist.

12. When the echo path is changed (such as when resuming telephone communication), reset the device either with the $\overline{\text{PDN}}$ pin, the SPDN bit [CR0-B7], the $\overline{\text{RST}}$ pin or the RST bit [CR0-B6].

13. The Pin Control Mode (the MCUSEL-pin = logic '1') which defines behaviors of this LSI by logic '0' / '1' to concerned input pins has less flexibility in comparison with the External MCU Mode (the MCUSEL-pin = logic '0') which defines behaviors of this LSI through control register setting due to its limitation of the available pin count. Therefore, basically, this LSI is recommended to use in the External MCU Mode.

PACKAGE DIMENSIONS

(Unit : mm)



Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn / 1 to 3Bi
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.26 TYP.
Rev. No./Last Revised	3/Jun. 24, 2005

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code, and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL7037-003-01Zz_Digest	Oct. 13, 2006	–	–	First edition
PEDL7037-003-02Zz_Digest	Nov. 29, 2006	18	18	As what is initialized by the $\overline{RST}$-pin, ALC acquired gain is added.
PEDL7037-003-03Zz_Digest	Dec. 11, 2006	24	24	Correction of REGOUT0, 1 output level after DVDD0, 1 stop to be fed in Figure 13
PEDL7037-003-04Zz_Digest	Feb. 19, 2007	23	23	Correction of REGOUT0, 1 output level after DVDD0, 1 stop to be fed in Figure 13
		24	24	Recovery of Figure 14 which was falsely corrected by PEDL7037-003-03Zz_Digest
PEDL7037-003-05Zz_Digest	May. 21, 2007	39	39	Update of Package Dimensions

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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