FEDL7074-004DIGEST-01
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# OKI Semiconductor

# ML7074-004GA

**VoIP CODEC**

This document contains minimum specifications. For full specifications, please contact your nearest Oki office or representative.

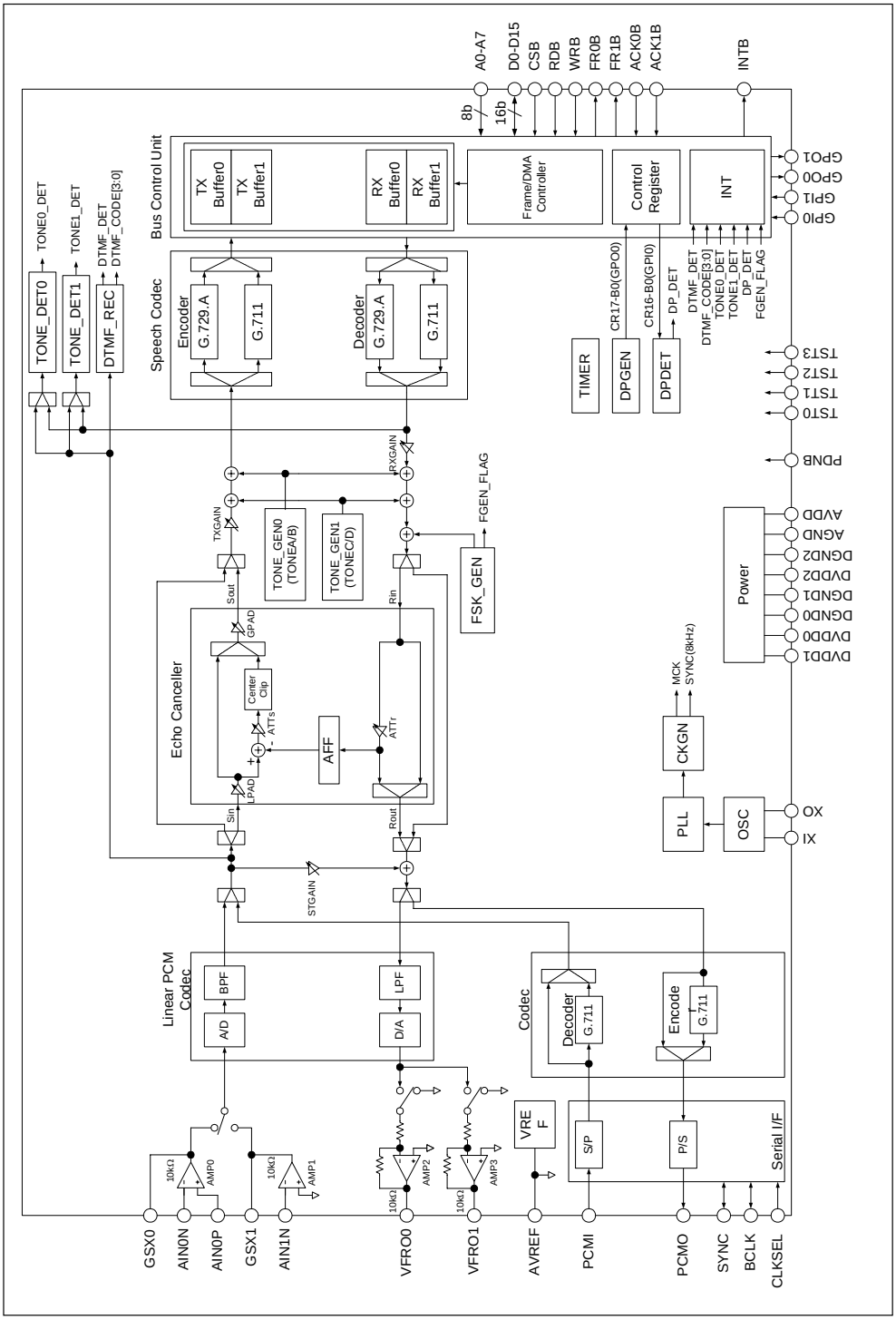
## GENERAL DESCRIPTION

The ML7074-004GA is a speech CODEC for VoIP. This LSI allows selection of G.729.A, or G.711 standard as a speech CODEC. The LSI is optimum for adding VoIP functions to TAs, routers, etc., since it has the functions of an echo canceller for 32 ms delay, DTMF detection, tone detection, tone generation, etc.

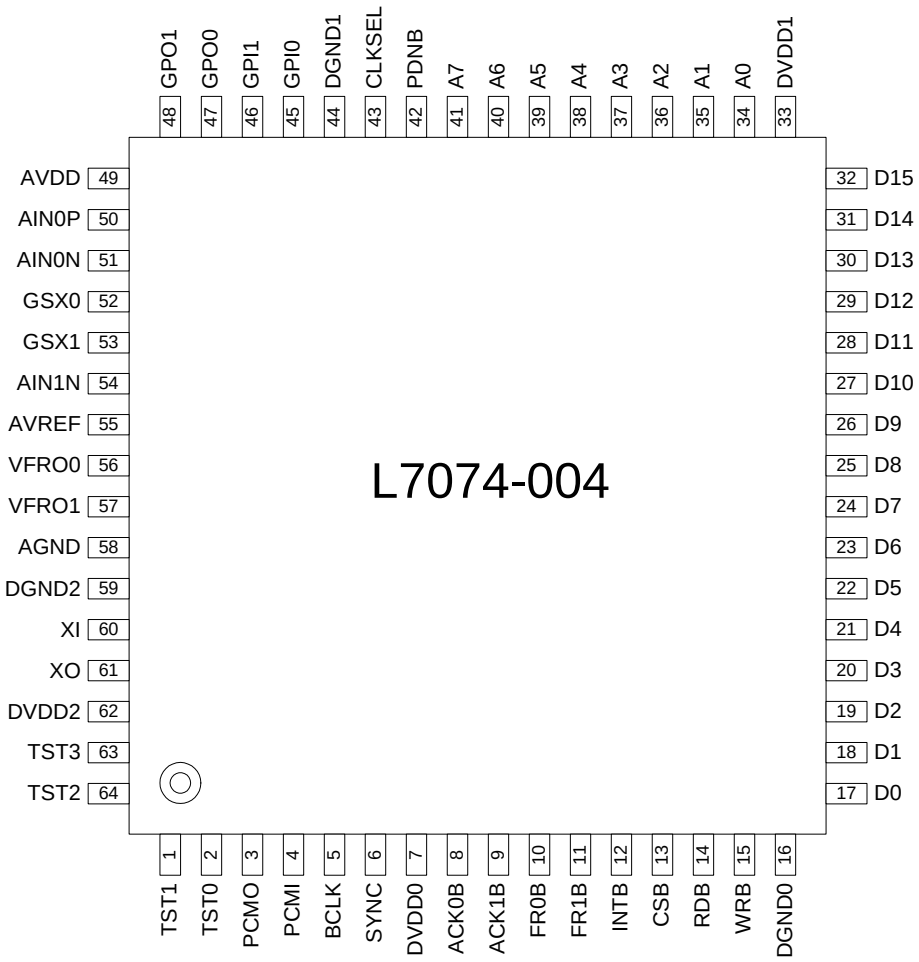
## FEATURES

- Single 3.3 V power supply operation ($DV_{DD}$0, 1, 2, $AV_{DD}$: 3.0 to 3.6 V)
- Speech CODEC:
  Selectable among G.729.A (8 kbps), G.711 (64 kbps) μ-law, and A-law
  Supports PLC (Packet Loss Concealment) function conforming to ITU-T G.711 Appendix I
- Echo canceller for 32 ms delay
- DTMF detect function
- Tone detect function: 2 systems (1650 Hz, 2100 Hz:  Detect frequency can be changed.)
- Tone generate function: 2 systems
- FSK generation function
- Dial pulse detect function
- Dial pulse transmit function
- Internal 1-channel 16-bit timer
- Built-in FIFO buffers (640 bytes) for transferring transmit and receive data
  Frame/DMA (slave) interface selectable.
- Master clock frequency: 4.096 MHz (crystal oscillation or external input)
- Hardware or software power down operation possible.
- Analog input/output type:
  Two built-in input amplifiers
  Two built-in output amplifiers, 10 kΩ driving
- Package:
  64-pin plastic QFP (QFP64-P-1414-0.80-BK)

## BLOCK DIAGRAM



## PIN ASSIGNMENT (TOP VIEW)




**64-pin plastic QFP**

## PIN DESCRIPTIONS

| Pin No. | Symbol | I/O | PDNB = "0" | Description |
|---|---|---|---|---|
| 1 | TST1 | I | "0" | Test control input 1: Normally input "0". |
| 2 | TST0 | I | "0" | Test control input 0: Normally input "0". |
| 3 | PCMO | O | "Hi-z" | PCM data output |
| 4 | PCMI | I | I | PCM data input |
| 5 | BCLK | I/O | I | CLKSEL = "0"<br>PCM shift clock input |
| | | | "L" | CLKSEL = "1"<br>PCM shift clock output |
| 6 | SYNC | I/O | I | CLKSEL = "0"<br>PCM sync signal 8 kHz input |
| | | | "L" | CLKSEL = "1"<br>PCM sync signal 8 kHz output |
| 7 | $DV_{DD}0$ | — | — | Digital power supply |
| 8 | ACK0B | I | I | Transmit buffer DMA access acknowledge signal input |
| 9 | ACK1B | I | I | Receive buffer DMA access acknowledge signal input |
| 10 | FR0B<br>(DMARQ0B) | O | "H" | FR0B: (CR11-B7 = "0")<br>Transmit buffer frame signal output<br>DMARQ0B: (CR11-B7 = "1")<br>Transmit buffer DMA access request signal output |
| 11 | FR1B<br>(DMARQ1B) | O | "H" | FR1B: (CR11-B7 = "0")<br>Receive buffer frame signal output<br>DMARQ1B: (CR11-B7 = "1")<br>Receive buffer DMA access request signal output |
| 12 | INTB | O | "H" | Interrupt request output<br>"L" level is output for about 1.0 μs when an interrupt is generated. |
| 13 | CSB | I | I | Chip select control input |
| 14 | RDB | I | I | Read control input |
| 15 | WRB | I | I | Write control input |
| 16 | DGND0 | — | I | Digital ground (0.0 V) |
| 17 | D0 | I/O | I | Data input/output |
| 18 | D1 | I/O | I | Data input/output |
| 19 | D2 | I/O | I | Data input/output |
| 20 | D3 | I/O | I | Data input/output |
| 21 | D4 | I/O | I | Data input/output |
| 22 | D5 | I/O | I | Data input/output |
| 23 | D6 | I/O | I | Data input/output |
| 24 | D7 | I/O | I | Data input/output |
| 25 | D8 | I/O | I | Data input/output<br>Fix to input state when using in 8-bit bus access (CR11-B5 = "1"). |
| 26 | D9 | I/O | I | Data input/output<br>Fix to input state when using in 8-bit bus access (CR11-B5 = "1"). |
| 27 | D10 | I/O | I | Data input/output<br>Fix to input state when using in 8-bit bus access (CR11-B5 = "1"). |
| 28 | D11 | I/O | I | Data input/output<br>Fix to input state when using in 8-bit bus access (CR11-B5 = "1"). |
| 29 | D12 | I/O | I | Data input/output<br>Fix to input state when using in 8-bit bus access (CR11-B5 = "1"). |
| 30 | D13 | I/O | I | Data input/output<br>Fix to input state when using in 8-bit bus access (CR11-B5 = "1"). |
| 31 | D14 | I/O | I | Data input/output<br>Fix to input state when using in 8-bit bus access (CR11-B5 = "1"). |
| 32 | D15 | I/O | I | Data input/output<br>Fix to input state when using in 8-bit bus access (CR11-B5 = "1"). |

| Pin No. | Symbol | I/O | PDNB = "0" | Description |
|---|---|---|---|---|
| 33 | $DV_{DD}1$ | — | — | Digital power supply |
| 34 | A0 | I | I | Address input |
| 35 | A1 | I | I | Address input |
| 36 | A2 | I | I | Address input |
| 37 | A3 | I | I | Address input |
| 38 | A4 | I | I | Address input |
| 39 | A5 | I | I | Address input |
| 40 | A6 | I | I | Address input |
| 41 | A7 | I | I | Address input |
| 42 | PDNB | I | "0" | Power down input<br>"0": Power down reset<br>"1": Normal operation |
| 43 | CLKSEL | I | I | SYNC and BCLK I/O control input<br>"0": SYNC and BCLK become inputs<br>"1": SYNC and BCLK become outputs |
| 44 | DGND1 | — | — | Digital ground (0.0 V) |
| 45 | GPI0 | I | I | General-purpose input pin 0 (5 V tolerant input)<br>/Secondary function: Dial pulse detect input pin |
| 46 | GPI1 | I | I | General-purpose input pin 1 (5 V tolerant input) |
| 47 | GPO0 | O | "L" | General-purpose output pin 0 (5 V tolerant output, can be pulled up externally)<br>/Secondary function: Dial pulse transmit pin |
| 48 | GPO1 | O | "L" | General-purpose output pin 1 (5 V tolerant output, can be pulled up externally) |
| 49 | $AV_{DD}$ | — | — | Analog power supply |
| 50 | AIN0P | I | I | AMP0 non-inverted input |
| 51 | AIN0N | I | I | AMP0 inverted input |
| 52 | GSX0 | O | "Hi-z" | AMP0 output (10 kΩ driving) |
| 53 | GSX1 | O | "Hi-z" | AMP1 output (10 kΩ driving) |
| 54 | AIN1N | I | I | AMP1 inverted input |
| 55 | AVREF | O | "L" | Analog signal ground (1.4 V) |
| 56 | VFRO0 | O | "Hi-z" | AMP2 Output (10 kΩ driving) |
| 57 | VFRO1 | O | "Hi-z" | AMP3 Output (10 kΩ driving) |
| 58 | AGND | — | | Analog ground (0.0 V) |
| 59 | DGND2 | — | | Digital ground (0.0 V) |
| 60 | XI | I | I | 4.096 MHz crystal oscillator I/F, 4.096 MHz clock input |
| 61 | XO | O | "H" | 4.096 MHz crystal oscillator I/F |
| 62 | $DV_{DD}2$ | — | | Digital power supply |
| 63 | TST3 | I | "0" | Test control input 3: Normally input "0". |
| 64 | TST2 | I | "0" | Test control input 2: Normally input "0". |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Conditions | Rating | Unit |
|---|---|---|---|---|
| Analog power supply voltage | VDA | — | –0.3 to 5.0 | V |
| Digital power supply voltage | $V_{DD}$ | — | –0.3 to 5.0 | V |
| Analog input voltage | VAIN | Analog pins | –0.3 to $V_{DD}$ + 0.3 | V |
| Digital input voltage | VDIN1 | Normal digital pins | –0.3 to $V_{DD}$ + 0.3 | V |
| | VDIN2 | 5 V tolerant pins | –0.3 to 6.0 | V |
| Storage temperature range | Tstg | — | –55 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

(Unless otherwise specified, $AV_{DD}$ = 3.0 to 3.6 V, $DV_{DD}$0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to +60°C)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Analog power supply voltage | VDA | — | 3.0 | 3.3 | 3.6 | V |
| Digital power supply voltage | $V_{DD}$ | — | 3.0 | 3.3 | 3.6 | V |
| Operating temperature range | Ta | — | –20 | — | 60 | °C |
| Digital high level input voltage | VIH1 | Digital input pins | 2.0 | — | $V_{DD}$+ 0.3 | V |
| | VIH2 | GPI0 and GPI1 pins | 2.0 | — | 5.5 | V |
| Digital low level input voltage | VIL | Digital pins | –0.3 | — | 0.8 | V |
| Digital input rise time | tIR | Digital pins | — | 2 | 20 | ns |
| Digital input fall time | tIF | Digital pins | — | 2 | 20 | ns |
| Digital output load capacitance | CDL | Digital pins | — | — | 50 | pF |
| Capacitance of bypass capacitor for AVREF | Cvref | Between AVREF and AGND | 2.2+0.1 | — | 4.7+0.1 | µF |
| Master clock frequency | Fmck | MCK | –0.01% | 4.096 | +0.01% | MHz |
| PCM shift clock frequency | Fbclk | BCLK (at input) | 64 | — | 2048 | kHz |
| PCM sync signal frequency | Fsync | SYNC (at input) | — | 8.0 | — | kHz |
| Clock duty ratio | DRCLK | MCK, BCLK (at input) | 40 | 50 | 60 | % |
| PCM sync timing | tBS | BCLK to SYNC (at input) | 100 | — | — | ns |
| | tSB | SYNC to BCLK (at input) | 100 | — | — | ns |
| PCM sync signal width | tWS | SYNC (at input) | 1BCLK | — | 100 | µs |

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

(Unless otherwise specified, $AV_{DD}$ = 3.0 to 3.6 V, $DV_{DD}$0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to +60°C)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power supply current | ISS | Standby state (PDNB = "0", $V_{DD}$ = 3.3 V, Ta = 25°C) | — | 5.0 | 20.0 | µA |
| | $I_{DD}1$ | Operating state 1 In the PCM/IF mode (SC_EN = "1", PCMIF_EN = "1", AFE_EN = "1") Connect a 4.096 MHz crystal oscillator between XI and XO. | — | 45.0 | 55.0 | mA |
| | $I_{DD}2$ | Operating state 2 When operating the whole system (SC_EN = "1", PCMIF_EN = "0", AFE_EN = "0") Connect a 4.096 MHz crystal oscillator between XI and XO. | — | 50.0 | 65.0 | mA |
| Digital input pin input leakage current | IIH | Vin = $DV_{DD}$ | — | 0.01 | 1.0 | µA |
| | IIL | Vin = DGND | –1.0 | –0.01 | — | µA |
| Digital I/O pin output leakage current | IOZH | Vout = $DV_{DD}$ | — | 0.01 | 1.0 | µA |
| | IOZL | Vout = DGND | –1.0 | –0.01 | — | µA |
| High level output voltage | VOH | Digital output pins, I/O pins IOH = 4.0 mA IOH = 1.0 mA (XO pin) | 2.2 | — | — | V |
| Low level output voltage | VOL | Digital output pins, I/O pins IOL = –4.0 mA IOL = –1.0 mA (XO pin) | — | — | 0.4 | V |
| Input capacitance *1 | CIN | Input pins | — | 8 | 12 | pF |

Note: *1 Guaranteed design value

**Analog Interface**

(Unless otherwise specified, $AV_{DD}$ = 3.0 to 3.6 V, $DV_{DD}$0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to +60°C)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input resistance *1 | RIN | AIN0N, AIN0P, AIN1N | 10 | — | — | MΩ |
| Output load resistance | RL | GSX0, GSX1, VFRO0, VFRO1 | 10 | — | — | kΩ |
| Output load capacitance | CL | Analog output pins | — | — | 50 | pF |
| Offset voltage | VOF | VFRO0, VFRO1 | –40 | — | 40 | mV |
| Output voltage level *2 | VO | GSX0, GSX1, VFRO0, VFRO1 RL = 10 kΩ | — | — | 1.3 | Vpp |

Notes:

*1 Guaranteed design value

*2 –7.7 dBm (600Ω) = 0 dBm0, +3.17 dBm0 = 1.3 Vpp

## AC Characteristics

### CODEC (Speech CODEC in G.711 (μ-law) Mode)

(Unless otherwise specified, $AV_{DD}$ = 3.0 to 3.6 V, $DV_{DD}$0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to +60°C)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | Frequency (Hz) | Level (dBm0) | | | | |
| Transmit frequency characteristics | LT1 | 0 to 60 | 0 | 25 | — | — | dB |
| | LT2 | 300 to 3000 | | –0.15 | — | 0.20 | dB |
| | LT3 | 1020 | | Reference value | | | — |
| | LT4 | 3300 | | –0.15 | — | 0.80 | dB |
| | LT5 | 3400 | | 0 | — | 0.80 | dB |
| | LT6 | 3968.75 | | 13 | — | — | dB |
| Receive frequency characteristics | LR2 | 0 to 3000 | 0 | –0.15 | — | 0.20 | dB |
| | LR3 | 1020 | | Reference value | | | — |
| | LR4 | 3300 | | –0.15 | — | 0.80 | dB |
| | LR5 | 3400 | | 0 | — | 0.80 | dB |
| | LR6 | 3968.75 | | 13 | — | — | dB |
| Transmit signal to noise ratio [*1] | SDT1 | 1020 | 3 | 35 | — | — | dBp |
| | SDT2 | | 0 | 35 | — | — | dBp |
| | SDT3 | | –30 | 35 | — | — | dBp |
| | SDT4 | | –40 | 28 | — | — | dBp |
| | SDT5 | | –45 | 23 | — | — | dBp |
| Receive signal to noise ratio [*1] | SDR1 | 1020 | 3 | 35 | — | — | dBp |
| | SDR2 | | 0 | 35 | — | — | dBp |
| | SDR3 | | –30 | 35 | — | — | dBp |
| | SDR4 | | –40 | 28 | — | — | dBp |
| | SDR5 | | –45 | 23 | — | — | dBp |
| Transmit inter-level loss error | GTT1 | 1020 | 3 | –0.2 | — | 0.2 | dB |
| | GTT2 | | –10 | Reference value | | | — |
| | GTT3 | | –40 | –0.2 | — | 0.2 | dB |
| | GTT4 | | –50 | –0.6 | — | 0.6 | dB |
| | GTT5 | | –55 | –1.2 | — | 1.2 | dB |
| Receive inter-level loss error | GTR1 | 1020 | 3 | –0.2 | — | 0.2 | dB |
| | GTR2 | | –10 | Reference value | | | — |
| | GTR3 | | –40 | –0.2 | — | 0.2 | dB |
| | GTR4 | | –50 | –0.6 | — | 0.6 | dB |
| | GTR5 | | –55 | –1.2 | — | 1.2 | dB |
| Idle channel noise [*1] | NIDLT | — | Analog input = AVREF | — | — | –68 | dBm0p |
| | NIDLR | — | PCMI = "1" | — | — | –72 | dBm0p |
| Transmit absolute level [*2] | AVT | 1020 | 0 | 0.285 | 0.320 | 0.359 | Vrms |
| Receive absolute level [*2] | AVR | 1020 | 0 | 0.285 | 0.320 | 0.359 | Vrms |
| Power supply noise reject ratio | PSRRT | Noise frequency range: 0 to 50 kHz Noise level: 50mVpp | — | 30 | — | — | dB |
| | PSRRR | | — | 30 | — | — | dB |

Notes: *1 Using P-message filter

*2 0.320 Vrms = 0 dBm0 = –7.7 dBm (600Ω)

**Gain Setting (Speech CODEC in G.711 (μ-law) Mode)**

(Unless otherwise specified, $AV_{DD}$ = 3.0 to 3.6 V, $DV_{DD}$0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to +60°C)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Transmit and receive gain setting accuracy | GAC | — | –1.0 | — | 1.0 | dB |

**Tone Output (Speech CODEC in G.711 (μ-law) Mode)**

(Unless otherwise specified, $AV_{DD}$ = 3.0 to 3.6 V, $DV_{DD}$0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to +60°C)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Frequency deviation | fDFT | Relative to set frequency | –1.5 | — | 1.5 | % |
| Output level | oLEV | Relative to set gain | –2.0 | — | 2.0 | dB |

**DTMF Detector, Other Detectors (Speech CODEC in G.711 (μ-law) Mode)**

(Unless otherwise specified, $AV_{DD}$ = 3.0 to 3.6 V, $DV_{DD}$0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to +60°C)

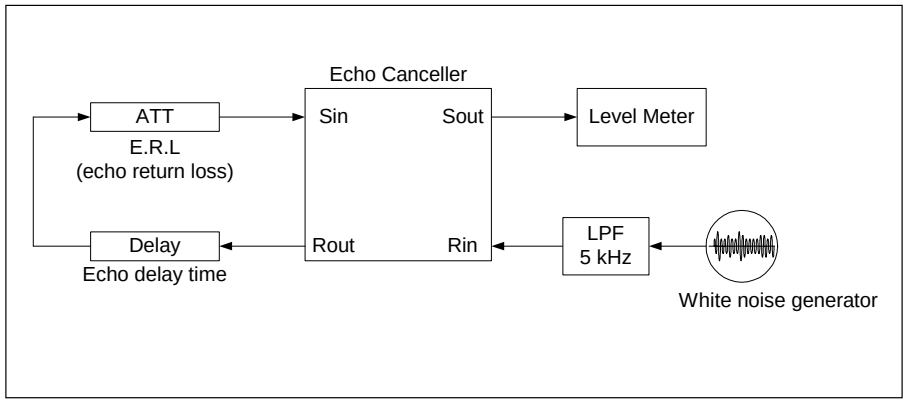
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Detect level accuracy | dLAC | Relative to set detect level | –2.5 | — | 2.5 | dB |

**Echo Canceller**

(Unless otherwise specified, $AV_{DD}$ = 3.0 to 3.6 V, $DV_{DD}$0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to +60°C)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Echo attenuation | eRES | In the analog I/F mode<br>In the PCM I/F (16-bit linear) mode | — | 35 | — | dB |
| | | In the PCM I/F (G.711) mode | | 30 | | |
| Erasable echo delay time | tECT | — | — | — | 32 | ms |

Measurement method



**PDNB, XO, AVREF Timings**

(Unless otherwise specified, $AV_{DD}$ = 3.0 to 3.6 V, $DV_{DD}$0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = −20 to +60°C)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power down signal pulse width | tPDNB | PDNB pin | 1 | — | — | µs |
| Oscillation start-up time | txtal | — | — | 2+α | 100 | ms |
| AVREF rise time | tAVREF | AVREF = 1.4 (90%)<br>C5 = 4.7 µF, C6 = 0.1 µF<br>(See Fig. 9.) | — | — | 600 | ms |
| Initialization mode start-up time | tINIT | — | — | 1 | — | s |

* α is a value that depends on the oscillation stabilizing time when using a crystal oscillator.

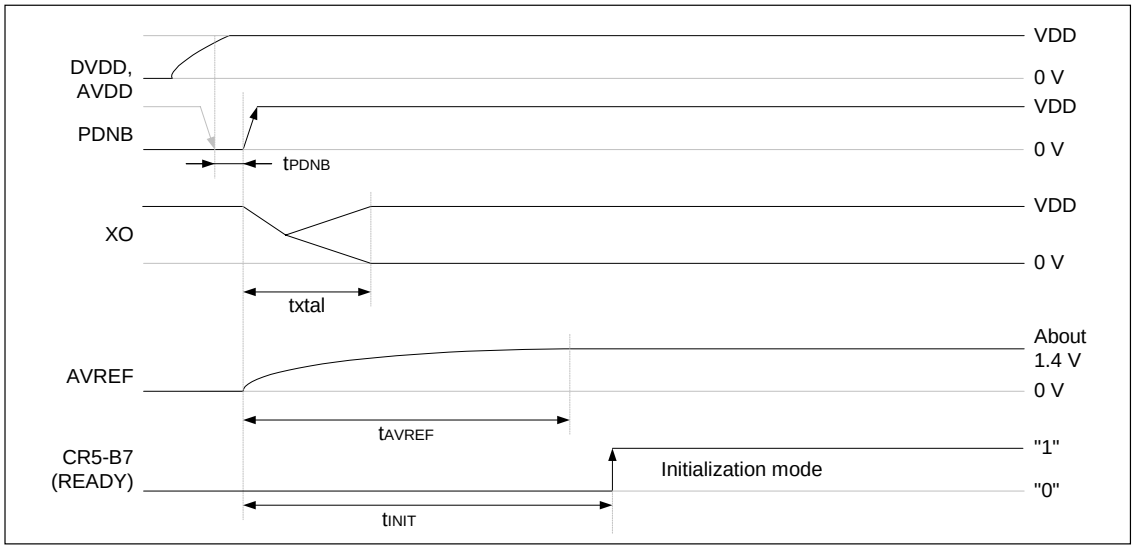



**Fig. 1 PDNB, XO, and AVREF timings**

**PCM I/F Mode**

(Unless otherwise specified, $AV_{DD}$ = 3.0 to 3.6 V, $DV_{DD}$0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = −20 to +60°C)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Bit clock frequency | fBCLK | CDL = 20pF(at output) | −0.1% | 64 | +0.1% | kHz |
| Bit clock duty ratio | dBCLK | CDL = 20pF(at output) | 45 | 50 | 55 | % |
| Sync signal frequency | fSYNC | CDL = 20pF(at output) | −0.1% | 8 | +0.1% | kHz |
| Sync signal duty ratio | dSYNC1 | CDL = 20pF(at output) At 64 kHz output | 12.4 | 12.5 | 12.6 | % |
| | dSYNC2 | CDL = 20pF(at output) At 128 kHz output | 6.24 | 6.25 | 6.26 | % |
| Transmit/receive signal sync timing | tBS | BCLK to SYNC (at output) | 100 | — | — | ns |
| | tSB | SYNC to BCLK (at output) | 100 | — | — | ns |
| Input setup time | tDS | — | 100 | — | — | ns |
| Input hold time | tDH | — | 100 | — | — | ns |
| Digital output delay time | tSDX | PCMO pin Pull-up, pull-down resistors RDL = 1 kΩ, CDL = 50 pF | — | — | 100 | ns |
| | tXD1 | | — | — | 100 | ns |
| Digital output hold time | tXD2 | | — | — | 100 | ns |
| | tXD3 | | — | — | 100 | ns |

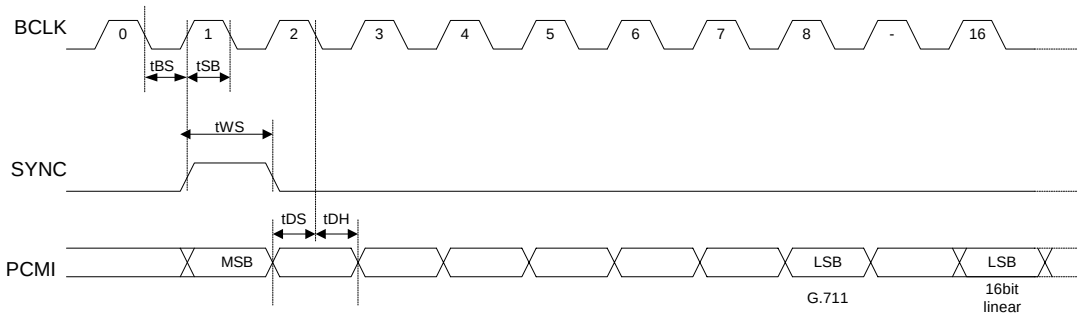



**Fig. 2 PCM I/F mode input timing (long frame)**

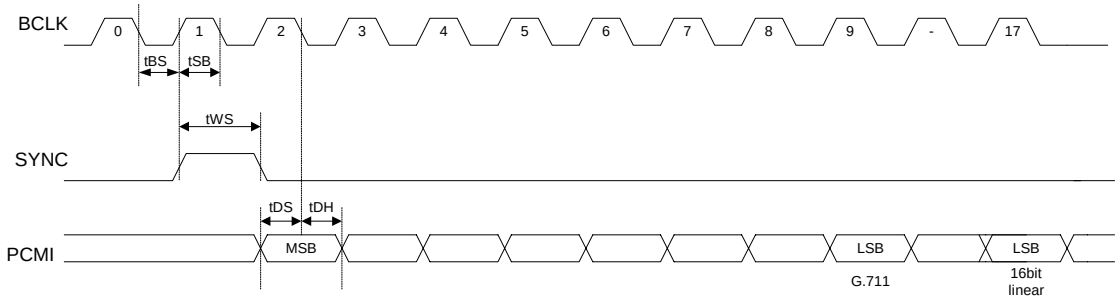



**Fig. 3 PCM I/F mode input timing (short frame)**

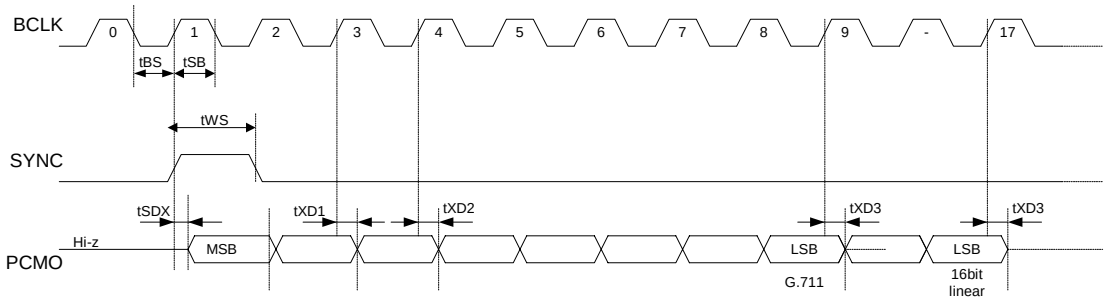



**Fig. 4 PCM I/F mode output timing (long frame)**

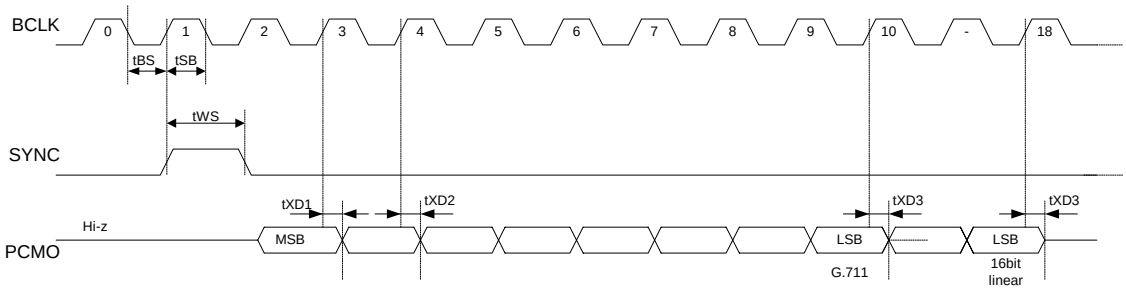



**Fig. 5 PCM I/F mode output timing (short frame)**

**Control Register Interface**

(Unless otherwise specified, $AV_{DD}$ = 3.0 to 3.6 V, $DV_{DD}$0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to +60°C)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Address setup time | tAS | CL = 50 pF | 10 | — | — | ns |
| Address hold time | tAH | | 10 | — | — | ns |
| Write data setup time | tWDS | | 10 | — | — | ns |
| Write data hold time | tWDH | | 10 | — | — | ns |
| CSB setup time | tCS | | 10 | — | — | ns |
| CSB hold time | tCH | | 10 | — | — | ns |
| WRB pulse width | tWW | | 10 | — | — | ns |
| Read data output delay time | tRDD | | — | — | 20 | ns |
| Read data output hold time | tRDH | | 3 | — | — | ns |
| RDB pulse width | tRW | | 25 | — | — | ns |
| CSB disable time | tCD | | 10 | — | — | ns |

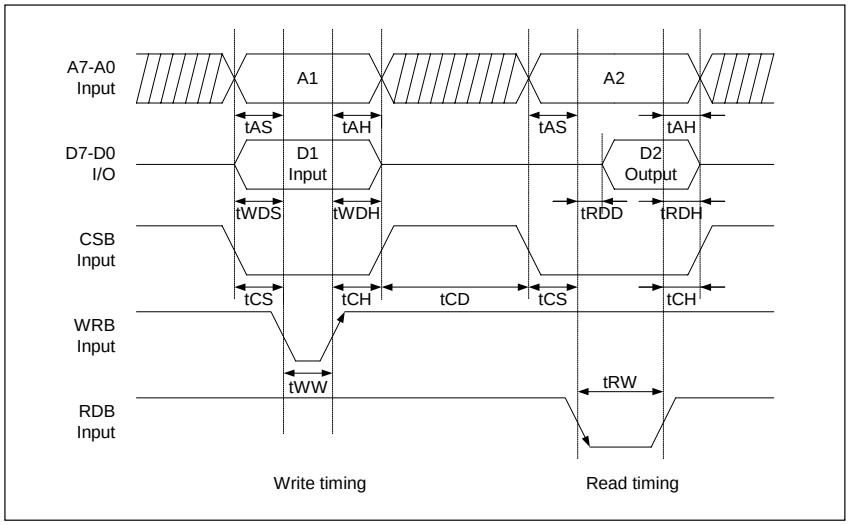



**Fig. 6 Control register interface**

**Transmit and Receive Buffer Interface (in Frame Mode)**

(Unless otherwise specified, $AV_{DD}$ = 3.0 to 3.6 V, $DV_{DD}$0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = −20 to +60°C)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| FR1B setup time | tF1S | CL = 50 pF | 3 | — | — | ns |
| FR1B output delay time | tF1D | | — | — | 20 | ns |
| Address setup time | tAS | | 10 | — | — | ns |
| Address hold time | tAH | | 10 | — | — | ns |
| Write data setup time | tWDS | | 10 | — | — | ns |
| Write data hold time | tWDH | | 10 | — | — | ns |
| CSB setup time | tCS | | 10 | — | — | ns |
| CSB hold time | tCH | | 10 | — | — | ns |
| WRB pulse width | tWW | | 10 | — | — | ns |
| FR0B setup time | tF0S | | 3 | — | — | ns |
| FR0B output delay time | tF0D | | — | — | 20 | ns |
| Read data output delay time | tRDD | | — | — | 30 | ns |
| Read data output hold time | tRDH | | 3 | — | — | ns |
| RDB pulse width | tRW | | 35 | — | — | ns |
| CSB disable time | tCD | | 10 | — | — | ns |

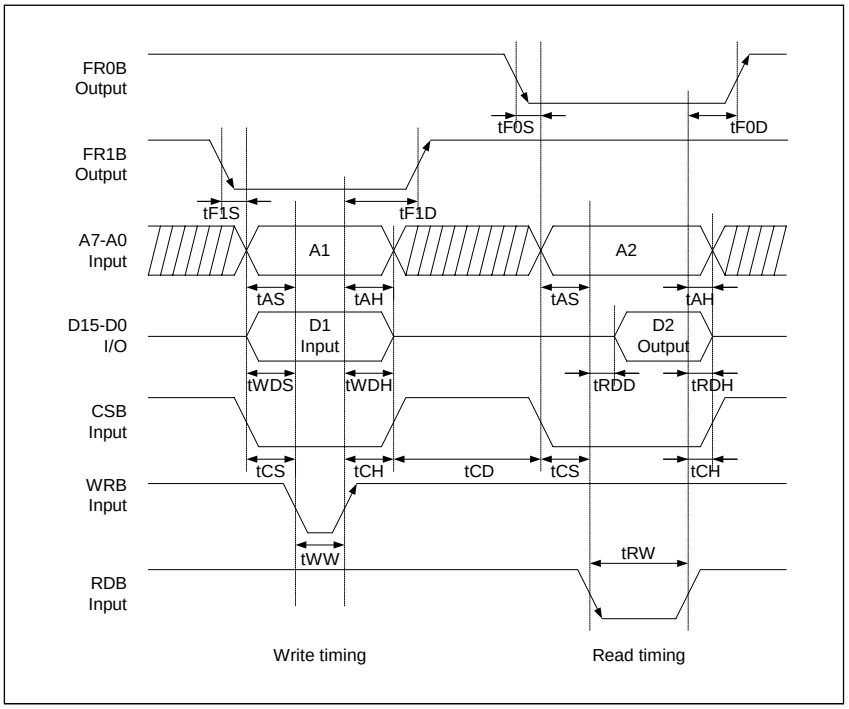



**Fig. 7 Transmit and receive buffer interface (in frame mode)**

**Transmit and Receive Buffer Interface (in DMA Mode)**

(Unless otherwise specified, $AV_{DD}$ = 3.0 to 3.6 V, $DV_{DD}$0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = −20 to +60°C)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| DMARQ1B setup time | tDR1S | CL = 50 pF | 3 | — | — | ns |
| DMARQ1B output delay time | tDR1RD | | — | — | 25 | ns |
| | tDR1FD | | — | — | 25 | ns |
| Address setup time | tAS | | 10 | — | — | ns |
| Address hold time | tAH | | 10 | — | — | ns |
| Write data setup time | tWDS | | 10 | — | — | ns |
| Write data hold time | tWDH | | 10 | — | — | ns |
| ACK setup time | tAKS | | 10 | — | — | ns |
| ACK hold time | tAKH | | 10 | — | — | ns |
| WRB pulse width | tWW | | 10 | — | — | ns |
| DMARQ0B setup time | tDR0S | | 3 | — | — | ns |
| DMARQ0B output delay time | tDR0RD | | — | — | 20 | ns |
| | tDR0FD | | — | — | 25 | ns |
| Read data output delay time | tRDD | | — | — | 30 | ns |
| Read data output hold time | tRDH | | 3 | — | — | ns |
| RDB pulse width | tRW | | 35 | — | — | ns |
| ACKB disable time | tAD | | 10 | — | — | ns |

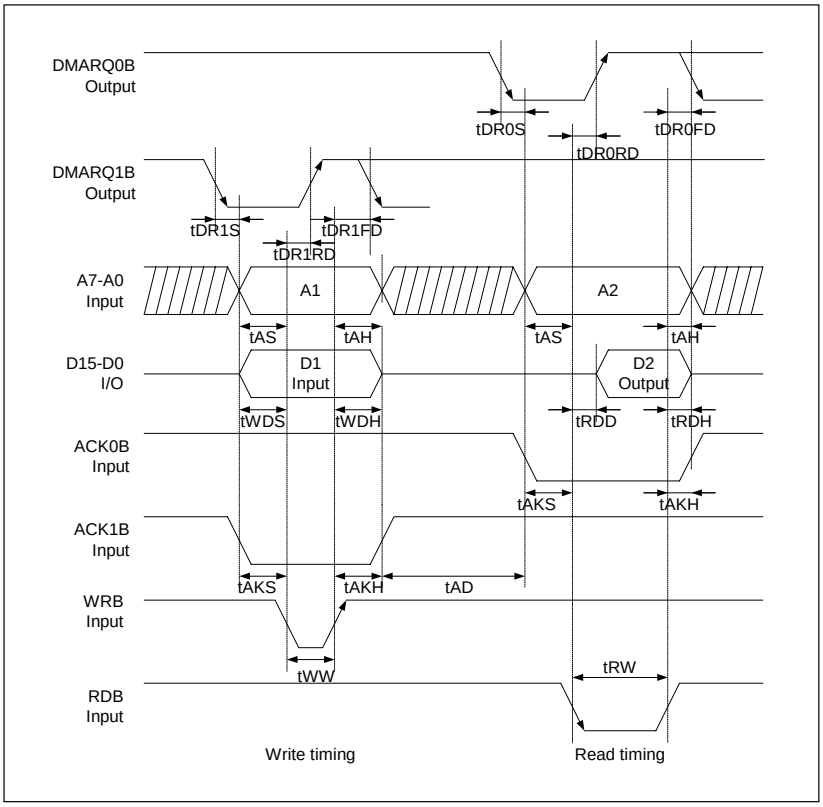



**Fig. 8 Transmit and receive buffer interface (in DMA mode)**

## PIN FUNCTION DESCRIPTIONS

### AIN0N, AIN0P, GSX0, AIN1N, GSX1

These are the analog transmit input and transmit level adjust pins. Each of AIN0N and AIN1N is connected to each of the inverting input pins of the built-in transmit amplifiers AMP0 and AMP1, and AIN0P is connected to the non-inverting input pin of AMP0. In addition, GSX0 and GSX1 are connected to the output pins of AMP0 and AMP1, respectively. The selection between AMP0 and AMP1 is made by CR10-B0. See Fig. 9 for the method of making level adjustment. During the power down mode (when PDNB = "0" or CR0-B7 = "1"), the outputs of GSX0 and GSX1 go to the high impedance state. If AMP0 is not used in the specific application of this LSI, short GSX0 with AIN0N and connect AIN0P with AVREF. When AMP1 is not used, short GSX1 with AIN1N.

Notice:
It is recommended to select the amplifier to be used before the conversation starts, since a small amount of noise will be generated if the amplifier selection is changed while conversation is in progress.

### VFRO0, VFRO1

These are analog receive output pins and are connected to the output pins of the built-in receive amplifiers AMP2 and AMP3, respectively. The output signals of VFRO0 and VFRO1 can be selected using CR10-B1 and CR10-B2, respectively. When selected ("1"), the received signal will be output, and when deselected ("0"), the AVREF signal (about 1.4 V) will be output. In the power down mode, these pins will be in the high impedance state. It is recommended to use these output signals via DC coupling capacitors.

Notice:
It is recommended to select the amplifier to be used before the conversation starts, since a small amount of noise is generated if the output selection is changed while the conversation is in progress.
At the time of resetting or releasing from the reset state, it is recommended to select the AVREF as outputs of VFRO0 and VFRO1.

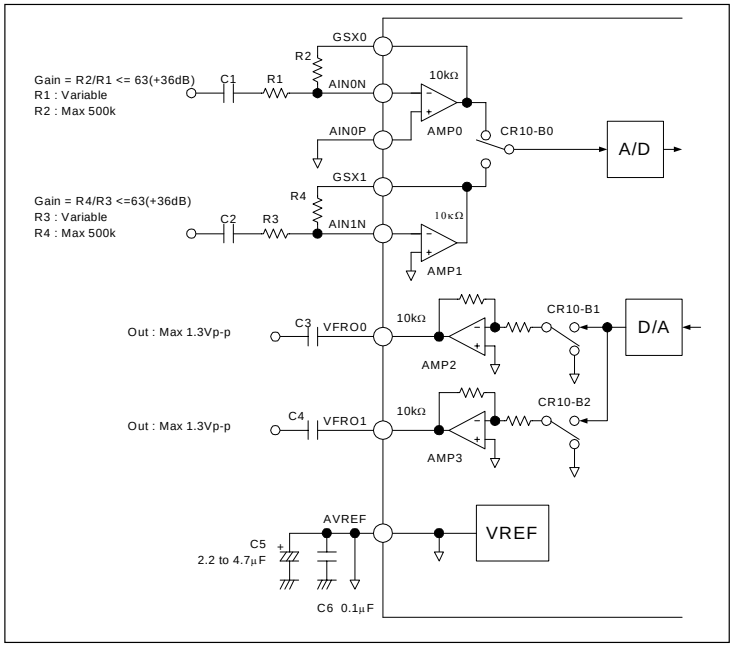
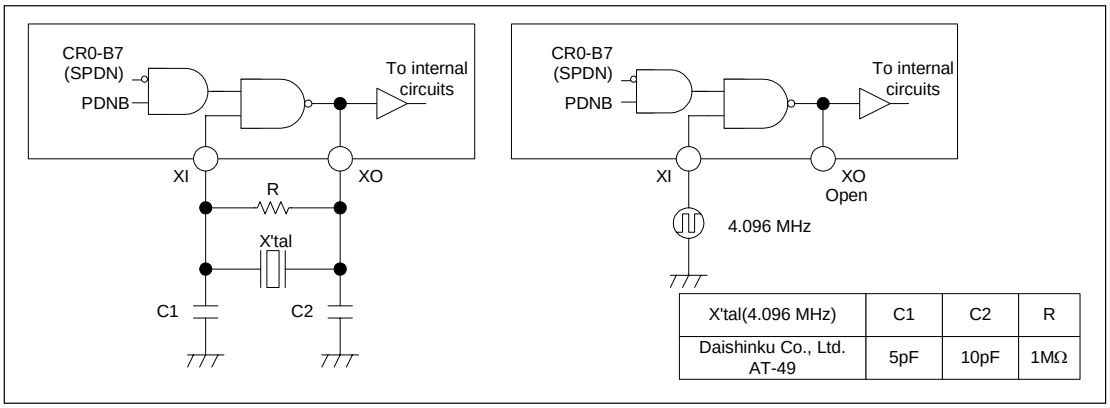



**Fig. 9 Analog interface**

**AVREF**
This is the output pin for the analog signal ground potential. The output potential at this pin will be about 1.4 V. Connect a 2.2 to 4.7 μF (aluminum electrolytic type) capacitor and a 0.1 μF (ceramic type) capacitor in parallel between this pin and the GND pin as bypass capacitors. The output at the AVREF pin goes to 0.0 V in the power down mode. The voltage starts rising after the power down mode is released (PDNB = "1" and also CR0-B7 = "0"). The rise time is about 0.6 seconds.

**XI, XO**
These are the pins for either connecting the crystal oscillator for the master clock or for inputting an external master clock signal.
The oscillations of the master clock oscillator will be stopped during a power down due to the PDNB signal or during a software power down due to CR0-B7 (SPDN). The oscillations start when the power down condition is released, and the internal clock supply of the LSI will be started after counting up the oscillation stabilization period (of about 16 ms). Examples of crystal oscillator connection and external master clock input are shown in Fig. 10.




| X'tal(4.096 MHz) | C1 | C2 | R |
|---|---|---|---|
| Daishinku Co., Ltd. AT-49 | 5pF | 10pF | 1MΩ |

**Fig. 10 Examples of oscillator circuit and clock input**

**PDNB**
This is the power down control input pin. The power down mode is entered when this pin goes to "0". In addition, this pin also has the function of resetting the LSI. In order to prevent wrong operation of the LSI, carry out the initial power-down reset after switching on the power using this PDNB pin. Also, keep the PDNB pin at "0" level for 1 μs or more to initiate the power down state.
Further, it is possible to carry out a power down reset of the LSI when the power is being supplied by performing control of CR0-B7 (SPDN) in the sequence "0" → "1" → "0".
The READY signal (CR5-B7) goes to "1" about 1.0 second after the power down mode is released thereby entering the mode of setting various functions (initialization mode). See Fig. 1 for the timings of PDNB and AVREF, XO, and the initialization mode.

Notice: At the time of switching on the power, start from the power down mode using PDNB.

**$DV_{DD}0$, $DV_{DD}1$, $DV_{DD}2$, $AV_{DD}$**
These are power supply pins. $DV_{DD}0$, 1, 2 are the power supply pins for the digital circuits while $AV_{DD}$ is the power supply pin for the analog circuits of the LSI. Connect these pins together in the neighborhood of the LSI and connect as bypass capacitors a 10 μF electrolytic capacitor and a 0.1 μF ceramic capacitor in parallel between the DGND and AGND pins.

**DGND0, DGND1, DGND2, AGND**
These are ground pins. GDND0, 1, 2 are the ground pins for the digital circuits and AGND is the ground pin for the analog circuits of the LSI. Connect these pins together in the neighborhood of the LSI.

**TST0, TST1, TST2, TST3**
These are input pins for testing purposes only. Keep the inputs to these pins at the "0" level during normal use conditions.

**INTB**
This is the interrupt request output pin. An "L" level is output for a duration of about 1.0 μs at this pin when there is a change in state of an interrupt cause.
This output will be maintained at the "H" level when there is no change in state of any of the interrupt causes. The actual interrupt cause generating the interrupt can be verified by reading CR3, CR4, and CR5. The different interrupt causes are described below.

- Underflow error (CR3-B0)
  An interrupt is generated when an internal read from the receive buffer occurs before the writing into the receive buffer from the MCU has been completed.
  An interrupt is generated when a normal writing is made in the receive buffer by the MCU and the underflow error is released.

- Overrun error (CR3-B1)
  An interrupt is generated when an internal write of the next data into the transmit buffer occurs before the transmit buffer data read out from the MCU has been completed.
  An interrupt is generated when a normal read out is made from the transmit buffer by the MCU and the overrun error is released.

- When a dial pulse is detected (CR4-B6).

- When a DTMF signal is detected (CR4-B4).

- When DTMF_CODEC0, 1, 2, 3 are detected (CR4-B0, B1, B2, B3).
  An interrupt is generated when a DTMF signal is detected.
  An interrupt is generated when there is a change from the DTMF signal detected state to the no-detected state.
  An interrupt is generated when there is a change in the detected code (CR4-B0, B1, B2, B3) in the condition in which a DTMF signal is being detected.

- When TONE0 is detected (CR3-B3).
  An interrupt is generated when a 1650 Hz tone signal is detected.
  An interrupt is generated when there is a change to the non-detection condition in the tone signal detection condition.

- When TONE1 is detected (CR3-B4).
  An interrupt is generated when a 2100 Hz tone signal is detected.
  An interrupt is generated when there is a change to the non-detection condition in the tone signal detection condition.

- When DSP_ERR is detected (CR3-B7).
  An interrupt is generated when any error occurs in the DSP inside the LSI.

- When FGEN_FLAG is cleared (CR5-B0).
  FGEN_FLAG is cleared to "0" and an interrupt is generated when data settings are enabled to output data setting register FGEN_D[7:0] (CR18) in the FSK generator.

**A0 to A7**
These are the address input pins for use during an access of the frame, DMA, or control registers. The different addresses will be the following.
Transmit buffer (TX Buffer)
A7 to A0 = 10xxxxxxb (the lower 6 bits are not valid)
Receive buffer (RX Buffer)
A7 to A0 = 01xxxxxxb (the lower 6 bits are not valid)
Control register (CR)
A7 to A0 = 00xxxxxxb

**D0 to D15**
These are the data input/output pins for use during an access of the frame, DMA, or control registers. Connect pull-up resistors to these pins since they are I/O pins. When the 8-bit bus access method is selected by CR11-B5, only D0 to D7 become valid. Since the higher 8 bits D8 to D15 will always be in the input state when the 8-bit bus access method is selected (CR11-B5 = "1"), tie them to "0" or "1" inputs.

**CSB**
This is the chip select input pin for use during a frame or control register access.

**RDB**
This is the read enable input pin for use during a frame, DMA, or control register access.

**WRB**
This is the write enable input pin for use during a frame, DMA, or control register access.

**FR0B (DMARQ0B)**

- FR0B (In frame mode, CR11-B7 = "0")
  This is the transmit frame output pin which outputs the signal when the transmit buffer is full during frame access. This pin outputs an "L" level when the transmit buffer becomes full, and maintains that "L" level output until a specific number of words are read out from the MCU.
- DMARQ0B (In DMA mode, CR11-B7 = "1")
  This is the DMA request output pin which outputs the signal when the transmit buffer is full during DMA access. This output becomes "L" when the transmit buffer becomes full, and returns to the "H" level automatically on the falling edge of the read enable signal (RDB = "1" → "0") when there is an acknowledgement signal (ACK0B = "0") from the MCU. This relationship is repeated until a specific number of words are read out from the MCU.

**FR1B (DMARQ1B)**

- FR1B (In frame mode, CR11-B7 = "0")
  This is the receive frame output pin which outputs the signal when the receive buffer is empty during frame access. This pin outputs an "L" level when the receive buffer becomes empty, and maintains that "L" level output until a specific number of words are written from the MCU.
- DMARQ1B (In DMA mode, CR11-B7 = "1")
  This is the DMA request output pin which outputs the signal when the receive buffer is empty during DMA access. This output becomes "L" when the receive buffer becomes empty, and returns to the "H" level automatically on the falling edge of the write enable signal (WRB = "1" → "0") when there is an acknowledgement signal (ACK1B = "0") from the MCU. This relationship is repeated until a specific number of words are written from the MCU.

**ACK0B**

This is the DMA acknowledgement input pin for the DMARQ0B signal during DMA access of the transmit buffer and becomes valid in the DMA mode (CR11-B7 = "1").
Tie this pin to "1" when using this LSI in the frame access mode (CR11-B7 = "0").

**ACK1B**

This is the DMA acknowledgement input pin for the DMARQ1B signal during DMA access of the receive buffer and becomes valid in the DMA mode (CR11-B7 = "1").
Tie this pin to "1" when using this LSI in the frame access mode (CR11-B7 = "0").

**GPI0, GPI1**

These are general-purpose input pins. The state ("1" or "0") of each of these GPI0 and GPI1 pins can be read out respectively from CR16-B0 and CR16-B1. Further, GPI0 becomes the input pin for the dial pulse detector (DPDET) in the secondary functions.

**GPO0, GPO1**

These are general-purpose output pins. The values set in CR17-B0 and CR17-B1 are output at these pins GPO0 and GPO1, respectively. Further, GPO0 becomes the output pin for the dial pulse generator (DPGEN) in the secondary functions.

**CLKSEL**
This is the input/output control input pin of SYNC and BCLK. The pin becomes input at "0" level and output at "1" level.

**SYNC**
This is the 8 kHz sync signal input/output pin of PCM signals. When CLKSEL is "0", input continuously an 8 kHz clock synchronous with BCLK. Further, when CLKSEL is "1", this pin outputs an 8 kHz clock synchronous with BCLK. Long frame synchronization is used when CR0-B1 (LONG/SHORT) is "0" and short frame synchronization is used when it is "1".

**BCLK**
This is the shift clock input/output pin for the PCM signal. When CLKSEL is "0", it is necessary to input to this pin a clock signal that is synchronous with SYNC. Input a 64 to 2048 kHz clock when the G.711 mode has been selected, and input a 128 to 2048 kHz clock when the 16-bit linear mode has been selected. When CLKSEL is "1", this pin outputs a clock that is synchronous with SYNC. This pin outputs a 64 kHz clock when the G.711 mode has been selected, and outputs an 128 kHz clock when the 16-bit linear mode or G.729.A mode has been selected.

Note: The input/output control and frequencies of the above SYNC and BLCK signals will be as shown in Table 1 below.

**Table 1 Input/output control of SYNC and BCLK**

| CLKSEL | SYNC | BCLK | Remarks |
|---|---|---|---|
| "0" | Input<br>(8 kHz) | Input<br>(64 kHz to 2048 kHz) | Input a continuous clock after starting the power supply.<br>Input a 64 to 2048 kHz clock when G.711 is selected.<br>Input a 128 to 2048 kHz clock when 16-bit linear mode is selected. |
| "1" | Output<br>(8 kHz) | Output<br>(64 kHz or 128 kHz) | An "L" level is output during the power down mode.<br>A 64 kHz clock is output when G.711 is selected.<br>A 128 kHz clock is output when G.729.A or 16-bit linear mode is selected. |

**PCMO**
This is the PCM signal output pin for the transmitting section. The PCM signal is output in synchronization with the rising edges of SYNC and BCLK. The PCMO outputs the data only during the valid data segment in the selected coding format and goes to the high impedance state during all other segments. The basic timing chart of the PCM I/F mode is shown in Fig. 11. The PCMO output will be in the high impedance state when the PCM I/F mode is not used (CR12-B0 = "0").

**PCMI**
This is the PCM signal input pin for the receiving section. The data is entered starting from the MSB by shift on the falling edge of BCLK.
The basic timing chart of the PCM I/F mode is shown in Fig. 11.
Fix input to "0" or "1" when the PCM I/F mode (CR12-B0 = "0") is not used.

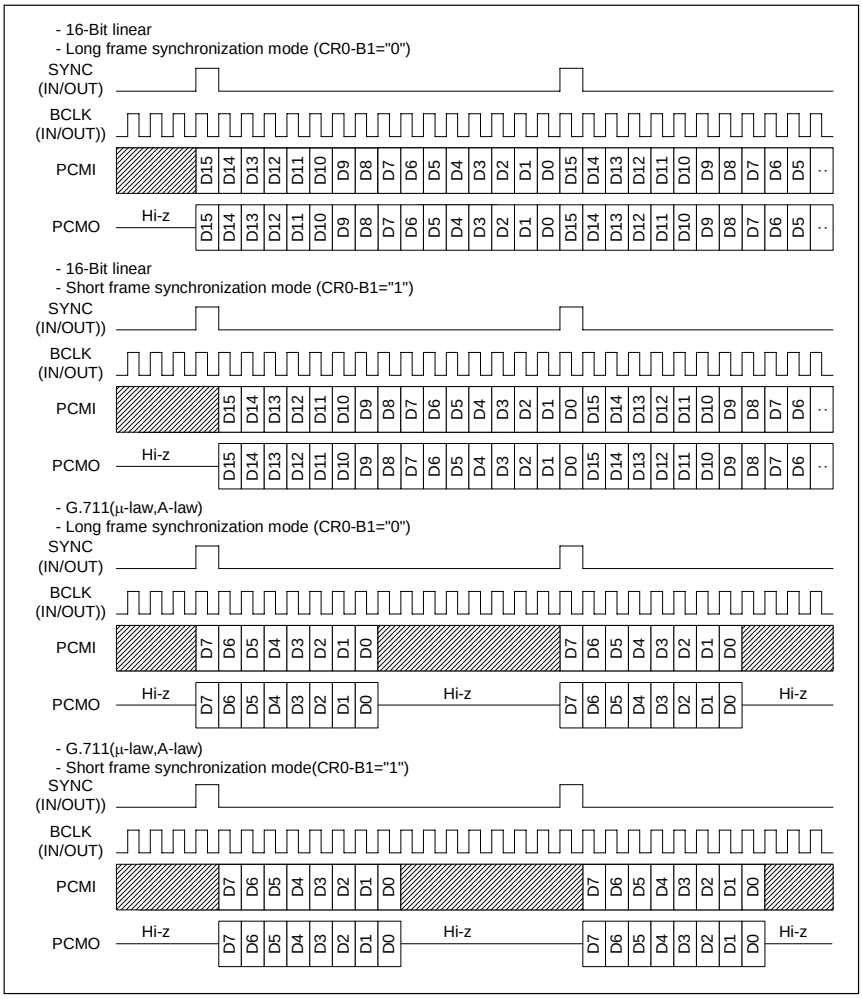
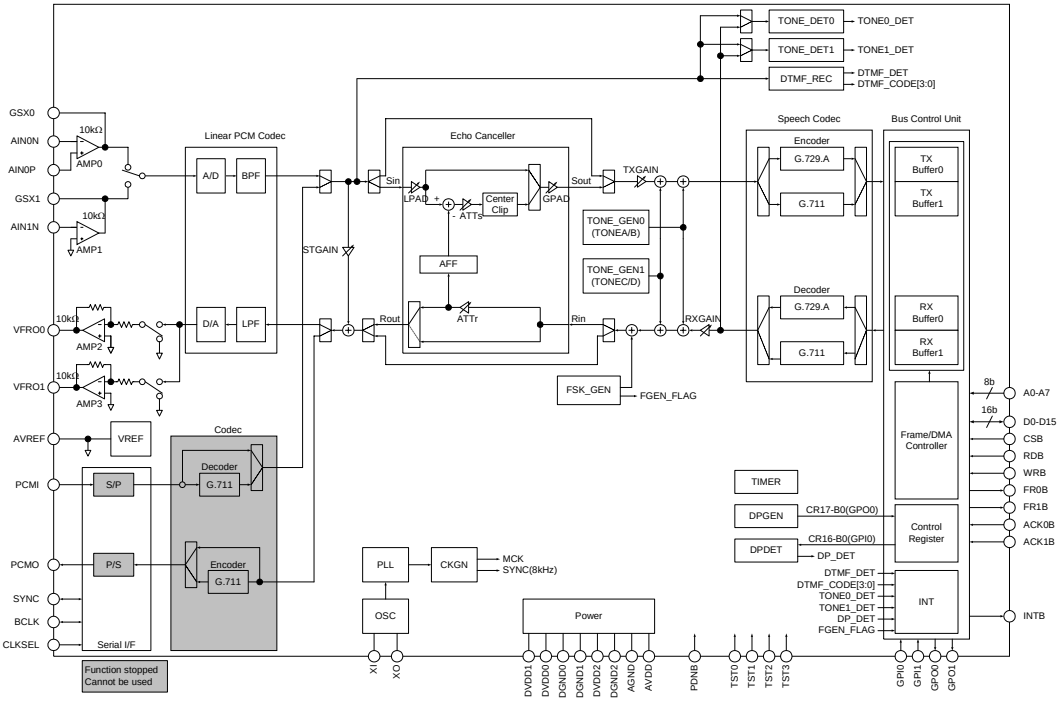



**Fig. 11 PCM I/F mode timing diagram**

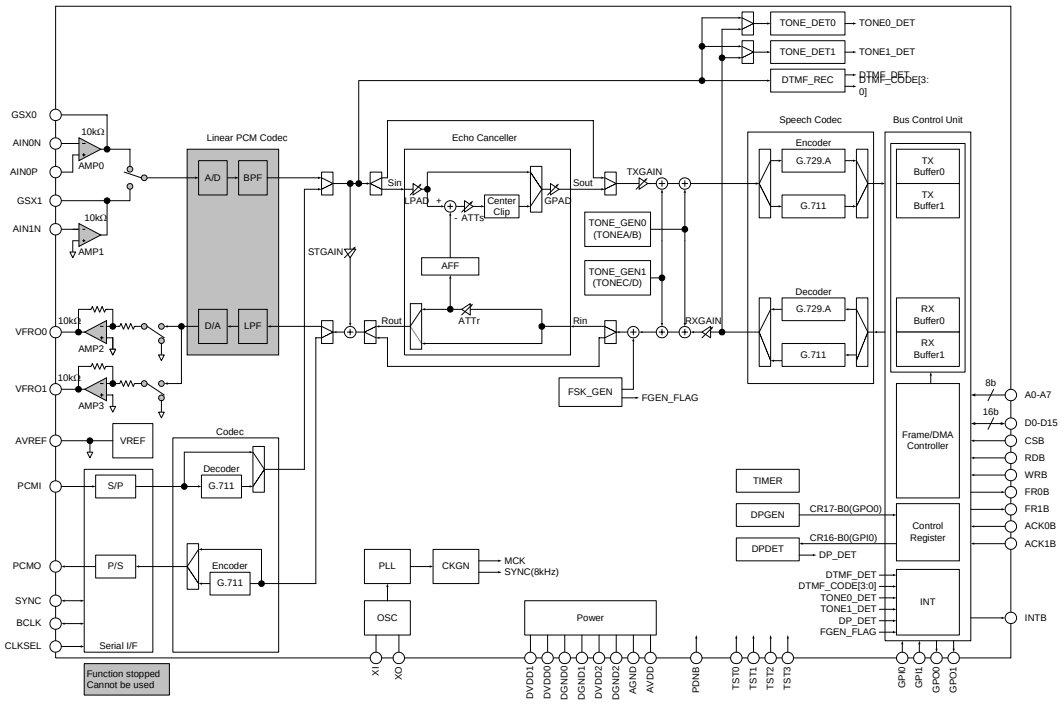
## EXAMPLE OF CONFIGURATION

### Analog I/F mode




Example of settings in the initialization mode
· CR15 = 40h * This is mandatory.
· CR6=0Fh,CR7=FFh,CR8=00h,CR9=01h,CR1=80h (Address : 0FFFh, Data : 0001h)
* This is mandatory. As for how to set them, refer to Method of Accessing and Controlling Internal Data Memory.
· CR11 = 00h (Frame/10 ms/16B/Speech CODEC = G.729.A)
· Various settings
· CR0 = 09h (OPE_STAT = “1”)

**PCM I/F Mode**




Examples of settings in the initialization mode

· CR15 = 40h * This is mandatory.

· CR6=0Fh,CR7=FFh,CR8=00h,CR9=01h,CR1=80h (Address : 0FFFh, Data : 0001h)

* This is mandatory. As for how to set them, refer to Method of Accessing and Controlling Internal Data Memory.·

· CR10 = 00h (VFRO1 = AVREF/VFRO0 = AVREF)

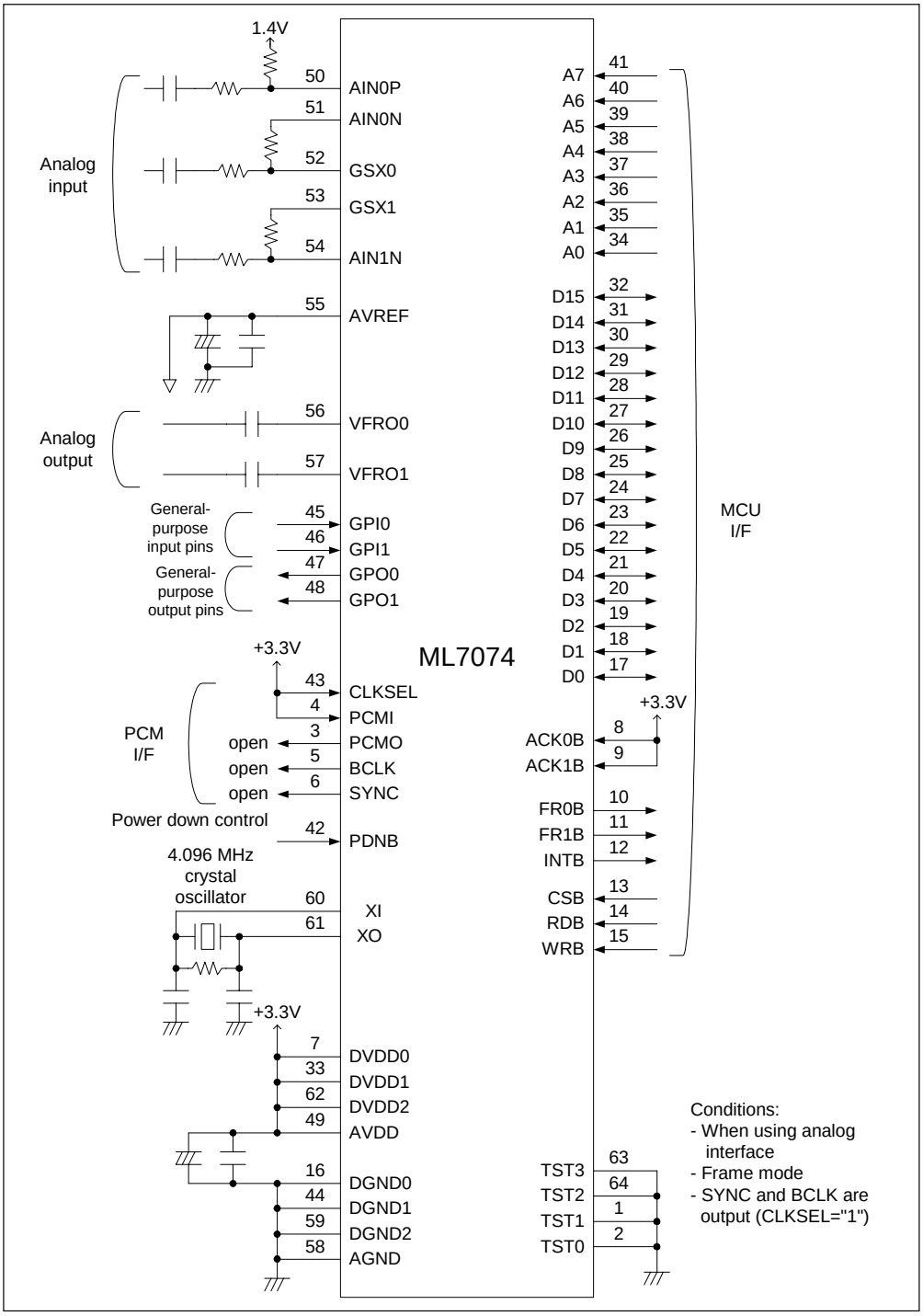
· CR11 = 00h (Frame/10 ms/16B/PCMIF = 16-bit linear)

· CR12 = 01h (Speech CODEC = G.729.A/PCMIF_EN = “1”)

· Various settings

· CR0 = 29h (AFE_EN = Power down/LONG/OPE_STAT = “1”)

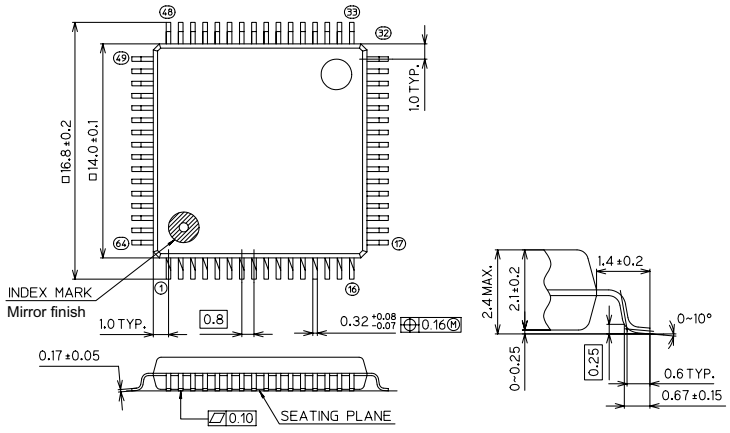
## EXAMPLE OF APPLICATION CIRCUIT



## PACKAGE DIMENSIONS

(Unit: mm)

QFP64-P-1414-0.80-BK




| | |
|---|---|
| Package material | Epoxy resin |
| Lead frame material | 42 alloy |
| Pin treatment | Solder plating (≥5µm) |
| Package weight (g) | 0.87 TYP. |
| Rev. No./Last Revised | 6/Feb. 23, 2001 |

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

## REVISION HISTORY

| Document No. | Date | Page | | Description |
|---|---|---|---|---|
| | | Previous Edition | Current Edition | |
| FEDL7074-004DIGEST-01 | Nov. 12, 2003 | – | – | Final edition 1 |

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