

# OKI Semiconductor

**FEDL7055-02**

Issue Date: Apr. 8, 2003

## ML7055

### Bluetooth Baseband Controller IC

#### GENERAL DESCRIPTION

The ML7055 is a CMOS digital IC for use in 2.4 GHz band Bluetooth™ systems. This IC incorporates the ARM7TDMI® as the CPU core, features a highly expandable architecture, and supports the interfaces for a variety of applications. Since the ML7055 has Oki's Bluetooth protocol stack software installed, when the IC is used in conjunction with the Bluetooth RF transceiver IC, data/voice communications are possible while maintaining interconnectivity with other Bluetooth systems.

#### FEATURES

- Conforms to Bluetooth Specification (Ver1.1)
- Designed for connection with the RF-LSI interface, such as the OKI RF-LSI interface (ML7050), the SKYWORKS RF-LSI interface (CX72303), or the BROADCOM RF-LSI interface (BCM2002X) that functions as the Bluetooth RF-LSI interface
- The high-speed, low-power ARM7TDMI™ is installed as the CPU core
- PCM-CVSD transcoder that provides high quality voice using the noise filter is installed
- Low power consumption in flexible power management modes according to operating modes of Bluetooth
- $\overline{\text{DETACH}}$  signal provides control of change to power-saving mode (STOP) and return request to normal mode.
- UART interface corresponding to baud rates up to 921.6 kbps
- I<sup>2</sup>C bus interface provides accesses to EEPROM or PCM-Codec
- Selectable 12 MHz or 13 MHz for the system clock
- Selectable 32 kHz or 32.768 kHz for the LPO clock
- Built-in programmed ROM eliminates external ROM/FLASH
- The packages are available in three types:
  - 63-pin WCSP for ML7055HB
  - 64-pin BGA for ML7055LA
  - 84-pin BGA for ML7055LP



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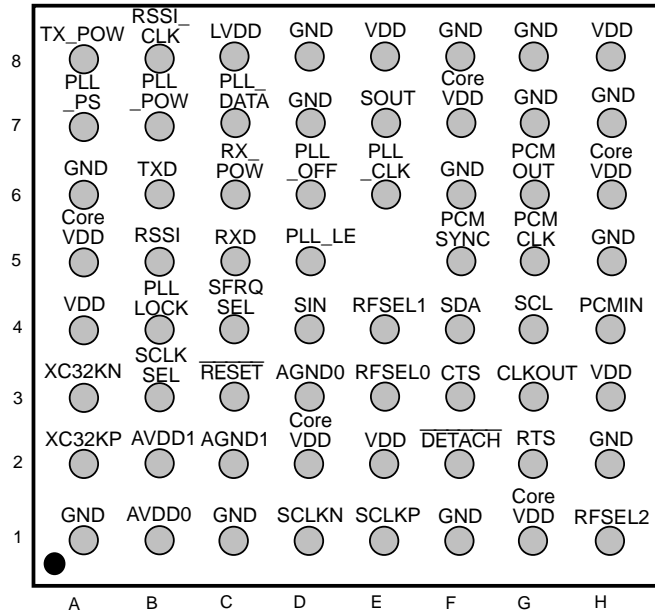
The information contained herein can change without notice owing to the product being under development.

**SPECIFICATIONS**

Process	0.16 $\mu$ m CMOS (5-layer metal wire)
Package	63-pin WCSP (P-VFLGA63-4.90×4.72-0.50-W) (Dimensions: 4.90 mm × 4.72 mm × 0.48 mm; pin pitch: 0.50 mm) 64-pin BGA (P-TFBGA64-0707-0.65) (Dimensions: 7 mm × 7 mm × 1.2 mm; pin pitch: 0.65 mm) 84-pin BGA (P-LFBGA84-0909-0.80) (Dimensions: 9 mm × 9 mm × 1.5 mm; pin pitch: 0.80 mm)
Supply current	22 mA (24 MHz operation)
Operating voltage ranges	2.70 to 3.6 V for input-output, 1.65 to 1.95 V for internal circuits
Operating frequency	24 MHz
Built-in ROM size	176 KB (for ARM program)
Built-in RAM size	24 KB
Input clocks	12 MHz or 13 MHz (system clock) 32 kHz or 32.768 kHz (LPO clock)
RF-LSI interface	OKI RF-LSI interface (ML7050) SKYWORKS RF-LSI interface (CX72303) BROADCOM RF-LSI interface (BCM2002X)
Installed interfaces	UART interface (up to 921.6 Kbps) General-purpose I/O interface (used as a pin for I <sup>2</sup> C bus interface depending on software installed) PCM interface (PCM Linear/A-law/ $\mu$ -law can be selected) DETACH interface
Timers	16-bit auto reload timer (1ch) 18-bit auto reload timer (1ch)
Interrupt controller	11 causes
Clock control circuit	Crystal oscillator circuit (12 MHz or 13 MHz, 32 kHz or 32.768 kHz) Internal PLL

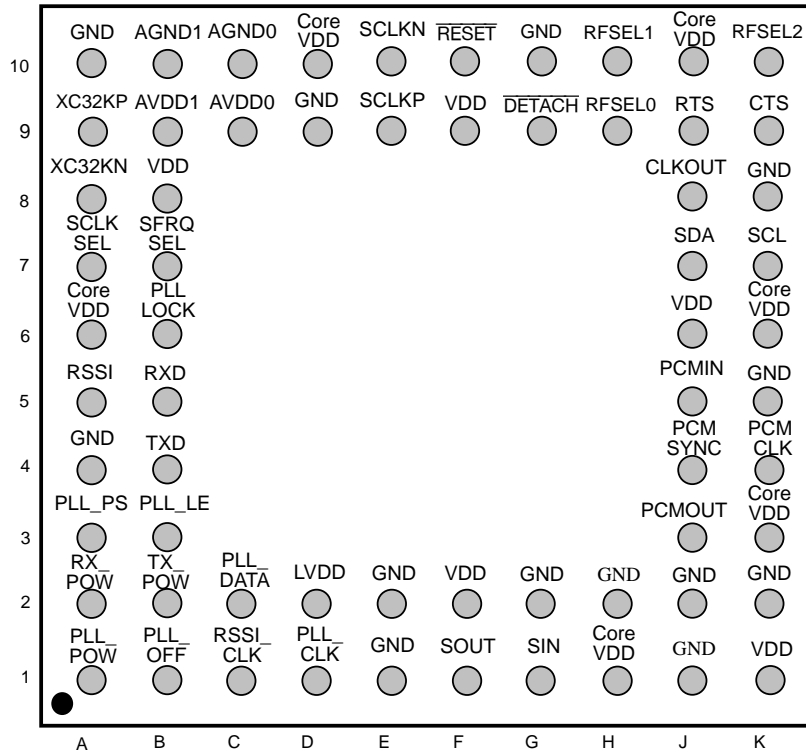
**PIN PLACEMENT**

**ML7055HB: 63-pin WCSP (P-VFLGA63-4.90 × 4.72-0.50-W)**



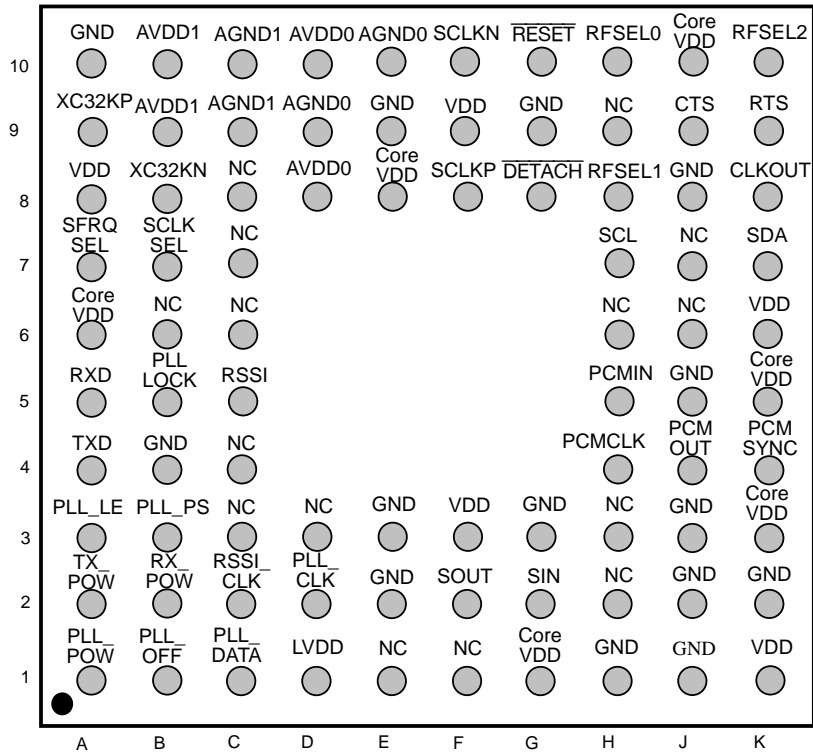
**TOP VIEW**

**ML055LA: 64-pin BGA (P-TFBGA64-0707-0.65)**



**TOP VIEW**

**ML7055LP: 84-pin BGA (P-LFBGA84-0909-0.80)**



**TOP VIEW**

## PIN DESCRIPTIONS

RF I/F							
Pin Name	Direction [*0]	Internal Pull Up/ Down, Schmitt	Initial Value	Pin Placement			Description
				ML7055 HB	ML7055 LA	ML7055 LP	
TXD	O	—	L L L	B6	B4	A4	ML7050: Transmit data output CX72303: Transmit data output BCM2002X: Transmit data output
RXD	I	—	— — —	C5	B5	A5	ML7050: Receive data input CX72303: Receive data input BCM2002X: Receive data input
PLL_DATA	O	—	X H L	C7	C2	C1	ML7050: Serial write data CX72303: Serial write data BCM2002X: Transmit enable
PLL_CLK	O	—	L L L	E6	D1	D2	ML7050: Serial clock CX72303: Serial clock BCM2002X: Serial clock
PLL_LE	O	—	L H L	D5	B3	A3	ML7050: Serial read enable 0: Negate, 1: Assert CX72303: Serial enable 0: Assert, 1: Negate BCM2002X: RF-LSI synthesizer on 0: Negate, 1: Assert
RSSI	I	Pull down	— — —	B5	A5	C5	ML7050: Receive field strength data input CX72303: Serial read data BCM2002X: Serial read data
RSSI_CLK	O	—	L L X	B8	C1	C2	ML7050: Receive field strength data clock CX72303: RF-LSI receiving characteristic control BCM2002X: System clock request
PLL_POW	O	—	H L H	B7	A1	A1	ML7050: Local PLL power control 0: Assert, 1: Negate CX72303: PA Power control 0: Negate, 1: Assert BCM2002X: Select serial transmit mode
TX_POW	O	—	H L L	A8	B2	A2	ML7050: Transmit enable 0: Assert, 1: Negate CX72303: Transmit enable 0: Negate, 1: Assert BCM2002X: Serial write data
RX_POW	O	—	H L L	C6	A2	B2	ML7050: Receive enable 0: Assert, 1: Negate CX72303: Receive enable 0: Negate, 1: Assert BCM2002X: Receive enable
PLL_PS	O	—	L X L	A7	A3	B3	ML7050: "L" CX72303: Power on reset 0: Assert (reset) 1: Negate BCM2002X: RF-LSI receiving characteristic control

[\*0] "I" = Input, "O" = Output, "I/O" = Input/Output

**RF I/F**

Pin Name	Direction [*0]	Internal Pull Up/Down, Schmitt	Initial Value	Pin Placement			Description
				ML7055 HB	ML7055 LA	ML7055 LP	
PLLLOCK	I	Pull down	— — —	B4	B6	B5	ML7050: — CX72303: — BCM2002X: 1MHz clock
PLL_OFF	O	—	H — L	D6	B1	B1	ML7050: PLL loop control 0: Open loop 1: Closed loop CX72303: Diversity output BCM2002X: PA Power control

**PCM I/F**

Pin Name	Direction	Internal Pull Up/Down, Schmitt	Initial Value	Pin Placement			Description
				ML7055 HB	ML7055 LA	ML7055 LP	
PCMOUT	O	—	L	G6	J3	J4	PCM data output
PCMIN	I	Pull up	—	H4	J5	H5	PCM data input
PCMSYNC	I/O	Pull down	—	F5	J4	K4	PCM sync signal (8 kHz), Initial setting: input (can be switched by an internal register)
PCMCLK	I/O	Pull down	—	G5	K4	H4	PCM clock (64 kHz/128 kHz) Initial setting: input (can be switched by an internal register)

Note: The PCM sync signal (8 kHz) must be guaranteed at the accuracy of  $\pm 50$  ppm if the PCMSYNC pin is configured as an input.

**UART I/F**

Pin Name	Direction	Internal Pull Up/Down, Schmitt	Initial Value	Pin Placement			Description
				ML7055 HB	ML7055 LA	ML7055 LP	
SOUT	O	—	H	E7	F1	F2	ACE transmit serial data
SIN	I	Schmitt	—	D4	G1	G2	ACE receive serial data
RTS	O	—	—	G2	J9	K9	ACE transmit data ready
CTS	I	—	H	F3	K9	J9	ACE transmit ready

**CLK and Configuration**

Pin Name	Direction	Internal Pull Up/Down, Schmitt	Initial Value	Pin Placement			Description
				ML7055 HB	ML7055 LA	ML7055 LP	
SCLKP	I	—	—	E1	E9	F8	System clock (12/13 MHz) pins (Power level: CMOS level)
SCLKN	O	—	—	D1	E10	F10	
XC32KP	I	—	—	A2	A9	A9	Subclock pins (for oscillator)
XC32KN	O	—	—	A3	A8	B8	
SCLKSEL	I	Pull down	—	B3	A7	B7	System clock frequency select pin L: Select CLK divided by internal PLL H: Select subclock
SFRQSEL	I	Pull down	—	C4	B7	A7	System clock frequency select pin L: 13 MHz H: 12 MHz
RFSEL0-2	I	—	—	[*1]	[*2]	[*3]	RF-LSI select pins RFSEL[2:0] 001: ML7050 (OKI) 010: CX72303 (SKYWOKS) 101: BCM2002X (BROADCOM) Others: Unused
$\overline{\text{RESET}}$	I	Schmitt	—	C3	F10	G10	Hardware reset pin (Reset = L)
$\overline{\text{DETACH}}$	I	Schmitt	—	F2	G9	G8	Sleep pin (Sleep = L)
SCL	O	—	L	G4	K7	H7	I <sup>2</sup> C serial clock
SDA	I/O	—	H	F4	J7	K7	I <sup>2</sup> C serial data
CLKOUT	O	—	—	G3	J8	K8	System clock (12/13 MHz) output pins

[\*1] RFSEL0: E3; RFSEL1: E4; RFSEL2: H1

[\*2] RFSEL0: H9; RFSEL1: H10; RFSEL2: K10

[\*3] RFSEL0: H10; RFSEL1: H8; RFSEL2: K10



NC							
Pin Name	Direction	Internal Pull Up/Down, Schmitt	Initial Value	Pin Placement			Description
				ML7055 HB	ML7055 LA	ML7055 LP	
NC				—	—	[*4]	No connection

[\*4] B6, C3, C4, C6, C7, C8, D3, E1, F1, H2, H3, H6, H9, J6, J7  
 Note: Do not wire under the NC pin.

#### Power, GND

Pin Name	Direction	Internal Pull Up/Down, Schmitt	Initial Value	Pin Placement			Description
				ML7055 HB	ML7055 LA	ML7055 LP	
V <sub>DD</sub>	—	—	—	[*5]	[*6]	[*7]	I/O power supply pin 2.70 to 3.6 V
CoreV <sub>DD</sub>	—	—	—	[*8]	[*9]	[*10]	Power supply pin for internal circuit 1.65 to 1.95 V
LV <sub>DD</sub>	—	—	—	C8	D2	D1	RF-I/O power supply pin (Same voltage to the V <sub>DD</sub> for RF-LSI)
GND	—	—	—	[*11]	[*12]	[*13]	Digital block ground pin
AV <sub>DD0</sub>	—	—	—	B1	C9	[*14]	Analog block power supply pin 1.65 to 1.95 V
AV <sub>DD1</sub>	—	—	—	B2	B9	[*15]	
AGND0	—	—	—	D3	C10	[*16]	Analog block ground pin
AGND1	—	—	—	C2	B10	[*17]	

[\*5] V<sub>DD</sub>: A4, E2, E8, H3, H8

[\*6] V<sub>DD</sub>: B8, F2, K1, J6, F9

[\*7] V<sub>DD</sub>: A8, F3, K1, K6, F9

[\*8] Core V<sub>DD</sub>: A5, D2, F7, G1, H6

[\*9] Core V<sub>DD</sub>: A6, H1, K3, K6, J10, D10

[\*10] Core V<sub>DD</sub>: A6, G1, K3, K5, J10, E8

[\*11] GND: A1, A6, C1, D7, D8, F1, F6, F8, G7, G8, H2, H5, H7

[\*12] GND: A4, A10, D9, E1, E2, G2, G10, H2, J1, J2, K2, K5, K8

[\*13] GND: A10, B4, E2, E3, E9, G3, G9, H1, J1, J2, J3, J5, J8, K2

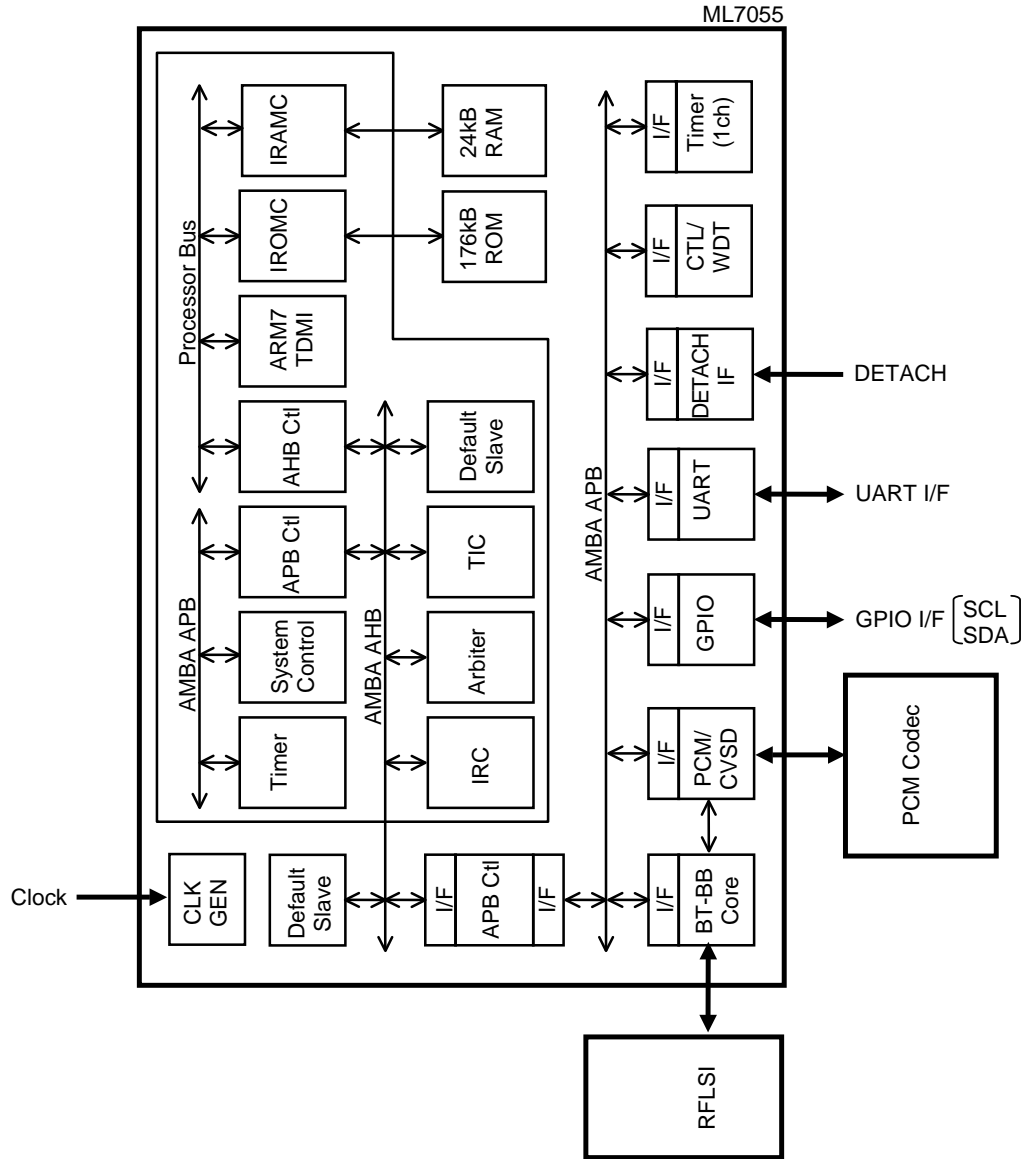
[\*14] AV<sub>DD0</sub>: D8, D10

[\*15] AV<sub>DD1</sub>: B9, B10

[\*16] AGND0: E10, D9

[\*17] AGND1: C9, C10

BLOCK DIAGRAM



## DESCRIPTION OF INTERNAL BLOCKS

### CLKGEN Block

- Generates a clock that is supplied to each block through SCLKP (12/13 MHz)
- STOP/HALT function

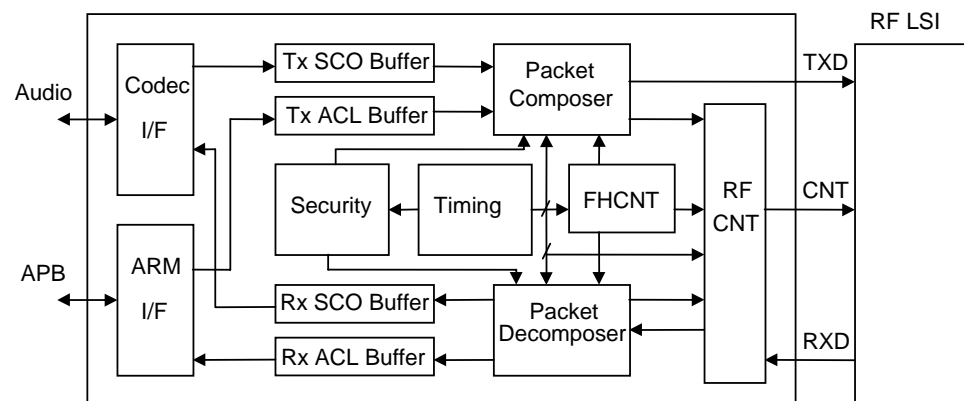
### CTL/WDT Block

- Control of the frequency division function of the internal main clock
- Control of clock supplied to each peripheral
- Control of reset of each peripheral
- STOP/HALT control
- Watchdog timer function (interrupt/reset)

### Timer Block

- 1 channel
- 18-bit timer counter
- Interrupt by compare function
- One shot, interval, or free-run mode

### Base band Core Block

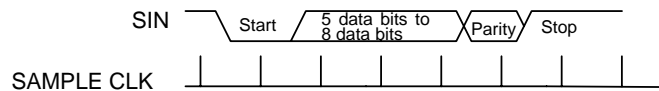


- RF Controller
  - RF power supply control (PLL, TX, RX)
  - Local PLL frequency division ratio setting
  - Receive clock regeneration function
  - Synchronization detection (synchronizing within the permissible error limit of SyncWord)
  - Receive clock re-timing function
- FH Controller hopping
  - Sequence control
  - Frequency hopping selection function
  - CRC computation's initial value selection function

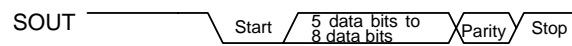
- Timing Generator
  - Bluetooth clock generation
  - Operation interrupts depend on mode (slot, scan, sniff, hold, park)
  - Sync detection timing generation (sync window  $\pm 10 \mu\text{s}$ )
  - PLL setting timing generation
  - Transmit/Receive timing generation
  - Multi-master timing management function
- Packet Composer
  - Access code generation (SyncWord generation, appending PR\*TRAILER)
  - Packet header generation (HEC generation, scrambling, FEC encoding)
  - Payload generation (CRC generation, encryption, scrambling, FEC encoding)
  - Packet synthesis
- Packet Decomposer
  - Packet decomposition (separating the packet header and the payload)
  - Packet header processing (FEC decoding, descrambling, HEC error detection, header information separation)
  - Payload processing (FEC decoding, descrambling, encryption decoding, CRC judgement, payload separation)
- Security
  - Various key generation functions (initialization, link key, encryption key)
  - Certification function
  - Encryption function

### UART Block

- Full-duplex buffering method
  - All status reporting function
  - Built-in 64-byte transmit/receive FIFO
  - Modem control based on CTS
  - Programmable serial interface
  - 5-, 6-, 7-, 8-bit characters
  - Generation and verification of odd parity, even parity, or no parity
  - 1, 1.5, or 2 stop bits
  - Programmable Baud Rate Generator (9600 bps to 921.6 kbps)
  - Error servicing for parity, overrun, and framing errors
- Configuration of 1 Data Frame during Reception

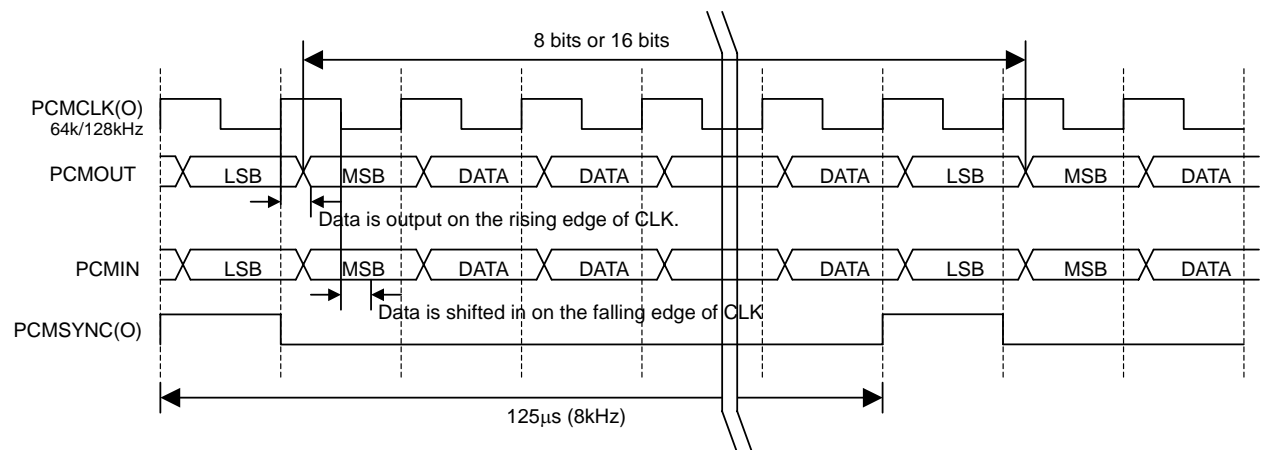


- Configuration of 1 Data Frame during Transmission

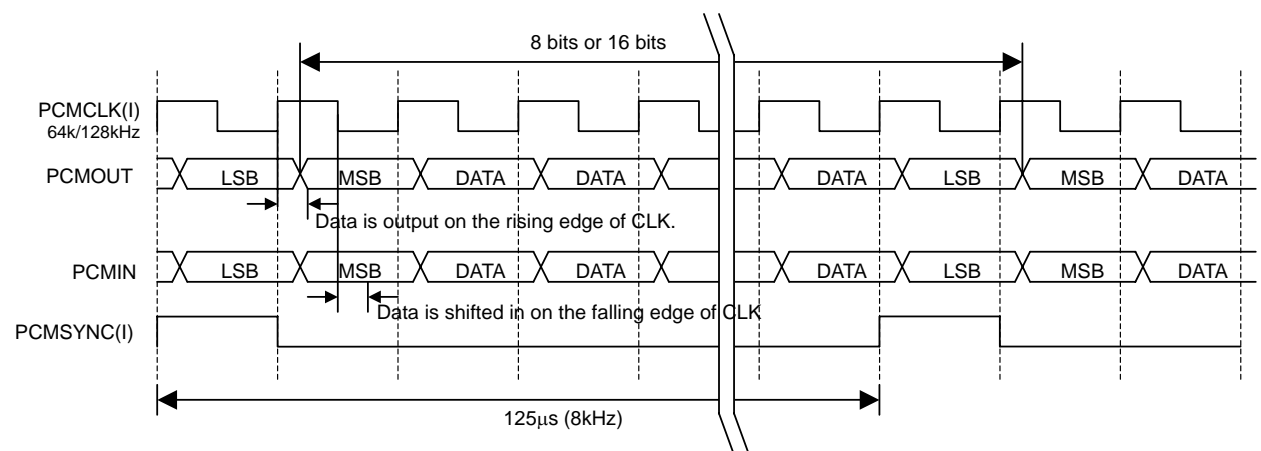


### PCM-CVSD Transcoder Block

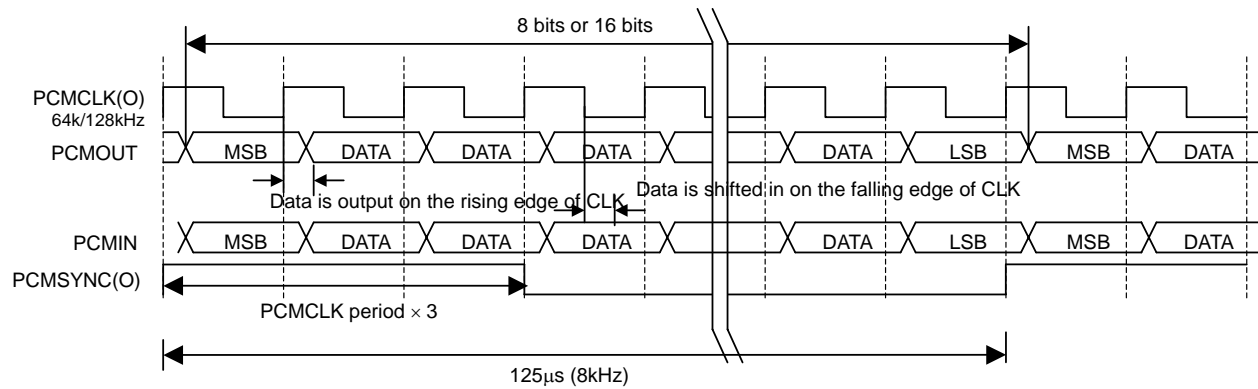
- Application side I/O:
  - PCM Codec
- Application-side format:
  - PCM linear (8, 14, 16 bits/sample, 8 kHz sampling frequency)/A-law/ $\mu$ -law
- Bluetooth-side format:
  - CVSD/A-law/ $\mu$ -law
- All combinations of the above conversions are supported
- PCMSYNC/PCMCLK I/O can be switched (initial setting: input)
- Timing in Short Mode and in PCMCLK and PCMSYNC Output Mode  
(For PCM data of 14 bits/sample, lower 2 bits of 16 bits are invalid.)



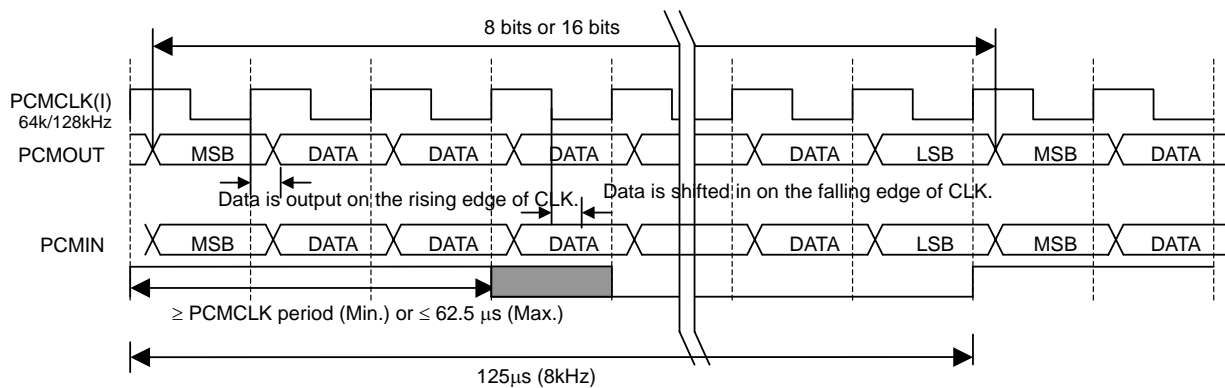
- Timing in Short Mode and in PCMCLK and PCMSYNC Input Mode.  
(For PCM data of 14 bits/sample, lower 2 bits of 16 bits are invalid.)



- Timing in Long Mode and in PCMCLK and PCMSYNC Output mode  
(For PCM data of 14 bits/sample, lower 2 bits of 16 bits are invalid.)



- Timing in Long Mode and in PCMCLK and PCMSYNC Input Mode.  
(For PCM data of 14 bits/sample, lower 2 bits of 16 bits are invalid.)



### DETACH Interface Block

- Generation of the request for change to (from) the stop mode by detection of the rising (falling) edge of the  $\overline{\text{DETACH}}$  signal

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Conditions	Rating	Unit
I/O power supply voltage	$V_{DD}/LV_{DD}$	—	-0.3 to +4.5	V
Core power supply voltage	$CoreV_{DD}/AV_{DD}$	—	-0.3 to +2.5	V
Input voltage	$V_I$	—	-0.3 to +4.5	V
Allowable power dissipation	$P_d$	—	0.62	W
Storage temperature	$T_{stg}$	—	-55 to 150	°C

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
I/O power supply voltage	$V_{DD}/LV_{DD}$	—	2.7	3.3	3.6	V
Core power supply voltage	$CoreV_{DD}/AV_{DD}$	—	1.65	1.8	1.95	V
"H" level input voltage	$V_{ih}$	—	2.2	—	$V_{DD}$	V
"L" level input voltage	$V_{il}$	—	0	—	0.8	V
Operating temperature	$T_a$	—	-40	—	85	°C

**ELECTRICAL CHARACTERISTICS****DC Characteristics**

( $V_{DD} = 2.7$  to  $3.6$  V,  $CoreV_{DD} = 1.65$  to  $1.95$  V,  $T_a = -40$  to  $+85$ °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" level output voltage	$V_{oh}$	$I_{oh} = -2$ mA, $3.0V \leq V_{dd} \leq 3.6V$	2.4	—	—	V
		$2.7V \leq V_{dd} < 3.0V$	2.2	—	—	
"L" level output voltage	$V_{ol}$	$I_{ol} = 2$ mA	—	—	0.4	V
Input leakage current	$I_i$	$V_i = GND$ to $3.6$ V	-10	—	10	$\mu A$
		$V_i = V_{DD}$ 50 k $\Omega$ Pull-down	10	66	200	
		$V_i = GND$ 50 k $\Omega$ Pull-up	-200	-66	-10	
Output leakage current	$I_o$	$V_o = GND$ to $V_{DD}$	-10	—	10	$\mu A$
		$V_o = V_{DD}$ 50 k $\Omega$ Pull-down	10	66	200	
Power supply current (during operation)	$I_{ddo}$	During 24 MHz operation	0	22	32	mA
Power supply current (during stand-by)	$I_{dds}$	CLK stopped	—	10	100	$\mu A$



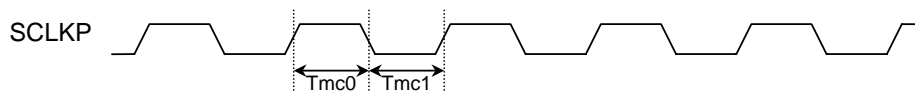
### Power Supply Current (IDD) Characteristics by Power Saving Mode

( $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ ,  $\text{Core}V_{DD} = 1.65\text{ V to }1.95\text{ V}$ ,  $T_a = -40\text{ to }85^\circ\text{C}$ )

Operating mode	Conditions	Min.	Typ.	Max.	Unit
STOP mode ( $\overline{\text{DETACH}} = \text{"L"}$ )	—	—	0.03	—	mA
Page Scan operating mode	Interval:1.28sec Window:11.25msec	—	2.5	—	
Poll Interval operating mod	Interval:40slot	—	3.5	—	
Sniff operating mode	Interval:2000slot Attempt:4frame	—	2.5	—	
Hold operating mode	Interval:4000slot	—	0.05	—	
ACL operating mode	DH1/DM1	—	22.0	—	
	RX:DH3/DM3 TX:DH1/DM1	—	22.0	—	
	RX:DH5/DM5 TX:DH1/DM1	—	22.0	—	

### AC Characteristics

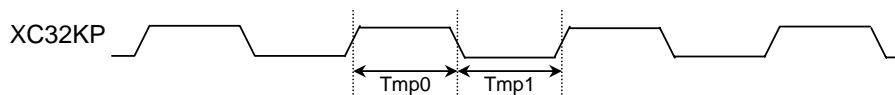
#### ⊙ System clock (SCLKP)



( $V_{DD} = 2.7\text{ to }3.6\text{ V}$ ,  $\text{Core}V_{DD} = 1.65\text{ to }1.95\text{ V}$ ,  $T_a = -40\text{ to }85^\circ\text{C}$ )

Parameter	Description	Min	Typ	Max	Unit
Tmc0	Duty in SCLKP "H" duration	40	50	60	%
Tmc1	Duty in SCLKP "L" duration	40	50	60	%

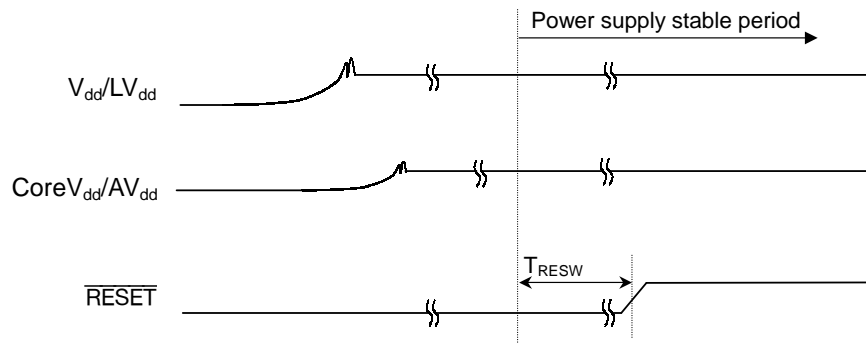
#### ⊙ Sub-clock (XC32KP)



( $V_{DD} = 2.7\text{ to }3.6\text{ V}$ ,  $\text{Core}V_{DD} = 1.65\text{ to }1.95\text{ V}$ ,  $T_a = -40\text{ to }85^\circ\text{C}$ )

Parameter	Description	Min	Typ	Max	Unit
Tmp0	Duty in XC32KP "H" duration	40	50	60	%
Tmp1	Duty in XC32KP "L" duration	40	50	60	%

⊙ Reset

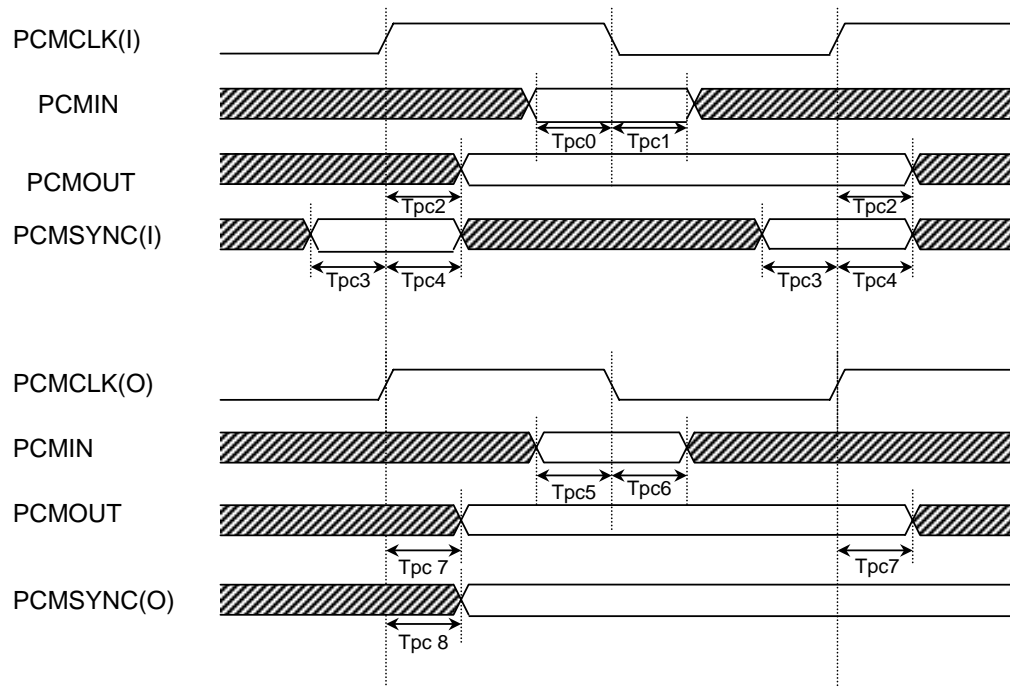


( $V_{DD} = 2.7$  to  $3.6V$ ,  $CoreV_{DD} = 1.65$  to  $1.95V$ ,  $T_a = -40$  to  $85^{\circ}C$ )

Parameter	Description	Min	Typ	Max	Unit
$T_{RESW}$	Reset pulse width	10	—	—	$\mu s$

Note : Apply "L" to the  $\overline{RESET}$  pin for 10  $\mu s$  or more after the power supply has been settled.

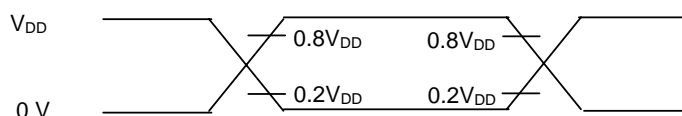
⊙ PCM interface



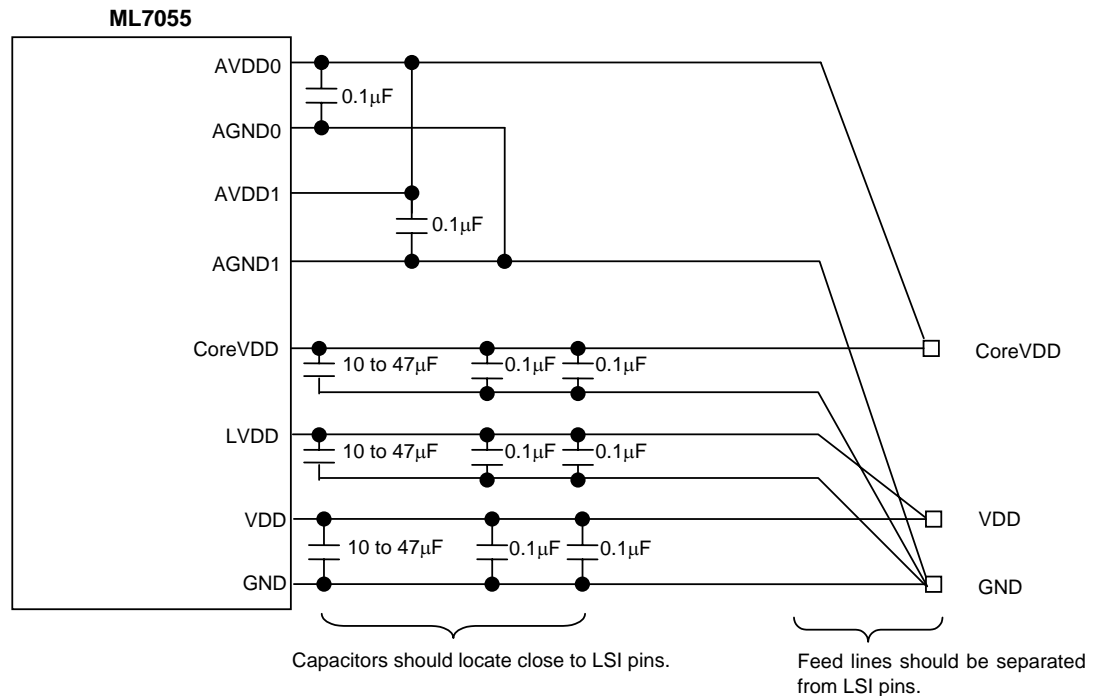
(V<sub>DD</sub> = 2.7 to 3.6V, CoreV<sub>DD</sub> = 1.65 to 1.95V, T<sub>a</sub> = -40 to 85°C)

Parameter	Description	Min	Typ	Max	Unit
Tpc0	PCMIN setup time relative to PCMLCK (input) falling edge	100	—	—	ns
Tpc1	PCMIN hold time relative to PCMLCK (input) falling edge	100	—	—	ns
Tpc2	PCMOUT delay time relative to PCMLCK (input) rising edge	—	—	250	ns
Tpc3	PCMSYNC (input) setup time relative to PCMLCK (input) rising edge	100	—	—	ns
Tpc4	PCMSYNC (input) hold time relative to PCMLCK (input) rising edge	100	—	—	ns
Tpc5	PCMIN setup time relative to PCMLCK (output) falling edge	100	—	—	ns
Tpc6	PCMIN hold time relative to PCMLCK (output) falling edge	100	—	—	ns
Tpc7	PCMOUT delay time relative to PCMLCK (output) rising edge	—	—	250	ns
Tpc8	Delay time from PCMLCK (output) rising edge to PCMSYNC (output)	—	—	150	ns

⊙ AC Characteristic Measuring Points



## REFERENCE FOR VOLTAGE SUPPLY CIRCUIT



### Example of ML7055 voltage supply circuit

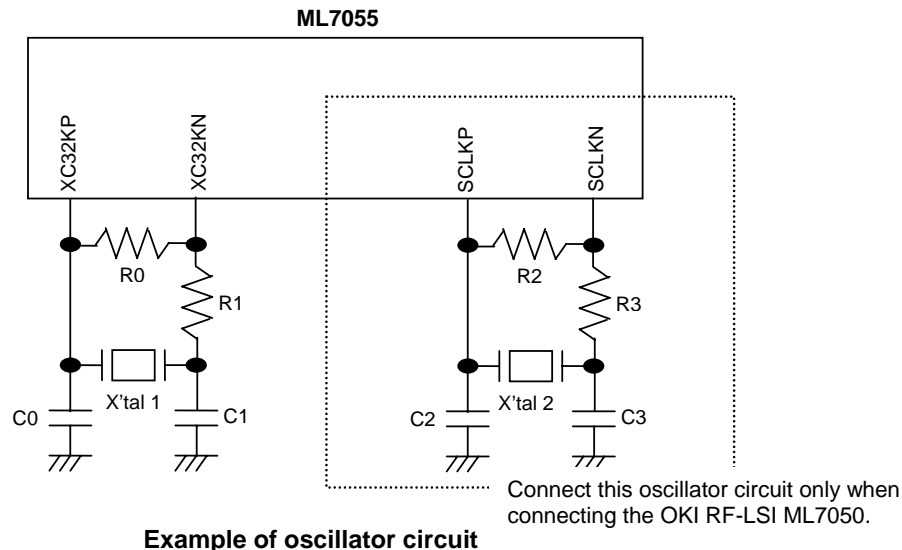
- Insert appropriate bypass capacitors between the  $V_{DD}$  and GND lines.

#### Note 1: Precautions to insert the bypass capacitors

- Use traces of  $V_{DD}$  and GND lines wider than those of the other signal lines.
- Keep the length of traces between the bypass capacitors and the  $V_{DD}$  line and between the bypass capacitors and the GND line as short as possible.
- Keep the length of traces between the bypass capacitors and the  $V_{DD}$  line and between the bypass capacitors and the GND line as equal as possible.

The circuit is subject to change according to the specific LSI board design. Please contact Oki Electric Industry Co., Ltd. for detailed information.

## REFERENCE FOR OSCILLATOR CIUCUIT



Note 1: The values of C0 and C1, and R0 and R1 should be determined according to the specifications for the external crystal X'tal 1 (32 or 32.768 kHz).

The values of C2 and C3, and R2 and R3 should be determined according to the specifications for the external crystal X'tal 2 (13 or 12 MHz).

Note 2: The crystal oscillator circuit should be connected to pins SCLKP and SCLKN only when the OKI RF-LSI (ML7050) is connected. In other cases, the system clock should be input from the RF-LSI to pin SCLKP.

Note 3: In the case of 13 MHz or 12 MHz system clock (SCLKP) input, make sure the crystal frequency tolerance is  $\pm 20$  ppm for temperature, supply voltage, and aging.

In the case of 32 kHz or 32.768 kHz sub-clock (XC32KP) input, make sure the crystal frequency tolerance is  $\pm 250$  ppm for temperature, supply voltage, and aging.

Note 4: Precautions to build a crystal oscillator circuit

- Keep length of wire traces as short as possible.
- Do not cross the crystal oscillator circuit wires over other signal line wires.
- Do not keep signal line wires through which high current flows close to the crystal oscillator circuit.
- Keep the grounding point of the capacitors in the oscillator circuit at the potential equal to GND. And do not connect the capacitors to the GND or GND lines through which high current flows.
- Do not output signals from the oscillator circuit.

The circuit is subject to change according to the specific LSI board design. Please contact Oki Electric Industry Co., Ltd. for detailed information. It is recommended to determine the final circuit values including the capacitance of the circuit board designed by the user.

## APPLICATION NOTES

### Clock Selection

- The system clock frequency is selected according to external pin SFRQSEL.
  - SFRQSEL = 0 : A 13 MHz clock is input to external pins SCLKP.
  - SFRQSEL = 1 : A 12 MHz clock is input to external pins SCLKP.
- The CPU clock supply source is selected according to external pin SCLKSEL.
  - SCLKSEL = 0 : Use the clock that was divided down from the internal PLL output of 192 MHz that was generated from external pins SCLKP. (Dividing ratios are selectable in the range of 1/6 to 1/16. Initial value is 1/8 (24 MHz).)
  - SCLKSEL = 1 : Use external pins XC32KP.

Note: The clock supply source can be set by the CLKCNTL register in the CTL/WDT block once the LSI is powered up.
- The frequency of CPU clock is selectable from the high speed (24 MHz) and low speed (16 MHz). This can be performed by the Vendor Specific Command.

### Setting the Reset

- Apply a “L” level to the  $\overline{\text{RESET}}$  pin for more than 10  $\mu\text{s}$  after power voltage is stabilized. When the system clock oscillator circuit is stable and the  $\overline{\text{RESET}}$  pin is at a “H” level, the internal reset is released and operation starts after the internal reset is held for 1.9 ms for the input clock of 13 MHz or 2.0 ms for the input clock of 12 MHz.

### Setting the UART Baud Rate

- It is possible to set the UART baud rate using the Vendor Specific Commands.

Available baud rate settings:  
 9600/19.2k/38.4k/56k/57.6k/115.2k/230.4k/345.6k/460.8k/921.6k  
 (Initial value is 115.2 kbps.)

### Setting the PCM-CVSD Transcoder

- It is possible to set the PCM-CVSD transcoders using the Vendor Specific Commands. For command details, contact Oki Electric Industry Co., Ltd.
- It is possible to set the following parameters using the VCCTL command:
  - PCMSYNC/PCMCLK mode (initial setting: input)
  - Mute reception (initial setting: OFF)
  - Mute transmission (initial setting: OFF)
  - Air coding
    - CVSD (initial setting)/ $\mu$ -law/A-law
  - Interface coding
    - Linear (initial setting)/ $\mu$ -law/A-law
  - PCM format (data width of one PCM Linear sample)
    - 8-bit (initial setting)/14-bit/16-bit
  - Serial interface format
    - Short frame (initial setting)/long frame

- Application interface mode  
PCM Codec I/F (initial setting)/APB I/F

#### XTAL Input Frequency of BCM2002X

- If the system clock is supplied from BCM2002X, the XTAL input frequency of BCM2002X must be 13 MHz. 12, 19.2, 19.68, or 19.8 MHz should not be applied.

#### XTAL Input Frequency of CX72303

- If the system clock is supplied from CX72303, the XTAL input frequency of CX72303 must be 13 MHz. 10 MHz should not be applied.

#### Required processes when interface pins are unused

- The following tables show the processes that should be performed when interface pins are not used.
- The pins that are not included in the following table should be left open.

##### RF I/F

Pin Name	Process When Pin Not Used	Comments
RXD	GND	
RSSI	Open or GND	
PLLLOCK	Open or GND	

##### UART I/F

Pin Name	Process When Pin Not Used	Comments
SIN	V <sub>DD</sub>	
CTS	GND	

##### PCM I/F

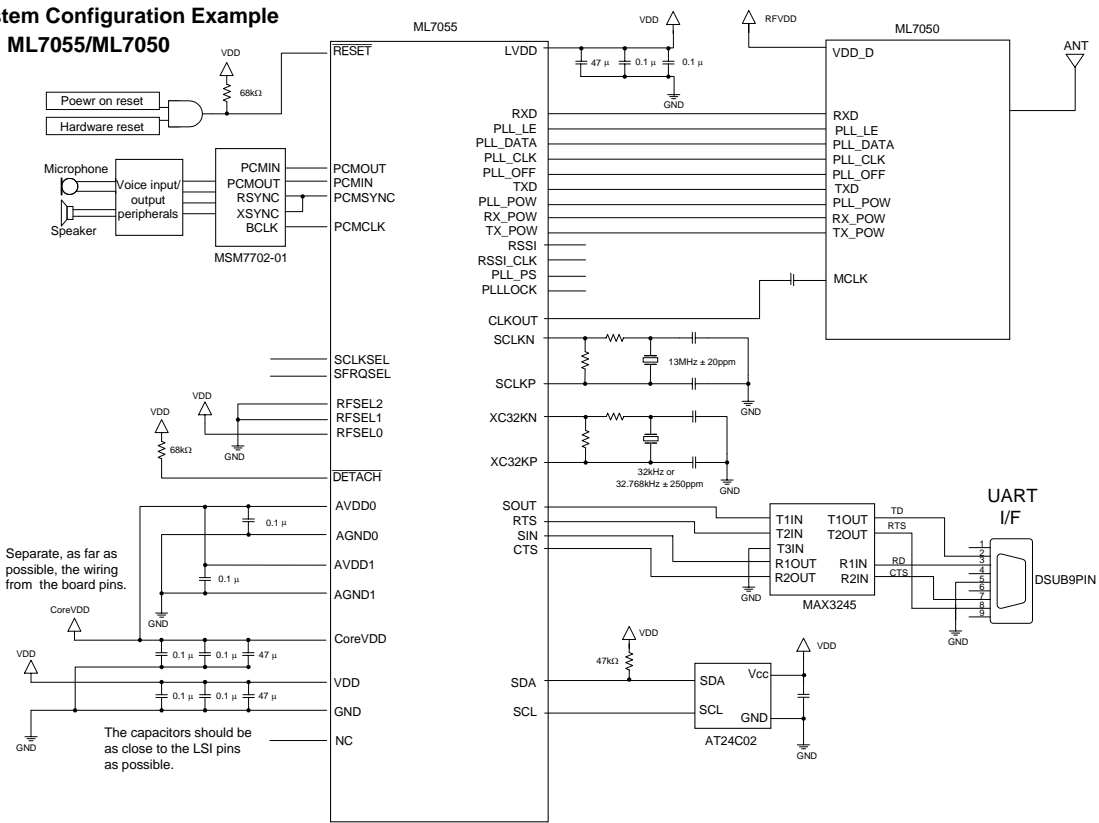
Pin Name	Process When Pin Not Used	Comments
PCMIN	Open or V <sub>DD</sub>	
PCMSYNC	Open or GND	
PCMCLK	Open or GND	

#### Processes of Other Pins

##### TEST I/F etc.

Pin Name	Process When Pin Not Used	Comments
DETACH	Pull up or V <sub>DD</sub>	

### System Configuration Example ML7055/ML7050

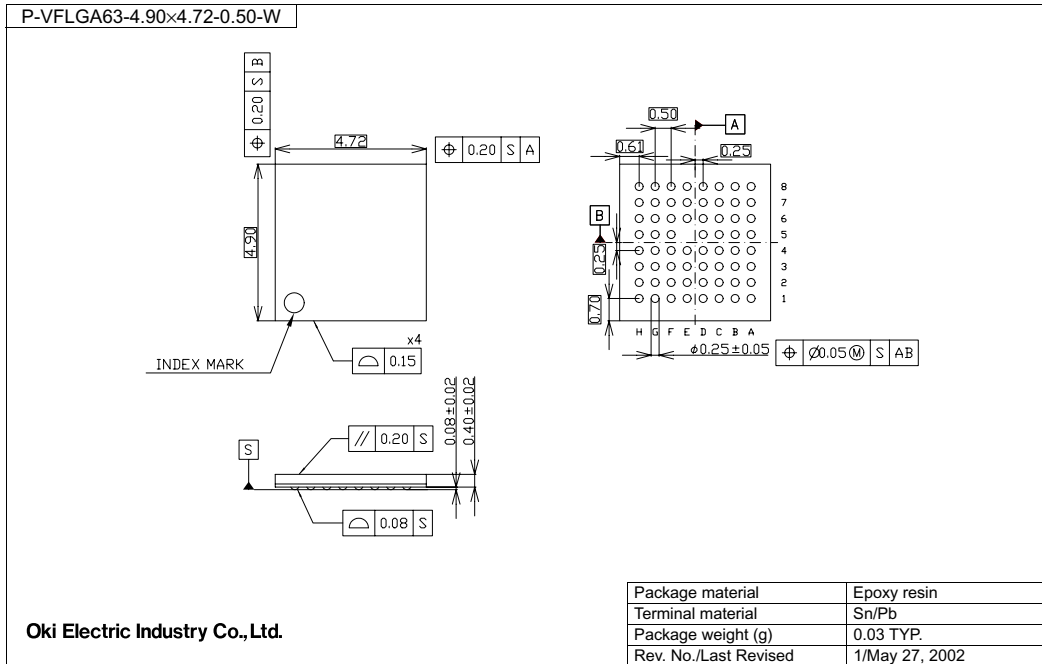




**PACKAGE DIMENSIONS**

**ML7055HB - 63pinWCSP (P-VFLGA63-4.90 × 4.72-0.50-W)**

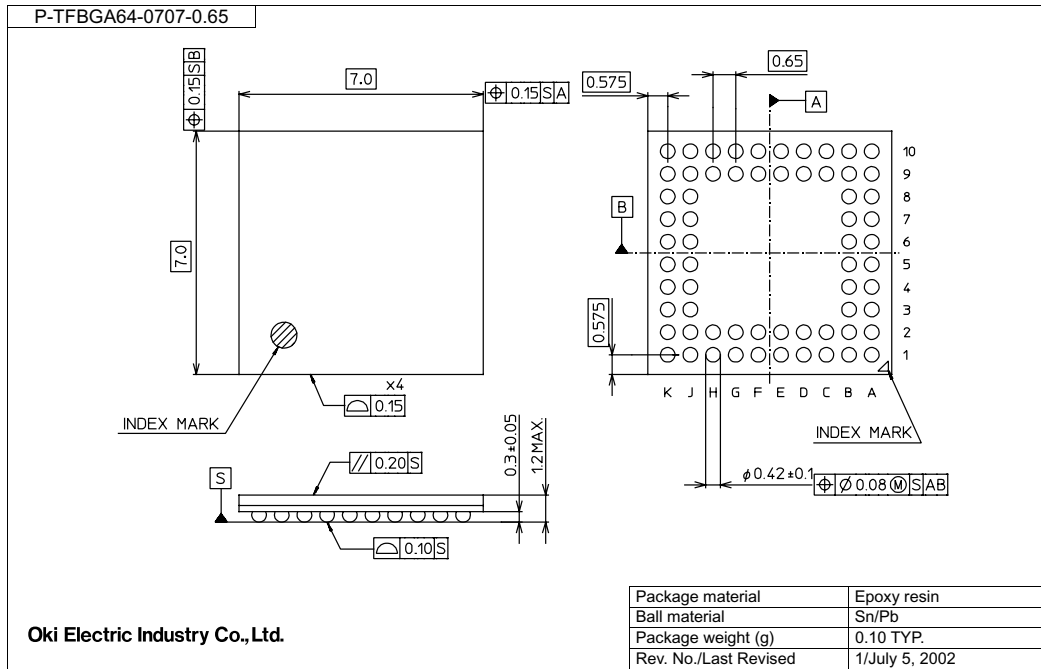
(Unit: mm)



Note: A lead-free package is available. Please contact Oki Sales Office/Distributors for more information.

ML7055LA - 64pinBGA (P-TFBGA64-0707-0.65)

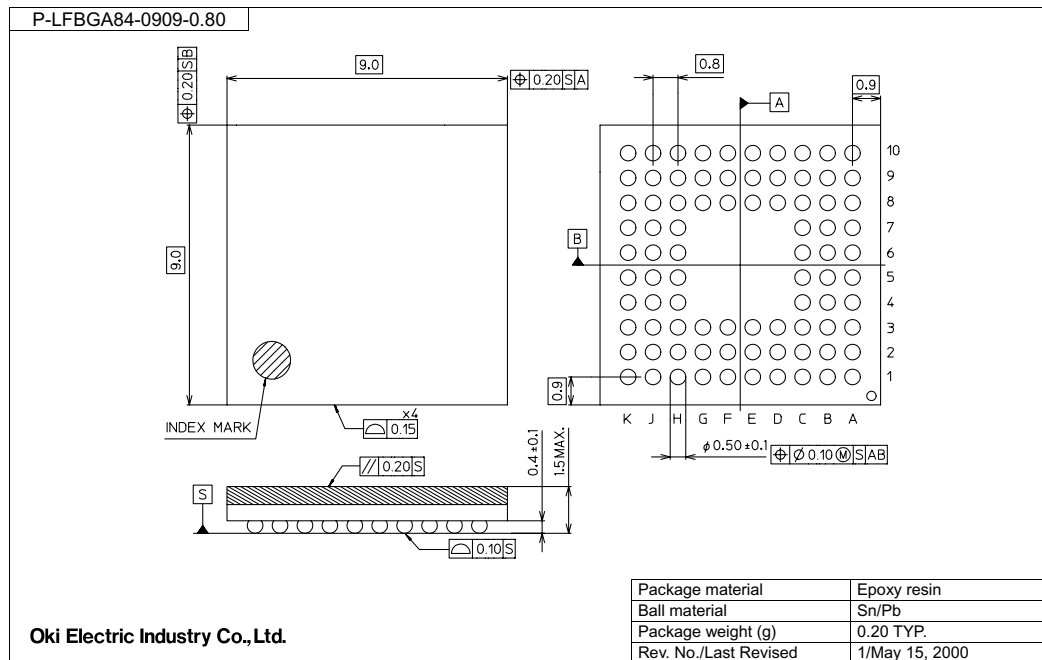
(Unit: mm)



Note: A lead-free package is available. Please contact Oki Sales Office/Distributors for more information.

## ML7055LP - 84pinBGA (P-LFBGA84-0909-0.80)

(Unit: mm)



Note: A lead-free package is available. Please contact Oki Sales Office/Distributors for more information.

## Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

**REVISION HISTORY**

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL7055-01	Aug.23, 2002	--	--	Preliminary edition 1
PEDL7055-02	Nov. 25, 2002	1	1	The contents of the "FEATURES" Section have been fully changed.
		--	2	Added the "SPECIFICATIONS" Section.
		2	3	The contents of the table in the "ABSOLUTE MAXIMUM RATINGS" Section have been partially changed.
				The voltage values of "Core VDD" have been added on the table in the "DC Characteristics" Section.
		3	4	The pin name has been changed from LPO_CLK to TCK.
		5	6	Eliminated the "LPO_CLK" row in the table of the "RF/IF" Section.
				Eliminated "Note" on the bottom side of the table of the "RF/IF" Section.
		6	7	The "Description" column of Pin name "TCK" in the table of the "JTAG I/F" Section has been partially changed.
		8	9	Added "REFERENCE FOR OSCILLATOR CIRCUIT" Section.
		11	13	"DETACH signal" has been changed to "DETECH signal" in the content of the "DETACH Interface Block" Section.
		12	14	Eliminated the "RESET signal input" Section and added the "Setting the Reset" Section.
		--	15	The "XTAL Input Frequency of BCM2002X" and "XTAL Input Frequency of CX72303" Sections have been added.
		13	15	Eliminated the "LPO_CLK" row of the "Pin name" column in the table of the "RF/IF" Section..
14-16	16-18	Changed the System Configuration Examples.		
FEDL7055-01	Dec. 17, 2002	1	1	Partially changed the contents of "FEATURES" Section.
		2	2	Changed the contents of "Package" row in the table.
		13	13	Partially added the contents of "UART Block" Section.
		13	14	Partially added the contents of "PCM-CVSD" Section.

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7055-01	Dec. 17, 2002	13	15	Partially eliminated the contents of "DETACH Interface Block" Section.
		—	17-19	Added "Power Supply Current Characteristics by Power Saving Mode" and "AC Characteristics" Sections.
		9	19	Partially added the contents of "REFERENCE FOR VOLTAGE SUPPLY CIRCUIT" Section.
		10	20	Partially added the contents of "REFERENCE FOR OSCILLATOR CIRCUIT" Section.
		14	22	Partially added the contents of "Clock Selection" Section.
		16	24	Partially changed the contents of "System Configuration Example" Section.
FEDL7055-02	Apr. 8, 2003	6	6	Partially added the contents of "RF I/F" Section.
		16	16	Partially added the contents of "DC Characteristics" Section.
		18	18	Partially eliminated the contents of "Reset" Section.
		23	23	Eliminated the "RESET" row in the table of the "TEST I/F" Section.

**NOTICE**

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