FEDL70512-04
Issue Date: Sep. 2, 2003

OKI Semiconductor

ML70512

Bluetooth Baseband Controller IC

GENERAL DESCRIPTION

The ML70512 is a CMOS digital IC for use in 2.4 GHz band Bluetooth™ systems. This IC incorporates the ARM7TDMI® as the CPU core, features a highly expandable architecture, and supports the interfaces for a variety of applications. Since the ML70512 has Oki's Bluetooth protocol stack software installed, when the IC is used in conjunction with the Bluetooth RF transceiver IC, data/voice communications are possible while maintaining interconnectivity with other Bluetooth systems.

FEATURES

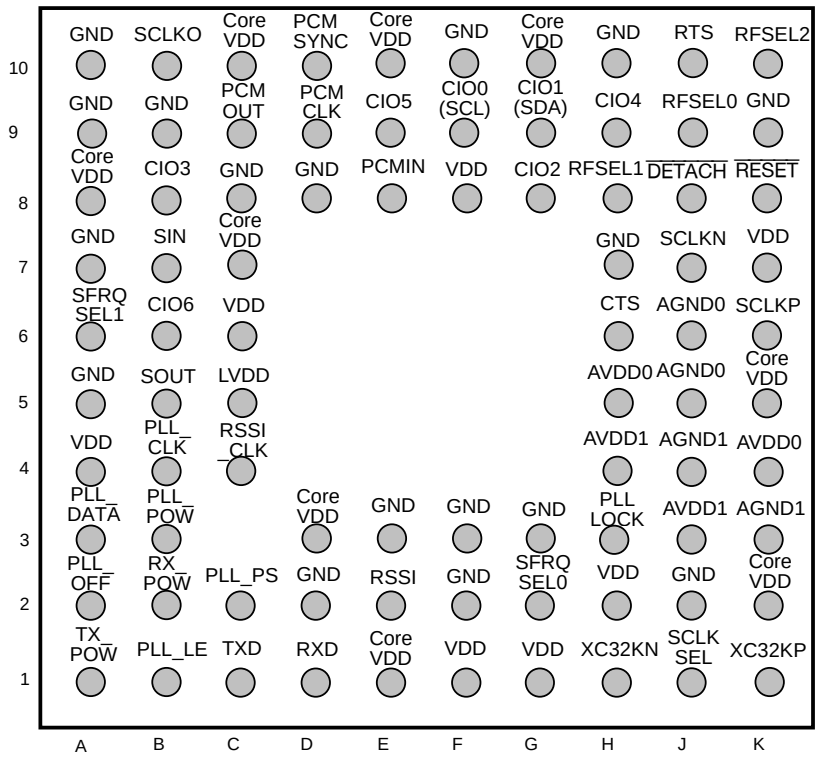
- Conforms to Bluetooth Specification (Ver1.1)
- Designed for connection with the RF-LSI interface, such as the OKI RF-LSI interface (ML7050, ML70561), the SKYWORKS RF-LSI interface (CX72303), or the BROADCOM RF-LSI interface (BCM2002X) that functions as the Bluetooth RF-LSI interface
- The high-speed, low-power ARM7TDMI™ is installed as the CPU core
- PCM-CVSD transcoder that provides high quality voice using the noise filter is installed
- Low power consumption in flexible power management modes according to operating modes of Bluetooth
- $\overline{\text{DETACH}}$ signal provides control of change to power-saving mode (STOP) and return request to normal mode.
- UART interface corresponding to baud rates up to 921.6 kbps
- I^2C bus interface provides accesses to EEPROM or PCM-Codec
- Selactable 12 MHz, 13 MHz, or 16 MHz for the system clock
- Selectable 32 kHz or 32.768 kHz for the LPO clock
- Built-in programmed ROM eliminates external ROM/FLASH
- The packages are available in two types:
  83-pin WCSP for ML70512HB
  84-pin BGA for ML70512LA

SPECIFICATIONS

Process	0.16 μm CMOS (5-layer metal wire)
Package	83-pin WCSP (P-VFLGA83-6.22×6.22-0.50-W) (Dimensions: 6.22 mm × 6.22 mm × 0.48 mm; pin pitch: 0.50 mm) 84-pin BGA (P-LFBGA84-0909-0.80) (Dimensions: 9 mm × 9 mm × 1.5 mm; pin pitch: 0.80 mm)
Supply current	23.4 mA (24 MHz operation)
Operating voltage ranges	2.70 to 3.6 V for input-output, 1.65 to 1.95 V for internal circuits
Operating frequency	24 MHz
Built-in ROM size	384 KB (for ARM program)
Built-in RAM size	72 KB
Input clocks	12 MHz, 13 MHz, or 16 MHz (system clock) 32 kHz or 32.768 kHz (LPO clock)
RF-LSI interface	OKI RF-LSI interface (ML7050, ML70561) SKYWORKS RF-LSI interface (CX72303) BROADCOM RF-LSI interface (BCM2002X)
Installed interfaces	UART interface (up to 921.6 Kbps) General-purpose I/O interface (Bits 0 and 1 are used as a pin for I^2C bus interface depending on software installed) PCM interface (PCM Linear/A-law/μ-law can be selected) DETACH interface
Timers	16-bit auto reload timer (1ch) 18-bit auto reload timer (3ch)
Interrupt controller	11 causes
Clock control circuit	Crystal oscillator circuit (12 MHz, 13 MHz, or 16 MHz, 32 kHz or 32.768 kHz) Internal PLL

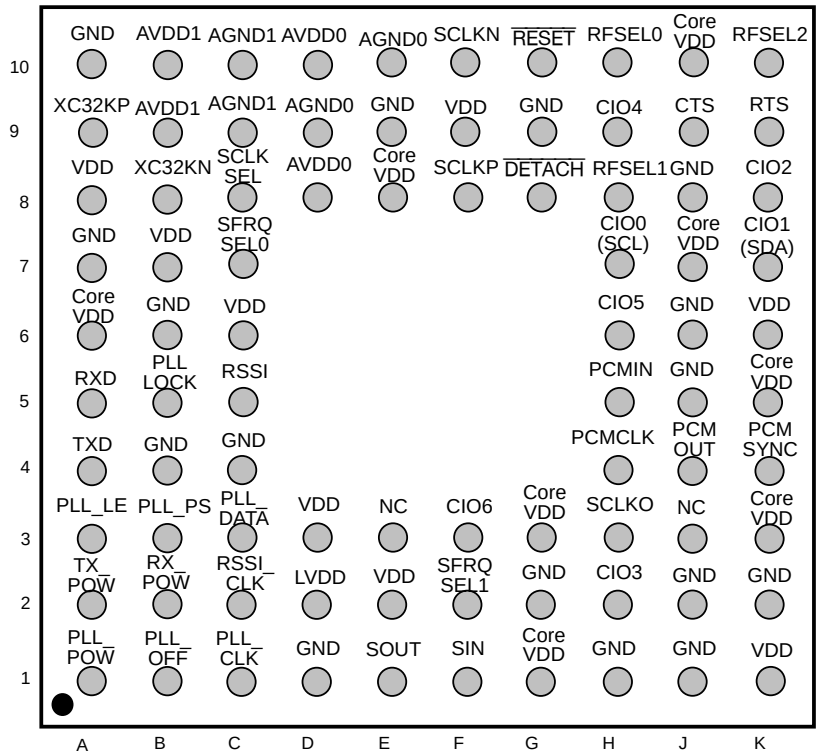
PIN PLACEMENT

ML70512HB: 83-pin WCSP (P-VFLGA83-6.22 × 6.22-0.50-W)



TOP VIEW

ML0512LA: 84-pin BGA (P-TFBGA84-0909-0.80)



TOP VIEW

PIN DESCRIPTIONS

RF I/F

Pin Name	Direc-tion [*0]	Internal Pull Up/ Down, Schmitt	Initial Value	Pin Placement		Description
				ML70512HB	ML70512LA	
TXD	O	—	L L L L	C1	A4	ML7050: Transmit data output CX72303: Transmit data output BCM2002X: Transmit data output ML70561: Transmit data output
RXD	I	—	— — — —	D1	A5	ML7050: Receive data input CX72303: Receive data input BCM2002X: Receive data input ML70561: Receive data input
PLL_DATA	O	—	X H L L	A3	C3	ML7050: Serial write data CX72303: Serial write data BCM2002X: Transmit enable ML70561: Transmit enable (Active H)
PLL_CLK	O	—	L L L L	B4	C1	ML7050: Serial clock CX72303: Serial clock BCM2002X: Serial clock ML70561: Serial clock
PLL_LE	O	—	L H L L	B1	A3	ML7050: Serial road enable 0: Negate, 1: Assert CX72303: Serial enable 0: Assert, 1: Negate BCM2002X: RF-LSI synthesizer on 0: Negate, 1: Assert ML70561: RF-LSI synthesizer on 0: Negate, 1: Assert
RSSI	I	—	— — — —	E2	C5	ML7050: Receive field strength data input CX72303: Serial read data BCM2002X: Serial read data ML70561: Serial read data
RSSI_CLK	O	—	H L H H	C4	C2	ML7050: Receive field strength data clock CX72303: RF-LSI receiving characteristic control BCM2002X: System clock request ML70561: System clock request
PLL_POW	O	—	H L H H	B3	A1	ML7050: Local PLL power control 0: Assert, 1: Negate CX72303: PA Power control 0: Negate, 1: Assert BCM2002X: Select serial transmit mode ML70561: Select serial transmit mode

Pin Name	Direc-tion [*0]	Internal Pull Up/ Down, Schmitt	Initial Value	Pin Placement		Description
				ML70512HB	ML70512LA	
TX_POW	O	—	H L L L	A1	A2	ML7050: Transmit enable 0: Assert, 1: Negate CX72303: Transmit enable 0: Negate, 1: Assert BCM2002X: Serial write data ML70561: Serial write data
RX_POW	O	—	H L L L	B2	B2	ML7050: Receive enable 0: Assert, 1: Negate CX72303: Receive enable 0: Negate, 1: Assert BCM2002X: Receive enable ML70561: Receive enable

[*0] "I" = Input, "O" = Output, "I/O" = Input/Output

RF I/F

Pin Name	Direc-tion [*0]	Internal Pull Up/ Down, Schmitt	Initial Value	Pin Placement		Description
				ML70512HB	ML70512LA	
PLL_PS	O	—	L L L L	C2	B3	ML7050: "L" CX72303: Power on reset 0: Assert (reset) 1: Negate BCM2002X: RF-LSI receiving characteristic control ML70561: SYNCWORD detection
PLLLOCK	I	—	— — — —	H3	B5	ML7050: — CX72303: — BCM2002X: 1MHz clock ML70561: Clock for 1 MHz transmit data
PLL_OFF	O	—	H — L L	A2	B1	ML7050: PLL loop control 0: Open loop 1: Closed loop CX72303: Diversity output BCM2002X: PA Power control ML70561: PA Power control

CLK and Configuration

Pin Name	Direc-tion	Internal Pull Up/ Down, Schmitt	Initial Value	Pin Placement		Description
				ML70512HB	ML70512LA	
SCLKP	I	—	—	K6	F8	System clock (12/13/16 MHz) pins (Power level: CMOS level)
SCLKN	O	—	—	J7	F10	
XC32KP	I	—	—	K1	A9	Subclock pins (for oscillator)
XC32KN	O	—	—	H1	B8	
SCLKSEL	I	—	—	J1	C8	System clock frequency select pin L: Select CLK divided by internal PLL H: Select subclock
SFRQSEL 0–1	I	—	—	*[1]	*[2]	System clock (SCLK) frequency select/ BCM crystal frequency select pins
RFSEL 0–2	I	—	—	*[3]	*[4]	RF-LSI select pins

SFRQSEL [1:0]	SCLK input frequency (RFSEL ≠ 101)	BCM crystal frequency (RFSEL = 101)
00	13 MHz	19.68 MHz
01	12 MHz	19.2 MHz
10	16 MHz	19.8 MHz
11	Reserved	13 MHz

RFSEL[2:0]	RF-LSI
001	ML7050 (OKI)
010	CX72303 (SKYWORKS)
011	ML70561 (OKI)
101	BCM2002X (BROSDCOM)
Others	Reserved

CLK and Configuration

Pin Name	Direc-tion	Internal Pull Up/ Down, Schmitt	Initial Value	Pin Placement		Description
				ML70512HB	ML70512LA	
RESET	I	Schmitt	—	K8	G10	Hardware reset pin (Reset = L)
DETACH	I	Schmitt	—	J8	G8	Sleep pin (Sleep = L)
SCLKO	O	—	—	B10	H3	System clock (12/13/16 MHz) output pins

[*1] SFRQSEL0: G2; SFRQSEL1: A6
[*2] SFRQSEL0: C7; SFRQSEL1: F2
[*3] RFSEL0: J9; RFSEL1: H8; RFSEL2: K10
[*4] RFSEL0: H10; RFSEL1: H8; RFSEL2: K10

PCM I/F

Pin Name	Direc-tion	Internal Pull Up/ Down, Schmitt	Initial Value	Pin Placement		Description
				ML70512HB	ML70512LA	
PCMOUT	O	—	L	C9	J4	PCM data output
PCMIN	I	Pull up	—	E8	H5	PCM data input
PCMSYNC	I/O	Pull down	—	D10	K4	PCM sync signal (8 kHz), Initial setting: input (can be switched by an internal register)
PCMCLK	I/O	Pull down	—	D9	H4	PCM clock (64 kHz/128 kHz) Initial setting: input (can be switched by an internal register)

Note: The PCM sync signal (8 kHz) must be guaranteed at the accuracy of ±50 ppm if the PCMSYNC pin is configured as an input.

UART I/F

Pin Name	Direc-tion	Internal Pull Up/ Down, Schmitt	Initial Value	Pin Placement		Description
				ML70512HB	ML70512LA	
SOUT	O	—	H	B5	E1	ACE transmit serial data
SIN	I	Schmitt	—	B7	F1	ACE receive serial data
RTS	O	—	—	J10	K9	ACE transmit data ready
CTS	I	—	H	H6	J9	ACE transmit ready

Port

Pin Name	Direc-tion	Internal Pull Up/ Down, Schmitt	Initial Value	Pin Placement		Description
				ML70512HB	ML70512LA	
CIO0 (SCL)	I/O	—	H	F9	H7	I^2C serial clock (output)
CIO1 (SDA)	I/O	—	—	G9	K7	I^2C serial data (input)
CIO2	I/O	—	—	G8	K8	General port (initial state: input)
CIO3	I/O	—	L	B8	H2	General port (initial state: output)
CIO4	I/O	—	H	H9	H9	General port (initial state: output)
CIO5	I/O	—	—	E9	H6	General port (initial state: input)
CIO6	I/O	—	—	B6	F3	General port (initial state: input)

NC

Pin Name	Direc-tion	Internal Pull Up/ Down, Schmitt	Initial Value	Pin Placement		Description
				ML70512HB	ML70512LA	
NC	—	—	—	—	[*4]	No connection

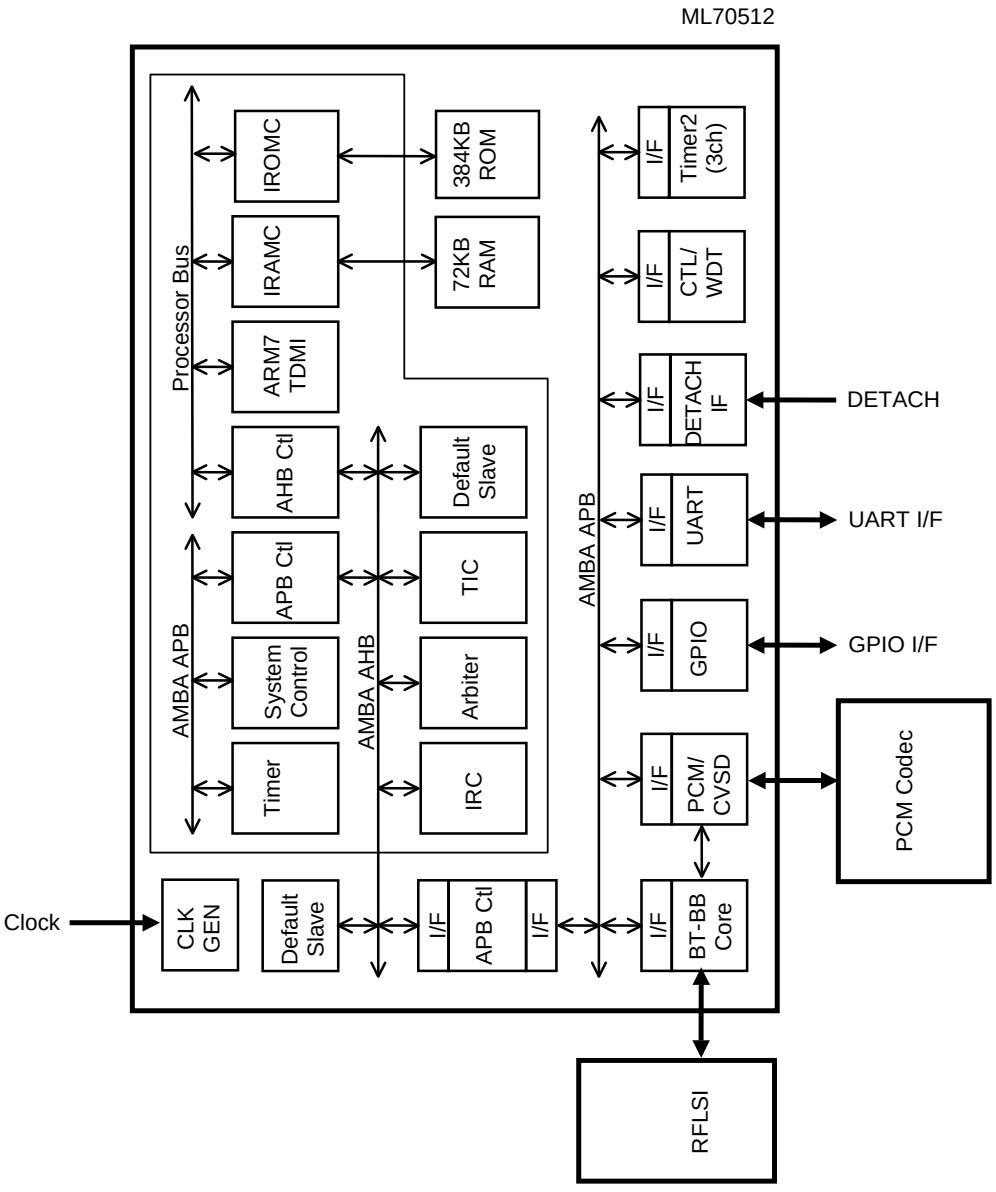
[*4] NC: E3, J3
Note: Do not wire under the NC pin.

Power, GND

Pin Name	Direc-tion	Internal Pull Up/ Down, Schmitt	Initial Value	Pin Placement		Description
				ML70512HB	ML70512LA	
V_{DD}	—	—	—	[*5]	[*6]	I/O power supply pin 2.70 to 3.6 V
CoreV_{DD}	—	—	—	[*7]	[*8]	Power supply pin for internal circuit 1.65 to 1.95 V
LV_{DD}	—	—	—	C5	D2	RF-I/O power suply pin (Same voltage to the V_{DD} for RF-LSI)
GND	—	—	—	[*9]	[*10]	Digital block ground pin
$AV_{DD}0$	—	—	—	[*11]	[*12]	Analog block power supply pin 1.65 to 1.95 V
$AV_{DD}1$	—	—	—	[*13]	[*14]	
AGND0	—	—	—	[*15]	[*16]	Analog block ground pin
AGND1	—	—	—	[*17]	[*18]	

[*5] V_{DD}: A4, C6, F1, F8, G1, H2, K7
[*6] V_{DD}: A8, B7, C6, D3, E2, F9, K1, K6
[*7] Core V_{DD}: A8, C7, C10, D3, E1, E10, G10, K2, K5
[*8] Core V_{DD}: A6, E8, G1, G3, J7, J10, K3, K5
[*9] GND: A5, A7, A9, A10, B9, C8, D2, D8, E3, F2, F3, F10, G3, H7, H10, J2, K9
[*10] GND: A7, A10, B4, B6, C4, D1, E9, G2, G9, H1, J1, J2, J5, J6, J8, K2
[*11] $AV_{DD}0$: H5, K4
[*12] $AV_{DD}0$: D8, D10
[*13] $AV_{DD}1$: H4, J3
[*14] $AV_{DD}1$: B9, B10
[*15] AGND0: J5, J6
[*16] AGND0: D9, E10
[*17] AGND1: J4, K3
[*18] AGND1: C9, C10

BLOCK DIAGRAM



DESCRIPTION OF INTERNAL BLOCKS

CLKGEN Block

- Generates a clock that is supplied to each block through SCLKP (12/13/16 MHz)
- STOP/HALT function

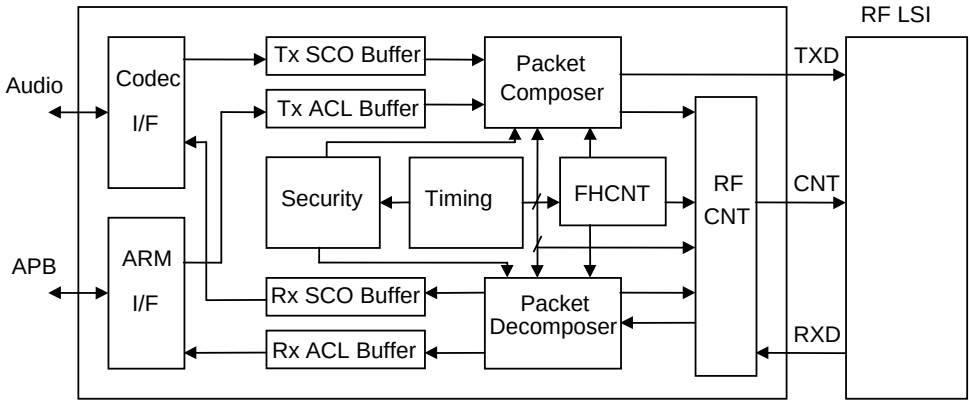
CTL/WDT Block

- Control of the frequency division function of the internal main clock
- Control of clock supplied to each peripheral
- Control of reset of each peripheral
- STOP/HALT control
- Watchdog timer function (interrupt/reset)

Timer Block

- 3 channels
- 18-bit timer counter
- Interrupt by compare function
- One shot, interval, or free-run mode

Base band Core Block



- RF Controller
  - RF power supply control (PLL, TX, RX)
  - Local PLL frequency division ratio setting
  - Receive clock regeneration function
  - Synchronization detection (synchronizing within the permissable error limit of SyncWord)
  - Receive clock re-timing function

- FH Controller hopping
  - Sequence control
  - Frequency hopping selection function
  - CRC computation's initial value selection function

- Timing Generator
  - Bluetooth clock generation
  - Operation interrupts depend on mode (slot, scan, sniff, hold, park)
  - Sync detection timing generation (sync window ±10 μs)
  - PLL setting timing generation
  - Transmit/Receive timing generation
  - Multi-master timing management function

- Packet Composer
  - Access code generation (SyncWord generation, appending PR*TRAILER)
  - Packet header generation (HEC generation, scrambling, FEC encoding)
  - Payload generation (CRC generation, encryption, scrambling, FEC encoding)
  - Packet synthesis

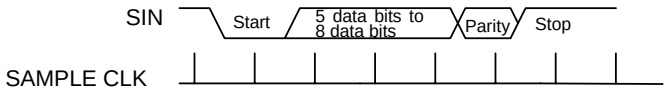
- Packet Decomposer
  - Packet decomposition (separating the packet header and the payload)
  - Packet header processing (FEC decoding, descrambling, HEC error detection, header information separation)
  - Payload processing (FEC decoding, descrambling, encryption decoding, CRC judgement, payload separation)

- Security
  - Various key generation functions (initialization, link key, encryption key)
  - Certification function
  - Encryption function

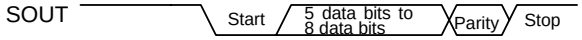
UART Block

- Full-duplex buffering method
- All status reporting function
- Built-in 64-byte transmit/receive FIFO
- Modem control based on CTS
- Programmable serial interface
- 5-, 6-, 7-, 8-bit characters
- Generation and verification of odd parity, even parity, or no parity
- 1, 1.5, or 2 stop bits
- Programmable Baud Rate Generator (9600 bps to 921.6 kbps)
- Error servicing for parity, overrun, and framing errors

- Configuration of 1 Data Frame during Reception



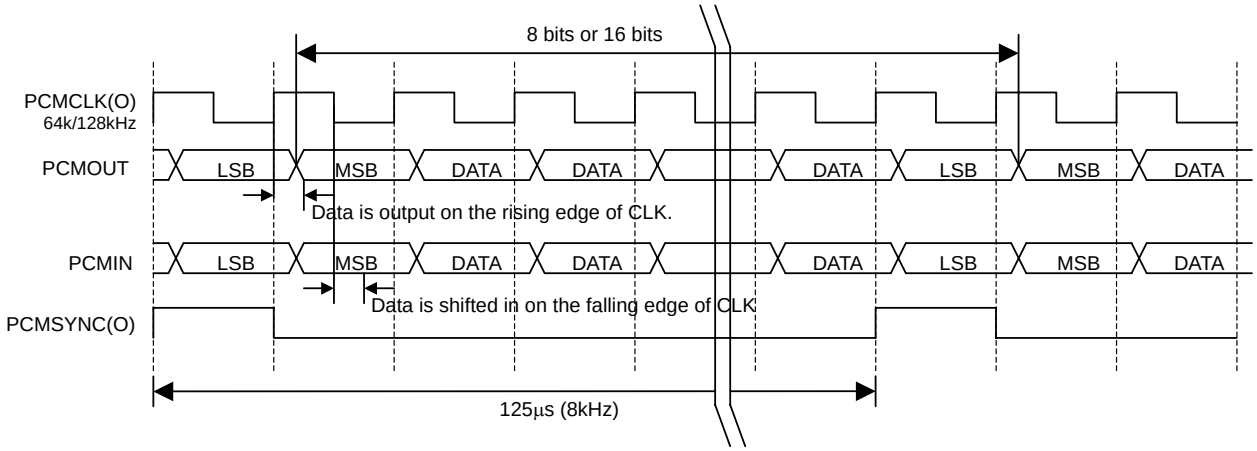
- Configuration of 1 Data Frame during Transmission



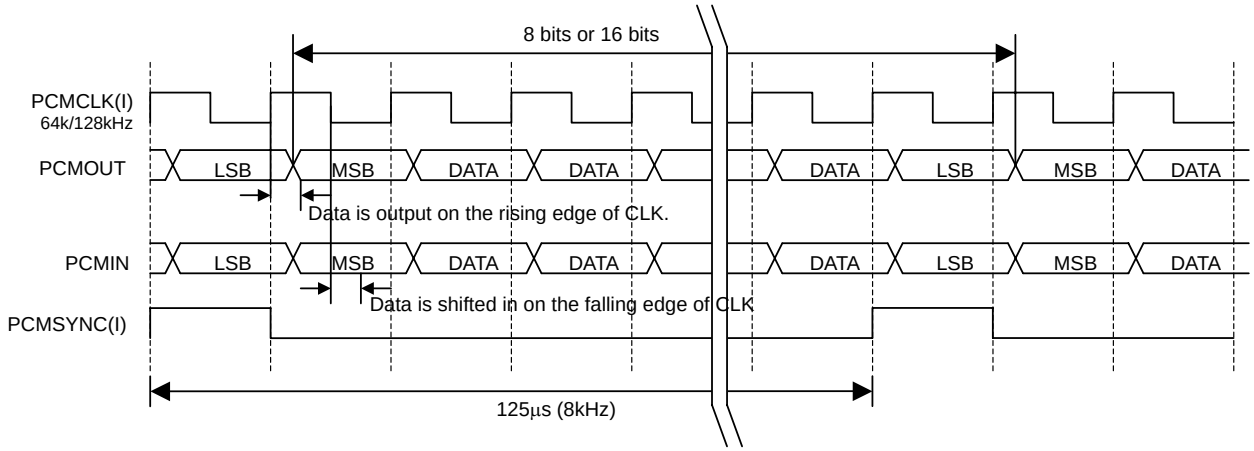
PCM-CVSD Transcoder Block

- Application side I/O:
  - PCM Codec
- Application-side format:
  - PCM linear (8, 14, 16 bits/sample, 8 kHz sampling frequency)/A-law/μ-law
- Bluetooth-side format:
  - CVSD/A-law/μ-law
- All combinations of the above conversions are supported
- PCMSYNC/PCMCLK I/O can be switched (initial setting: input)

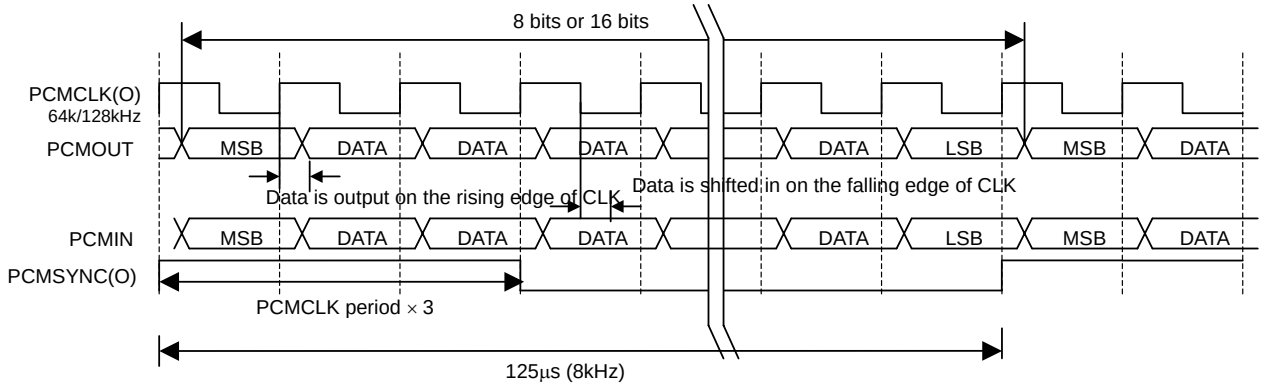
- Timing in Short Mode and in PCMCLK and PCMSYNC Output Mode
  (For PCM data of 14 bits/sample, lower 2 bits of 16 bits are invalid.)



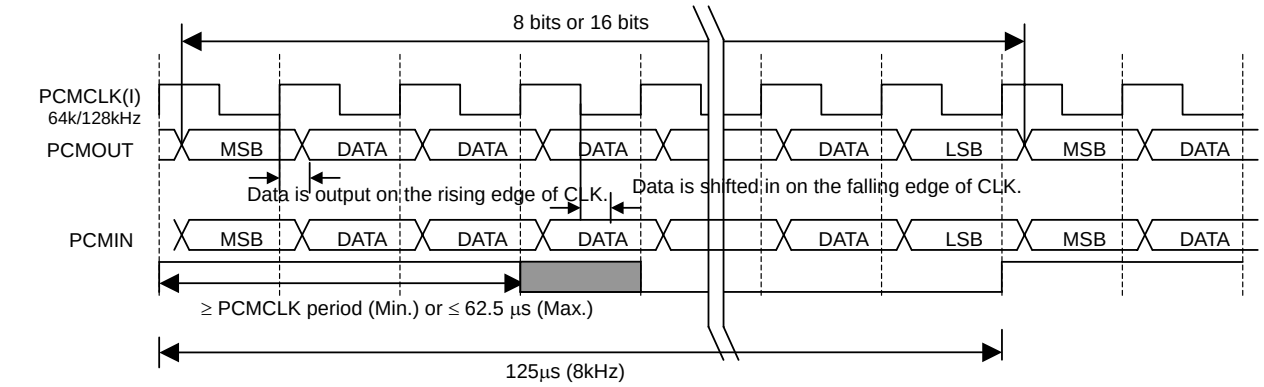
- Timing in Short Mode and in PCMCLK and PCMSYNC Input Mode.
  (For PCM data of 14 bits/sample, lower 2 bits of 16 bits are invalid.)



- Timing in Long Mode and in PCMCLK and PCMSYNC Output mode
  (For PCM data of 14 bits/sample, lower 2 bits of 16 bits are invalid.)



- Timing in Long Mode and in PCMCLK and PCMSYNC Input Mode.
  (For PCM data of 14 bits/sample, lower 2 bits of 16 bits are invalid.)



DETACH Interface Block

- Generation of the request for change to (from) the stop mode by detection of the rising (falling) edge of the $\overline{\text{DETACH}}$ signal
- Generation of the request for restore from the stop mode by detection of a SIN signal level change

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
I/O power supply voltage	V_{DD}/LV_{DD}	—	–0.3 to +4.5	V
Core power supply voltage	CoreV_{DD}/AV_{DD}	—	–0.3 to +2.5	V
Input voltage	V_I	—	–0.3 to +4.5	V
Allowable power dissipation	P_d	—	0.62	W
Storage temperature	T_{stg}	—	–55 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
I/O power supply voltage	V_{DD}/LV_{DD}	—	2.7	3.3	3.6	V
Core power supply voltage	CoreV_{DD}/AV_{DD}	—	1.65	1.8	1.95	V
"H" level input voltage	Vih	—	2.2	—	V_{DD}	V
"L" level input voltage	Vil	—	0	—	0.8	V
Operating temperature	Ta	—	–40	—	85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 to 3.6 V, CoreV_{DD} = 1.65 to 1.95 V, Ta = –40 to +85°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"H" level output voltage	Voh	Ioh = –2 mA	3.0V≤Vdd≤3.6V	2.4	—	—	V
			2.7V≤Vdd<3.0V	2.2	—	—	
"L" level output voltage	Vol	Iol = 2 mA		—	—	0.4	V
Input leakage current	Ii	Vi = GND to 3.6 V		–10	—	10	µA
		Vi = V_{DD} 50 kΩ Pull-down		10	66	200	
		Vi = GND 50 kΩ Pull-up		–200	–66	–10	
Output leakage current	Io	Vo = GND to V_{DD}		–10	—	10	µA
		Vo = V_{DD} 50 kΩ Pull-down		10	66	200	
Power supply current (during operation)	Iddo	During 24 MHz operation		0	23.4	33	mA
Power supply current (during stand-by)	Idds	CLK stopped		—	50	250	µA

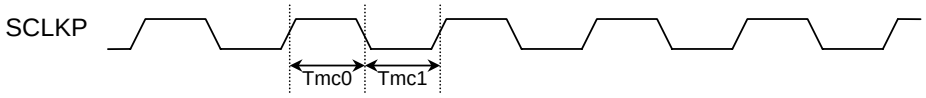
Power Supply Current (IDDO) Characteristics by Power Saving Mode

(V_{DD} = 2.7 V to 3.6V, CoreV_{DD} = 1.65 V to 1.95V, Ta = -40 to 85°C)

Operating mode	Conditions	Min.	Typ.	Max.	Unit
STOP mode ($\overline{\text{DETACH}}$ = "L")	—	—	0.05	—	mA
Page Scan operating mode	Interval:1.28sec Window:22.5msec	—	1.5	—	
Poll Interval operating mod	Interval:40slot	—	12.1	—	
Sniff operating mode	Interval:2000slot Attempt:4frame	—	1.7	—	
Hold operating mode	Interval:4000slot	—	4.9	—	
ACL operating mode	DH1/DM1	—	23.4	—	
	RX:DH3/DM3 TX:DH1/DM1	—	20.5	—	
	RX:DH5/DM5 TX:DH1/DM1	—	19.6	—	

AC Characteristics

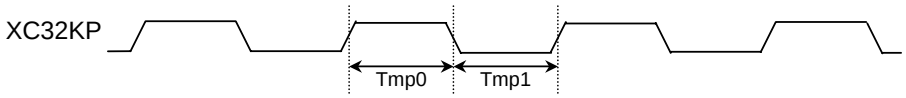
⊙ System clock (SCLKP)



(V_{DD} = 2.7 to 3.6V, CoreV_{DD} = 1.65 to 1.95V, Ta = -40 to 85°C)

Parameter	Description	Min	Typ	Max	Unit
Tmc0	Duty in SCLKP “H” duration	40	50	60	%
Tmc1	Duty in SCLKP “L” duration	40	50	60	%

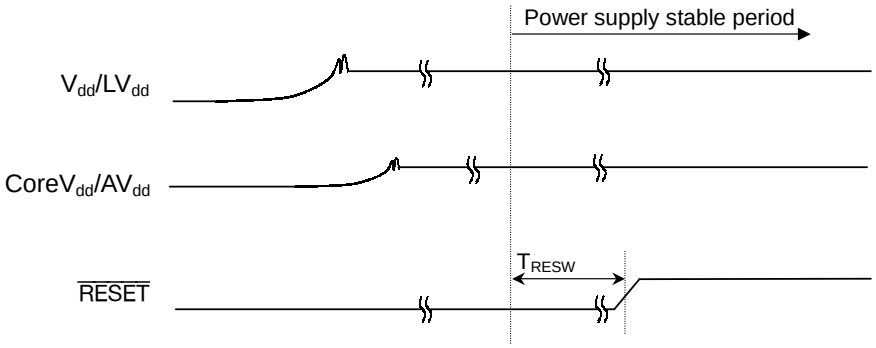
⊙ Sub-clock (XC32KP)



(V_{DD} = 2.7 to 3.6V, CoreV_{DD} = 1.65 to 1.95V, Ta = -40 to 85°C)

Parameter	Description	Min	Typ	Max	Unit
Tmp0	Duty in XC32KP “H” duration	40	50	60	%
Tmp1	Duty in XC32KP “L” duration	40	50	60	%

⊙ Reset

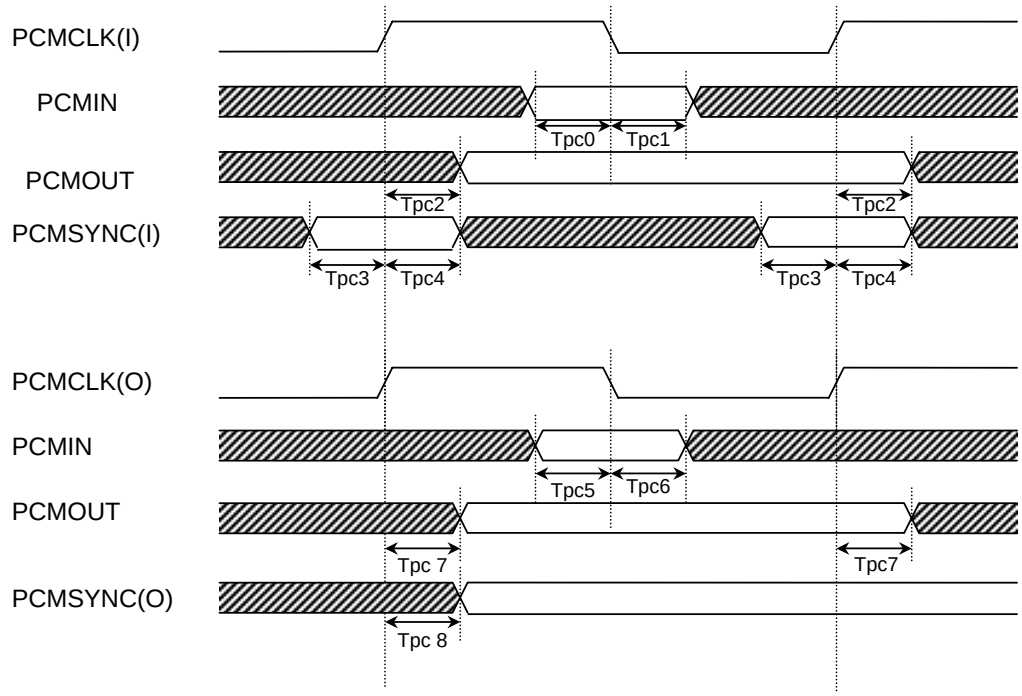


(V_{DD} = 2.7 to 3.6V, $CoreV_{DD}$ = 1.65 to 1.95V, Ta = -40 to 85°C)

Parameter	Description	Min	Typ	Max	Unit
T_{RESW}	Reset pulse width	10	—	—	µs

Note : Apply "L" to the $\overline{RESET}$ pin for 10 µsec or more after the power supply has been settled.

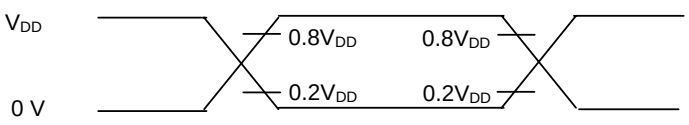
⊙ PCM interface



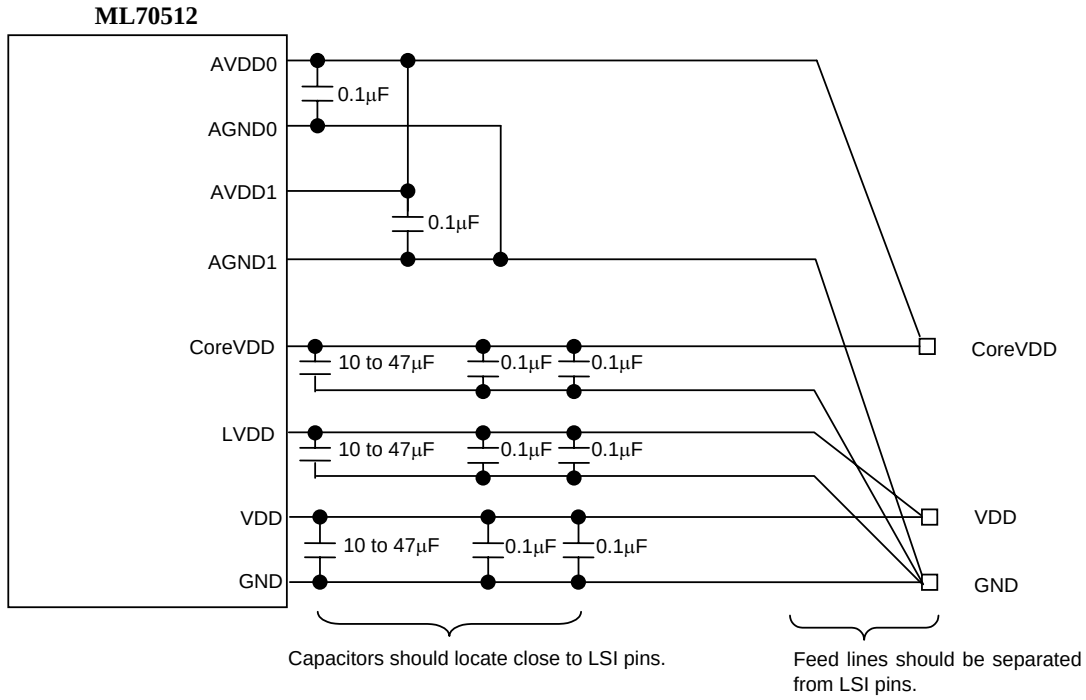
(Vdd = 2.7 to 3.6V, CoreVdd = 1.65 to 1.95V, Ta = -40 to 85°C)

Parameter	Description	Min	Typ	Max	Unit
Tpc0	PCMIN setup time relative to PCMCLK (input) falling edge	100	—	—	ns
Tpc1	PCMIN hold time relative to PCMCLK (input) falling edge	100	—	—	ns
Tpc2	PCMOUT delay time relative to PCMCLK (input) rising edge	—	—	250	ns
Tpc3	PCMSYNC (input) setup time relative to PCMCLK (input) rising edge	100	—	—	ns
Tpc4	PCMSYNC (input) hold time relative to PCMCLK (input) rising edge	100	—	—	ns
Tpc5	PCMIN setup time relative to PCMCLK (output) falling edge	100	—	—	ns
Tpc6	PCMIN hold time relative to PCMCLK (output) falling edge	100	—	—	ns
Tpc7	PCMOUT delay time relative to PCMCLK (output) rising edge	—	—	250	ns
Tpc8	Delay time from PCMCLK (output) rising edge to PCMSYNC (output)	—	—	150	ns

⊙ AC Characteristic Measuring Points



REFERENCE FOR VOLTAGE SUPPLY CIRCUIT



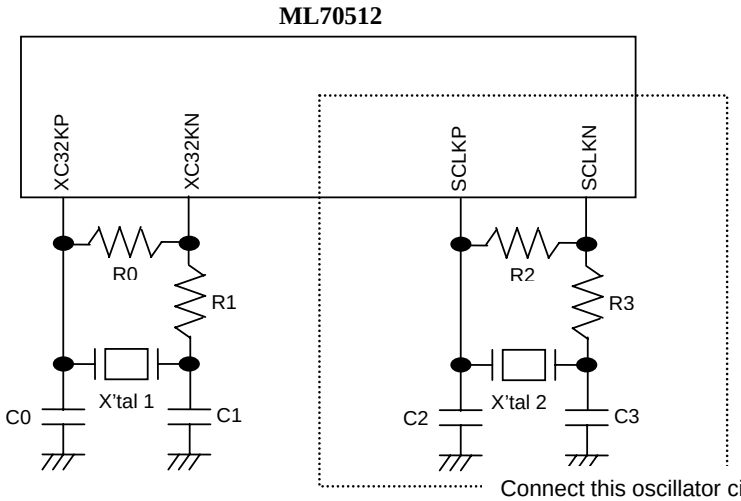
Example of ML70512 voltage supply circuit

- Insert appropriate bypass capacitors between the V_{DD} and GND lines.

Note 1: Precautions to insert the bypass capacitors
- Use traces of V_{DD} and GND lines wider than those of the other signal lines.
- Keep the length of traces between the bypass capacitors and the V_{DD} line and between the bypass capacitors and the GND line as short as possible.
- Keep the length of traces between the bypass capacitors and the V_{DD} line and between the bypass capacitors and the GND line as equal as possible.

The circuit is subject to change according to the specific LSI board design. Please contact Oki Electric Industry Co., Ltd. for detailed information.

REFERENCE FOR OSCILLATOR CIUCUIT



Example of oscillator circ

Note 1: The values of C0 and C1, and R0 and R1 should be determined according to the specifications for the external crystal X'tal 1 (32 or 32.768 kHz).
The values of C2 and C3, and R2 and R3 should be determined according to the specifications for the external crystal X'tal 2 (12, 13, or 16 MHz).

Note 2: The crystal oscillator circuit should be connected to pins SCLKP and SCLKN only when the OKI RF-LSI (ML7050) is connected. In other cases, the system clock should be input from the RF-LSI to pin SCLKP.

Note 3: In the case of 12 MHz, 13 MHz, or 16 MHz system clock (SCLKP) input, make sure the crystal frequency tolerance is ±20 ppm for temperature, supply voltage, and aging.
In the case of 32 kHz or 32.768 kHz sub-clock (XC32KP) input, make sure the crystal frequency tolerance is ±250 ppm for temperature, supply voltage, and aging.

Note 4: Precautions to build a crystal oscillator circuit
- Keep length of wire traces as short as possible.
- Do not cross the crystal oscillator circuit wires over other signal line wires.
- Do not keep signal line wires through which high current flows close to the crystal oscillator circuit.
- Keep the grounding point of the capacitors in the oscillator circuit at the potential equal to GND. And do not connect the capacitors to the GND or GND lines through which high current flows.
- Do not output signals from the oscillator circuit.

The circuit is subject to change according to the specific LSI board design. Please contact Oki Electric Industry Co., Ltd. for detailed information. It is recommended to determine the final circuit values including the capacitance of the circuit board designed by the user.

APPLICATION NOTES

Clock Selection

- The system clock frequency is selected according to external pin SFRQSEL.

  SFRQSEL = 00 : A 13 MHz clock is input to external pin SCLKP.
  SFRQSEL = 01 : A 12 MHz clock is input to external pin SCLKP.
  SFRQSEL = 10 : A 16 MHz clock is input to external pin SCLKP.

  A 12 MHz clock is input to external pin SCLKP regardless of SFRQSEL when BCM2002X is selected (RFSEL = 101).

- The CPU clock supply source is selected according to external pin SCLKSEL.

  SCLKSEL = 0 : Use the clock that was divided down from the internal PLL output of 192 MHz that was generated from external pins SCLKP. (Dividing ratios are selectable in the range of 1/6 to 1/16. Initial value is 1/8 (24 MHz).)
  SCLKSEL = 1 : Use external pins XC32KP.

  Note: The clock supply source can be set by the CLKCNTL register in the CTL/WDT block once the LSI is powered up.

- The frequency of CPU clock is selectable from the high speed (24 MHz) and low speed (16 MHz). This can be performed by the Vendor Specific Command.

Setting the Reset

- Apply "L" level to the $\overline{\text{RESET}}$ pin for more than 10 µs after power voltage is stabilized. When the system clock oscillator circuit is stable and the $\overline{\text{RESET}}$ pin is at "H" level, the internal reset is released and operation starts after the internal reset is held for 1.9 ms for the input clock of 13 MHz, 2.0 ms for the input clock of 12 MHz, or 1.5 ms for the input clock of 16 MHz.
  Moreover, after power voltage is stable, the values of SCLKSEL, SFRQSEL0-1, and RFSEL0-2 should be determined before the $\overline{\text{RESET}}$ pin is at "H" level.

Setting the UART Baud Rate

- It is possible to set the UART baud rate using the Vendor Specific Commands.

  Available baud rate settings:
  9600/19.2k/38.4k/56k/57.6k/115.2k/230.4k/345.6k/460.8k/921.6k
  (Initial value is 115.2 kbps.)

Setting the PCM-CVSD Transcoder

- It is possible to set the PCM-CVSD transcoders using the Vendor Specific Commands.
  For command details, contact Oki Electric Industry Co., Ltd.

- It is possible to set the following parameters using the VCCTL command:
  - PCMSYNC/PCMCLK mode (initial setting: input)
  - Mute reception (initial setting: OFF)
  - Mute transmission (initial setting: OFF)
  - Aircoding
    CVSD (initial setting)/μ-law/A-law
  - Interface coding
    Linear (initial setting)/μ-law/A-law
  - PCM format (data width of one PCM Linear sample)
    8-bit (initial setting)/14-bit/16-bit
  - Serial interface format
    Short frame (initial setting)/long frame
  - Application interface mode
    PCM Codec I/F (initial setting)/APB I/F

XTAL Input Frequency of BCM2002X

- If the system clock is supplied from BCM2002X, the XTAL input frequency of BCM2002X must be 13, 19.2, 19.68, or 19.8 MHz. 12 MHz should not be applied.

XTAL Input Frequency of CX72303

- If the system clock is supplied from CX72303, the XTAL input frequency of CX72303 must be 13 MHz. 10 MHz should not be applied.

Required processes when interface pins are unused

- The following tables show the processes that should be performed when interface pins are not used.
- The pins that are not included in the following table should be left open.

RF I/F

Pin Name	Process When Pin Not Used	Comments
RXD	GND	
RSSI	GND	
PLLLOCK	GND	

UART I/F

Pin Name	Process When Pin Not Used	Comments
SIN	V_{DD}	
CTS	GND	

PCM I/F

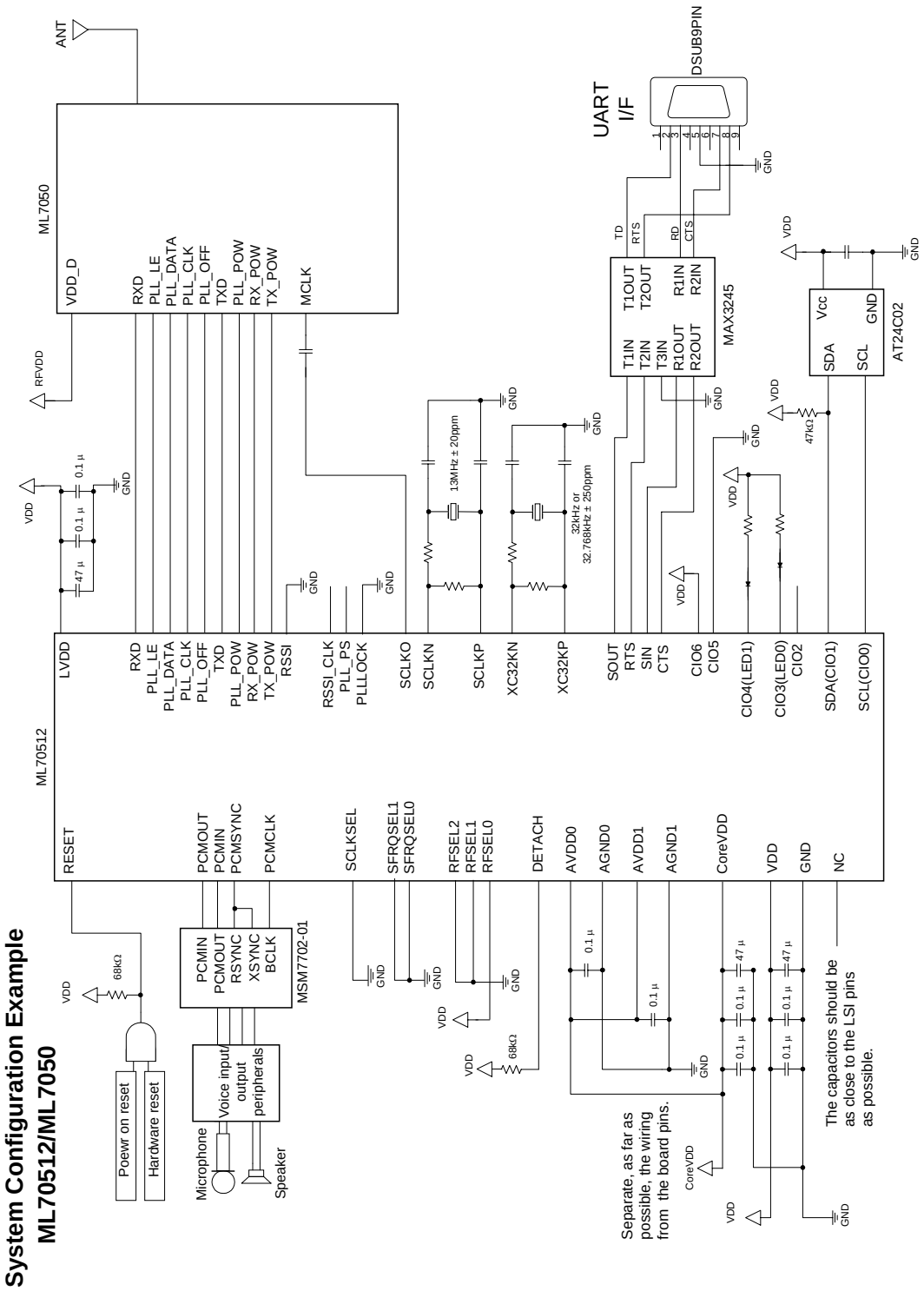
Pin Name	Process When Pin Not Used	Comments
PCMIN	Open or V_{DD}	
PCMSYNC	Open or GND	
PCMCLK	Open or GND	

Processes of Other Pins

TEST I/F etc.

Pin Name	Process When Pin Not Used	Comments
$\overline{\text{DETACH}}$	Pull up or V_{DD}	

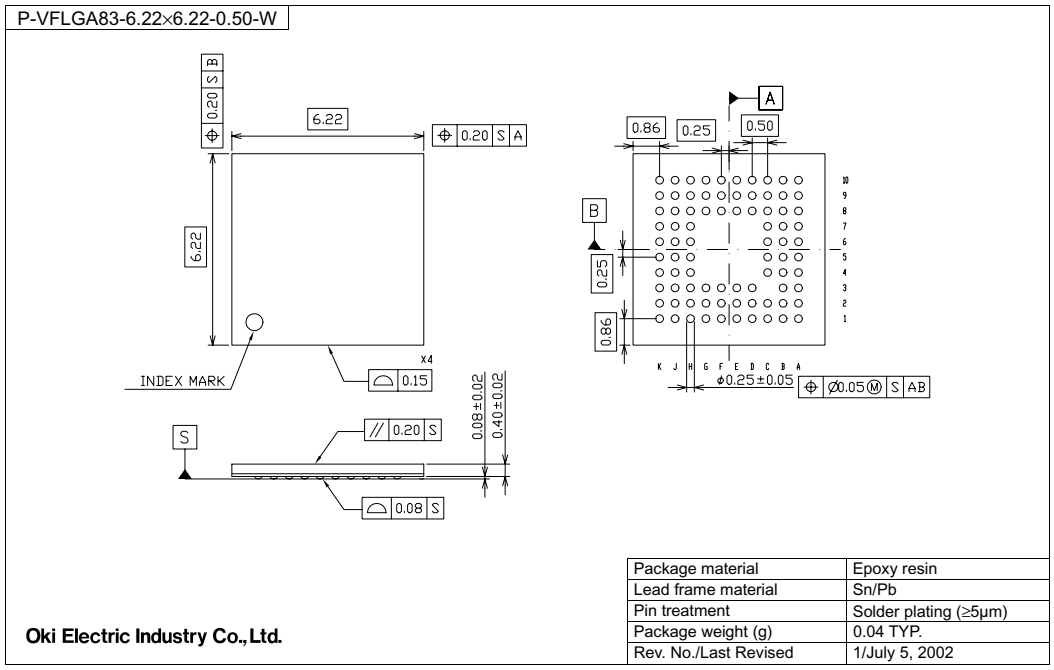
System Configuration Example
ML70512/ML7050



PACKAGE DIMENSIONS

ML70512HB - 83pinWCSP (P-VFLGA83-6.22 × 6.22-0.50-W)

(Unit: mm)



Package material	Epoxy resin
Lead frame material	Sn/Pb
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.04 TYP.
Rev. No./Last Revised	1/July 5, 2002

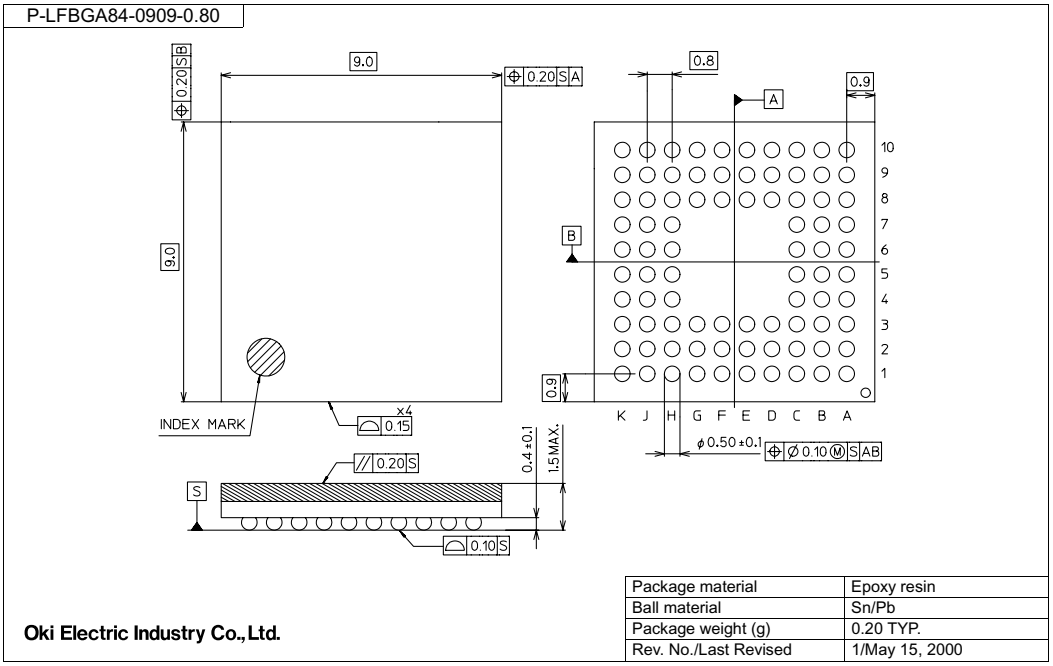
Note: A lead-free package is available. Please contact Oki Sales Office/Distributors for more information.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

ML70512LA - 84pin BGA (P-LFBGA84-0909-0.80)

(Unit: mm)



Package material	Epoxy resin
Ball material	Sn/Pb
Package weight (g)	0.20 TYP.
Rev. No./Last Revised	1/May 15, 2000

Note: A lead-free package is available. Please contact Oki Sales Office/Distributors for more information.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL70512-01	Feb. 17, 2003	–-	–-	Final edition 1
FEDL70512-02	Mar. 18, 2003	–-	–-	Final edition 2
		23	23	Eliminated the "$\overline{\text{RESET}}$" row in the table of the "TEST I/F " Section.
FEDL70512-03	Apr. 8, 2003	–-	–-	Final edition 3
		18	18	Partially eliminated the contents of "Reset" Section.
FEDL70512-04	Sep. 2, 2003	2	2	Partially eliminated the contents of "SPECIFICATIONS" Section.
		17	17	Partially eliminated the contents of "DC Characteristics" Section.
		18	18	Partially eliminated the contents of "Power Supply Current (IDDO) Characteristics by Power Saving Mode" Section.
		23	23	Partially eliminated the contents of "Setting the Reset" Section.

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not, unless specifically authorized by Oki, authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans.
   Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.

8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.