



# Mobile KBC with Super I/O, SFI, ADC and DAC with SMSC SentinelAlert!<sup>TM</sup>

## PRODUCT FEATURES

Data Brief

- 3.3V Operation with 5V Tolerant Buffers
- ACPI 1.0b/2.0 and PC99a/PC2001 Compliant
- LPC Interface with Clock Run Support
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - 15 Direct IRQs
  - Three 8-Bit DMA Channels
  - ACPI SCI Interface
  - nSMI
  - Shadowed write only registers
- LPC/Firmware Hub Host Flash Interface
  - Single Byte FWH Memory Read and FWH Memory Write Support
  - FWH ID Support
  - 16MB FWH Flash and Register Addressing, 128K Legacy BIOS Addressing
  - Single Byte LPC Memory Read and LPC Memory Write Support
- Serial Peripheral Interface (SPI)
  - 3-pin Full Duplex serial communication interface.
  - Dual Ported Controller with Keeper Circuit
- 8 MByte Shared FlashROM Interface (SFI)
  - 8051/Host CPU Hardware Arbitrated Interface
  - 0.5 - 8MB - Host System BIOS & 8051 Keyboard
  - 8051 64KB Code Space Accessible as Separate 32KB Pages in Flash
  - Low-Power Flash Access Modes
  - 8051-Programmable Flash Access Protection
    - Read/Write/No-Access Protection
    - Variable Bank Sizes
- Host Flash Address Redirection for Recovery
- Serial Flash Programming Interface
- Two Power Planes
  - Low Standby Current in Sleep Mode
  - Intelligent Auto Power Management for Super I/O
  - Main powered blocks power supplied by standby power plane and controlled by power management signals
- 3-Port ACPI Embedded Controller Interface
- Configuration Register Set
  - Compatible with ISA Plug-and-Play Standard (Version 1.0a)
  - Four Pin Selectable Addressing Options
  - 8051-Programmable Base Address
- High-Performance Embedded 8051 Keyboard and System Controller
  - Provides System Power Management
  - System Watch Dog Timer (WDT)
  - 8042 Style Host Interface Relocatable to 480 Different Base I/O Addresses
  - Supports Interrupt and Polling Access
  - Interrupt Accelerator
  - 512 Bytes Data RAM
  - 2 Kilobytes Scratch ROM/RAM
  - On-Chip Memory-Mapped Control Registers
  - Up to 18x8 Keyboard Scan Matrix
  - Two 16 Bit Timer/Counters
  - Eleven 8051 Interrupt Sources
  - Thirty-Two 8-Bit, Host/8051 Mailbox Registers
  - Thirty-six Maskable Hardware Wake-Up Events
  - Fast GATEA20
  - Fast CPU\_RESET
  - Multiple Clock Sources and Operating Frequencies up to 32MHz
  - IDLE and SLEEP Modes
  - Low Power Fail-Safe Ring Oscillator  $\pm 10\%$  Accuracy
  - Hibernation Timer with programmable wake-up from 0.5ms to 128 minutes
  - 8051-Driven 16550A UART
    - 16-Byte Send/Receive FIFOs
    - External Baud Clock Option
  - Power-Fail Status Register
- Advanced Infrared Communications Controller (IRCC 2.0)
  - IrDA V1.2 (4Mbps), HPSIR, ASKIR, Consumer IR Support
  - Two IR Ports
  - Relocatable Base I/O Address

- Consumer Infrared Communications Controller (CIRCC2.0)
  - 96 Base I/O Address, 15 IRQ Options and 3 DMA Options
  - CIR supports NEC and RC5 framing
  - CIR supports RC6 framing under Philips license (p/n KBC1100P only)
  - 8051 access to RC6, RC5, and NEC received data
  - 8051/Host wakeup from specific RC5 and NEC received data
- Battery Backed Resources
  - 32KHz clock generator
  - 1 Week Wakeup timer
- Two 8584-Style SMBus Controllers
  - 8051 Host Interface Logic Allows Master or Slave Operation
  - Controllers are Fully Operational on Standby Power
  - 2 Ports per Controller
- Four independent Hardware Driven PS/2 Ports
  - Fully functional on Main and/or Suspend Power
  - PS/2 edge Wake Capable
  - Wake on specific mouse protocol
  - Wake on specific keyboard protocol
- 102 General Purpose I/O Pins
- Six Programmable Pulse-Width Modulator Outputs
  - Multiple clock Sources and Independent Clock Rates
  - 8 Bit Duty Cycle Granularity
- Three Fan Tachometer Inputs
- Four Programmable 16-bit Counter/Timers
- Serial Port
  - Host-Driven High-Speed 16C550A-Compatible UART with 16-Byte Send/Receive FIFOs
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
  - Relocatable to 480 Different Base I/O Addresses
  - 15 IRQ Options
- Direct Battery Management with SMSC SentinelAlert!
  - Analog to Digital Converter with
    - 8 channels, 8b/10b conversion
    - 20ms conversion time for 8 channels
  - Digital to Analog Converter with SMSC SentinelAlert!
    - 3 channels, 8b conversion
    - 1.5ms conversion time for 3 channels
  - 2-GPIO's with SMSC SentinelAlert!
  - 2-Single pin SMSC BudgetBus Sensor Interface Ports
  - HW\_PROTECT# output thermal event indication
- MCU Serial Debug Port
- Integrated Standby Power Reset Generator
- 176 Pin TQFP Package, Green, Lead-Free Package also available



**ORDER NUMBER(S): KBC1100-RD FOR 176 PIN, TQFP PACKAGE; KBC1100-RT FOR 176 PIN TQFP PACKAGE (GREEN, LEAD-FREE)**



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## General Description

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The KBC1100 is an integrated Keyboard/System Management Controller which incorporates a high-performance 8051 Micro-Controller, an LPC Bus Interface which provides a Firmware Hub Interface and integrated Super I/O/LPC Resources. The KBC1100 is powered by two separate supply planes (VCC1, VCC0) to provide “instant on” and sophisticated system power management functions. The KBC1100 power control circuitry supports multiple low power-down modes.

The KBC1100 incorporates a Direct Battery Management (DBM) with SMSC SentinelAlert! accessible by the 8051. Together with external remote temperature sensor(s) can provide complete Analog Monitoring & Control System. The KBC1100 DBM includes an 8 channel ADC, a 3 channel DAC with SMSC SentinelAlert! and up to 2 SMSC SentinelAlert! GPIO's, two channel one-pin Temperature Sensor Communication Links, and a hardware protect output that requires no programming or 8051 intervention to operate.

The KBC1100 incorporates a Standby Power Reset Generator (RESGEN) which monitors the VCC1 power input and generates the internal VCC1 power on reset for the KBC1100. The KBC1100 also outputs VCC1RST# which can be used to reset the Flash memory on the Shared Flash Interface (SFI).

A block diagram of the KBC1100 including the distribution of the supply planes is shown below in [Figure 1 on page 5](#).

# Block Diagram

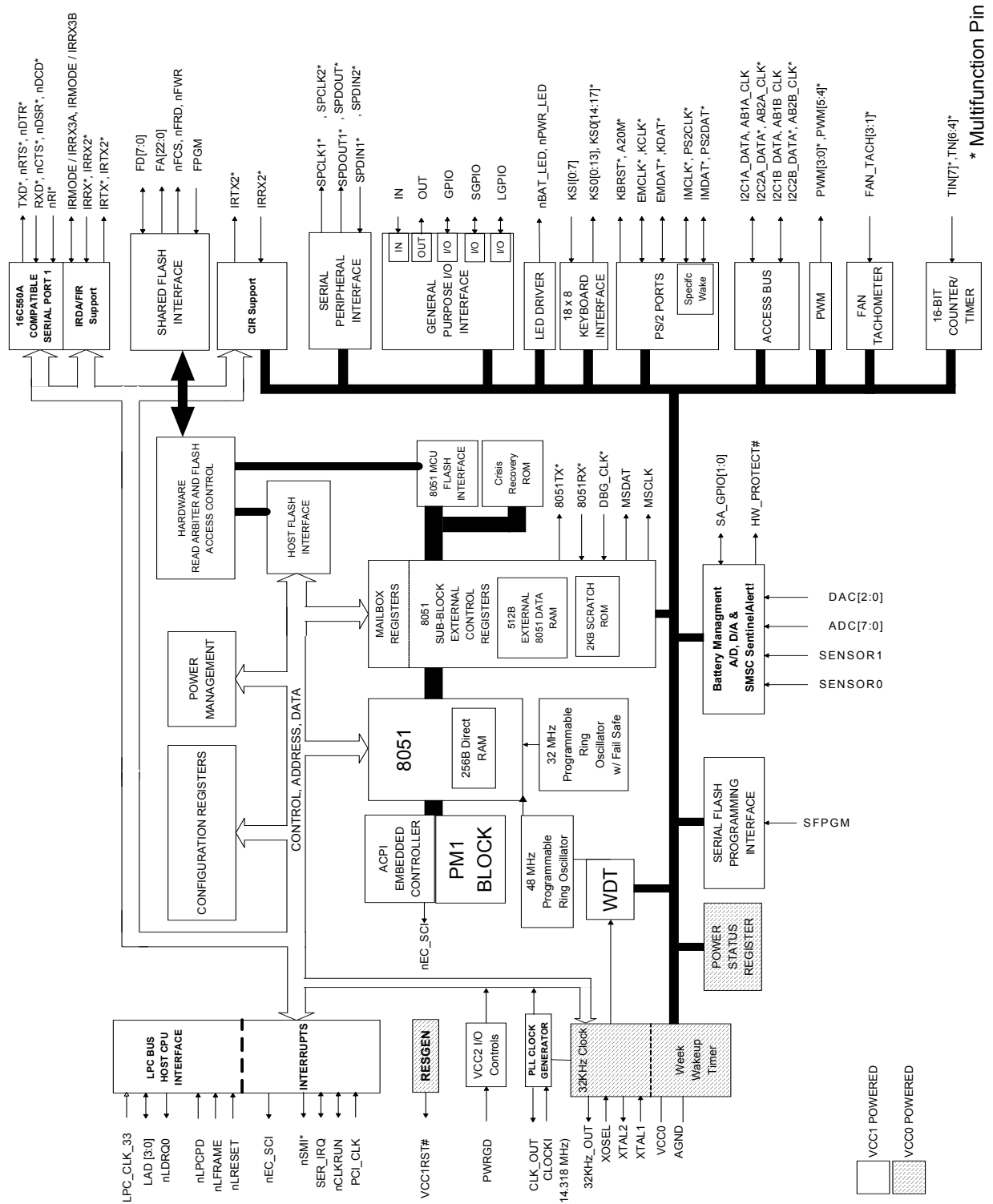


Figure 1 KBC1100 Block Diagram

# Package Outline

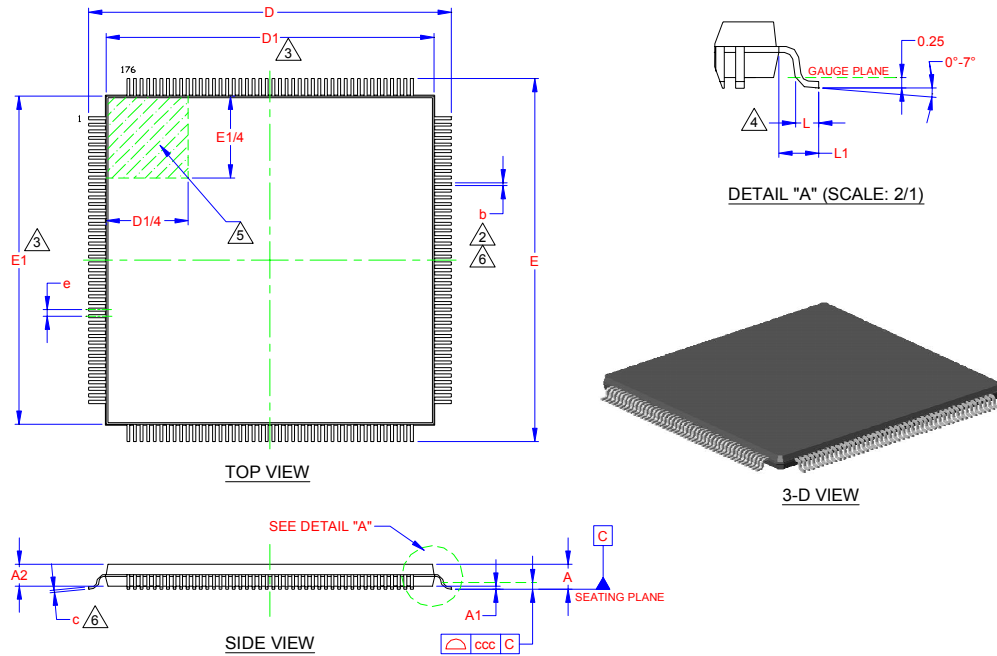


Figure 2 176-Pin TQFP Package Outline, 20X20X1.4 Body, 0.4 mm Footprint

Table 1 176-Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARK
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	1.40	1.45	Body Thickness
D/E	21.80	~	22.20	X/Y Span
D1/E1	19.80	20.00	20.20	X/Y Body Size
c	0.09	~	0.20	Lead Foot Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	1.00 REF			Lead Length
e	0.40 BSC			Lead Pitch
b	0.13	~	0.23	Lead Width
ccc	~	~	0.08	Coplanarity

**Notes:**

- All dimensions are in millimeter.
- True position spread tolerance of each lead is  $\pm 0.035$  mm at maximum material condition.
- Dimensions D1 and E1 do not include mold protrusions. Maximum allowed protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
- Dimension L is measured at the gauge plane, 0.25 mm above the seating plane.
- Details of pin 1 identifier are optional but must be located within the zone indicated.
- Dimensions "b" and "c" apply to the flat section of the lead between 0.10mm and 0.25mm from the lead tip.