iChip™

iChip CO120SQ

Data Sheet

Ver. 1.11

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Revision History 11-1200-03		
Version	**Date**	**Description**
0.56	July 2005	Preliminary Release for iChip CO120SQ.
0.66	September 2005	In WiFi flavors the interrupt signal is negative (-LANINT) and is LOW to signal WiFi data ready. Changed–-DTRH signal to SLEEP_DIS.
1.00	September 2006	Added modem flavor.
1.11	November 2006	Added two-wire interface and USB device interface, edited content.

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1 Introduction

Description

The iChip™ CO120SQ Internet Controller™ is a high-performance, firmware-based intelligent peripheral device that provides Internet connectivity solutions for a wide range of embedded devices. The firmware provides IP communication via a modem, LAN controller, or WiFi CF adapter. CO120SQ is packaged in an RoHS-compliant TQFP 64-pin form factor.

Its serial host interface supports throughput up to 250 kbits/second. CO120SQ also features a Power Save mode and will include a Sleep mode for energy conservation. CO120SQ operates in the industrial temperature range and is RoHS-compliant.

CO120SQ is powered from a single 3.3-volt supply and incorporates an internal 1.8-volt converter for its CPU core.

As an embedded, self-contained Internet engine, iChip acts as mediator device between a host processor and an Internet communications platform. By completely offloading Internet connectivity and standard protocols, it relieves the host from the burden of handling Internet communications. From the perspective of a host device, the complexity of establishing and maintaining Internet-related sessions are reduced to simple, straightforward commands that are entirely dealt with within iChip's domain.

A serial or USB[1] channel is used to directly interface iChip to a device's host processor. iChip accesses the Internet using one of three communication links: modem (wired or wireless), 10/100BaseT LAN (with an additional Ethernet controller), or 802.11b Wireless LAN (with an external compact flash adapter that uses the PRISM 2.5/3.0 802.11b WiFi chipset).

Through its host Application Programming Interface (API), iChip accepts commands formatted in Connect One's AT+i™ extension to the industry-standard Hayes AT command set. iChip supports several levels of status reporting to the host.

Commands are available to store and manipulate functional and Internet-related non-volatile parameter data; to support up to 10 simultaneous TCP and UDP sockets to send and receive data over the Internet; to support up to two listening sockets; to send email; to open and close FTP files; to fetch HTML web pages, and to perform serial-to-IP routing.

iChip CO120SQ is the first in a new series of programmable chips that feature an open architecture. You can choose from a variety of firmware versions (flavors) that can be downloaded from Connect One's Web site. Each firmware flavor defines a different functional subset. Flavors also define different pin-out assignments to support separate communication links: cellular or dialup modem, 10/100BaseT LAN or 802.11b WiFi. The firmware flavors are downloaded into iChip using its factory-installed non-volatile Boot Loader. By default, CO120SQ is shipped from the factory with only the Boot Loader pre-installed.

Note 1: The USB device link is a future implementation.

2 Functional Block Diagram

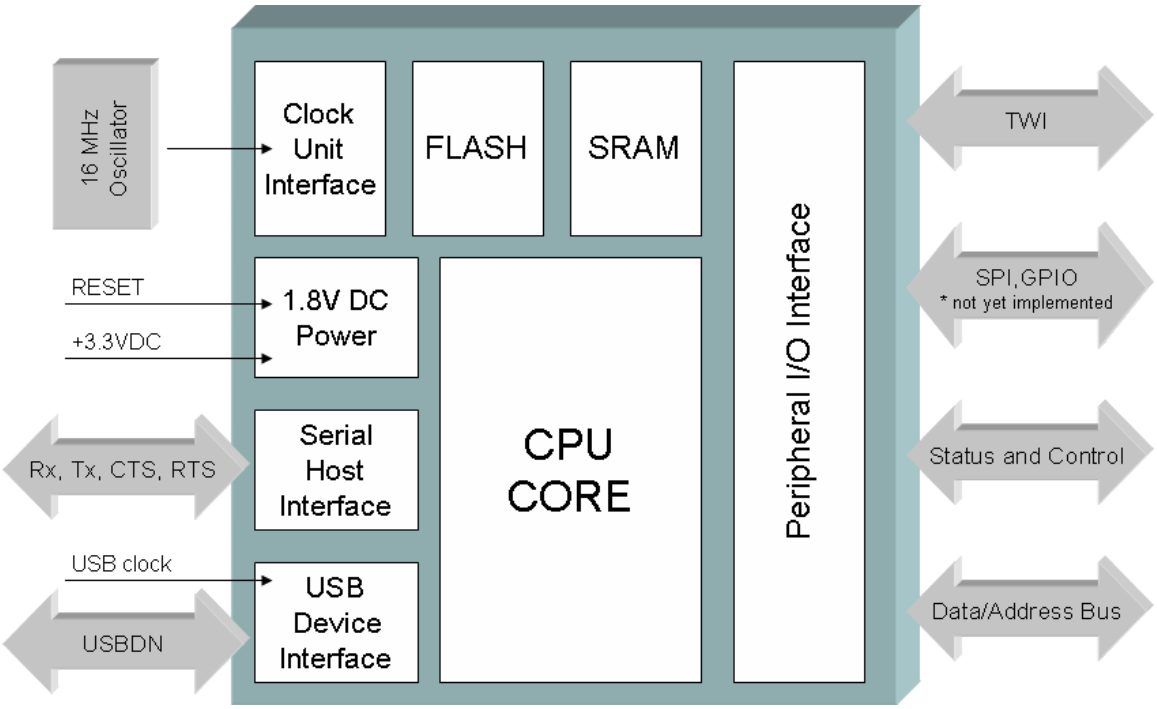


Figure 2-1: iChip Functional Block Diagram

3 Features

General Features

- Microprocessor-controllable through a serial connection.
- Driven by Connect One's "AT+i" extension to the AT command set.
- Stand-alone Internet communication capabilities.
- Opens up to 10 simultaneous TCP or UDP sockets and up to 2 Listen (server) sockets.
- Power Save and Sleep modes for power conservation purposes (Sleep mode to be implemented).
- Single 3.3-volt power supply, CMOS technology, with internal 1.8-volt for CPU core.
- Onboard non-volatile memory stores all functional and Internet-related parameters.
- Supports several layers of status reports.
- Internal "watchdog" guard circuit.
- Auto baud rate detection.
- Supports up to 250Kbps throughput.
- Includes hardware and software flow control.
- Updateable firmware.
- 64-pin TQFP package (10 x 10 x 1.6 mm).
- RoHS–compliant.

Internet Protocol Support

- Basic Protocols: PPP, LCP, IPCP, PAP, CHAP, IP, ICMP, UDP, TCP, PING, DNS, DHCP.
- Optional Protocols, depending on firmware flavor: SMTP, HTTP, FTP, SNTP.
- Optional Web/WAP server with internal 24KB storage for Web site.
- Optional remotely updateable firmware.
- Optional SerialNET mode for Serial-to-Internet routing.

Modem Flavor Features

- Supports dialup Internet Protocols: PPP, LCP, IPCP, with PAP or CHAP authentication.
- Supports data modems up to 56Kbps.
- Supports CDMA, CDMA2000, EDGE, GPRS, GSM and TDMA wireless modems.
- RAS support for dial-in PPP connection.
- "Stay online" feature for multiple send/receive sessions.
- Transparent mode supports direct modem commands.
- "Always online" mode with communications "watchdog" and automatic reconnect.
- IP Registration.

LAN Flavor Features

- Supports LAN Internet Protocols ARP, ICMP, and DHCP.
- Provides 10/100BaseT Ethernet LAN connectivity via ASIX AX88796L or SMSC LAN91C111 Ethernet controllers.

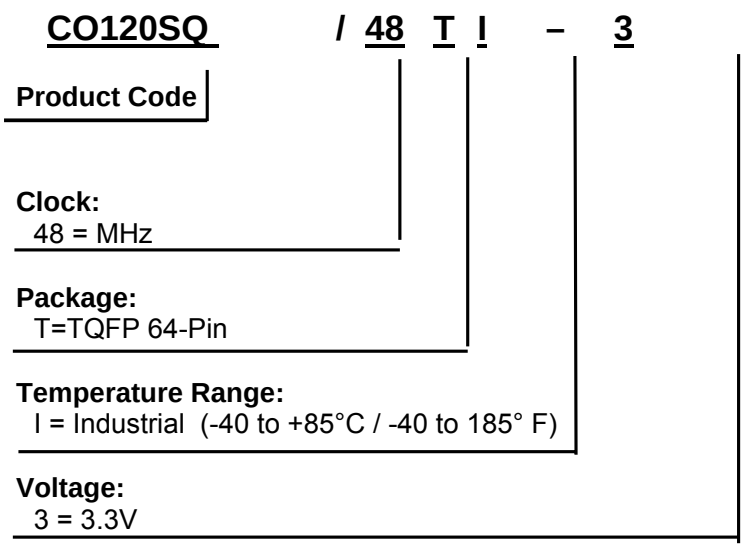
WiFi Flavor Features

- Supports LAN Internet Protocols ARP, ICMP, and DHCP.
- Support for PRISM 2.5/3.0 802.11b CF WiFi adapter.
- Supports WEP-based security.
- Supports WPA security.
- Future support for WPA2 security.

4 Ordering Information

4.1 iChip Order Number

Connect One's standard products are available in several packages and operating ranges. The order number (valid combination) is formed by a combination of the elements below.



5 Functional Description

5.1 Overview

Connect One's CO120SQ iChip Internet Controller is an integrated, firmware-driven, self-contained Internet engine that is available in a 64-pin TQFP package. iChip accepts simple ASCII commands from a host CPU via USB[1] or a serial communication channel and manages an Internet communication session through a linked modem, Ethernet controller, or an 802.11b WiFi CF adapter card.

iChip CO120SQ has several applicable firmware "flavors" that define its pin-out and functionality. Each flavor defines a different pin-out and feature set. iChip is supplied only with a preloaded Boot Loader, which may be used to download the desired firmware flavor. iChip contains non-volatile FLASH memory to store the selected firmware flavor and all Internet-related operational parameters.

Connect One offers iChip firmware flavors that may be used to manipulate TCP and UDP sockets; function as a Web server (to be implemented), retrieve Web server contents over HTTP 1.1; send textual Email messages; utilize FTP to manipulate, send or receive files; or serve as a serial-to-Internet router (to extend a local serial port over TCP or UDP sockets across the Internet). iChip CO120SQ firmware flavors include drivers necessary to drive a landline or cellular modem, an external SMSC LAN91C111 or ASIX AX88796L Ethernet LAN controller in a 10/100BaseT Ethernet environment, or an 802.11b WiFi CF adapter card that is based on the PRISM 2.5/3.0 WiFi chipset.

5.2 Technical Specifications

5.2.1 General

iChip constitutes a complete Internet Protocol (IP) messaging solution for non-PC embedded devices. It acts as a mediator device to completely offload the host processor of Internet-related software and activities. An industry-standard USB[1] or asynchronous serial link connects iChip to the host processor. Programming, monitoring and control are fully supported using Connect One's AT+i extension to the standard AT command set.

5.2.2 Operation

All iChip Internet and parameter operations are controlled by AT+i commands.

5.2.2.1 Command Mode

iChip commands are implemented using the AT+i command set. Hardware or software flow control exists on the serial channel between the host and iChip.

5.2.2.2 Internet Mode

iChip enters Internet mode after being issued an Internet command such as to send an Email message, open a socket, etc. iChip attempts to establish an Internet connection and carry out the required activity through the LAN, WiFi adapter, or modem. While in this mode, AT+i commands are supported to monitor and control the process when needed.

Note 1: Future implementation.

5.2.2.3 SerialNET Mode

iChip's SerialNET mode option extends a local asynchronous serial link to a TCP or UDP socket across the Internet. Its main purpose is to allow simple devices, which normally interact over a serial line, to interact in a similar fashion across a network, without requiring any changes in the device itself. iChip contains a set of associated operational parameters, which define the nature of the desired network connection. iChip supports both Server and Client modes in SerialNET mode. AT+i commands are not required to operate SerialNET mode. Thus, SerialNET mode may be used in existing systems with little or no need to modify the application program.

5.2.2.4 Power Save Mode

When Power Save mode is enabled, iChip automatically shuts down most of its circuits after a period of five seconds of inactivity on the host serial port. The inactivity timeout is a parameter set by the host. Renewed activity on the host serial port, modem serial port, or the LAN controller will restore iChip to full operation mode.

5.2.2.5 Sleep Mode

In Sleep mode, iChip completely shuts down all its circuits. iChip power consumption goes to an absolute minimum. iChip is restarted with the Reset signal. This mode has not been implemented yet.

Note: For this mode to be properly used, pin 20 (SLEEP_DIS) must be pulled-down to GND.

5.2.3 Host Serial Connection

iChip supports a full-duplex, TTL-level serial communications link with the host processor. Full EIA-232-D hardware flow control, including Tx, Rx, CTS, and RTS lines, is supported.

CO120SQ supports standard baud rate configurations from 2,400 bps up to 115,200 bps with auto baud rate detection and one high-speed, non-standard, 250Kbps on the host asynchronous serial communications channel. The default baud rate may be changed permanently by using the AT+iBDRF command.

5.2.4 Hardware and Software Flow Control

Hardware flow control is supported between the host serial connection and iChip. Flow control is programmed via the AT+iFLW command. The default flow control method is set to “Wait/Continue” software flow control (which is similar to XON/XOFF software flow control) between iChip and the host processor.

The hardware flow control method frees the host CPU from monitoring and handling the software flow control. The host can program iChip to either use hardware flow control or “Wait/Continue” software flow control. The flow control mechanism is based on the RTS/CTS signals.

6 Pin Descriptions

6.1 10/100BaseT LAN Connection

6.1.1 Pin Assignments (LAN Connection)

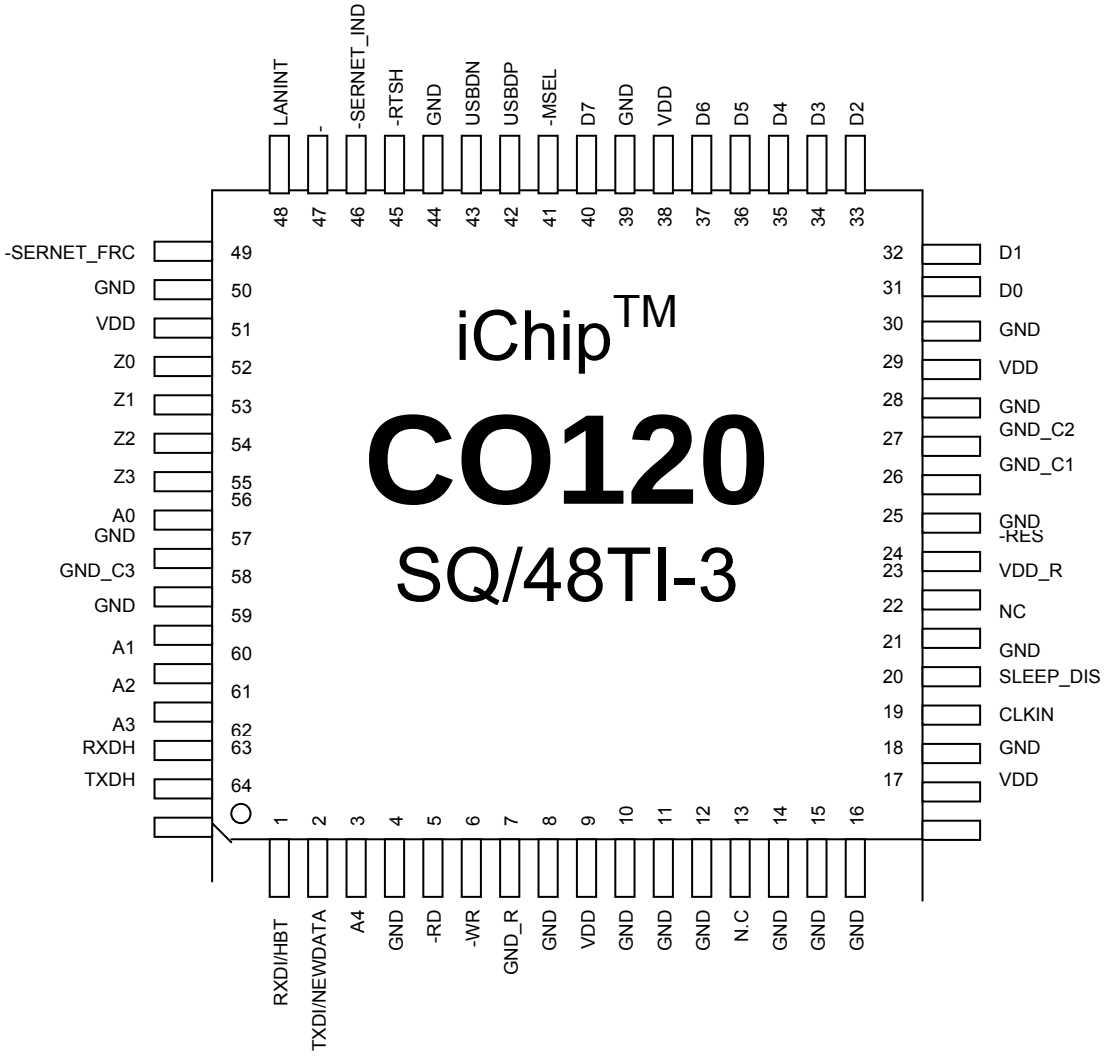


Figure 6-1: Pin Assignment for 64-pin TQFP 10/100BaseT LAN Connection

6.1.2 Pin Functional Descriptions (LAN Connection)

6.1.2.1 Miscellaneous Signals (LAN Connection)

Signal	Type	Pin No.	Description
-MSEL	I(PU)	41	Mode Select: • When this pin is held LOW during power up for at least 5 seconds, iChip will automatically enter to monitor mode. • When this pin is held LOW during power up for less than 5 seconds, it forces iChip into auto baud rate detection. • If iChip is in SerialNET mode, iChip exits SerialNET mode. When not used, can be left Not Connected.
-RESIN	I(ST)	24	-RESET INPUT: When -RESIN is LOW, iChip immediately terminates its present activity and clears its internal logic. -RESIN must be held LOW for at least 10 ms after power reaches 90%. This input is provided with a Schmitt trigger to facilitate power-on reset generation via an RC network.
CLKIN	I	19	Oscillator Input: The Oscillator must be 16MHz.
RXDI/ NEWDATA	I/OD	1	**Monitor Mode:** RXDI (O) This pin supplies asynchronous serial receive data for ICP (In-Circuit Programming) mode. **Application Mode:** Heartbeat (O) Provides a 50% duty cycle, 40 mSec period square wave when iChip firmware runs properly. This signal is Open Drain; it must be connected with a 10K pull-up resistor when used as Heartbeat output.
RXDI/ NEWDATA	O	2	**Monitor Mode:** TXDI (O) This pin supplies asynchronous serial transmit data for ICP (In-Circuit Programming) mode. **Application Mode:** NEWDATA (O) This signal is raised when new data in one or more sockets is available. It is lowered when any socket data is read.
-SERNET_ IND	O	46	SerialNET indicator: When LOW, indicates that iChip is in SerialNET mode.

Signal	Type	Pin No.	Description
-SERNET_ FRC	I(PU)	49	Force SerialNET mode: When this pin is LOW, iChip is forced into SerialNET mode. When this pin is HIGH, SerialNET mode is managed with AT+i commands. Leave Not Connected when not in use. Not implemented.
Z[0,1]	IO	53, 52	General Purpose I/O (GPIO): Reserved for future use. These pins should be left NC (Not Connected).
Z[2]	TWCK	54	Two-wire clock.
Z[3]	TWD	55	Two-wire data.
GND	P	4, 8, 10, 11, 12, 14, 15, 16, 18, 21, 25, 28, 30, 39, 44, 50, 57, 59	Ground: iChip Ground signal.
GND_C1	---	26	Must connect this pin with 1uF capacitor to GND (pin 25). For internal 1.8V power supply.
GND_C2	---	27	Must connect this pin with 33pF and 10uF capacitors to GND (pin 28). For internal 1.8V power supply.
GND_C3	---	58	Must connect this pin with 33pF and 10uF capacitors to GND (pin 57). For internal 1.8V power supply.
GND_R	---	7	Must connect this pin with 10K resistor to GND.
VDD	P	9, 17, 29, 38, 51	Power Supply: These pins supply power (+3.3V) to iChip's I/O pins.
VDD_R	---	23	Must connect this pin with 10K resistor to VDD.
NC	---	13, 22	NC (Not Connected) pins.
SLEEP_DIS	I	20	Sleep Disable: When this pin is HIGH, Sleep Mode is Disabled. When this pin is LOW, iChip enters Sleep Mode according to its settings and configuration. Not implemented.

6.1.2.2 Host Serial Interface Signals (LAN Connection)

Signal	Type	Pin No.	Description
TXDH	O	64	Transmit Data Host: This pin supplies asynchronous serial transmit data to the host.
RXDH	I(PU)	63	Receive Data Host: This pin supplies asynchronous serial receive data from the host. When not used, can be left open.
USBDN	IO	43	USB bi-directional data (data+). This pin requires an external pull-up to VDD to maintain a high level.
USBDP	IO	42	USB bi-directional data (data-).
-CTSH/ USBclock	I(PD)	47	**Serial Host Connection:** Clear-to-Send Host (-CTSH) is active only when host hardware flow control is enabled. When –CTSH is LOW, flow control is enabled for the host serial port. This means that iChip can transmit to the host. When –CTSH is HIGH, iChip stops transmitting to the host. –CTSH is sampled only at the beginning of a transmission frame. If –CTSH is raised while a character frame is transmitted, that frame is completed. **USB Device Connection:** USB clock must be a 4 MHz square-wave clock signal. When not used, can be left open.
-RTSH	O	45	Ready-to-Send Host: -RTSH is active only when host hardware flow control is enabled. When -RTSH is LOW, flow control is enabled for the host serial port, i.e., the host may transmit to iChip. When -RTSH is HIGH, iChip indicates that its receiver is busy and cannot receive data from host. When not used, can be left open.

6.1.2.3 Local Bus Signals (LAN Connection)

Signal	Type	Pin No.	Description
D[7-0]	IO	40, 37, 36, 35, 34, 33, 32, 31	Data BUS: These pins supply data to/from the iChip. These pins should be connected to the data BUS of the LAN controller.
A[4-0]	O	3, 62, 61, 60, 56	Address BUS: These pins supply addresses to the iChip. These pins should be connected to the address BUS of the LAN controller.
-RD	O	5	READ: This pin indicates that iChip is performing a read cycle. This pin should be connected to -RD on the LAN controller.
-WR	O	6	WRITE: This pin indicates that iChip is performing a write cycle. This pin should be connected to -WR on the LAN controller.
-LANINT	I	48	LAN Interrupt. When HIGH, this signal indicates that the LAN controller has information for iChip.

Legend:

I	-	Input
O	-	Output
I(PU)	-	Input with 100k pull-up resistor
I(PD)	-	Input with 100k pull-down resistor
I(ST)	-	Schmitt trigger input
I/O	-	Input / Output
I/OD	-	Input / Output Open Drain
P	-	Power signal

6.2 802.11b WiFi Connection

6.2.1 Pin Assignments (WiFi Connection)

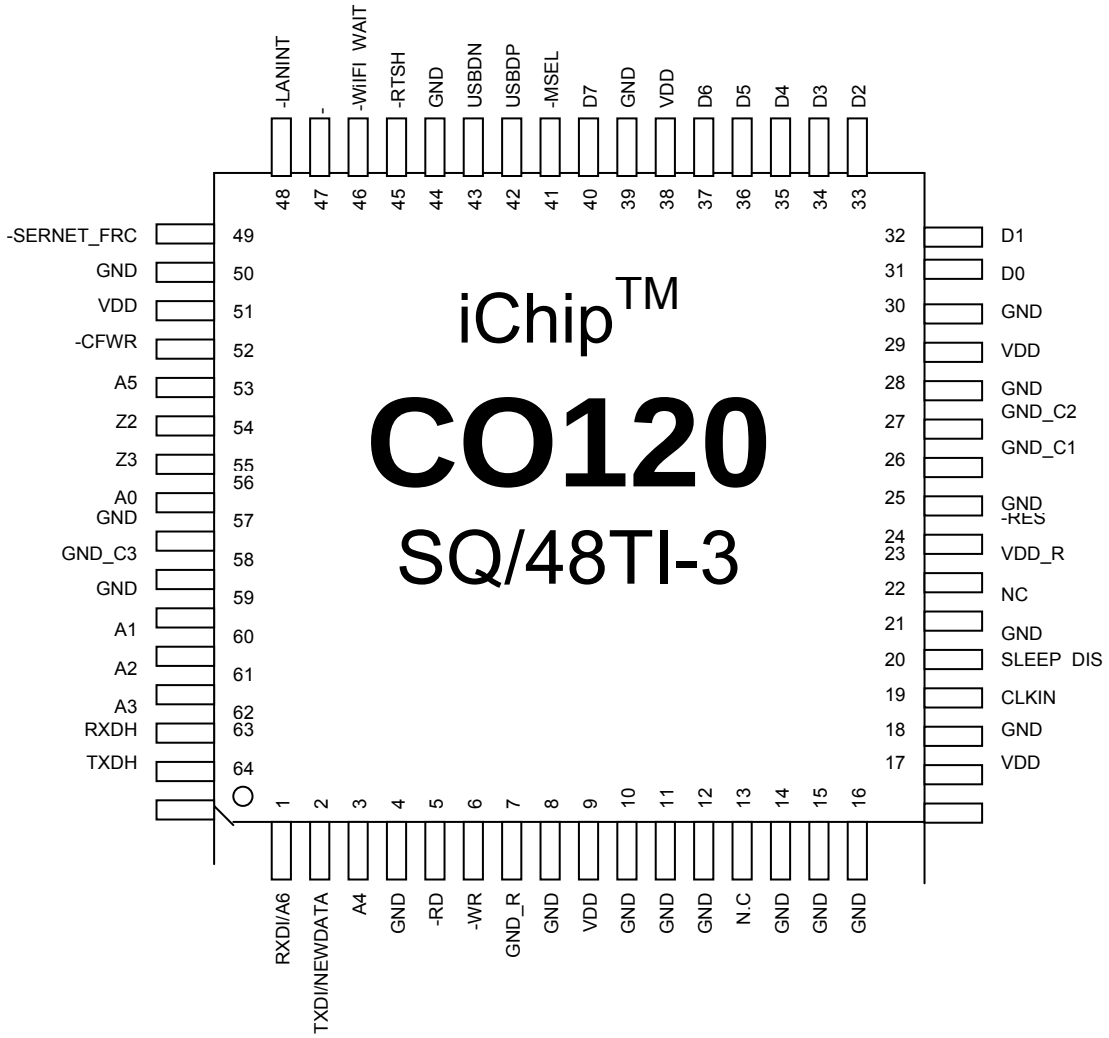


Figure 6-2: Pin Assignment for 64-pin TQFP 802.11b WiFi Connection

6.2.2 Pin Functional Descriptions (WiFi Connection)

6.2.2.1 Miscellaneous Signals (WiFi Connection)

Signal	Type	Pin No.	Description
-MSEL	I(PU)	41	Mode Select: • When this pin is held LOW during power up for at least 5 seconds, iChip will automatically enter monitor mode. • When this pin is held LOW during power up for less than 5 seconds, it forces iChip into auto baud rate detection. • If iChip is in SerialNET mode, iChip exits SerialNET mode. When not used, can be left Not Connected.
-RESIN	I(ST)	24	-RESET INPUT: When -RESIN is LOW, iChip immediately terminates its present activity and clears its internal logic. -RESIN must be held LOW for at least 10 ms after power reaches 90%. This input is provided with a Schmitt trigger to facilitate power-on reset generation via an RC network.
CLKIN	I	19	Oscillator Input: The Oscillator must be 16MHz.
TXDI/ NEWDATA	O	2	**Monitor Mode:** TXDI (O) This pin supplies asynchronous serial transmit data for ICP (In-Circuit Programming) mode. **Application Mode:** NEWDATA (O) This signal is raised when new data in one or more sockets is available. It is lowered when ***any*** socket data is read.
-SERNET_ FRC	I(PU)	49	Force SerialNET mode: When this pin is LOW, iChip is forced into SerialNET mode. When this pin is HIGH, SerialNET mode is managed with AT+i commands. Leave Not Connected when not in use. Not implemented.
Z[0,1]	IO	53, 52	General Purpose I/O (GPIO): Reserved for future use. These pins should be left NC (Not Connected).
Z[2]	TWCK	54	Two-wire clock.

Signal	Type	Pin No.	Description
Z[3]	TWD	55	Two-wire data.
GND	P	4, 8, 10, 11, 12, 14, 15, 16, 18, 21, 25, 28, 30, 39, 44, 50, 57, 59	Ground: iChip Ground signal.
GND_C1	---	26	Must connect this pin with 1uF capacitor to GND (pin 25). For internal 1.8V power supply.
GND_C2	---	27	Must connect this pin with 33pF and 10uF capacitors to GND (pin 28). For internal 1.8V power supply.
GND_C3	---	58	Must connect this pin with 33pF and 10uF capacitors to GND (pin 57). For internal 1.8V power supply.
GND_R	---	7	Must connect this pin with 10K resistor to GND.
VDD	P	9, 17, 29, 38, 51	Power Supply: These pins supply power (+3.3V) to iChip's I/O pins.
VDD_R	---	23	Must connect this pin with 10K resistor to VDD.
NC	---	13, 22, 42, 43	NC (Not Connected) pins.
SLEEP_DIS	I	20	Sleep Disable: When this pin is HIGH, Sleep Mode is Disabled. When this pin is LOW, iChip shall enter Sleep Mode according to its settings and configuration. Not implemented.

6.2.2.2 Host Serial Interface Signals (WiFi Connection)

Signal	Type	Pin No.	Description
TXDH	O	64	Transmit Data Host: This pin supplies asynchronous serial transmit data to the host.
RXDH	I(PU)	63	Receive Data Host: This pin supplies asynchronous serial receive data from the host. When not used, can be left open.
USBDN	IO	43	USB bi-directional data (data+). This pin requires an external pull-up to VDD to maintain a high level.
USBDP	IO	42	USB bi-directional data (data-).
-CTSH/ USBclock	I(PD)	47	**Serial Host Connection:** Clear-to-Send Host (-CTSH) is active only when host hardware flow control is enabled. When –CTSH is LOW, flow control is enabled for the host serial port. This means that iChip can transmit to the host. When –CTSH is HIGH, iChip stops transmitting to the host. –CTSH is sampled only at the beginning of a transmission frame. If –CTSH is raised while a character frame is transmitted, that frame is completed. **USB Device Connection:** USB clock must be a 4 MHz square-wave clock signal. When not used, can be left open.
-RTSH	O	45	Ready-to-Send Host: -RTSH is active only when host hardware flow control is enabled. When -RTSH is LOW, flow control is enabled for the host serial port, i.e., the host may transmit to iChip. When -RTSH is HIGH, iChip indicates that its receiver is busy and cannot receive data from host. When not used, can be left open.

6.2.2.3 Local Bus Signals (WiFi Connection)

Signal	Type	Pin No.	Description
D[7-0]	IO	40, 37, 36, 35, 34, 33, 32, 31	Data BUS: These pins supply data to/from the iChip. These pins should be connected to the CF data BUS.
A[5-0]	O	53, 3, 62, 61, 60, 56	Address BUS: These pins supply addresses to the iChip. These pins should be connected to the CF address BUS.
RXDI/A6	I/OD	1	**Monitor Mode:** RXDI (I) This pin supplies asynchronous serial receive data for ICP (In-Circuit Programming) mode. **Application Mode:** A6 (O) WiFi Address line 6. This pin should be connected to the CF address BUS. This signal is Open drain; it must be connected with a 10K pull-up resistor when used as A6 output.
-WIFI_ WAIT	I	46	WiFi adapter WAIT signal. When –WIFI_WAIT is low, iChip waits for WiFi adapter.
-RD	O	5	READ: This pin indicates that iChip is performing a read cycle. This pin should be connected to the CF BUS -RD signal.
-WR	O	6	WRITE: This pin indicates that iChip is performing a write cycle. This pin should be connected to the CF BUS -WR signal.
-CFWR	O	52	-CFWR: This pin indicates that iChip is performing a write I/O cycle. This pin should be connected to the CF BUS -IOWR signal. Note that the -IORD signal on the CF BUS must be connected to VDD.
-LANINT	I	48	WLAN Interrupt. When LOW, this signal indicates that the WiFi controller has pending information.

Legend:	I	-	Input
	O	-	Output
	I(PU)	-	Input with 100k pull-up resistor
	I(PD)	-	Input with 100k pull-down resistor
	I(ST)	-	Schmitt trigger input
	I/O	-	Input / Output
	I/OD	-	Input / Output Open Drain
	P	-	Power signal

6.3 Modem Connection

6.3.1 Pin Assignments (Modem Connection)

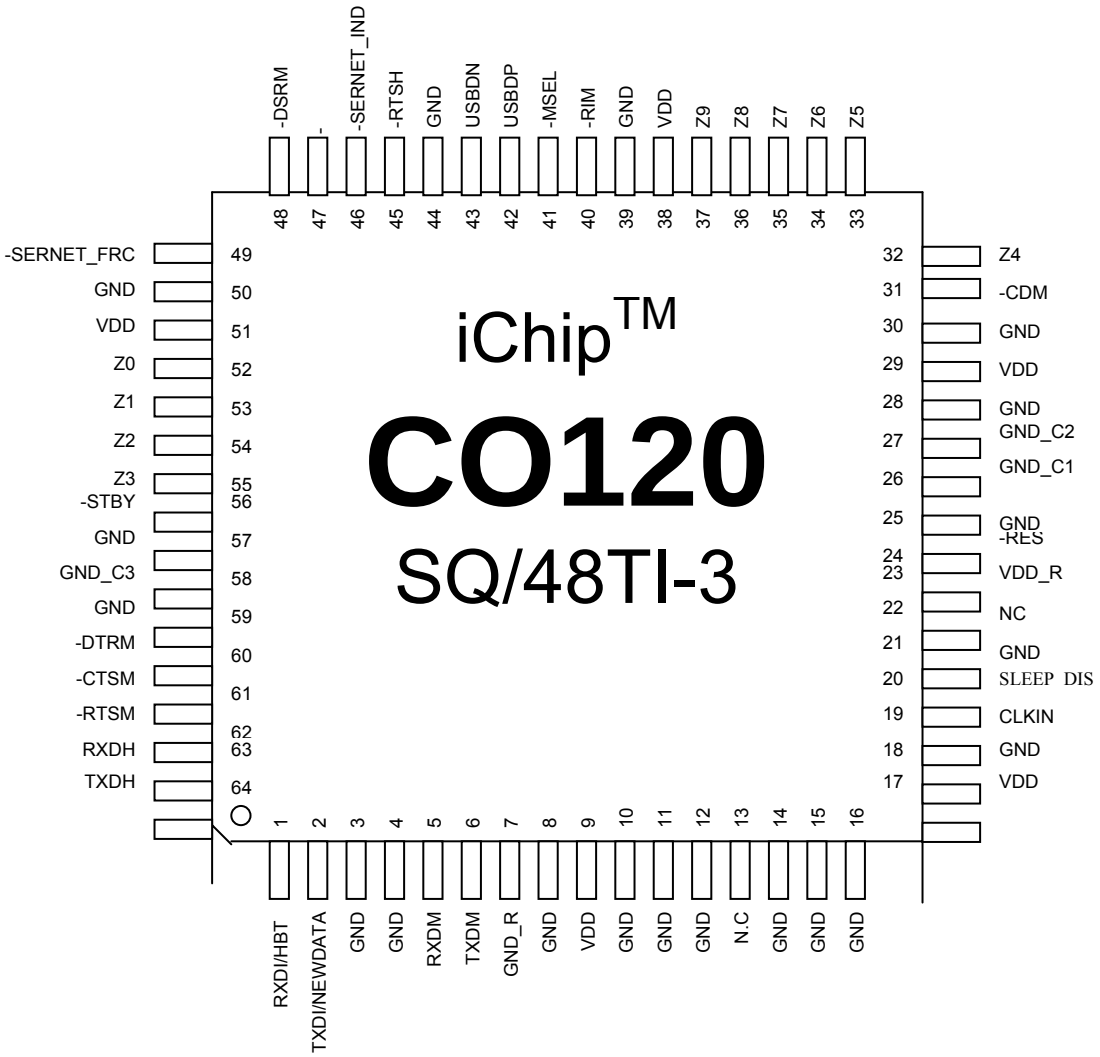


Figure 6-3: Pin Assignment for 64-pin TQFP Modem Connection

6.3.2 Pin Functional Descriptions (Modem Connection)

6.3.2.1 Miscellaneous Signals (Modem Connection)

Signal	Type	Pin No.	Description
-MSEL	I(PU)	41	Mode Select: • When this pin is held LOW during power up for at least 5 seconds, iChip will automatically enter monitor mode. • When this pin is held LOW during power up for less than 5 seconds, it forces iChip into auto baud rate detection. • If iChip is in SerialNET mode, iChip exits SerialNET mode. When not used, can be left Not Connected.
-RESIN	I(ST)	24	-RESET INPUT: When -RESIN is LOW, iChip immediately terminates its present activity and clears its internal logic. -RESIN must be held LOW for at least 10 ms after power reaches 90%. This input is provided with a Schmitt trigger to facilitate power-on reset generation via an RC network.
CLKIN	I	19	Oscillator Input: The Oscillator must be 16MHz.
RXDI/HBT	I/OD	1	**Monitor Mode:** RXDI (I) This pin supplies asynchronous serial receive data for ICP (In-Circuit Programming) mode. **Application Mode:** Heart Beat (O) Provides a 50% duty cycle, 40 mSec period square wave when iChip firmware is properly running. This signal is Open drain; it must be connected with a 10K pull up resistor when used as Heartbeat output.
TXDI / NEWDATA	O	2	**Monitor Mode:** TXDI (O) This pin supplies asynchronous serial transmit data for ICP (In-Circuit Programming) mode. **Application Mode:** NEWDATA (O) This signal is raised when new data in one or more sockets is available. It is lowered when any

Signal	Type	Pin No.	Description
			socket data is read.
-SERNET_IND	O	46	SerialNET Indicator: When Low, it indicates that iChip is in SerialNET Mode.
-SERNET_FRC	I(PU)	49	Force SerialNet mode: When this pin is LOW, iChip is forced into SerialNET mode. When this pin is HIGH, SerialNET mode is managed with AT+i commands. Leave Not Connected when not in use. Not implemented.
Z[0-1, 4-9]	IO	37, 36, 35, 34, 33, 32, 53, 52	General Purpose I/O (GPIO): Reserved for future use. These pins should be left Not Connected (NC).
Z[2]	TWCK	54	Two-wire clock.
Z[3]	TWD	55	Two-wire data.
GND	P	3, 4, 8, 10, 11, 12, 14, 15, 16, 18, 21, 25, 28, 30, 39, 44, 50, 57, 79	Ground: iChip Ground signal.
GND_C1	---	26	Must connect this pin with 1uF capacitor to GND (pin 25). For internal 1.8V power supply.
GND_C2	---	27	Must connect this pin with 33pF and 10uF capacitors to GND (pin 28). For internal 1.8V power supply.
GND_C3	---	58	Must connect this pin with 33pF and 10uF capacitors to GND (pin 57). For internal 1.8V power supply.
GND_R	---	7	Must connect this pin with 10K resistor to GND.
VDD	P	9, 17, 29, 38, 51	Power supply: This pin supplies power (+3.3V) to iChip's I/O pins.
VDD_R	---	23	Must connect this pin with 10K resistor to VDD.
NC	---	13, 22	Not Connected pins.
SLEEP_DIS	I	20	Sleep Disable: When this pin is HIGH, iChip's Sleep

Signal	Type	Pin No.	Description
			Mode is disabled. When this pin is LOW, iChip enters Sleep Mode according to its parameter settings. Not implemented.
-STBY	I(PU)	56	Standby Mode: When iChip is LOW, it goes into Standby Mode.

6.3.2.2 Host Serial Interface Signals

Signal	Type	Pin No.	Description
TXDH	O	64	Transmit Data Host: This pin supplies asynchronous serial transmit data to the host.
RXDH	I(PU)	63	Receive Data Host: This pin supplies asynchronous serial receive data from the host. When not used, can be left open.
USBDN	IO	43	USB bidirectional data (data +). This pin requires an external pull-up to VDD to maintain a high level.
USBDP	IO	42	USB bidirectional data (data -).
-CTSH/ USBclock	I(PD)	47	**Serial Host Connection:** Clear-to-Send Host (-CTSH) is active only when host hardware flow control is enabled. When -CTSH is LOW, flow control is enabled for the host serial port, i.e., iChip may transmit to the host. When -CTSH is HIGH, iChip stops transmitting to the host. -CTSH is sampled only at the beginning of a transmission frame. If -CTSH is raised while a character frame is being transmitted, that frame is completed. **USB Client Connection**: USB clock must be 4MHz square-wave clock signal. When not used, can be left open.
-RTSH	O	45	Ready-to-Send Host: -RTSH is active only when host hardware flow control is enabled. When -RTSH is LOW, flow control is enabled for the host serial port, i.e., the host may transmit to iChip. When -RTSH is HIGH, iChip indicates that its receiver is busy and cannot receive data from host. When not used, can be left open.

6.3.2.3 Serial Modem Signals

Signal	Type	Pin No.	Description
TXDM	O	6	Transmit Data Modem: This pin provides asynchronous serial transmit data to the modem from the serial port. This pin must remain HIGH on reset.
RXDM	I	5	Receive Data Modem: This pin provides asynchronous serial receive data from the modem from the asynchronous modem serial port. When this pin is not used, connect it to VDD.
-CTSM	I(PD)	61	Clear-to-Send Modem: -CTSM is active only when modem hardware flow control is enabled. When –CTSM is LOW, flow control is enabled for the modem serial port. That is, iChip can transmit to the modem. When –CTSM is HIGH, the iChip transmitter holds its data in the serial port transmit register. When not used, can be left open.
-RTSM	O	62	Ready-to-Send Modem: -RTSM is active only when modem hardware flow control is enabled. When –RTSM is LOW, flow control is enabled for the modem serial port. That is, the modem can transmit to iChip. When –RTSM is HIGH, iChip indicates that its receiver is busy and cannot receive data from the modem. When not used, can be left open.
-DSRM	I(PD)	48	Data Set Ready Modem: When –DSRM is LOW, it indicates that the modem is attached and ready to communicate with iChip. When not used, can be left open.
-DTRM	O	60	Data Terminal Ready Modem: When –DTRM is LOW, it indicates to the modem that iChip is attached and ready to communicate.
-CDM	I(PD)	31	Carrier Detect Modem: This pin indicates to iChip that the modem detects a carrier signal.

-RIM	I(PU)	40	Ring Indicator Modem: This pin indicates to iChip that the modem communication device detects a ring signal.

Legend:

I	-	Input
O	-	Output
I(PU)	-	Input with 100k pull up resistor
I(PD)	-	Input with 100k pull down resistor
I(ST)	-	Schmitt trigger input
I/O	-	Input / Output
I/OD	-	Input / Output Open Drain
P	-	Power signal

7 Electrical Specifications

7.1 Environmental Specifications

7.1.1 Absolute Maximum Ratings

Parameter	Rating
VDD	-0.3 to +4 Volts
Vin	-0.3 to +4 Volts
Operating temperature	-40° to +85°C (-40° to 185°F)
Storage temperature	-40° to 125°C (-40° to 257°F)

Table 7-1: Environmental Specifications – Maximum Ratings

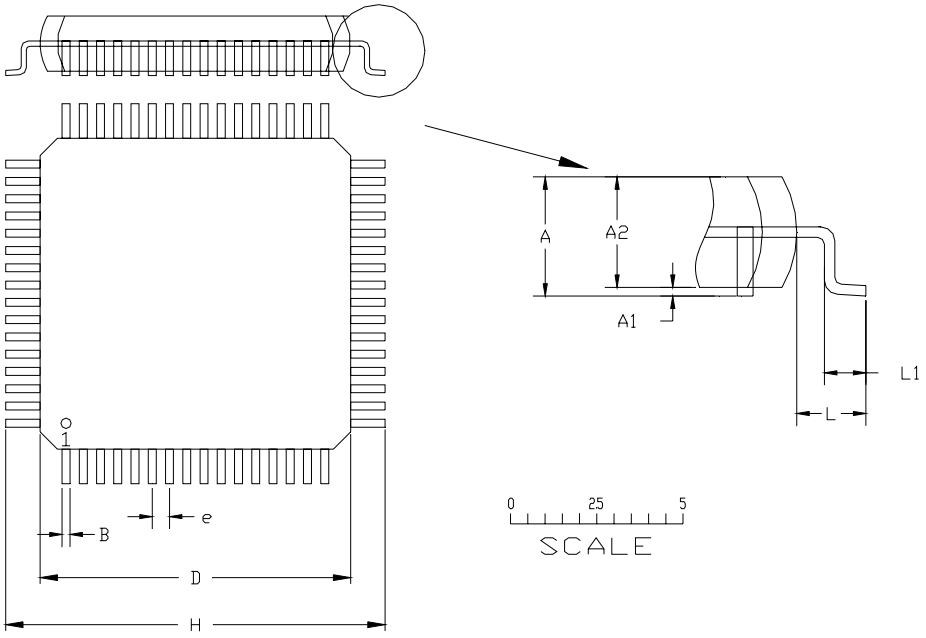
7.1.2 DC Operating Characteristics

Parameter	Min	Typical	Max	Units
VDD	3.0	3.3	3.6	Volts
High-level Input[1]	0.7VDD			Volts
Low-level Input[1]			0.3VDD	Volts
High-level Output @4mA	VDD -0.8			Volts
Low-level Output @4mA			0.4	Volts
Input leakage current			TBD	uA
Power supply current from VDD (Operating Mode)		TBD	TBD	mA
Power supply current from VDD (Power Save Mode)		TBD		uA
Power supply current from VDD (Sleep Mode)		TBD		uA
Input Capacitance		TBD		pF
Reset pulse	10			mSec

Table 7-2: DC Operating Characteristics

8 Mechanical Dimensions

Side View



Top View

Figure 8-1: CO120SQ Mechanical Dimensions

	A	A1	A2	L	L1	B	e	D	H
Minimum		0.05	1.35		0.45	0.17			
Typical				1.00	0.60	0.22	0.50	10	12
Maximum	1.6	0.15	1.45		0.75	0.27			

Table 8-1CO120SQ Dimension

9 Recommended Soldering Profile

Reflow profile	Description of characteristics	Process
Preheat	Initial heating of the component leads.	1-3ºC/Sec 100ºC to 125ºC
Thermal Soak	Solder paste dries out and flux activates.	100ºC to 175ºC Maximum 120 Sec.
Reflow	Time above 183ºC peak temperature.	60 to 120 Sec.
	Peak reflow temperature.	240ºC
Cooling	Time within 5ºC of actual peak temperature.	Maximum 4ºC/Sec

Table 9-1 Recommended Soldering Profile

Note: A maximum of three reflow passes allowed per device.

10 iChip Designs

10.1 Serial Host and Ethernet LAN Environment

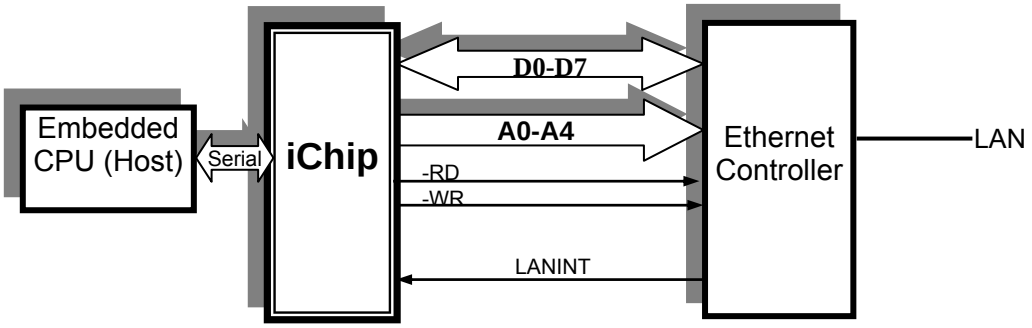


Figure 10-1: Serial Host and Ethernet Controller Environment

10.2 Serial Host and 802.11b WiFi Environment

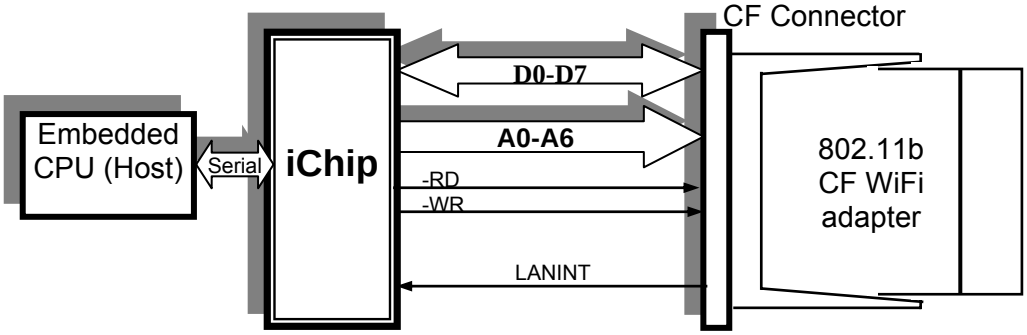


Figure 10-2: Serial Host and 802.11b WiFi Adapter

10.3 Serial Host and Modem Environment

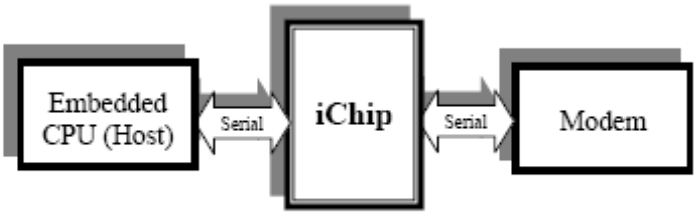


Figure 10-3: Serial Host and Modem

10.4 Selecting the Reset Circuit

10.4.1 RC Network

The reset signal may be designed with an RC network. τ should be greater than 10 mSec. This is a low-cost solution.

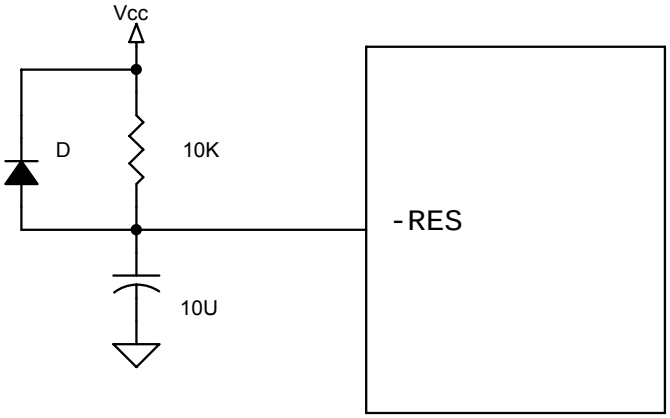


Figure 10-4: RC Reset Circuit

10.4.2 Supervisory Circuit

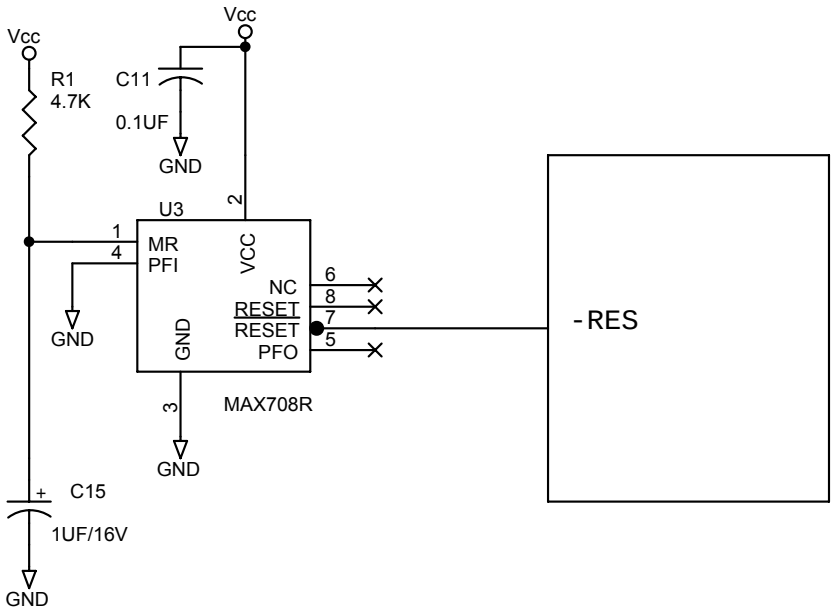


Figure 10-5: Supervisory Reset Circuit

11 Protocol Compliance

iChip CO120SQ flavors comply with the following Internet standards:

RFC 768	User Datagram Protocol (UDP)
RFC 791	Internet Protocol (IP)
RFC 792	Internet Control Message Protocol (ICMP)
RFC 793	Transmission Control Protocol (TCP)
RFC 821	Simple Mail Transfer Protocol (SMTP)
RFC 822	Standard for the Format of ARPA Internet Text Messages
RFC 826	Ethernet Address Resolution Protocol (ARP)
RFC 959	File Transfer Protocol (FTP)
RFC 1034	DOMAIN NAMES (DNS) - Concepts and Facilities
RFC 1035	DOMAIN NAMES (DNS) - Implementation and Specification
RFC 1321	MD5 Message Digest Algorithm
RFC 1331	Point-to-Point Protocol (PPP)
RFC 1332	Internet Protocol Control Protocol (IPCP)
RFC 1334	Password Authentication Protocol (PAP)
RFC 1570	PPP Link Control Protocol (LCP) Extensions
RFC 1661	PPP
RFC 1877	PPP IPCP Extensions for Name Server Addresses
RFC 2030	Simple Network Time Protocol (SNTP)
RFC 2068	HyperText Transfer Protocol HTTP/1.1
RFC 2131	Dynamic Host Configuration Protocol (DHCP)
RFC 2132	DHCP Options (only relevant parts)

Table 11-1: Internet Protocol Compliance

12 List of Terms and Acronyms

AT+i™	**Connect One's** Internet extension to the industry-standard Hayes AT command set. Supports simplified Internet connectivity commands in the spirit of the AT syntax.
Base64	**Encoding scheme**, which converts arbitrary binary data into a 64-character subset of US ASCII. The encoded data is 33% larger than the original data.
CHAP	**Challenge-Handshake Authentication Protocol**
DNS	**Domain Name System**. Defines the structure of Internet names and their association with IP addresses.
FTP	**File Transfer Protocol**. Used to provide file and directory services for remote server file systems.
iChip™	Connect One's Internet Controller for embedded Internet connectivity.
ICMP	**Internet Control Message Protocol**. Network layer Internet protocol that reports errors and provides other information relevant to IP packet processing.
IP	**Internet Protocol**. Provides for transmitting blocks of data, called datagrams, from sources to destinations, which are hosts identified by fixed length addresses. Also provides for fragmentation and reassemble of long datagrams, if necessary.
IPCP	**Internet Protocol Control Protocol**
ISP	**Internet Service Provider**. Commercial company that provides Internet access to end (mostly PC) users through a dial-up connection.
LCP	**Link Control Protocol.** Negotiates data link characteristics and tests the integrity of the link.
"Leave on Server"	An option designating whether retrieved email messages are left intact on the server for subsequent downloads or are deleted from the server after successful download.
PAP	**Password Authentication Protocol.** Used optionally by PPP to identify a user to the ISP.
ping	ICMP protocol **ECHO message** and its reply. Often used to debug IP networks and to test the accessibility of a network device.
PPP	**Point-to-Point Protocol.** Communications protocol used to send data across serial communication links, such as modems.
RFC	**Request For Comments**. Collections of standards that define the way remote computers communicate over the Internet.
SMTP	**Simple Mail Transfer Protocol**. Provides for transferring mail reliably and efficiently over the Internet.
SNTP	**Simple Network Time Protocol.** Used to retrieve accurate time of day from a networked time server. The accurate UTC/GMT time is retrieved.

TCP	**Transmission Control Protocol**. Provides reliable stream-oriented connections over the Internet. Works in conjunction with its underlying IP protocol.

Table 12-1: Terms and Acronyms