AsahiKASEI
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AK4141

NICAM/A2/EIA-J Digital Stereo Decoder

GENERAL DESCRIPTION

The AK4141 is a NICAM/A2/EIA-J stereo decoder, which is optimized for Digital TV application. The AK4141 achieves no alignment, few external components and high audio performance by digital stereo decoding architecture. The AK4141 integrates a stereo sample rate converter (SRC) for asynchronous digital audio sources such as HDMI, digital tuner, digital switches and sound processing functions such as 5-band equalizers. The AK4141 supports major audio data formats (MSB/LSB justified, I^2S and TDM) to interface with DSP, ADC, DAC. Therefore, the AK4141 is suitable for the AV systems such as Digital TV and DVR.

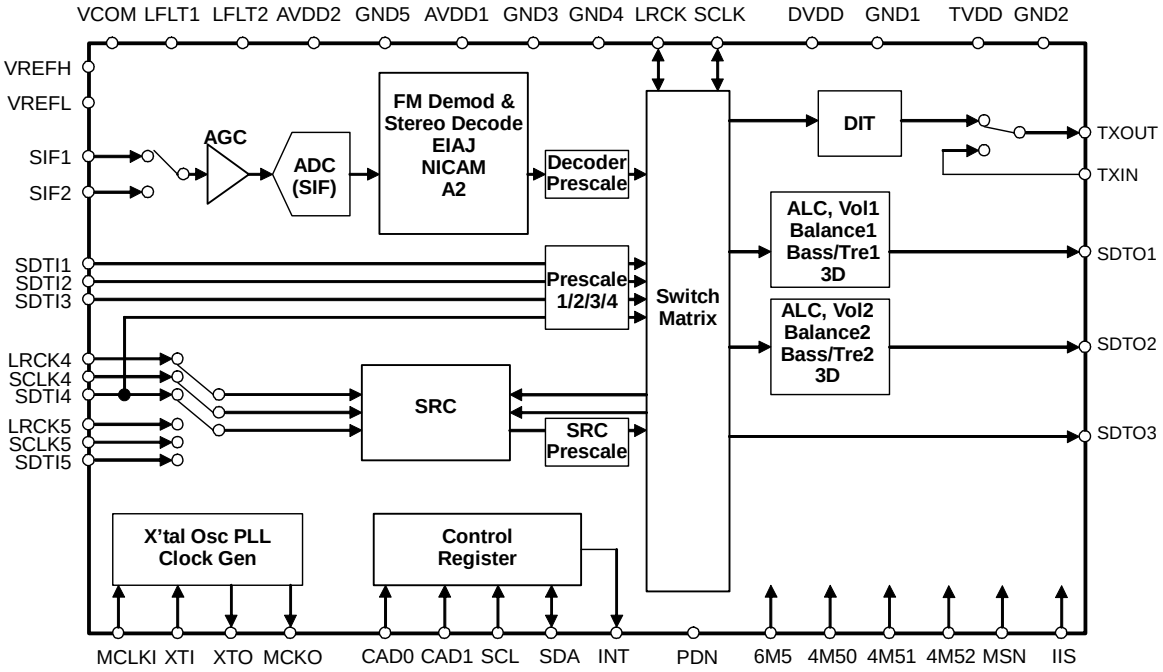
FEATURES

1. Stereo Decoding
- ☐ Capable of receiving Sound Intermediate Frequency (SIF) with Selector and FM Demodulation
- ☐ Automatic Gain Control (AGC: 100mVpp ~ 1Vpp) for SIF input
- ☐ Alignment Free Digital Stereo Decoding
  - EIA-J
  - NICAM: B/G, L, I, D/K with FM/AM Mono
  - A2: B/G, D/K1, D/K2, D/K3, M/N
- ☐ Automatic/Manual Stereo Decoding Standard Selection
- ☐ Automatic/Manual Audio Mode (Stereo/MONO/two sounds) Selection
- ☐ Signal Quality Detection for Auto Selection Mode
- ☐ High FM Deviation Option (max: 540kHz)
- ☐ I2S sampling rate (fs): 32k/44.1k/48kHz

2. Audio Processing (Two Stereos)
- ☐ Automatic Level Control (ALC)
- ☐ Balance
- ☐ 5-band Equalizer
- ☐ Stereo Separation Emphasis
- ☐ Digital Volume Control with Soft Mute (+12dB~-115dB, 0.5dB/step)
- ☐ Audio Data Interface:
  - I2S input x 5 (2 inputs: SRC available)
  - I2S output x 3
  - Master/Slave Mode
  - Audio Format: 24bit Left justified /Right justified / I^2S or TDM

3. Asynchronous Sample Rate Converter (SRC)
- ☐ Input Sample Rate: 8k~192kHz
- ☐ fso/fsi: 1/6~6

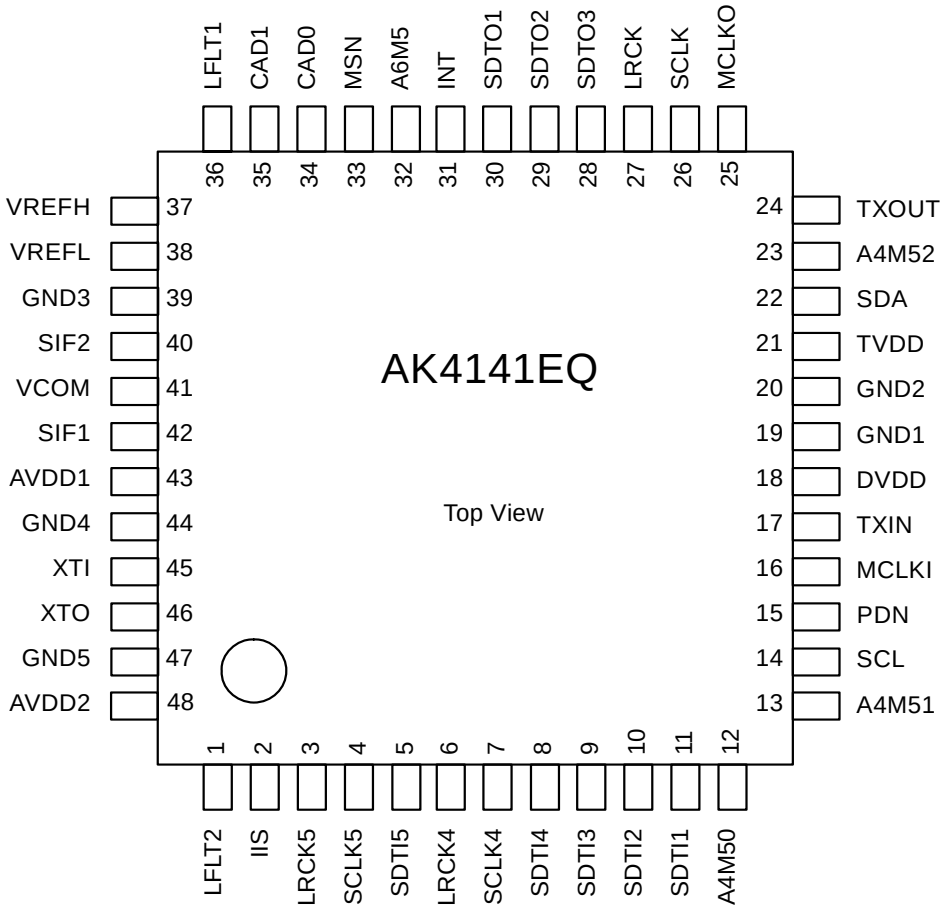
4. Digital Audio Interface Transmitter (DIT) with Through Mode
5. Integrated X'tal Oscillator
6. Master Clock: 256fs/384fs/512fs/768fs/1024fs
7. I2C-bus Control Interface
8. Power Supply: DVDD=1.8V±0.1V, AVDD=3.3V±0.3V, TVDD=1.7V~3.6V
9. Ta: -20 ~ 85°C
10. Package: 48pin LQFP



■ Ordering Guide

AK4141EQ	-20 ~ +85°C 48pin LQFP (0.5mm pitch)
AKD4141	Evaluation Board for AK4141

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	FILT2	O	PLL Loop Filter 2 Pin A 0.68μF capacitor should be connected to GND5 externally. Hi-Z when PDN Pin = "L".
2	IIS	I	Audio Data Format Select Pin. ORed with ODIF bit, ORed with IDIF0 bit. "L": 24bit Left justified if IDIF0 bit = "0"(default) "H": 24/16 bit IIS
3	LRCK5	I	Input Channel Clock 5 Pin
4	SCLK5	I	Audio Serial Data Clock 5 Pin
5	SDTI5	I	Audio Serial Data Input 5 Pin
6	LRCK4	I	Input Channel Clock 4 Pin
7	SCLK4	I	Audio Serial Data Clock 4 Pin
8	SDTI4	I	Audio Serial Data Input 4 Pin Should be synchronized to LRCK and SCLK when SRC is not used.
9	SDTI3	I	Audio Serial Data Input 3 Pin
10	SDTI2	I	Audio Serial Data Input 2 Pin
11	SDTI1	I	Audio Serial Data Input 1 Pin
12	A4M50	I	Decoder Standard Preference Control 0 Pin for 4.5MHz Carrier This pin is internally XORed with A4M50 bit (default = "1").
13	A4M51	I	Decoder Standard Preference Control 1 Pin for 4.5MHz Carrier This pin is internally XORed with A4M51 bit (default = "1").
14	SCL	I	Control Data Clock Pin for I2C bus
15	PDN	I	Power-Down Mode & Reset Pin When "L", the AK4141 is powered-down, all registers are reset. And then all digital output pins go "L". The AK4141 must be reset once upon power-up.
16	MCKI	I	Master Clock Input Pin
17	TXIN	I	S/PDIF Input Pin For through output. No Input Amplifier integrated.
18	DVDD	-	Digital Power Supply Pin, 1.7V~1.9V
19	GND1	-	Ground Pin, 0V
20	GND2	-	Ground Pin, 0V
21	TVDD	-	I/O Buffer Power Supply Pin, 1.7V~3.6V
22	SDA	I/O	Control Data Pin for I2C bus
23	A4M52	I	Decoder Standard Preference Control 2 Pin for 4.5MHz Carrier This pin is internally ORed with A4M52 bit (default = "0").
24	TXOUT	O	S/PDIF Output pin. Outputs "L" when PDN Pin = "L".
25	MCKO	O	Master Clock Output Pin. Outputs "L" when PDN Pin = "L".
26	SCLK	I/O	Audio Serial Data Clock Pin. Outputs "L" when PDN Pin = "L" and MSN Pin = "H". Hi-Z when PDN Pin = "L" and MSN Pin = "L".
27	LRCK	I/O	Input Channel Clock Pin Outputs "L" when PDN Pin = "L" and MSN Pin = "H". Hi-Z when PDN Pin = "L" and MSN Pin = "L".
28	SDTO3	O	Audio Serial Data Output 3 Pin Outputs "L" when PDN Pin = "L".
29	SDTO2	O	Audio Serial Data Output 2 Pin Outputs "L" when PDN Pin = "L".
30	SDTO1	O	Audio Serial Data Output 1 Pin Outputs "L" when PDN Pin = "L".

PIN/FUNCTION

31	INT	O	Interrupt Pin Outputs “L” when PDN Pin = “L”.
32	A6M5	I	Decoder Standard Preference Control for 6.5MHz carrier. “L”: SECAM L NICAM “H”: D/K1, D/K2, D/K3 or D/K NICAM This Pin is internally ORed with A6M5 bit (default = “0”).
33	MSN	I	Master Mode Select Pin “L”: Slave mode if CKS[2:0] bits = “000”(default) “H”: Master mode of MCLK = 256fs if CKS2 bit = “0”(default)
34	CAD0	I	Chip Address 0 pin Should match CAD0 bit in I2C first byte.
35	CAD1	I	Chip Address 1 pin Should match CAD1 bit in I2C first byte.
36	FILT1	O	PLL Loop Filter 1 Pin A 4.7nF capacitor should be connected to GND3 externally. Hi-Z when PDN Pin = “L”.
37	VREFH	O	ADC Voltage Reference High Pin A 0.1μF capacitor should be connected to GND3, and another 0.1μF capacitor should be connected to VREFL Pin externally. Hi-Z when PDN Pin = “L”.
38	VREFL	O	ADC Voltage Reference Low Pin A 0.1μF capacitor should be connected to GND3 externally. Hi-Z when PDN Pin = “L”.
39	GND3	-	Ground Pin, 0V
40	SIF2	I	Sound Intermediate Frequency(SIF) Input 2 Pin
41	VCOM	O	ADC Common Voltage Output Pin. A 1μF capacitor should be connected to GND3 externally. Hi-Z when PDN Pin = “L”.
42	SIF1	I	Sound Intermediate Frequency(SIF) Input 1 Pin
43	AVDD1	-	Analog Power Supply Pin, 3.0V~3.6V
44	GND4	-	Ground Pin, 0V
45	XTI	I	X'tal Input Pin
46	XTO	O	X'tal Output Pin. Outputs “L” when PDN pin = “L”.
47	GND5	-	Ground Pin, 0V
48	AVDD2	-	Analog Power Supply Pin, 3.0V~3.6V

Note: All digital input pins should not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	SIF1, SIF2	These pins should be connected to GND through 10nF capacitor.
Digital	TXOUT, MCLKO, SDTO1, SDTO2, SDTO3, INT, LRCK(master mode), SCLK(master mode)	These pins should be open.
	LRCK5, SCLK5, SDTI5, LRCK4, SCLK4, SDTI4, LRCK(slave mode), SCLK(slave mode), SDTI3, SDTI2, SDTI1, A4M50, A4M51, A4M52, A6M5, SCL, MCLKI, TXIN, SDA, IIS, MSN, CAD1, CAD0	These pins should be connected to GND.

ABSOLUTE MAXIMUM RATINGS

(GND1=GND2=GND3=GND4=GND5=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog	AVDD	-0.3	4.3	V
	Digital	DVDD	-0.3	2.4	V
	Digital I/O	TVDD	-0.3	4.3	V
Input Current, Any Pin Except Supply		IIN	-	±10	mA
Analog Input Voltage (SIF1, SIF2 pin)		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (Note 2)		VIND	–0.3	TVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–20	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. LRCK5, SCLK5, SDTI5, LRCK4, SCLK4, SDTI4, LRCK(slave mode), SCLK(slave mode), SDTI3, SDTI2, SDTI1, A4M50, A4M51, A4M52, A6M5, SCL, MCLKI, TXIN, SDA, IIS, MSN, CAD1 and CAD0 pin.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(GND1=GND2=GND3=GND4=GND5=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	AVDD	AVDD	3.0	3.3	3.6	V
	DVDD	DVDD	1.7	1.8	1.9	V
	TVDD	TVDD	DVDD	3.3	3.6	V

WARNING: AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

AUDIO CHARACTERISTICS

(Ta=25°C; AVDD=3.3V, DVDD=1.8V, TVDD=3.3V; GND1=GND2=GND3=GND4=GND5=0V; fs=48kHz; SCLK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=50Hz ~ 13kHz; unless otherwise specified)

SIF & Demodulator Parameter	**min**	**typ**	**max**	**Units**
SIF Input Impedance				
GSEL bit = 0	4.05	4.50		kohm
GSEL bit = 1	5.09	5.66		kohm
SIF Separation (Note 3)	30	50		dB
AGC step width		0.64		dB
Input Voltage				
1 or 2 FM Carriers				
GSEL bit = "0"	0.1		1.4	Vpp
GSEL bit = "1"	0.1		1.0	Vpp
1 FM and 1 NICAM Carrier				
GSEL bit = "0"	0.1		1.4	Vpp
GSEL bit = "1"	0.1		1.0	Vpp
1 AM and 1 NICAM Carrier				
GSEL bit = "0"	0.1		0.8	Vpp
GSEL bit = "1"	0.1		0.8	Vpp
1 NICAM Only				
GSEL bit = "0"	0.05		1.0	Vpp
GSEL bit = "1"	0.05		1.0	Vpp
Max FM-deviation (approx.)				
Normal			+/-180	kHz
High deviation			+/-360	kHz
Very High Deviation			+/-540	kHz
NICAM Characteristics	**min**	**typ**	**max**	**Units**
Output level (1kHz, 0dBr)	-1.5		+1.5	dB
S/N	74	80		dB
THD+N		0.05	0.15	%
NICAM Bit Error Rate (FM+ NICAM, normal condition)			1	10^{-7}
Frequency response (20 ~ 15kHz, -12dB, dual)	-1		+1	dB
NICAM Crosstalk attenuation (dual)	80			dB
Channel separation (stereo)	80			dB
FM Characteristics (Note 4)	**min**	**typ**	**max**	**Units**
Output level (1kHz, 0dBr)	-1.5		+1.5	dB
S/N	67	73		dB
THD+N		0.1	0.3	%
Frequency response (20 ~ 12kHz, -12dB, dual)	-1		+1	dB
FM Crosstalk attenuation (dual)	75	85		dB
Channel separation (stereo)	30	40		dB
AM Characteristics	**min**	**typ**	**max**	**Units**
S/N	47	62		dB
THD+N		1.2	3	%
Frequency response (20 ~ 12kHz, -12dB, dual)	-2.5		+1	dB

Note 3. Selected SIF pin is connected to GND through 10nF capacitor.
Note 4. 1 FM-Carrier, 5.5MHz.

AUDIO CHARACTERISTICS (Continued)

(Ta=25°C; AVDD=3.3V, DVDD=1.8V, TVDD=3.3V; GND1=GND2=GND3=GND4=GND5=0V; fs=48kHz; SCLK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=50Hz ~ 13kHz; unless otherwise specified)

EIAJ Characteristics	min	typ	max	Units
S/N				
Stereo	54	60		dB
Sub	54	60		dB
THD+N (1kHz L or R or Sub 100%)				
Stereo		0.3	0.9	%
Sub		0.3	0.9	%
Frequency response				
Stereo (20 ~ 12kHz, 100%EIM)	-1		+1	dB
Sub (20 ~ 12kHz, 100%EIM)	-1		+1	dB
Channel separation (stereo)	30	40		dB

SRC CHARACTERISTICS

(Ta=25°C; AVDD=3.3V, DVDD=1.8V, TVDD=3.3V; GND1=GND2=GND3=GND4=GND5=0V; fs=48kHz; SCLK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ FSO/2; unless otherwise specified)

Parameter	Symbol	min	typ	max	Units
SRC Characteristics:					
Resolution				20	Bits
Input Sample Rate	FSI	8		216	kHz
Output Sample Rate	FSO	32		48	kHz
THD+N (Input = 1kHz, 0dBFS, Note 5)					
FSO/FSI = 48kHz/8kHz		-	-100	-	dB
FSO/FSI = 48kHz/32kHz		-	-100	-	dB
FSO/FSI = 48kHz/192kHz		-	-100	-	dB
Worst Case (FSO/FSI = 32kHz/176.4kHz)		-	-91	-81	dB
Dynamic Range (Input = 1kHz, –60dBFS, A-weighted, Note 5)					
FSO/FSI = 48kHz/8kHz		-	115	-	dB
FSO/FSI = 48kHz/32kHz		-	115	-	dB
FSO/FSI = 48kHz/192kHz		-	115	-	dB
Worst Case (FSO/FSI = 48kHz/32kHz)		111	115	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	1/6		6	-

Note 5. Measured by Audio Precision System Two Cascade.

Power Supplies				
Parameter	**min**	**typ**	**max**	**Units**
Power Supply Current				
Normal Operation (PDN pin = "H")				
TVDD		5	8	mA
AVDD1+AVDD2		20	28	mA
DVDD		61	92	mA
Power-Down Mode (PDN pin = "L"; Note: 1)				
TVDD		10	100	μA
AVDD1+AVDD2		10	100	μA
DVDD		10	100	μA

Note: 1. All digital inputs including clock pins are held at DVDD or GND.

SRC FILTER CHARACTERISTICS

(Ta=25°C; AVDD=3.0 ~ 3.6V, DVDD=1.7V~ 1.9V, TVDD=1.7 ~ 3.6V; GND1=GND2=GND3=GND4=GND5=0V)

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband –0.01dB	0.985 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
	0.905 ≤ FSO/FSI < 0.985	PB	0		0.4167FSI	kHz
	0.714 ≤ FSO/FSI < 0.905	PB	0		0.3195FSI	kHz
	0.656 ≤ FSO/FSI < 0.714	PB	0		0.2852FSI	kHz
	0.536 ≤ FSO/FSI < 0.656	PB	0		0.2182FSI	kHz
	0.492 ≤ FSO/FSI < 0.536	PB	0		0.2177FSI	kHz
	0.452 ≤ FSO/FSI < 0.492	PB	0		0.1948FSI	kHz
	0.357 ≤ FSO/FSI < 0.452	PB	0		0.1458FSI	kHz
	0.324 ≤ FSO/FSI < 0.357	PB	0		0.1302FSI	kHz
	0.246 ≤ FSO/FSI < 0.324	PB	0		0.0917FSI	kHz
	0.226 ≤ FSO/FSI < 0.246	PB	0		0.0826FSI	kHz
	0.1667 ≤ FSO/FSI < 0.226	PB	0		0.0583FSI	kHz
Stopband	0.985 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI			kHz
	0.905 ≤ FSO/FSI < 0.985	SB	0.5021FSI			kHz
	0.714 ≤ FSO/FSI < 0.905	SB	0.3965FSI			kHz
	0.656 ≤ FSO/FSI < 0.714	SB	0.3643FSI			kHz
	0.536 ≤ FSO/FSI < 0.656	SB	0.2974FSI			kHz
	0.492 ≤ FSO/FSI < 0.536	SB	0.2813FSI			kHz
	0.452 ≤ FSO/FSI < 0.492	SB	0.2604FSI			kHz
	0.357 ≤ FSO/FSI < 0.452	SB	0.2116FSI			kHz
	0.324 ≤ FSO/FSI < 0.357	SB	0.1969FSI			kHz
	0.246 ≤ FSO/FSI < 0.324	SB	0.1573FSI			kHz
	0.226 ≤ FSO/FSI < 0.246	SB	0.1471FSI			kHz
	0.1667 ≤ FSO/FSI < 0.226	SB	0.1020FSI			kHz
Passband Ripple		PR			±0.01	dB
Stopband Attenuation	0.985 ≤ FSO/FSI ≤ 6.000	SA	102.2			dB
	0.905 ≤ FSO/FSI < 0.985	SA	100.4			dB
	0.714 ≤ FSO/FSI < 0.905	SA	99.0			dB
	0.656 ≤ FSO/FSI < 0.714	SA	101.6			dB
	0.536 ≤ FSO/FSI < 0.656	SA	99.5			dB
	0.492 ≤ FSO/FSI < 0.536	SA	95.2			dB
	0.452 ≤ FSO/FSI < 0.492	SA	96.6			dB
	0.357 ≤ FSO/FSI < 0.452	SA	97.0			dB
	0.324 ≤ FSO/FSI < 0.357	SA	94.4			dB
	0.246 ≤ FSO/FSI < 0.324	SA	95.8			dB
	0.226 ≤ FSO/FSI < 0.246	SA	95.0			dB
	0.1667 ≤ FSO/FSI < 0.226	SA	73.7			dB
Group Delay	(Note 6)	GD	-	56	-	1/fs

Note 6. This value is the time from the rising edge of LRCK after data is input to rising edge of LRCK after data is output, when LRCK for Output data corresponds with LRCK for Input.

DC CHARACTERISTICS

(Ta=25°C; AVDD=3.0 ~ 3.6V, DVDD=1.7V~ 1.9V, TVDD=1.7 ~ 3.6V; GND1=GND2=GND3=GND4=GND5=0V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage					
TVDD < 2.7V	VIH	80%TVDD	-	-	V
TVDD ≥ 2.7V	VIH	70%TVDD	-	-	V
Low-Level Input Voltage					
TVDD < 2.7V	VIL	-	-	20%TVDD	V
TVDD ≥ 2.7V	VIL	-	-	30%TVDD	V
High-Level Output Voltage (Iout=-400μA)	VOH	TVDD-0.4	-	-	V
Low-Level Output Voltage (Iout= -400μA(except SDA pin), 3mA(SDA pin))	VOL	-		0.4	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=-20~ 85°C; AVDD= 3.0~3.6V, DVDD=1.7~1.9V TVDD=1.7~3.6V; GND1=GND2=GND3=GND4=GND5=0V; C_L=20pF; unless otherwise specified)

Parameter		Symbol	min	typ	max	Units
Crystal Resonator Frequency		fXTAL		256fs		
fs=32kHz				8.192		MHz
fs=44.1kHz				11.2896		MHz
fs=48kHz				12.288		MHz
Master Clock Timing						
Master Clock	128fs:	fCLK	4.096		6.144	MHz
	Pulse Width Low	tCLKL	65			ns
	Pulse Width High	tCLKH	65			ns
	192fs:	fCLK	6.144		9.216	MHz
	Pulse Width Low	tCLKL	43			ns
	Pulse Width High	tCLKH	43			ns
	256fs:	fCLK	8.192		12.288	MHz
	Pulse Width Low	tCLKL	27			ns
	Pulse Width High	tCLKH	27			ns
	384fs:	fCLK	12.288		18.432	MHz
	Pulse Width Low	tCLKL	20			ns
	Pulse Width High	tCLKH	20			ns
	512fs:	fCLK	16.384		24.576	MHz
	Pulse Width Low	tCLKL	16			ns
	Pulse Width High	tCLKH	16			ns
	768fs:	fCLK	24.576		36.864	MHz
	Pulse Width Low	tCLKL	11			ns
	Pulse Width High	tCLKH	11			ns
	1024fs:	fCLK	32.768		49.152	MHz
	Pulse Width Low	tCLKL	8			ns
	Pulse Width High	tCLKH	8			ns

SWITCHING CHARACTERISTICS (Continued)

(Ta=-20~ 85°C; AVDD= 3.0~3.6V, DVDD=1.7~1.9V TVDD=1.7~3.6V; GND1=GND2=GND3=GND4=GND5=0V; C_L=20pF; unless otherwise specified)

Parameter (Note 8)	Symbol	min	typ	max	Units
LRCK Timing (Slave Mode)					
Normal mode (TDM="0")					
LRCK Frequency	fs	32		48	kHz
Duty Cycle	Duty	45		55	%
TDM256 mode (TDM="1")					
LRCK Frequency	fs	32		48	kHz
"H" time	tLRH	1/256fs			ns
"L" time	tLRL	1/256fs			ns
SRC Input					
LRCK Frequency	fs	8		192	KHz
Duty Cycle	Duty	45		55	%
LRCK Timing (Master Mode)					
Normal mode (TDM="0")					
LRCK Frequency	fs	32		48	kHz
Duty Cycle	Duty		50		%
TDM256 mode (TDM="1")					
LRCK Frequency	fs	32		48	kHz
"H" time (Note 7)	tLRH		1/8fs		ns
Audio Interface Timing (Slave mode)					
Normal mode (TDM="0")					
SCLK Period	tBCK	160			ns
SCLK Pulse Width Low	tBCKL	65			ns
Pulse Width High	tBCKH	65			ns
LRCK Edge to SCLK "↑" (Note 9)	tLRB	30			ns
SCLK "↑" to LRCK Edge (Note 9)	tBLR	30			ns
LRCK to SDTO(MSB) (Except I^2S mode)	tLRS			35	ns
SCLK "↓" to SDTO	tBSD			35	ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
TDM256 mode (TDM="1")					
SCLK Period	tBCK	81			ns
SCLK Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCK Edge to SCLK "↑" (Note 9)	tLRB	20			ns
SCLK "↑" to LRCK Edge (Note 9)	tBLR	20			ns
SCLK "↓" to SDTO	tBSD			20	ns
TDMIN Hold Time	tSDH	10			ns
TDMIN Setup Time	tSDS	10			ns
SRC Input (Note 10)					
SCLK Period	tBCK	81			ns
SCLK Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCK Edge to SCLK "↑" (Note 9)	tLRB	20			ns
SCLK "↑" to LRCK Edge (Note 9)	tBLR	20			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns

SWITCHING CHARACTERISTICS (Continued)

(Ta=-20~ 85°C; AVDD= 3.0~3.6V, DVDD=1.7~1.9V TVDD=1.7~3.6V; GND1=GND2=GND3=GND4=GND5=0V; C_L=20pF; unless otherwise specified)

Parameter (Note 8)	Symbol	min	typ	max	Units
Audio Interface Timing (Master mode)					
Normal mode (TDM="0")					
SCLK Frequency	fBCK		64fs		Hz
SCLK Duty	dBCK		50		%
SCLK "↓" to LRCK	tMBLR	–20		20	ns
SCLK "↓" to SDTO	tBSD	–40		40	ns
TDM256 mode (TDM="1")					
SCLK Frequency	fBCK		256fs		Hz
SCLK Duty (Note 11)	dBCK		50		%
SCLK "↓" to LRCK	tMBLR	–12		12	ns
SCLK "↓" to SDTO	tBSD	–20		20	ns
TDMIN Hold Time	tSDH	10			ns
TDMIN Setup Time	tSDS	10			ns
Power-Down & Reset Timing					
PDN Pulse Width (Note 12)	tPD	150			ns
PDN "↑" to SDTO valid (Note 13)	tPDV		TBD		1/fs

Note 7. "L" time at I²S format.
Note 8. SCLK= SCLK/SCLK4/SCLK5, LRCK= SCLK/LRCK4/LRCK5 unless otherwise specified.
Note 9. SCLK rising edge must not occur at the same time as LRCK edge.
Note 10. SCLK= SCLK4/SCLK5, LRCK= LRCK4/LRCK5.
Note 11. This value is when fs=48kHz or 44.1kHz. When fs=32kHz, L=(5/9x100)% and H=(4/9x100)%.
Note 12. The AK4141 can be reset by bringing the PDN pin = "L".
Note 13. This cycle is the number of LRCK rising edges from the PDN pin = "H".

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (I²C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 14)	tHD:DAT	0		0.9	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on SDA	Cb	0		400	pF

Note 14. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 15. I²C is a registered trademark of Philips Semiconductors.

■ Timing Diagram

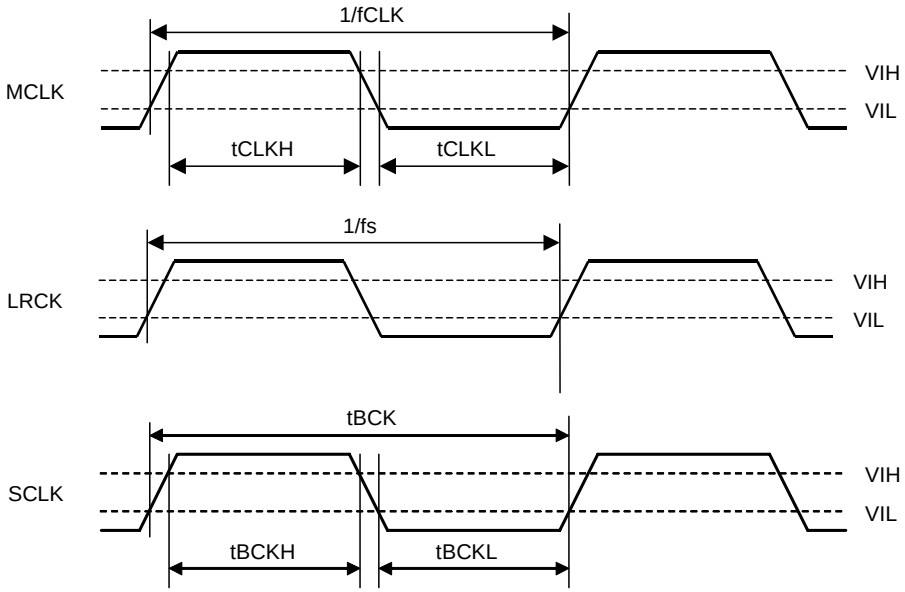


Figure 1. Clock Timing (TDM bit = "0")

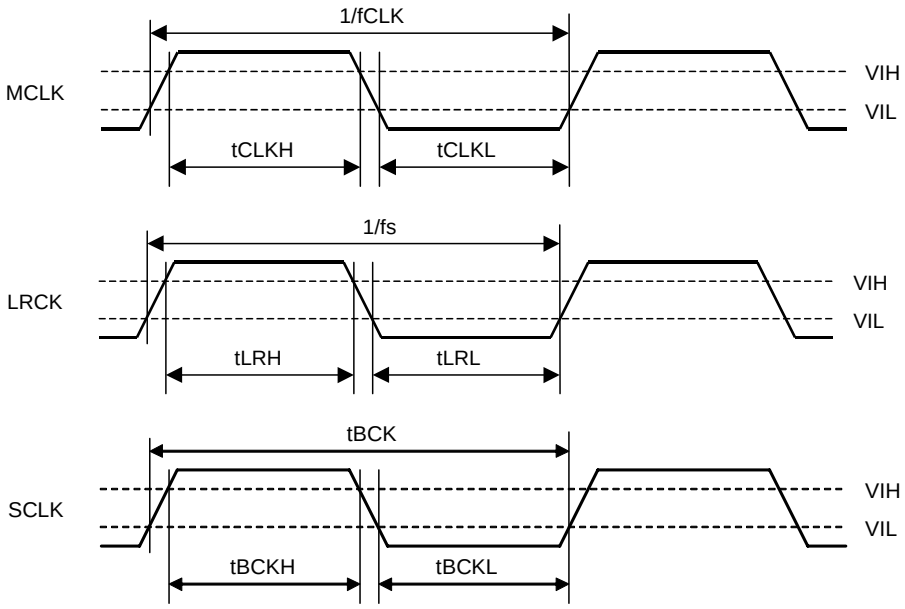


Figure 2. Clock Timing (TDM bit = "1")

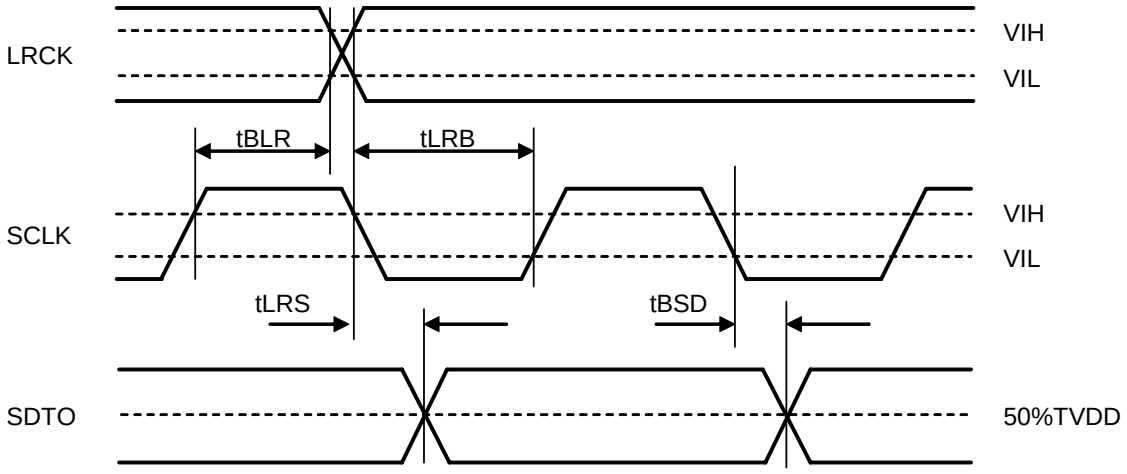


Figure 3. Audio Interface Timing (Slave mode, Normal Mode)

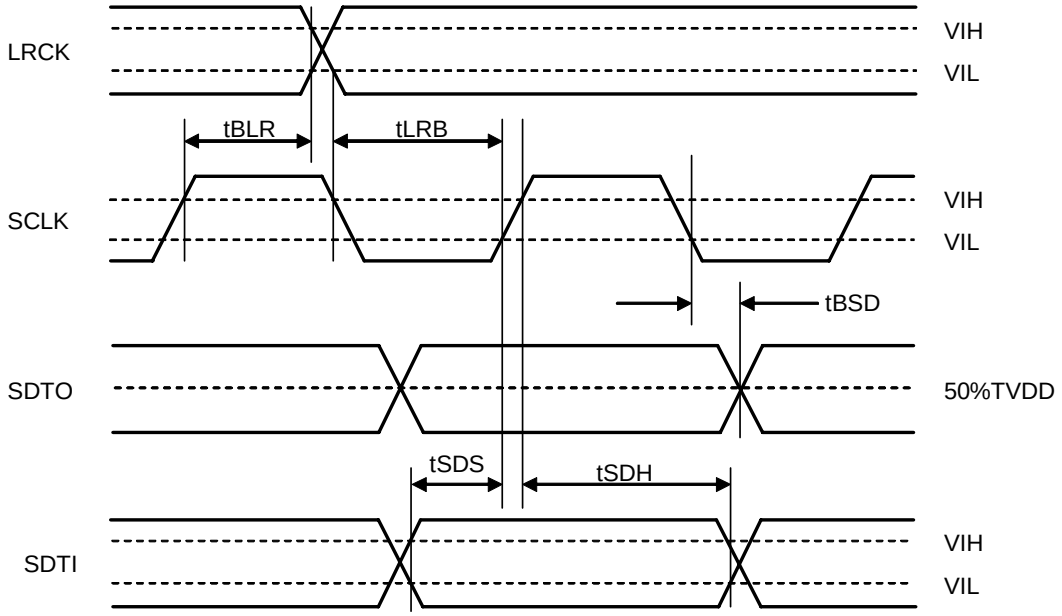


Figure 4. Audio Interface Timing (Slave mode, TDM Mode)

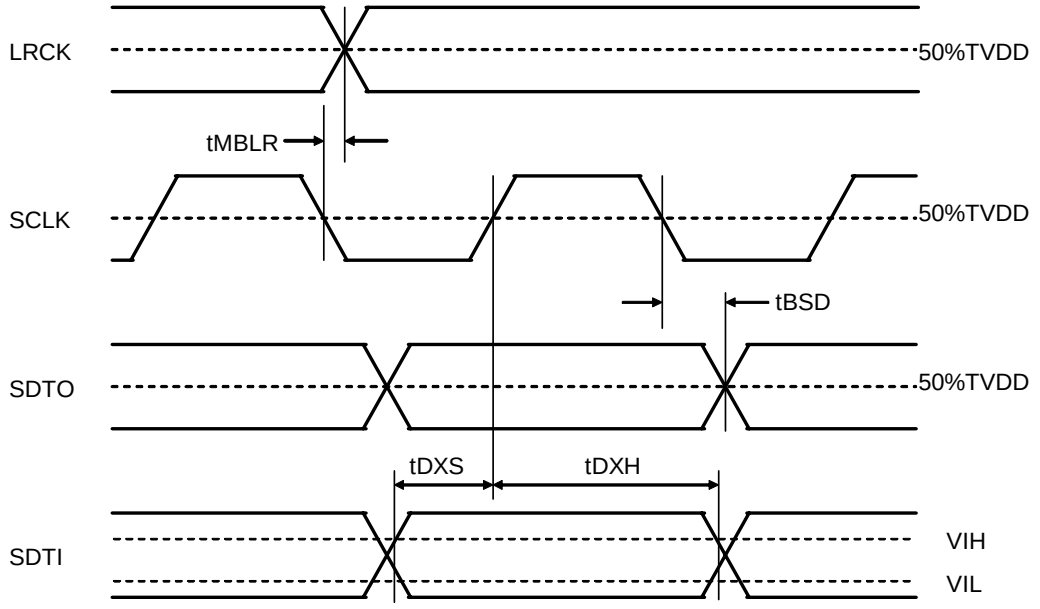


Figure 5. Audio Interface Timing (Master mode, Normal Mode)

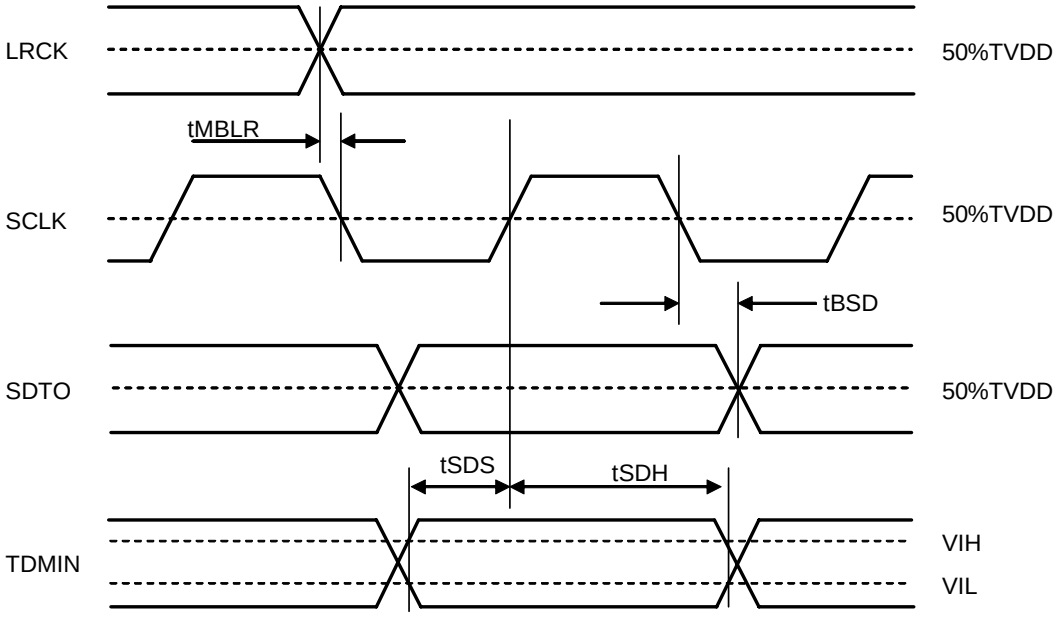


Figure 6. Audio Interface Timing (Master mode, TDM Mode)

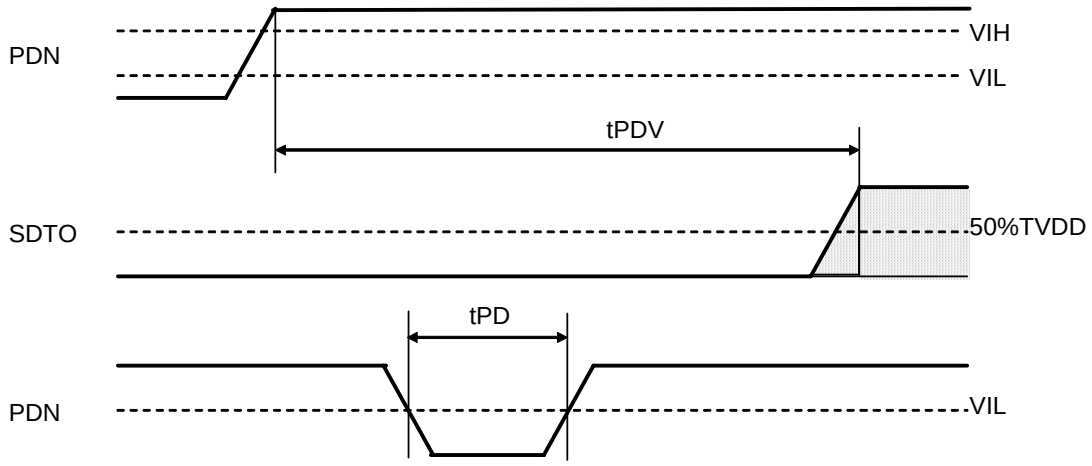


Figure 7. Power Down & Reset Timing

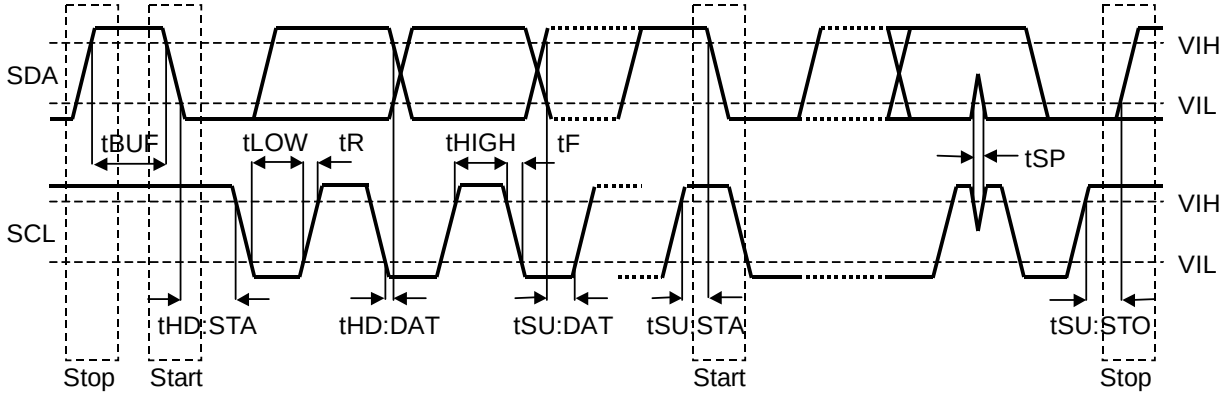


Figure 8. I^2C Bus mode Timing

OPERATION OVERVIEW

■ System Clock

The external clocks, which are required to operate the AK4141, are MCLK(or XTI), LRCK and SCLK. The MCLK(or XTI) should always be present whenever the AK4141 is in normal operation, and should be synchronized with LRCK but the phase is not critical. The on-chip X'tal oscillator or external system clock through MCKI can be used for the AK4141 operation. If the external clocks are not present, the AK4141 should be in the power-down mode (PDN pin = "L") or in the reset mode (RSTN bit = "0"). After exiting reset at power-up etc., the AK4141 is in the power-down mode until MCLK(or XTI) and LRCK are input.

The AK4141 supports both master mode (SCLK, LRCK = output) and slave mode (SCLK, LRCK = input). The AK4141 is master mode when MSN pin = "H", slave mode when MSN pin = "L". SRC inputs (SCLK4/5, LRCK4/5) are always slave mode (input) and can operate asynchronously.

PDN pin	MSN pin	SCLK, LRCK	SCLK4/5, LRCK4/5
L	L	Input (slave mode)	Input (slave mode)
	H	Output "L" (master mode)	Input (slave mode)
H	L	Input (slave mode)	Input (slave mode)
	H	Output (master mode)	Input (slave mode)

note: when CKS2-0 bits are default.

Table 1. Master/Salve Mode

The MSN pin and the CKS2-0 bits select the clock frequency (Table 2). The external clock (X'tal or MCKI) should always be supplied except in the power-down mode. The AK4141 is in power-down mode until the clock is supplied.

MSN pin	CKS2 bit	CKS1 bit	CKS0 bit	Master /Slave	Master Clock Speed
L	0	0	0	Slave	128fs, 192fs, 256fs, 384fs, 512fs, 768fs, 1024fs (register default)
L	0	0	1	Master	128fs
L	0	1	0	Master	192fs
L	0	1	1	Master	256fs
L	1	0	0	Master	384fs
L	1	0	1	Master	512fs
L	1	1	0	Master	768fs
L	1	1	1	Master	1024fs
H	0	x	x	Master	256fs (register default)
H	1	x	x	Master	1024fs

(x: Don't care.)

Table 2. System clock control

LRCK	MCLK (MHz)						
fs	128fs	192fs	256fs	384fs	512fs	768fs	1024fs
32.0kHz	4.0960	6.1440	8.1920	12.2880	16.3840	24.5760	32.7680
44.1kHz	5.6448	7.5264	11.2896	16.9344	22.5792	33.8688	45.1584
48.0kHz	6.1440	9.2160	12.2880	18.4320	24.5760	36.8640	49.1520

Table 3. System clock example

■ Multi-standard Stereo Decoding

The AK4141 receives the Sound IF(SIF) signal and demodulates/decodes according to NICAM/A2/EIA-J standards. The AK4141 can automatically select the stereo standard according to the actual input signal, the A4M5[2-0] pins(XORed with A4M5[2-0] bits, default = "011") and the A6M5 pin (XORed with A6M5 bit) setting.

A6M5 bit	A6M5 pin	Decoder Standard Preference1
0 (default)	L	SECAM L NICAM
0 (default)	H	D/K1, D/K2, D/K3 or D/K NICAM
1	L	D/K1, D/K2, D/K3 or D/K NICAM
1	H	SECAM L NICAM

Table 4. Decoder Standard Preference 1 (for 6.5MHz carrier)

A4M5[2-0] pins	Decoder Standard Preference2
LLL	PAL (Chroma Carrier)
LLH	M-Korea
LHL	EIAJ
LHH	Reserved
HLL	Reserved
HLH	Reserved
HHL	Reserved
HHH	Reserved

Table 5. Decoder Standard Preference 2 (for 4.5MHz carrier. Pin control. A4M5[2-0] bits = "011"(default))

A4M5[2-0] bits	Decoder Standard Preference2
00H	Reserved
01H	EIAJ
02H	M-Korea
03H	PAL (Chroma Carrier)
04H	Reserved
05H	Reserved
06H	Reserved
07H	Reserved

Table 6. Decoder Standard Preference 2 (for 4.5MHz carrier. Register control. A4M5[2-0] pins = "LLL")

■ Audio Serial Interface Format

The IDIF[1-0] and ODIF bit control the audio format for SCLK, SCLK4/5, LRCK, LRCK4/5, SDTI[1-5] and SDTO[1-3]. ODIF bit and IDIF0 bit are ORed with DIF pin. When the TDM bit = "1", the TDM mode is enabled. The SRC inputs (SDTI [4-5]) ignore the TDM bit and operate in normal mode. In all modes the serial data is MSB-first, 2's complement format. The SDTO1-3 pins are clocked out on the falling edge of SCLK pin and the SDTI[1-3] pins are latched on the rising edge of SCLK pin. The SDTI[4-5] pins are latched on the rising edge of SCLK[4-5] pins. In SRC bypass mode, The SCLK[4-5] and LRCK[4-5] should be synchronized to LRCK.

1. Normal mode: TDM bit = "0"
   The TDM bit = "0" sets the AK4141 audio serial interface format to the normal mode. The IIS pin, DIF1-0 bits and ODIF bit select following serial data format (Table 7, Table 8)

MSN pin	IIS pin	IDIF1 bit	IDIF0 bit	Mode	Input Audio Data Format	LRCK		BICK	
						L/R	I/O	speed	I/O
L	L	0	0	0	20bit Right Justified	H/L	I	≥ 16fs	I
			1	1	24bit Right Justified			≥ 48fs	
		1	0	2	24bit Left Justified (register default)			≥ 48fs	
			1	3	24/16bit I2S	L/H		32fs or ≥ 48fs	
	H	0	x	2	24bit Right Justified	H/L		≥ 48fs	
		1		3	24/16bit I2S (register default)	L/H		32fs or ≥ 48fs	
H	L	0	0	4	16bit Right Justified	H/L	O	64fs	O
			1	5	24bit Right Justified				
		1	0	6	24bit Left Justified (register default)				
			1	7	24/16bit I2S	L/H			
	H	0	x	6	24bit Right Justified	H/L			
		1		7	24/16bit I2S (register default)	L/H			

(x: Don't care.)

Table 7. Input Audio Data Format control

MSN pin	IIS pin	ODIF bit	Mode	Output Audio Data Format	LRCK		SCLK	
					L/R	I/O	speed	I/O
L	L	0	8	24bit Left Justified (register default)	H/L	I	≥ 48fs	I
		1	9	24/16bit I2S	L/H		32fs or ≥ 48fs	
	H	x	9	24/16bit I2S (register default)	L/H		32fs or ≥ 48fs	
H	L	0	10	24bit Left Justified (register default)	H/L	O	64fs	O
		1	11	24/16bit I2S	L/H			
	H	x	11	24/16bit I2S (register default)	L/H			

(x: Don't care.)

Table 8. Output Audio Data Format control

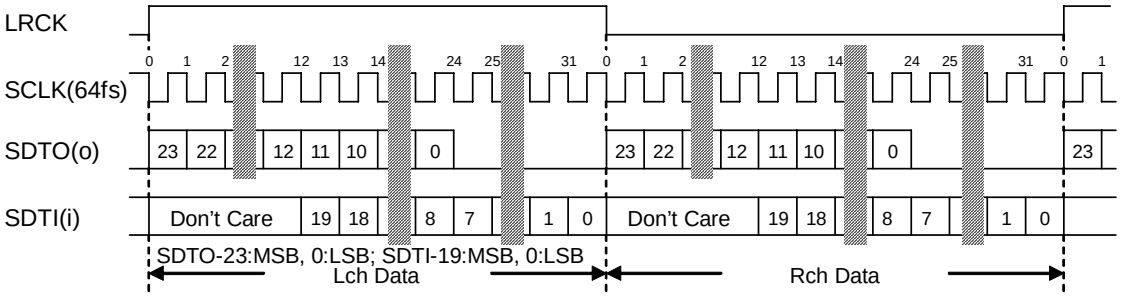


Figure 9. Mode 0/4/8/10 Timing

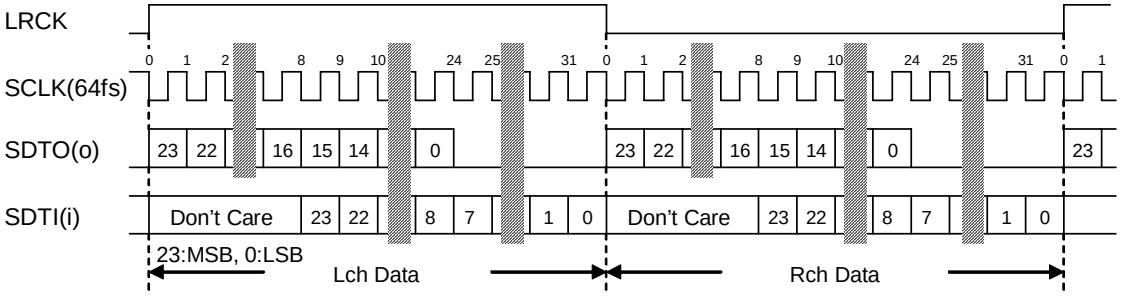


Figure 10. Mode 1/5 Timing

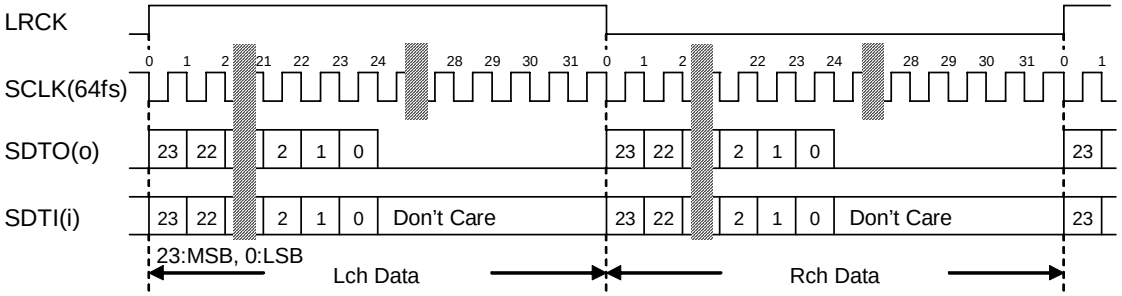


Figure 11. Mode 2/6 Timing

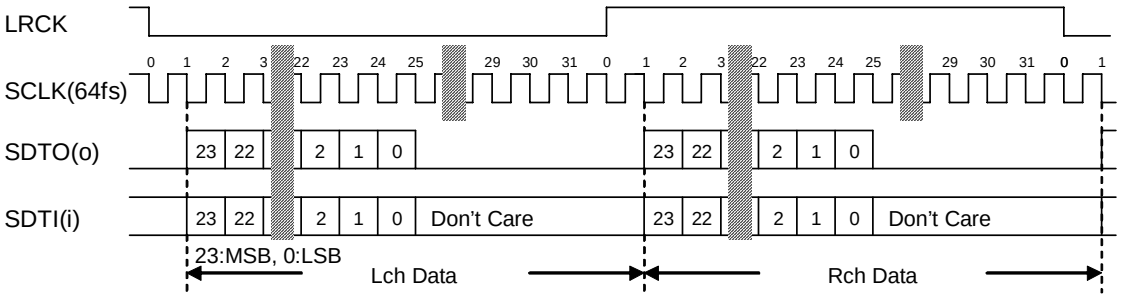


Figure 12. Mode 3/7/9/11 Timing

2. TDM mode: TDM bit = "1"

The TDM bits = "1" set the AK4141 audio serial interface format to the TDM mode. The eight channel serial data (SDTI1/2/3 and SDTI4 at non-SRC mode) is input through the SDTI1 pin. The six channel serial data is output through the SDTO1 pin. The SDTI2/3/4/5 pins are not used for TDM input and the SDTO2/3 pins outputs "L".

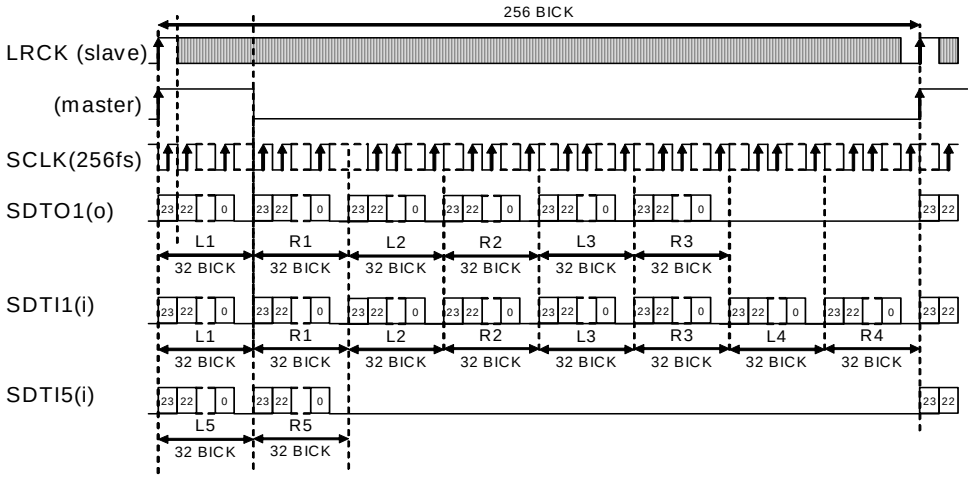


Figure 13. TDM MSB Justified Timing

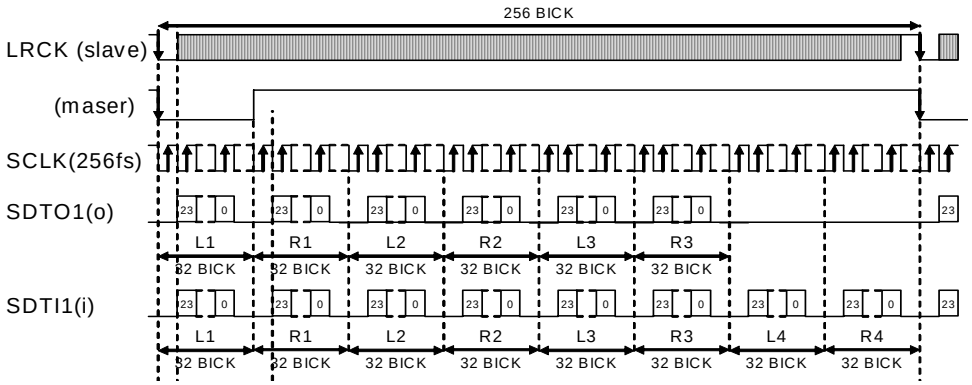
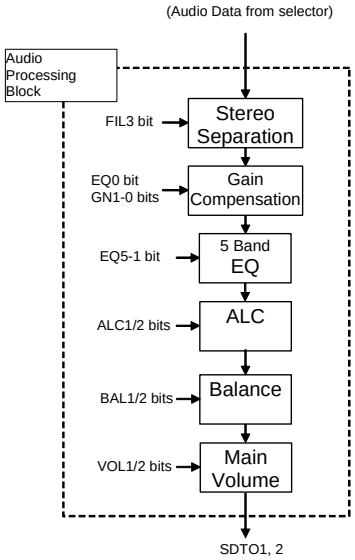


Figure 14. TDM IIS Timing

■ Digital Block

The digital block consists of block diagram as shown in Figure 15.



(1) Stereo Separation: Digital Separation Emphasis Filter (See "Digital Programmable Filter Circuit")
(2) Gain Compensation: Composed of the Equalizer (EQ0) and the Gain (0bB/+12dB/+24dB). Compensate the frequency response and the gain after the Stereo Separation Emphasis Filter.
(3) 5-Band Notch: Applicable to use as Equalizer or Notch Filter. (See "Digital Programmable Filter")
(4) ALC: Input Digital Volume with ALC function. (See "ALC Operation")
(5) Balance: Stereo Balance Control.
(6) Main Volume: Stereo Main Volume Control.

Figure 15 Audio Processing Block

■ Digital Programmable Filter Circuit

(1) Stereo Separation Emphasis Filter (FIL3)

FIL3 is used to emphasize the stereo separation of stereo data. F3A1[13:0], F3A2[13:0] and F3B1[13:0], F3B1[13:0] bits set the filter coefficient of FIL3 for SDTO1/2 respectively. FIL3 becomes High Pass Filter (HPF) at F3AS1/2 bit = "1", and Low Pass Filter (LPF) at F3AS1/2 bit = "0". F3BP1/2 bit controls ON/OFF of FIL3. When Stereo Separation Emphasis Filter is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when F3BP1/2 bit = "0".

1) When FIL3 is set to "HPF"

fs: Sampling frequency
fc: Cut-off frequency
K: Filter gain [dB] (0dB ≥ K ≥ −10dB)

Register setting (Figure 15)
FIL3: F3AS1/2 bit = "1", F3A1[13:0], F3A1[13:0] bits =A, F3B1[13:0], F3B2[13:0] bits =B
(MSB=F3A113(F3A213), F3B13(F3B213); LSB=F3A10(F3A20), F3B10(F3B20))

$$A = 10^{K/20} \times \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

2) When FIL3 is set to "LPF"

fs: Sampling frequency
fc: Cut-off frequency
K: Filter gain [dB] (0dB ≥ K ≥ −10dB)

Register setting (Figure 15)
FIL3: F3AS1/2 bit = "0", F3A1[13:0], F3A1[13:0] bits =A, F3B1[13:0], F3B2[13:0] bits =B
(MSB= F3A113(F3A213), F3B13(F3B213); LSB= F3A10(F3A20), F3B10(F3B20))

$$A = 10^{K/20} \times \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

(2) Gain Compensation (EQ0)

Gain Compensation is used to compensate the frequency response and the gain that is changed by Stereo Separation Emphasis Filter. Gain Compensation is composed of the Equalizer (EQ0) and the Gain (0dB/+12dB/+24dB). E0A1[15:0], E0A215:0], E0B1[15:0] and E0B2[15:0] bits set the coefficient of EQ0. GN1[1:0], GN2[1:0] bits set the gain (Table 9).

fs: Sampling frequency
fc_1: Pole frequency
fc_2: Zero-point frequency
K: Filter gain [dB] (Maximum +12dB)

Register setting (Figure 15)
E0A1[15:0], E0A2[15:0] bits =A, E0B1[13:0], E0B2[13:0] bits =B, E0C1[15:0], E0C2[15:0] bits =C
(MSB=E0A115(E0A215),E0B113(E0B213), E0C115(E0C215); LSB=E0A10(E0A20), E0B10(E0B20), E0C10(E0C20))

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc_1/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}$$

Transfer function

$$H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$$

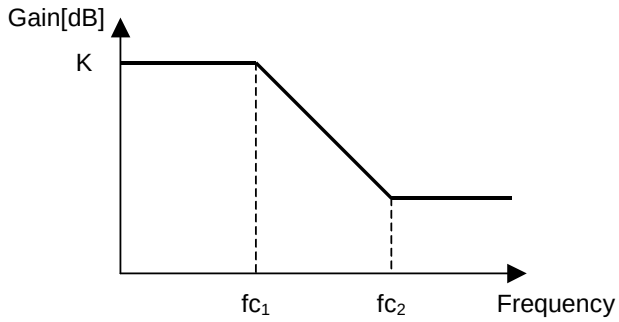


Figure 16. EQ0 Frequency Response

GN1	GN0	Gain	
0	0	0dB	(default)
0	1	+12dB	
1	x	+24dB	

Table 9. Gain select of gain block (x: Don't care)

(3) 5 Band Equalizer

The center frequencies and cut/boost amount are the followings.

- Center frequency: 100Hz, 250Hz, 1kHz, 3.5kHz, 10kHz (Note 16, Note 17)
- Cut/Boost amount: Minimum –10.5dB, Maximum +12dB, Step 1.5dB

Note 16: These are the frequencies when the sampling frequency is 44.1kHz. These frequencies are proportional to the sampling frequency.
Note 17: 100Hz is not center frequency but the frequency component lower than 100Hz is controlled.
Note 18: 10kHz is not center frequency but the frequency component higher than 10kHz is controlled.

EQ1/2 bits control ON/OFF of this Equalizer and these Boost amount are set by EQx3-0 bit as shown in Table 23.

EQA3-0: Select the boost level of 100Hz
EQB3-0: Select the boost level of 250Hz
EQC3-0: Select the boost level of 1kHz
EQD3-0: Select the boost level of 3.5kHz
EQE3-0: Select the boost level of 10kHz

EQx3-0	Boost amount	
0H	+12.0dB	
1H	+10.5dB	
2H	+9.0dB	
3H	+7.5dB	
:	:	
8H	0dB	(default)
:	:	
DH	–7.5dB	
EH	–9.0dB	
FH	–10.5dB	

Table 10. Boost amount of 5 Band Equalizer

■ ALC Operation

1. ALC Limiter Operation

During the ALC limiter operation, when either Lch or Rch exceeds the ALC limiter detection level (Table 11), the VOL value (same value for both L and R) is attenuated automatically by the amount defined by the ALC limiter ATT step (Table 12). The VOL is then set to the same value for both channels.

When ZELMN bit = "0" (zero cross detection is enabled), the VOL value is changed by ALC limiter operation at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. ZTM1-0 bits set the zero crossing timeout period of both ALC limiter and recovery operation (Table 13).

When ZELMN bit = "1" (zero cross detection is disabled), VOL value is immediately (period: 1/fs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless of the setting of LMAT1-0 bits.

The attenuate operation is executed continuously until the input signal level becomes ALC limiter detection level (Table 11) or less. After completing the attenuate operation, unless ALC bit is changed to "0", the operation repeats when the input signal level exceeds LMTH1-0 bits.

LMTH1	LMTH0	ALC Limiter Detection Level	ALC Recovery Waiting Counter Reset Level	
0	0	ALC Output ≥ –2.5dBFS	–2.5dBFS > ALC Output ≥ –4.1dBFS	(default)
0	1	ALC Output ≥ –4.1dBFS	–4.1dBFS > ALC Output ≥ –6.0dBFS	
1	0	ALC Output ≥ –6.0dBFS	–6.0dBFS > ALC Output ≥ –8.5dBFS	
1	1	ALC Output ≥ –8.5dBFS	–8.5dBFS > ALC Output ≥ –12dBFS	

Table 11. ALC Limiter Detection Level / Recovery Counter Reset Level

LMAT1	LMAT0	ALC1 Limiter ATT Step				
		ALC1 Output ≥ LMTH	ALC1 Output ≥ FS	ALC1 Output ≥ FS + 6dB	ALC1 Output ≥ FS + 12dB	
0	0	1	1	1	1	(default)
0	1	2	2	2	2	
1	0	2	4	4	8	
1	1	1	2	4	8	

Table 12. ALC Limiter ATT Step

ZTM1	ZTM0		Zero Crossing Timeout Period			
			32kHz	44.1kHz	48kHz	
0	0	128/fs	4.0ms	2.9ms	2.7ms	(default)
0	1	256/fs	8.0ms	5.8ms	5.3ms	
1	0	512/fs	16.0ms	11.6ms	10.7ms	
1	1	1024/fs	32.0ms	23.2ms	21.3ms	

Table 13. ALC Zero Crossing Timeout Period

2. ALC Recovery Operation

The ALC recovery operation waits for the WTM2-0 bits (Table 14) to be set after completing the ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 11) during the wait time, the ALC recovery operation is executed. The VOL value is automatically incremented by RGAIN1-0 bits (Table 15) up to the set reference level (Table 16) with zero crossing detection which timeout period is set by ZTM1-0 bits (Table 13). Then the IVL and IVR are set to the same value for both channels. The ALC recovery operation is executed at a period set by WTM2-0 bits. When zero cross is detected at both channels during the wait period set by WTM2-0 bits, the ALC recovery operation waits until WTM2-0 period and the next recovery operation is executed.

For example, when the current VOL value is 30H and RGAIN1-0 bits are set to "01", VOL is changed to 32H in the auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the VOL value exceeds the reference level (REF7-0), the VOL values are not increased.

When
"ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)" during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level (LMTH1-0) > Output Signal",
the waiting timer of ALC recovery operation starts.

The ALC operation corresponds to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to microphone instantaneously, the quality of small signal level in the large noise can be improved by this fast recovery operation. The speed of first recovery operation is set by RFST1-0 bits(Table 17).

WTM2	WTM1	WTM0		ALC Recovery Operation Waiting Period			
				32kHz	44.1kHz	48kHz	
0	0	0	128/fs	4.0ms	2.9ms	2.7ms	(default)
0	0	1	256/fs	8.0ms	5.8ms	5.3ms	
0	1	0	512/fs	16.0ms	11.6ms	10.7ms	
0	1	1	1024/fs	32.0ms	23.2ms	21.3ms	
1	0	0	2048/fs	64.0ms	46.4ms	42.7ms	
1	0	1	4096/fs	128.0ms	92.9ms	85.3ms	
1	1	0	8192/fs	256.0ms	185.8ms	170.7ms	
1	1	1	16384/fs	512.0ms	371.5ms	341.3ms	

Table 14. ALC Recovery Operation Waiting Period

RGAIN1	RGAIN0	GAIN STEP		
0	0	1 step	0.375dB	(default)
0	1	2 step	0.750dB	
1	0	3 step	1.125dB	
1	1	4 step	1.500dB	

Table 15. ALC Recovery GAIN Step

IREF17-10bits IREF27-10bits	GAIN(0dB)	Step
F1H	+36.0	0.375dB
F0H	+35.625	
EFH	+35.25	
:	:	
E1H	+30.0(default)	
:	:	
92H	+0.375	
91H	0.0	
90H	-0.375	
:	:	
2H	-53.625	
1H	-54.0	
0H	MUTE	

Table 16. Reference Level at ALC Recovery operation for ALC1/2

RFST1 bit	RFST0 bit	Recovery Speed	
0	0	x 4	(default)
0	1	x 8	
1	0	x 16	
1	1	N/A	

Table 17. Fast Recovery Speed Setting (N/A: Not available)

3. Example of ALC Operation

Table 18 shows the example of the ALC setting.

Register Name	Comment	fs=44.1kHz	
		Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable
ZTM1-0	Zero crossing timeout period	11	23.2ms
WTM2-0	Recovery waiting period *WTM2-0 bits should be the same data as ZTM1-0 bits	100	46.4ms
IREF5-0	Maximum gain at recovery operation	28H	+6dB
LMAT1-0	Limiter ATT step	00	1 step
RGAIN1-0	Recovery GAIN step	00	1 step
RFST1-0	Fast Recovery Speed	00	4 times

Table 18. Example of the ALC Setting

The following registers should not be changed during the ALC operation.

- **LMTH1-0, LMAT1-0, WTM2-0, ZTM1-0, RGAIN1-0, REF7-0, ZELMN, RFST1-0**

■ Basic Operation Sequence Example

Condition:
Master mode (MSN pin = “H”), Audio Data Format = I2S (IIS pin = “H”), Clock source = X’tal (12.288MHz, 256fs), fs=48kHz, SIF input = SIF1 pin.

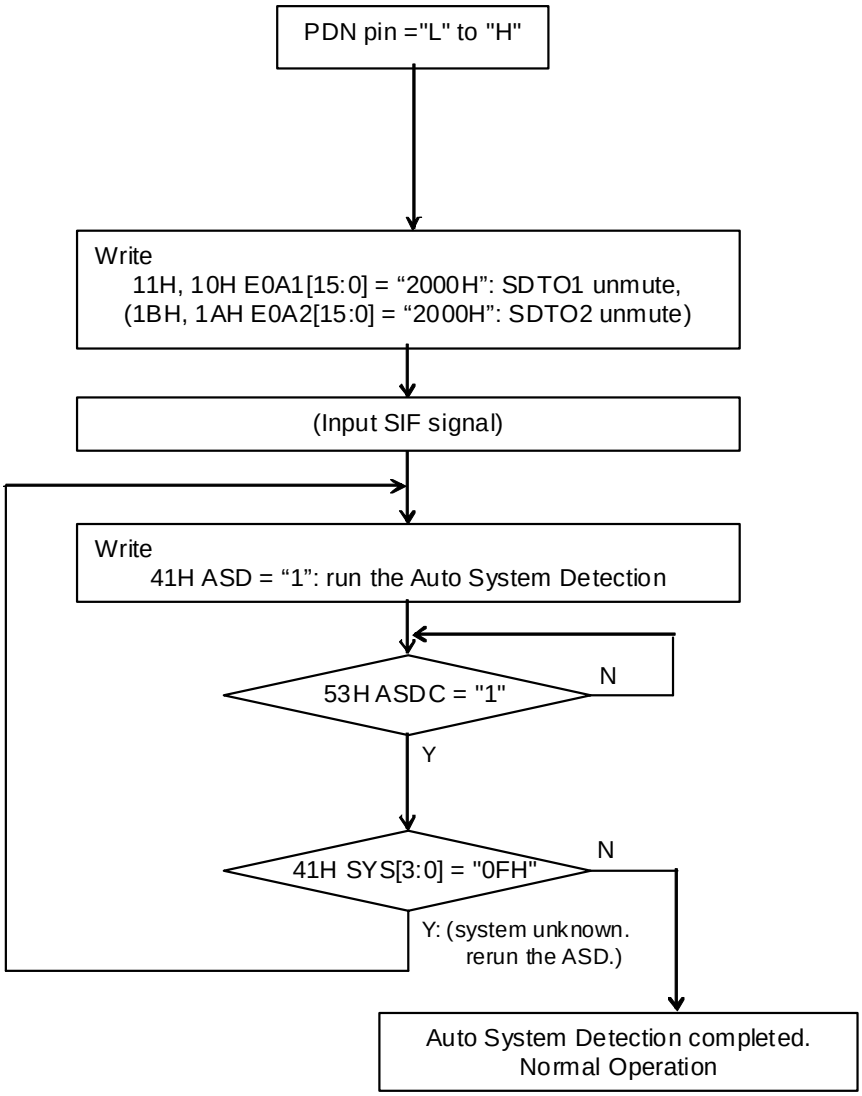


Figure 17. Basic Operation Sequence Example

■ Serial Control Interface

The AK4141 supports fast-mode I^2C-bus system (max: 400kHz).

1. Data transfer

All commands are preceded by a START condition. After the START condition, a slave address is sent. After the AK4141 recognizes the START condition, the device interfaced to the bus waits of the slave address to be transmitted over the SDA line. If the transmitted slave address matches an address for one of the devices, the designated slave device pulls the SDA line to LOW (ACKNOWLEDGE). The data transfer is always terminated by a STOP condition generated by the master device.

1-1. Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW except for the START and the STOP condition.

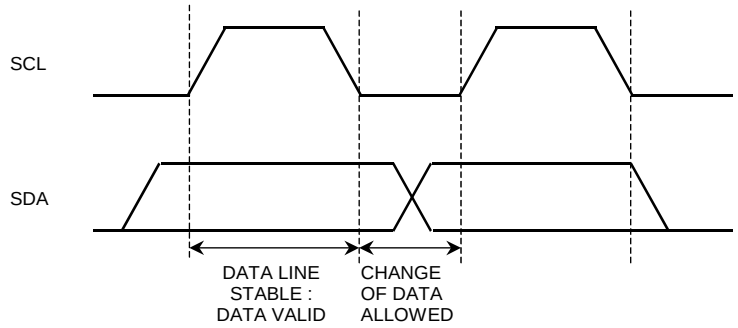


Figure 18. Data transfer

1-2. START and STOP condition

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. All sequences start from the START condition.
A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. All sequences end by the STOP condition.

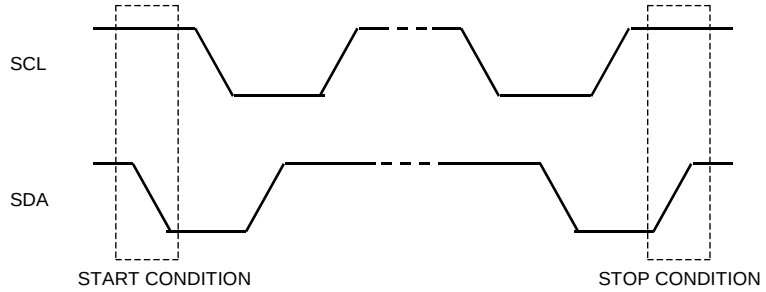


Figure 19. START and STOP conditions

1-3. ACKNOWLEDGE

ACKNOWLEDGE is a software convention used to indicate successful data transfers. The transmitter will release the SDA line (HIGH) after transmitting eight bits. The receiver must pull down the SDA line during the acknowledge clock pulse so that that it remains stable "L" during "H" period of this clock pulse. The AK4141 generates an acknowledge after each byte is received.
In read mode, the slave, the AK4141 transmits eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no STOP condition is generated by the master, the slave will continue transmitting data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the STOP condition.

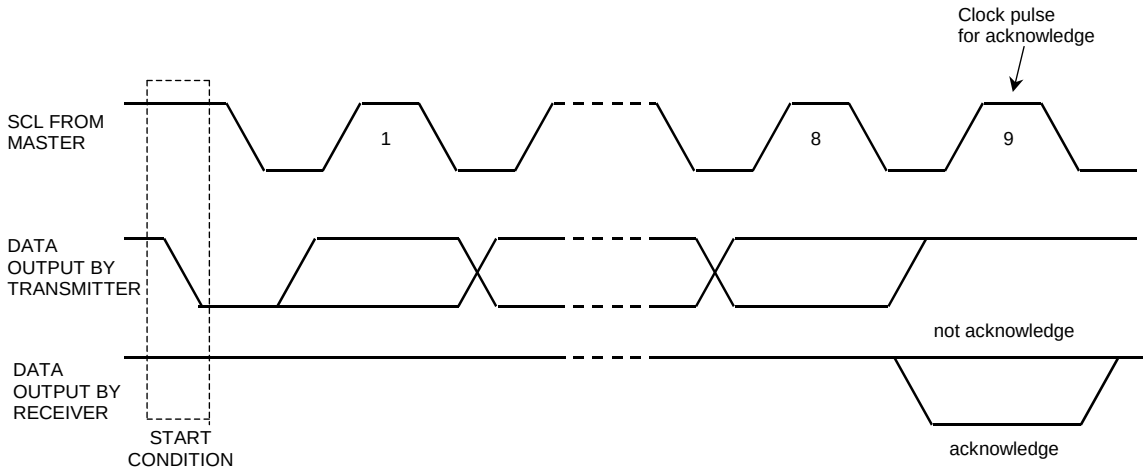


Figure 20. Acknowledge on the I^2C-bus

1-4. FIRST BYTE

The first byte, which includes seven bits of slave address and one bit of R/W bit, is sent after the START condition. If the transmitted slave address matches an address for one of the device, the receiver who has been addressed pulls down the SDA line.
The most significant four bits of the slave address are fixed as "1000". The next three bits are CAD1, CAD0 (device address bits) and "0". These three bits identify the specific device on the bus. The setting such as CAD/CAD0 = "11" is not available. The eighth bit (LSB) of the first byte (R/W bit) defines whether the master requests a write or read condition. A "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

1	0	0	0	CAD1	CAD0	0	R/W

(CAD1-CAD0 bits should match with CAD1-CAD0 pins)

Figure 21. The First Byte

CAD1 pin	CAD0 pin	R/W	First Byte
L	L	Write	80H
L	L	Read	81H
L	H	Write	84H
L	H	Read	85H
H	L	Write	88H
H	L	Read	89H
H	H	Write	N/A
H	H	Read	N/A

(N/A: Not available)

Table 19. The First Byte Setting

(2)-2. WRITE Operations

Set R/W bit = "0" for the WRITE operation of the AK4141.
After receipt the start condition and the first byte, the AK4141 generates an acknowledge, and awaits the second byte (register address). The second byte consists of the address for control registers of AK4141. The format is MSB first.

A7	A6	A5	A4	A3	A2	A1	A0

Figure 22. The Second Byte

After receipt the second byte, the AK4141 generates an acknowledge, and awaits the third byte. Those data after the second byte contain control data. The format is MSB first, 8bits.

D7	D6	D5	D4	D3	D2	D1	D0

Figure 23. Byte structure after the second byte

The AK4141 is capable of more than one byte write operation by one sequence.
After receipt of the third byte, the AK4141 generates an acknowledge, and awaits the next data again. The master can transmit more than one word instead of terminating the write cycle after the first data word is transferred. After the receipt of each data, the internal 8bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds TBDH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

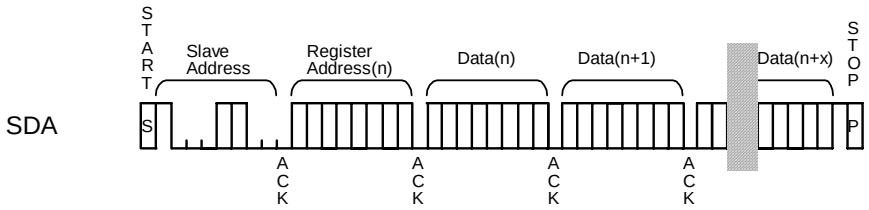


Figure 24. WRITE Operation

(2)-3. READ Operations

Set R/W bit = "1" for the READ operation of the AK4141.
After transmission of the data, the master can read next address's data by generating the acknowledge instead of terminating the write cycle after the receipt of the first data word. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceed TBDH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.
The AK4141 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.
ADC/DAC part register can not be read.

(2)-3-1. CURRENT ADDRESS READ

The AK4141 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address "n", the next CURRENT READ operation would access data from the address "n+1".
After receipt of the slave address with R/W bit set to "1", the AK4141 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generate the stop condition, the AK4141 discontinues transmission

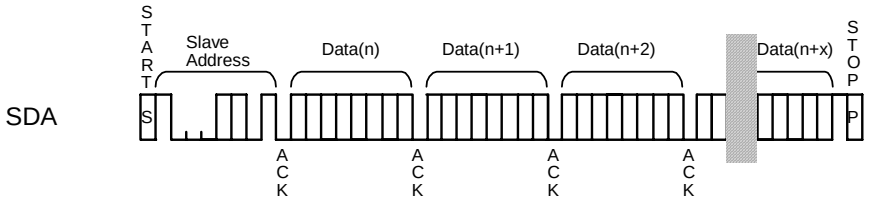


Figure 25. CURRENT ADDRESS READ

(2)-3-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation.
The master issues the start condition, slave address(R/W="0") and then the register address to read. After the register address's acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4141 generates an acknowledge, 1byte data and increments the internal address counter by 1. If the master does not generate an acknowledge but generate the stop condition, the AK4141 discontinues transmission.

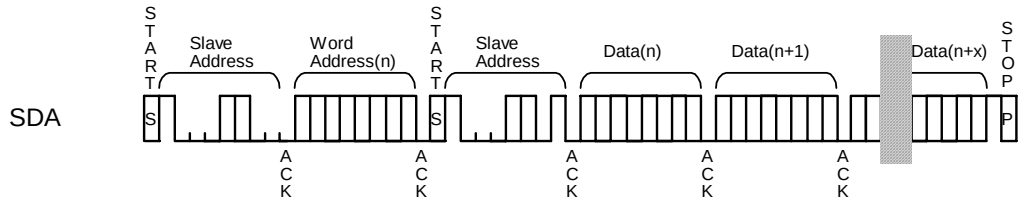


Figure 26. RANDOM READ

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
General Control									
00H	Power Management	PWDT	PWSR	PWOS	PWDE	AFEM1	0	ROLL	RSTN
01H	Clock Control	MCKE	MCKD	FS[1:0]		0	CKS[2:0]		
02H	Audio Data Format	TDM	0	IDIF[1:0]		0			ODIF
Switch									
03H	Switch Matrix 0	BPSR	SWSR	SWCK	SWSF	SMUT3	SMUT2	SMUT1	SMUTT
04H	Switch Matrix 1	V	DIT[2:0]			DIT16	SD1[2:0]		
05H	Switch Matrix 2	0	SD2[2:0]			0	SD3[2:0]		
Prescale									
06H	Decoder Prescale	GSEL2	GSEL1	0	DPRE[4:0]				
07H	Input 1 Prescale	0			I1PRE[4:0]				
08H	Input 2 Prescale	0			I2PRE[4:0]				
09H	Input 3 Prescale	0			I3PRE[4:0]				
0AH	Input 4 Prescale	0			I4PRE[4:0]				
0BH	SRC Prescale	0			SPRE[4:0]				
3D Enhancement									
0CH	FIL3 Coefficient 0	F3A1[7:0]							
0DH	FIL3 Coefficient 1	F3AS1	F3BP1	F3A1[13:8]					
0EH	FIL3 Coefficient 2	F3B1[7:0]							
0FH	FIL3 Coefficient 3	0		F3B1[13:8]					
10H	EQ0-efficient 0	E0A1[7:0]							
11H	EQ0-efficient 1	E0A1[15:8]							
12H	EQ0-efficient 2	E0B1[7:0]							
13H	EQ0-efficient 3	GN1[1:0]		E0B1[13:8]					
14H	EQ0-efficient 4	E0C1[7:0]							
15H	EQ0-efficient 5	E0C1[15:8]							
16H	FIL3 Coefficient 0	F3A2[7:0]							
17H	FIL3 Coefficient 1	F3AS2	F3BP2	F3A2[13:8]					
18H	FIL3 Coefficient 2	F3B2[7:0]							
19H	FIL3 Coefficient 3	0		F3B2[13:8]					
1AH	EQ0-efficient 0	E0A2[7:0]							
1BH	EQ0-efficient 1	E0A2[15:8]							
1CH	EQ0-efficient 2	E0B2[7:0]							
1DH	EQ0-efficient 3	GN2[1:0]		E0B2[13:8]					
1EH	EQ0-efficient 4	E0C2[7:0]							
1FH	EQ0-efficient 5	E0C2[15:8]							
EQ									
20H	EQ1 Control 250Hz/100Hz	EQB1[3:0]				EQA1[3:0]			
21H	EQ1 Control 3.5kHz/1kHz	EQD1[3:0]				EQC1[3:0]			
22H	EQ1 Control 10kHz	EQ1	0			EQE1[3:0]			
23H	EQ2 Control 250Hz/100Hz	EQB2[3:0]				EQA2[3:0]			
24H	EQ2 Control 3.5kHz/1kHz	EQD2[3:0]				EQC2[3:0]			
25H	EQ2 Control 10kHz	EQ2	0			EQE2[3:0]			
ALC									
26H	Timer Select1	0	WTM1[2:0]			ZTM1[1:0]		RFST1[1:0]	
27H	ALC1 Mode Control 1	ALC1	ZELMN1	RGAIN1[1:0]		LMAT1[1:0]		LMTH1[1:0]	
28H	ALC1 Mode Control 2	IREF1[7:0]							
29H	Timer Select2	0	WTM2[2:0]			ZTM2[1:0]		RFST2[1:0]	
27H	ALC2 Mode Control 1	ALC2	ZELMN2	RGAIN2[1:0]		LMAT2[1:0]		LMTH2[1:0]	
2BH	ALC2 Mode Control 2	IREF2[7:0]							

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
Balance									
2CH	Balance Mode Control	0							BMOD
2DH	Balance 1 Control	BAL1[7:0]							
2EH	Balance 2 Control	BAL2[7:0]							
Volume									
2FH	Main Volume 1 Control	VOL1[7:0]							
30H	Main Volume 2 Control	VOL2[7:0]							
DIT C bit									
31H	Channel Status 1	0	CS[27:24]				CS3	CS2	CS1
32H	Channel Status 2	0				CS[41:40]		CS[29:28]	
33H	Channel Status 3	CS[15:8]							
34H	Channel Status 4	CS[39:36]				CS[35:33]			CS32
Decoder									
40H	SIF AGC Manual Control	AGOFF	0	IFVOL[5:0]					
41H	System Select	0			ASD	SYS[3:0]			
42H	Standard Select	0			ID[1:0]		STD[2:0]		
43H	Sample Rate	0						DECFS[1:0]	
44H	FM/AM Demod Control	0	DM1LP[2]	DM1DV[2]	DM1LP[1:0]		DM1MD	DM1DV[1:0]	
45H	Demod 1 Carrier Freq Ctrl 1	DM1F[15:8]							
46H	Demod 1 Carrier Freq Ctrl 0	DM1F[7:0]							
47H	FM/DQPSK Dem Ctrl	0			DM2LP[1:0]		DM2MD	0	
48H	Demod 2 Carrier Freq Ctrl 1	DM2F[15:8]							
49H	Demod 2 Carrier Freq Ctrl 0	DM2F[7:0]							
4AH	Decoder Output Control	LOR	ROL	LRSM	AUTO	LSEL[1:0]		RSEL[1:0]	
4BH	Audio Mode Detect	0						AMOD[1:0]	
4CH	Pilot PLL Status	0							LOCK
4DH	NICAM Error Rate 1	NERR[15:8]							
4EH	NICAM Error Rate 0	NERR[7:0]							
4FH	NICAM Control Bits 1	NIAD[10:3]							
50H	NICAM Control Bits 0	NIAD[2:0]			NICT[4:0]				
51H	SIF AGC Control	AGAT[3:0]				AGDC[3:0]			
52H	AGC Control for AM	AMAT[3:0]				AMDC[3:0]			
53H	Status	ASDC	BI	IMONO	MONO	SNDST[1:0]		C2DET	C1DET
54H	Status Pin Control	0					ASTAT	STAP	STAE
55H	A/D headroom	0					HDRM[2:0]		
56H	AGC Freeze	0							AGFRZ
57H	Stereo Carrier Search Ctrl	0				CHMD[1:0]		SREN[1:0]	
58H	Stereo Carrier Search Result	0	SRIND	SRCMP	SRST	SRRSL[3:0]			
59H	Audio Output Result	LOR	ROL	LRSUM	0	LRSL[1:0]		RRSL[1:0]	
5AH	Mute Control / Status	0	AAOMT	ASDMT	LMT	RMT	MANMT	MUTEL	MUTER
5BH	Auto System Detect Control	0				A6M5	A4M5[2:0]		
5CH	Decoder AVC	0			DATK[1:0]		DDEC[1:0]		AVCE
5DH	Level Prescaler Control	0							PRECTL
5EH	Prescaler L	PREL[7:0]							
5FH	Prescaler R	PRER[7:0]							
60H	Manual Output Level L	LEVL[7:0]							
61H	Manual Output Level R	LEVR[7:0]							

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
62H	Carrier 1 Average Frequency 1	CR1F[15:8]							
63H	Carrier 1 Average Frequency 0	CR1F[7:0]							
64H	Carrier 1 Phase Noise 1	CR1P[15:8]							
65H	Carrier 1 Phase Noise 0	CR1P[7:0]							
66H	Carrier 1 Average Magnitude 1	CR1M[15:8]							
67H	Carrier 1 Average Magnitude 0	CR1M[7:0]							
68H	Carrier 1 Magnitude Noise 1	CR1N[15:8]							
69H	Carrier 1 Magnitude Noise 0	CR1N[7:0]							
6AH	Carrier 1 Signal Quality 1	CR1Q[15:8]							
6BH	Carrier 1 Signal Quality 0	CR1Q[7:0]							
6CH	Carrier 2 Average Frequency 1	CR2F[15:8]							
6DH	Carrier 2 Average Frequency 0	CR2F[7:0]							
6EH	Carrier 2 Average Magnitude 1	CR2M[15:8]							
6FH	Carrier 2 Average Magnitude 0	CR2M[7:0]							
70H	Carrier 2 Magnitude Noise 1	CR2N[15:8]							
71H	Carrier 2 Magnitude Noise 0	CR2N[7:0]							
72H	Carrier 2 Signal Quality 1	CR2Q[15:8]							
73H	Carrier 2 Signal Quality 0	CR2Q[7:0]							
74H	Pilot Magnitude	PLTM[7:0]							
75H	FM Subcarrier Magnitude	SUBM[7:0]							
76H	FM Subcarrier Noise	SUBN[7:0]							
77H	N/A	00H							
78H	N/A	00H							
79H	N/A	00H							
7AH	N/A	00H							
7BH	Carrier 1 Quality Threshold High	C1QTH[7:0]							
7CH	Carrier 1 Quality Threshold Low	C1QTL[7:0]							
7DH	Carrier 2 Quality Threshold High	C2QTH[7:0]							
7EH	Carrier 2 Quality Threshold Low	C2QTL[7:0]							
7FH	Carrier 1 Phase Noise Threshold High	C1PTH[7:0]							
80H	Carrier 1 Phase Noise Threshold Low	C1PTL[7:0]							
81H	FM Sub Magnitude Threshold High	FSMTH[7:0]							
82H	FM Sub Magnitude Threshold Low	FSMTL[7:0]							
83H	FM Sub Noise Threshold High	FSNTH[7:0]							
84H	FM Sub Noise Threshold Low	FSNTL[7:0]							
85H	NCM Err Rate Threshold High	NERTH[7:0]							
86H	NCM Err Rate Threshold Low	NERTL[7:0]							
87H	N/A	00H							
88H	N/A	00H							
89H	N/A	00H							
8AH	N/A	00H							
8BH	Carrier Magnitude ASD Threshold	ASDMT[7:0]							
8CH	Carrier Freq ASD Threshold	ASDFT[7:0]							
8DH	Carrier FM Quality ASD Threshold	ASQT[7:0]							
8EH	Carrier AM Noise ASD Threshold	AANT[7:0]							
8FH	NICAM Noise ASD Threshold	ANNT[7:0]							
90H	NICAM Noise High	NICN[15:8]							
91H	NICAM Noise Low	NICN[7:0]							
92H	Carrier FM Quality SCS Threshold	SQLT[7:0]							
93H	NICAM Noise SCS Threshold	SNST[7:0]							
94H	AVC Level Threshold High	AVCH[7:0]							
95H	AVC Level Threshold Low	AVCL[7:0]							

Note:
For addresses from 96H ~ 1FH, data must not be written.
When PDN pin goes "L", the registers are initialized to their default values.
When RSTN bit goes "0", the only internal timing is reset and the registers are not initialized to their default values.
The bits shown as "0" should be written "0".

■ Register Definitions

General Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	PWDT	PWSR	PWOS	PWDE	AFEM1	0	ROLL	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	0	0	0	1

RSTN: Timing Reset Control
0: Timing Reset
1: Normal Operation (default)

ROLL: Roll Over Address Control
0: roll-over to 00H from 61H and 95H (default)
1: roll-over to 00H from 95H but not from 61H.

AFEM[1]: AFE Mode 1
Write "1" into this bit.
0: SIF HPF ON (default)
1: SIF HPF OFF

PWDE: Stereo Decoder Power Control
0: Power down
1: Power up (default)

PWOS: X'tal Oscillator Power Control
0: Power down
1: Power up (default)

PWSR: SRC Power Control
0: Power down
1: Power up (default)

PWDT: DIT Power Control
0: Power down
1: Power up (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Clock Control	MCKE	MCKD	FS[1:0]		0	CKS[2:0]		
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

CKS[2:0]

CKS1 bit is ORed with the MSN pin. CKS0 bit is ORed with the MSN pin.

CKS[2:0]	Master/Slave
00	Slave (default)
01	Master 128fs
02	Master 192fs
03	Master 256fs
04	Master 384fs
05	Master 512fs
06	Master 768fs
07	Master 1024fs

Table 20. Master/Slave

FS[1:0]: Sampling Rate Control

FS[1:0] bits should be changed when the RSTN bit = "L"

FS[1:0]	Sample Rate
00	48kHz (default)
01	32kHz
02	44.1kHz
03	reserved

Table 21. Sample Rate

MCKD/MCKE: Master clock output control

MCKD bit	MCKE bit	Sample Rate
0	0	Outputs "L" (default)
0	1	Outputs X'tal (or MCKI) frequency x 1/4.
1	0	Outputs X'tal (or MCKI) frequency x 1/2.
1	1	Outputs X'tal (or MCKI) frequency.

Note: MCKO≤512fs

Table 22. Sample Rate

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Audio Data Format	TDM	0	IDIF[1:0]		0			ODIF
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	0	0	0	0

ODIF: Output Data Format
ODIF bit is ORed with IIS pin.
0: 24bit Left Justified (default)
1: 24/16bit I2S

IDIF[1:0]: Input Data Format
IDIF0 bit is ORed with IIS pin.
00: 16bit Right Justified
01: 24bit Right Justified
02: 24bit Left Justified (default)
03: 24/16bit I2S

TDM: TDM mode enable
0: Normal Data Format Mode (default)
1: TDM Data Format Mode

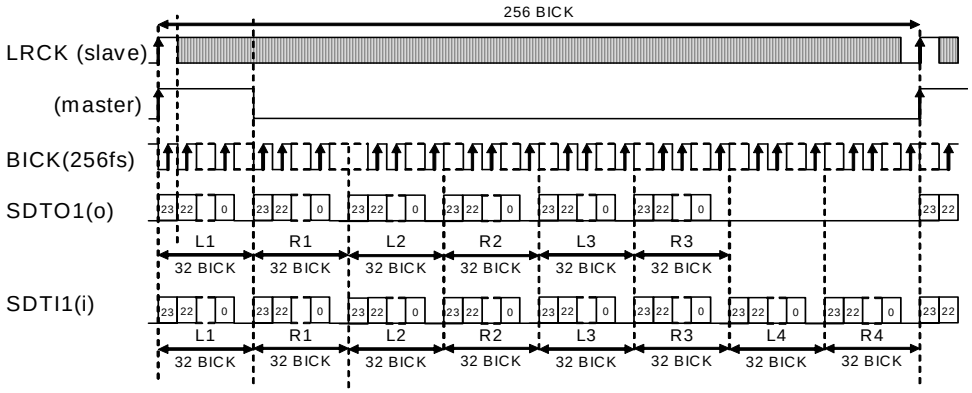


Figure 27. TDM MSB Justified Timing

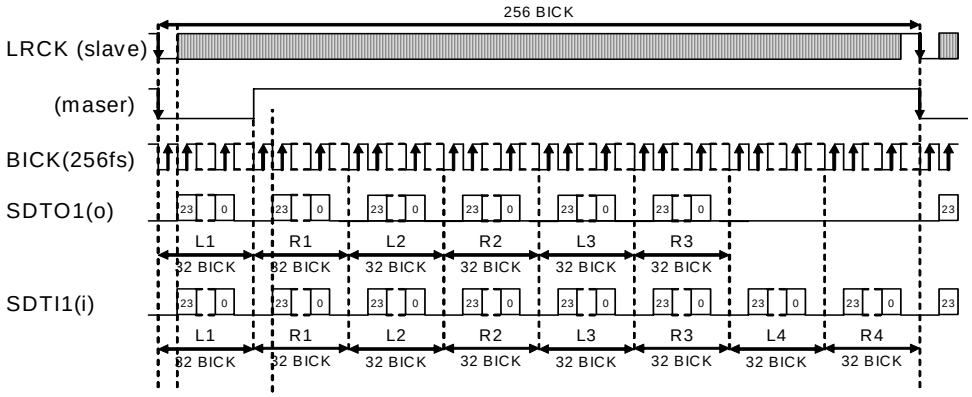


Figure 28. TDM IIS Timing

Switch

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Switch Matrix 0	BPSR	SWSR	SWCK	SWSF	SMUT3	SMUT2	SMUT1	SMUTT
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MUTET: DIT Audio Data Soft Mute Control
0: Unmute (default)
1: Soft Mute

MUTE1: SDTO1 Soft Mute Control
0: Unmute (default)
1: Soft Mute

MUTE2: SDTO2 Soft Mute Control
0: Unmute (default)
1: Soft Mute

MUTE3: SDTO3 Soft Mute Control
0: Unmute (default)
1: Soft Mute

SWSF: SIF Input Control
0: SIF1 (default)
1: SIF2

SWCK: MCLK/X'tal Control
0: X'tal (default)
1: MCLK

SWSR: SRC Input Control
0: SDTI4 (default)
1: SDTI5

BPSR: SRC Bypass
0: SRC Mode (default)
1: SRC Bypass Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Switch Matrix 1	V	DIT[2:0]			0	SD1[2:0]		
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SD1[2:0]: SDTO1 Source Data Control
- 00: Decoder (default)
- 01: SDTI1
- 02: SDRI2
- 03: SDRI3
- 04: SDRI4
- 05: SRC
- 06: reserved
- 07: Mute

DIT[2:0]: DIT Source Data Control
- 00: Decoder (default)
- 01: SDTI1
- 02: SDRI2
- 03: SDRI3
- 04: SDRI4
- 05: SRC
- 06: TXIN (TX through)
- 07: Mute

V: DIT Validity bit Control
- 0: V bit = "0" (default)
- 1: V bit = "1"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Switch Matrix 2	0	SD2[2:0]			0	SD3[2:0]		
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SD2[2:0]: SDTO2 Source Data Control
- 00: Decoder (default)
- 01: SDTI1
- 02: SDRI2
- 03: SDRI3
- 04: SDRI4
- 05: SRC
- 06: reserved
- 07: Mute

SD3[2:0]: SDTO3 Source Data Control
- 00: Decoder (default)
- 01: SDTI1
- 02: SDRI2
- 03: SDRI3
- 04: SDRI4
- 05: SRC
- 06: reserved
- 07: Mute

Prescale

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Decoder Prescale	GSEL2	GSEL1	0	DPRE[4:0]				
07H	Input 1 Prescale	0			I1PRE[4:0]				
08H	Input 2 Prescale	0			I2PRE[4:0]				
09H	Input 3 Prescale	0			I3PRE[4:0]				
0AH	Input 4 Prescale	0			I4PRE[4:0]				
0BH	SRC Prescale	0			SPRE[4:0]				
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	1

DPRE[4:0]: Decoder Prescale
I1PRE[4:0]: SDTI1 Prescale
I2PRE[4:0]: SDTI2 Prescale
I3PRE[4:0]: SDTI3 Prescale
I4PRE[4:0]: SDTI4 Prescale
SPRE[4:0]: SRC Prescale

1F: +18dB
1E: +17dB
…
0E: +1dB
0D: 0dB (default)
…
01: -12dB
00: Mute

GSEL2
0 : SIF2 high gain mode S2D-Gain=7.5dB(default)
1 : SIF2 low gain mode S2D-Gain=4.5dB

GSEL1
0 : SIF1 high gain mode S2D-Gain=7.5dB(default)
1 : SIF1 low gain mode S2D-Gain=4.5dB

3D Enhancement 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	FIL3 Coefficient 0	F3A1[7:0]							
0DH	FIL3 Coefficient 1	F3AS1	F3BP1	F3A1[13:8]					
0EH	FIL3 Coefficient 2	F3B1[7:0]							
0FH	FIL3 Coefficient 3	0		F3B1[13:8]					
10H	EQ0-efficient 0	E0A1[7:0]							
11H	EQ0-efficient 1	E0A1[15:8]							
12H	EQ0-efficient 2	E0B1[7:0]							
13H	EQ0-efficient 3	GN1[1:0]		E0B1[13:8]					
14H	EQ0-efficient 4	E0C1[7:0]							
15H	EQ0-efficient 5	E0C1[15:8]							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

F3A1[13:0], F3B1[13-0]: FIL3 (Stereo Separation Emphasis Filter) Coefficient (14bit x 2)
Default: "0000H"

F3BP1: FIL3 (Stereo Separation Emphasis Filter) Bypass
0: ON
1: Bypass (default)

F3AS1: FIL3 (Stereo Separation Emphasis Filter) Select 1
0: LPF (default)
1: HPF

E0A1[15:0], E0B1[13:0], E0C1[15:0]: EQ (Gain Compensation Filter) Coefficient (14bit x 2 + 16bit x 1)
default: "2000H"

GN1[1:0]: Additional Gain Select 1
0: 0dB (default)
1: +12dB
2: +24dB
3: +24dB

3D Enhancement 2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	FIL3 Coefficient 0	F3A2[7:0]							
17H	FIL3 Coefficient 1	F3AS2	F3BP2	F3A2[13:8]					
18H	FIL3 Coefficient 2	F3B2[7:0]							
19H	FIL3 Coefficient 3	0		F3B2[13:8]					
1AH	EQ0-efficient 0	E0A2[7:0]							
1BH	EQ0-efficient 1	E0A2[15:8]							
1CH	EQ0-efficient 2	E0B2[7:0]							
1DH	EQ0-efficient 3	GN2[1:0]		E0B2[13:8]					
1EH	EQ0-efficient 4	E0C2[7:0]							
1FH	EQ0-efficient 5	E0C2[15:8]							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

F3A2[13:0], F3B2[13-0]: FIL3 (Stereo Separation Emphasis Filter) Coefficient (14bit x 2)
Default: “0000H”

F3BP2: FIL3 (Stereo Separation Emphasis Filter) Bypass
0: ON
1: Bypass (default)

F3AS2: FIL3 (Stereo Separation Emphasis Filter) Select 2
0: LPF (default)
1: HPF

E0A2[15:0], E0B2[13:0], E0C2[15:0]: EQ (Gain Compensation Filter) Coefficient (14bit x 2 + 16bit x 1)
default: “2000H”

GN2[1:0]: Additional Gain Select 2
0: 0dB (default)
1: +12dB
2: +24dB
3: +24dB

Equalizer 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
20H	EQ Control 250Hz/100Hz	EQB1[3:0]				EQA1[3:0]			
21H	EQ Control 3.5kHz/1kHz	EQD1[3:0]				EQC1[3:0]			
22H	EQ Control 10kHz	EQ1	0			EQE1[3:0]			
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	1	0	0	0

EQA1[3:0]: Select the boost level of 100Hz
EQB1[3:0]: Select the boost level of 250Hz
EQC1[3:0]: Select the boost level of 1kHz
EQD1[3:0]: Select the boost level of 3.5kHz
EQE1[3:0]: Select the boost level of 10kHz

EQ1: Equalizer1 Enable
0: Disable
1: Enable (default)

Equalizer 2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
23H	EQ Control 250Hz/100Hz	EQB2[3:0]				EQA2[3:0]			
24H	EQ Control 3.5kHz/1kHz	EQD2[3:0]				EQC2[3:0]			
25H	EQ Contro2 10kHz	EQ2	0			EQE2[3:0]			
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	1	0	0	0

EQA2[3:0]: Select the boost level of 100Hz
EQB2[3:0]: Select the boost level of 250Hz
EQC2[3:0]: Select the boost level of 1kHz
EQD2[3:0]: Select the boost level of 3.5kHz
EQE2[3:0]: Select the boost level of 10kHz

EQ2: Equalizer2 Enable
0: Disable
1: Enable (default)

EQx1[3:0], EQx2[3:0]	Boost amount	
0H	+12.0dB	
1H	+10.5dB	
2H	+9.0dB	
3H	+7.5dB	
:	:	
8H	0dB	(default)
:	:	
DH	−7.5dB	
EH	−9.0dB	
FH	−10.5dB	

Table 23. Boost amount of 5 Band Equalizer

ALC1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
26H	Timer Select	0	WTM1[2:0]			ZTM1[1:0]		RFST1[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

WTM1[2:0]: ALC1 Recovery Waiting Period

WTM1[2-0] bits set a period of recovery operation when no limiter operation occurs during ALC1 operation. Default= "000" (128/fs).

WTM12	WTM11	WTM10	ALC Recovery Operation Waiting Period				
				32kHz	44.1kHz	48kHz	
0	0	0	128/fs	4.0ms	2.9ms	2.7ms	(default)
0	0	1	256/fs	8.0ms	5.8ms	5.3ms	
0	1	0	512/fs	16.0ms	11.6ms	10.7ms	
0	1	1	1024/fs	32.0ms	23.2ms	21.3ms	
1	0	0	2048/fs	64.0ms	46.4ms	42.7ms	
1	0	1	4096/fs	128.0ms	92.9ms	85.3ms	
1	1	0	8192/fs	256.0ms	185.8ms	170.7ms	
1	1	1	16384/fs	512.0ms	371.5ms	341.3ms	

Table 24. ALC Recovery Operation Waiting Period

ZTM1[1:0]: ALC1 Zero Crossing Timeout Period

At ALC1 recovery operation, the gain changes only when zero crossing or timeout. Default= "00" (128/fs).

ZTM11	ZTM10	ALC1 Zero Crossing Timeout Period				
			32kHz	44.1kHz	48kHz	
0	0	128/fs	4.0ms	2.9ms	2.7ms	(default)
0	1	256/fs	8.0ms	5.8ms	5.3ms	
1	0	512/fs	16.0ms	11.6ms	10.7ms	
1	1	1024/fs	32.0ms	23.2ms	21.3ms	

Table 25. ALC1 Zero Crossing Timeout Period

RFST1[1:0]: ALC1 Fast Recovery Speed

Default: "00"(x 4 speed)

RFST11 bit	RFST10 bit	Fast Recovery Speed	
0	0	x 4	(default)
0	1	x 8	
1	0	x 16	
1	1	N/A	

Table 26. ALC1 Fast Recovery Speed (N/A: NOT available)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
27H	ALC Mode Control 1	ALC1	ZELMN1	RGAIN1[1:0]		LMAT1[1:0]		LMTH1[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LMTH1[1:0]: ALC1 Limiter Detection Level / Recovery Waiting Counter Reset Level
Default: "00"

LMTH11	LMTH10	Limiter Detection Level	Recovery Waiting Counter Reset Level	
0	0	ALC Output ≥ –2.5dBFS	–2.5dBFS > ALC Output ≥ –4.1dBFS	(default)
0	1	ALC Output ≥ –4.1dBFS	–4.1dBFS > ALC Output ≥ –6.0dBFS	
1	0	ALC Output ≥ –6.0dBFS	–6.0dBFS > ALC Output ≥ –8.5dBFS	
1	1	ALC Output ≥ –8.5dBFS	–8.5dBFS > ALC Output ≥ –12dBFS	

Table 27. ALC1 Limiter Detection Level / Recovery Waiting Counter Reset Level

LMAT1[1:0]: ALC1 Limiter ATT Step
Default: "00"

LMAT11	LMAT10	ALC1 Limiter ATT Step				
		ALC1 Output ≥ LMTH	ALC1 Output ≥ FS	ALC1 Output ≥ FS + 6dB	ALC1 Output ≥ FS + 12dB	
0	0	1	1	1	1	(default)
0	1	2	2	2	2	
1	0	2	4	4	8	
1	1	1	2	4	8	

Table 28. ALC1 Limiter ATT Step

RGAIN1[1:0]: ALC1 Recovery GAIN Step
Default: "00"

RGAIN11	RGAIN10	GAIN STEP		
0	0	1 step	0.375dB	(default)
0	1	2 step	0.750dB	
1	0	3 step	1.125dB	
1	1	4 step	1.500dB	

Table 29. ALC1 Recovery GAIN Step

ZELMN1: Enable zero crossing detection at ALC1 Limiter operation
0: Enable (default)
1: Disable

ALC1: ALC1 Enable
0: ALC Disable (default)
1: ALC Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
28H	ALC Mode Control 2	IREF1[7:0]							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	1	0	0	0	1

IREF1[7-0]: Reference value at ALC1 Recovery Operation
0.375dB step, 242 Level. Default: "91H" (0.0dB)

IREF1[7-0]bits	GAIN(0dB)	Step
F1H	+36.0	0.375dB
F0H	+35.625	
EFH	+35.25	
:	:	
C5H	+19.5	
:	:	
92H	+0.375	
91H	0.0 (default)	
90H	-0.375	
:	:	
02H	-53.625	
01H	-54.0	
00H	MUTE	

Table 30. Reference value at ALC1 Recovery Operation

ALC2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
29H	Timer Select	0	WTM2[2:0]			ZTM2[1:0]		RFST2[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

WTM2[2:0]: ALC2 Recovery Waiting Period

WTM2[2-0] bits set a period of recovery operation when any limiter operation does not occur during ALC2 operation. Default= "000" (128/fs).

WTM22	WTM21	WTM20	ALC Recovery Operation Waiting Period				
				32kHz	44.1kHz	48kHz	
0	0	0	128/fs	4.0ms	2.9ms	2.7ms	(default)
0	0	1	256/fs	8.0ms	5.8ms	5.3ms	
0	1	0	512/fs	16.0ms	11.6ms	10.7ms	
0	1	1	1024/fs	32.0ms	23.2ms	21.3ms	
1	0	0	2048/fs	64.0ms	46.4ms	42.7ms	
1	0	1	4096/fs	128.0ms	92.9ms	85.3ms	
1	1	0	8192/fs	256.0ms	185.8ms	170.7ms	
1	1	1	16384/fs	512.0ms	371.5ms	341.3ms	

Table 31. ALC2 Recovery Waiting Period

ZTM2[1:0]: ALC2 Zero Crossing Timeout Period

At ALC2 recovery operation, the gain changes only when zero crossing or timeout. Default= "00" (128/fs).

ZTM21	ZTM20	ALC2 Zero Crossing Timeout Period				
			32kHz	44.1kHz	48kHz	
0	0	128/fs	4.0ms	2.9ms	2.7ms	(default)
0	1	256/fs	8.0ms	5.8ms	5.3ms	
1	0	512/fs	16.0ms	11.6ms	10.7ms	
1	1	1024/fs	32.0ms	23.2ms	21.3ms	

Table 32. ALC2 Zero Crossing Timeout Period

RFST2[1:0]: ALC2 Fast Recovery Speed

Default: "00"(x 4 speed)

RFST21 bit	RFST20 bit	Fast Recovery Speed	
0	0	x 4	(default)
0	1	x 8	
1	0	x 16	
1	1	N/A	

Table 33. ALC2 Fast Recovery Speed (N/A: Not available)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2AH	ALC Mode Control 1	ALC2	ZELMN2	RGAIN2[1:0]		LMAT2[1:0]		LMTH2[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LMTH2[1:0]: ALC2 Limiter Detection Level / Recovery Waiting Counter Reset Level
Default: "00"

LMTH21	LMTH20	Limiter Detection Level	Recovery Waiting Counter Reset Level	
0	0	ALC Output ≥ –2.5dBFS	–2.5dBFS > ALC Output ≥ –4.1dBFS	(default)
0	1	ALC Output ≥ –4.1dBFS	–4.1dBFS > ALC Output ≥ –6.0dBFS	
1	0	ALC Output ≥ –6.0dBFS	–6.0dBFS > ALC Output ≥ –8.5dBFS	
1	1	ALC Output ≥ –8.5dBFS	–8.5dBFS > ALC Output ≥ –12dBFS	

Table 34. ALC2 Limiter Detection Level / Recovery Waiting Counter Reset Level

LMAT2[1:0]: ALC2 Limiter ATT Step
Default: "00"

LMAT21	LMAT20	ALC2 Limiter ATT Step				
		ALC2 Output ≥ LMTH	ALC2 Output ≥ LMTH	ALC2 Output ≥ LMTH	ALC2 Output ≥ LMTH	
0	0	1	1	1	1	(default)
0	1	2	2	2	2	
1	0	2	4	4	8	
1	1	1	2	4	8	

Table 35. ALC2 Limiter ATT Step

RGAIN21[1:0]: ALC2 Recovery GAIN Step
Default: "00"

RGAIN21	RGAIN20	GAIN STEP		
0	0	1 step	0.375dB	(default)
0	1	2 step	0.750dB	
1	0	3 step	1.125dB	
1	1	4 step	1.500dB	

Table 36. ALC2 Recovery GAIN Step

ZELMN2: Enable zero crossing detection at ALC2 Limiter operation
0: Enable (default)
1: Disable

ALC2: ALC2 Enable
0: ALC Disable (default)
1: ALC Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2BH	ALC Mode Control 2	IREF2[7:0]							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	1	0	0	0	1

IREF2[7:0]: Reference value at ALC2 Recovery Operation
0.375dB step, 242 Level. Default: "91H" (0.0dB)

IREF2[7:0]bits	GAIN(0dB)	Step
F1H	+36.0	0.375dB
F0H	+35.625	
EFH	+35.25	
:	:	
C5H	+19.5	
:	:	
92H	+0.375	
91H	0.0 (default)	
90H	-0.375	
:	:	
2H	-53.625	
1H	-54.0	
0H	MUTE	

Table 37. Reference value at ALC2 Recovery Operation

Balance

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2CH	Balance Mode Control	0							BMODE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

BMODE: Balance Mode
0: Linear step
1: Log step (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2DH	Balance 1 Control	BAL1[7:0]							
2EH	Balance 2 Control	BAL2[7:0]							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BAL1[7:0]: Balance 1 Control
BAL2[7:0]: Balance 2 Control

Linear Mode
7F: L=mute, R=100%
7E: L=0.8%, R=100%
…
01: L=99.2%, R=100%
00: L=100%, R=100% (default)
FF: L=100%, R=99.2%
…
82: L=100%, R=0.8%
81: L=100%, R=Mute
Log Mode
7F: L=mute, R=0dB
7E: L=-126dB, R=0dB
…
01: L=-1dB, R=0dB
00: L=0dB, R=0dB (default)
FF: L=0dB, R=-1dB
…
81: L=0dB, R=-127dB
80: L=0dB, R=-Mute

Main Volume

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2FH	Main Volume 1 Control	VOL1[7:0]							
30H	Main Volume 2 Control	VOL2[7:0]							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	0

VOL1[7:0]: Main Volume 1 Control
VOL2[7:0]: Main Volume 2 Control

VOL1[7:0], VOL2[7:0]	Volume Gain	
00H	+12dB	
01H	+11.5dB	
02H	+11.0dB	
:	:	
17H	+0.5dB	
18H	0dB	(default)
19H	-0.5dB	
	:	
FEH	-115dB	
FFH	MUTE (-∞)	

Table 38. Main Volume Control 1/2

DIT C-bit control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
31H	Channel Status 1	0	CS[27:24]				CS3	CS2	CS1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	1	0

CS1
0: Audio (default)
1: Non-Audio

CS2
0: Copyright
1: Non-Copyright (default)

CS3
0: No Pre-emphasis (default)
1: 50/15μsec Pre-emphasis

CS24, 25, 26, 27: Sampling Frequency
0010: 22.05kHz
0000: 44.1kHz
0001: 88.2kHz
0011: 176.4kHz
0110: 24kHz
0100: 48kHz (default)
0101: 96kHz
0111: 192kHz
1100: 32kHz
1000: Sampling frequency is not indicated
1001: 768kHz
Others: reserved

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
32H	Channel Status 2	0				CS[41:40]		CS[29:28]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

CS28, 29: Clock Accuracy
00: Standard mode (default)
01: Variable pitch mode
10: High accuracy mode
11: Reserved

CS40, 41: CGMS-A
00: Copying is permitted without restriction (default)
01: Copying not be used
10: One generation of copies may be used
11: No copying is permitted

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
33H	Channel Status 3	CS[15:8]							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

CS8-15: Category code (refer IEC60958-3.)
00110000: Digital Audio Broadcast Reception in Europe (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
34H	Channel Status 4	CS[39:36]				CS[35:33]			CS32
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

CS32: Maximum word length
0: Maximum sample word length is 20 bits (default)
1: Maximum sample word length is 24 bits

CS33, 34, 35: Word length
If the bit32 (CS32 bit) = "1"
000: Word length not indicated (default)
100: 20 bit
010: 22 bit
001: 23 bit
101: 24 bit
011: 21 bit
If the bit32 (CS32 bit) = "0"
000: Word length not indicated (default)
100: 16 bit
010: 18 bit
001: 19 bit
101: 20 bit
011: 17 bit

CS36, 37, 38, 39:Original Sampling Frequency
1111: 44.1kHz
1110: 88.2kHz
1101: 22.05kHz
1100: 176.4kHz
1011: 48kHz
1010: 96kHz
1001: 24kHz
1000: 192kHz
0111: Reserved
0110: 8kHz
0101: 11.025kHz
0100: 12kHz
0011: 32kHz
0010: Reserved
0001: 16kHz
0000: Original Sampling frequency is not indicated (default)

All other C bits are fixed to "0".

Decoder

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
40H	SIF AGC Manual Control	AGOFF	0	IFVOL[5:0]					
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

AGOFF: AGC disable

AGOFF	AGC status	
0	Enabled	(default)
1	Disabled	

Table 39. AGC disable

IFVOL[5:0]: SIF volume control

These bits are ignored when AGOFF bit = "0". PGA-Gain = (52+IFVOL*2)/(75-IFVOL). The total gain of the system is the sum of IFVOL bits setting and GSEL1/GSEL2 bits setting.

IFVOL[5:0]	SIF Gain	
00H	-3.18dB	(default)
01H	-2.74dB	
02H	-2.30dB	
:	:	
2DH	+21.89dB	
2EH	+22.63dB	
2FH	+23.42dB	

Table 40. SIF volume control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
41H	System Select	0			ASD	SYS[3:0]			
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	1	1

ASD

Enable automatic system detection. ASD is initiated when a 1 is written to this bit. Automatically returns to 0 when ASD is complete.

ASD	Automatic system detection	
00H	Disabled	(default)
01H	Enabled	

Table 41. Automatic system detection

SYS[3:0]

TV system select. This register is overridden by automatic system detection when it is initiated. It Becomes read-only while ASD is enabled, but returns to R/W when ASD is completed. Note that if ASD cannot identify the system, SYS[3:0] will be set to 0xF and the decoder will be set to the FM-Stereo (Radio-Europe) mode.

SYS[3:0]	TV System	Sound Carrier Positions	Sound Modulation	
00H	B/G	5.5/5.7421875	FM-Stereo (A2)	
01H	B/G	5.5/5.85	FM-Mono/NICAM	
02H	L	6.5/5.85	AM-Mono/NICAM	
03H	I	6.0/6.552	FM-Mono/NICAM	
04H	D/K	6.5/6.2578125	FM-Stereo (A2, D/K1)	
05H	D/K	6.5/6.7421875	FM-Stereo (A2, D/K2)	
06H	D/K	6.5/5.7421875	FM-Stereo (A2, D/K3)	
07H	D/K	6.5/5.85	FM-Mono/NICAM (D/K, NICAM)	
08H	M/N	4.5/4.724212	FM-Stereo (A2)	
09H	M/N	4.5	FM-Stereo (EIA-J)	
0AH	M/N	4.5	N/A	
0BH	FM-Radio	4.5	FM-Stereo (Radio - US)	
0CH-0EH	FM-Radio	4.5	FM-Stereo (Radio - Europe)	
0FH	FM-Radio	4.5	Unknown/FM-Stereo (Radio - Europe)	(default)

Table 42. TV system select (N/A: NOT available) (N/A: Not available)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
42H	Standard Select	0			ID[1:0]		STD[2:0]		
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	1

ID[1:0]

ID detector mode. EIA-J and A2 may carry identification tones used to identify the transmitted audio mode: mono, stereo, or bilingual. This word determines the standard that the ID detector assumes the received audio to be in. A2 has two variations of the identification tone, A2 and A2M. Normally, the contents of this word are updated automatically to reflect the standard chosen in the system select (SYS[3:0]) register, but this word may also be overwritten manually.

ID[1:0]	ID Detector Mode	
00H	EIAJ	(default)
01H	A2	
02H	A2M	
03H	A2M	

Table 43. ID Detector Mode

STD[2:0]

Decoding standard select. Normally, the contents of this word are updated automatically to reflect the standard chosen in the system select (SYS[3:0]) register, but this word may also be overwritten manually.

STD[2:0]	Decoding Standard	
00H	reserved	
01H	reserved	
02H	reserved	
03H	EIA-J	
04H	A2	
05H	FM Radio (75μs)	
06H	FM Radio (50μs)	
07H	NICAM	(default)

Table 44. Decoding Standard

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
43H	Decoder Sample Rate							DECFS[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DECFS[1:0]	Decoder Sample Rate
00H	48kHz (default)
01H	32kHz
02H	44.1kHz
03H	reserved

Table 45. Sample Rate

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
44H	FM/AM Demod Control	0	DM1LP[2]	DM1DV[2]	DM1LP[1:0]		DM1MD	DM1DV[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DM1LP[2:0]

Demod 1 filter select. This word is ignored while ASD is running.

DM1LP[2:0]	Demod 1 Filter	
00H	50 kHz lowpass	(default)
01H	100 kHz lowpass	
02H	384 kHz lowpass	
03H	540kHz lowpass	
04H	200kHz lowpass	
05H	Reserved	
06H	Reserved	
07H	Reserved	

Table 46. Demod 1 Filter

DM1MD

Demod 1 FM/AM mode. This bit is ignored while ASD is running.

DM1MD	Demod 1 FM/AM Mode	
00H	FM	(default)
01H	AM	

Table 47. Automatic system detection

DM1DV [2:0]

Demod 1 maximum FM deviation. This word is ignored while ASD is running

DM1DV [2:0]	Demod 1 Maximum FM Deviation	
00H	50 kHz	(default)
01H	100 kHz	
02H	384 kHz	
03H	540 kHz	
04H	200 kHz	
05H	Reserved	
06H	Reserved	
07H	Reserved	

Table 48. Demod 1 Maximum FM Deviation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
45H	Dem1 Carrier Freq Ctrl 1	DM1F[15:8]							
46H	Dem1 Carrier Freq Ctrl 0	DM1F[7:0]							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DM1F[15:0]

Demod 1 carrier frequency. This word is ignored while ASD is running. This value represents the frequency shift required to bring the carrier to 0Hz, so it typically has a negative value. A positive value shifts the carrier up.

DM1F = -Fc/Fs x 2^{16} (in 2's complement)

Fc = Nominal frequency of carrier to be demodulated (in Hz)
Fs = Input sample rate (in Hz), see the Sample Rate Register table (Table 45) for the input sample rate that corresponds to the selected output sample rate. The Table 49 represents typical values, which is not meant to be restrictive. Any 16-bit value may be used as needed.

Standard Values for Fc	DM1F[15:0]	
	fs=48kHz/32kHz	fs=44.1kHz
4.5MHz	0xC180	0xBBF9
5.5MHz	0xB39C	0xACDB
6.0MHz	0xACAB	0xA54C
6.5MHz	0xA5B9	0x9DBD

Table 49. Demod 1 carrier frequency

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
47H	FM/DQPSK Dem Ctrl	0			DM2LP[1:0]		DM2MD	0	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DM2MD

Demod 2 FM/DQPSK mode. This bit is ignored while ASD is running.

DM2MD	Demod 2 FM/DQPSK Mode	
00H	FM	(default)
01H	DQPSK	

Table 50. Automatic system detection

DM2LP[1:0]

Demod 2 filter select. This word is ignored while ASD is running.

DM2LP[1:0]	Demod 2 Filter	
00H	50 kHz lowpass	(default)
01H	728kbit/s Root Raised Cosine 40% rolloff lowpass	
02H	728kbit/s Root Raised Cosine 100% rolloff lowpass	
03H	Reserved	

Table 51. Demod 2 Filter

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
48H	Dem2 Carrier Freq Ctrl 1	DM2F[15:8]							
49H	Dem2 Carrier Freq Ctrl 0	DM2F[7:0]							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DM2F[15:0]

Demod 2 carrier frequency. This word is ignored while ASD is running. This value represents the frequency shift required to bring the carrier to 0 Hz, so it typically has a negative value. A positive value shifts the carrier up.

DM2F = -Fc/Fs x 2^{16} (in 2's complement)

Fc = Nominal frequency of carrier to be demodulated (in Hz)
Fs = Input sample rate (in Hz), see the Sample Rate Register table for the input sample rate that corresponds to the selected output sample rate. The following table represents typical values, and is not meant to be restrictive. Any 16-bit value may be used as needed.

Standard Values for Fc	DM2F[15:0]		
	fs=48kHz/32kHz	fs=44.1kHz	
4.724212MHz	0xBE63	0xB895	(default)
5.7421875MHz	0xB03F	0xA932	
5.85MHz	0xAEC0	0xA791	
6.2578125MHz	0xA916	0xA166	
6.552MHz	0xA500	0x9CF4	
6.7421875MHz	0xA25C	0x9A14	

Table 52. Demod 2 carrier frequency

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
4AH	Decoder Output Control	LOR	ROL	LRSM	AUTO	LSEL[1:0]		RSEL[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	1	0	1

AUTO

Automatic audio output select enable. When it is enabled, the automatic output select monitors the signal conditions and outputs the appropriate audio signals continuously. When disabled, and in dual sound carrier mode, the applicable demodulator output is muted if the quality of the signal is too poor.

AUTO	Automatic audio output	
00H	Disabled	
01H	Enabled	(default)

Table 53. Automatic audio output

LSEL[1:0]

Left output select. When automatic audio output select is disabled, the left output will output a signal according to the value of this word. When AUTO is enabled, this word is used to determine the preferred output as shown in the Table 55.

Left Preferred Outputs for AUTO = "0"					
LSEL[1:0]	EIA-J	A2	NICAM	FM Radio	
00H	Mono	Mono	AMono	Mono	
01H	L	L	L	L	(default)
02H	A	A	A	Mono	
03H	B	B	B	L-R	

Table 54. Left Output for AUTO= "0"

Left Preferred Outputs for AUTO = "1" (in poor signal conditions, the output in parentheses is automatically selected)						
LSEL[1:0]	EIA-J, A2 (Stereo or Unknown), FM Radio	EIAJ, A2 (Mono)	EIA-J, A2 (Dual Mono)	NICAM (Stereo)	NICAM (Mono/ Data)	NICAM (Dual Mono)
00H	L (Mono)	Mono	A	L (AMono)	A (AMono)	A (AMono)
01H						
02H						
03H			B(A)			B (AMono)

Table 55. Left Output for AUTO= "1"

RSEL[1:0]

Right output select. When automatic audio output select is disabled, the right output will output a signal according to the value of this word. When AUTO is enabled, this word is used to determine the preferred output as shown in the Table 70.

Right Outputs for AUTO = "0"					
RSEL[1:0]	EIA-J	A2	NICAM	FM Radio	
00H	Mono	Mono	AMono	Mono	
01H	R	R	R	R	(default)
02H	A	A	A	Mono	
03H	B	B	B	L-R	

Table 56. Right Output for AUTO= "0"

Right Outputs for AUTO = "1" (in poor signal conditions, the output in parentheses is automatically selected)						
RSEL[1:0]	EIA-J, A2 (Stereo or Unknown), FM Radio	EIAJ, A2 (Mono)	EIA-J, A2 (Dual Mono)	NICAM (Stereo)	NICAM (Mono/ Data)	NICAM (Dual Mono)
00H	R(Mono)	Mono	A	R (AMono)	A (AMono)	A (AMono)
01H						
02H						
03H			B(A)			B (AMono)

Table 57. Right Output for AUTO= "1"

LRSM

Left and right summing mode. Provides capability to sum the left and right channels.

LRSM	Left / Right Outputs	
00H	Standard Mode Left and right outputs are unchanged.	(default)
01H	Summing Mode L = R = (LStndrd + RStndrd) / 2 LStndrd and RStndrd are defined as what the left and right outputs would be if LRSM were 0(inactive)	

Table 58. LSEL Definition

ROL

Right channel outputs left channel audio. Provides capability for the right channel to output the left channel audio.

ROL	RSEL Definition	
00H	Standard Definition (LSEL defined according to Table 54, Table 55)	(default)
01H	Left Channel Definition (LSEL defined according to Table 56, Table 57)	

Table 59. LSEL Definition

LOR

Left channel outputs right channel audio. Provides capability for the left channel to output the right channel audio.

LOR	LSEL Definition	
00H	Standard Definition (LSEL defined according to Table 56, Table 57)	Default
01H	Right Channel Definition (LSEL defined according to Table 54, Table 55)	

Table 60. LSEL Definition

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
4BH	Audio Mode Detect	0						AMOD[1:0]	
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

AMOD[1:0]

Audio mode detected. Some of the audio standards include an identification signal used to identify whether a mono, stereo, or bilingual signal is broadcasted. This word contains the decoded result.

Value	EIA-J	A2	NICAM	FM Radio
00H	Mono	Mono	N/A	N/A
01H	Stereo	Stereo	N/A	N/A
02H	Bilingual	Bilingual	N/A	N/A
03H	N/A	N/A	N/A	N/A

Table 61. Detected Audio mode (N/A: Not available)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
4CH	Pilot PLL Lock	0							LOCK
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

LOCK

Pilot PLL lock status.

LOCK	Pilot PLL lock status	
00H	PLL unlocked	(default)
01H	PLL locked	

Table 62. Pilot PLL lock status

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
4DH	NICAM Error Rate 1	NERR[15:8]							
4EH	NICAM Error Rate 0	NERR[7:0]							
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

NERR[15:0]
NICAM error rate high/low byte. Minimum achievable value is 0x003F. When reading these registers, always read the high byte first. The low byte is only updated when the high byte is read. This ensures that the values read from the two registers come from the same 16-bit word.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
4FH	NICAM Control Bits 1	NIAD[10:3]							
50H	NICAM Control Bits 0	NIAD[2:0]			NICT[4:0]				
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

NIAD[10:0]
NICAM additional data bits reserved for future use.

NICT[4:0]
NICAM control bits high byte. When reading these registers always read the high byte first. The low byte is only updated when the high byte is read. This ensures that the values read from the two registers come from the same 16-bit word.

NICT4	Definition
0	The analog sound signal is not carrying the same program as the digital signal.
1	The analog sound signal is carrying the same program as the digital stereo signal (or mono signal in M1 frames.)

Table 63. NICAM control bits 1

Application Control Information			Contents of 704-bit sound/data block
NICT 3	NICT 2	NICT 1	
0	0	0	Stereo signal comprising alternate A-channel and B-channel samples.
0	0	1	One mono signal and one 352 kbit/s transparent data channel transmitted in alternate frames.
0	1	0	Two independent mono sound signals transmitted in alternate frames (designated M1 and M2.)
0	1	1	One 704 kbit/s transparent data channel.
1	0	0	Undefined.
1	0	1	Undefined.
1	1	0	Undefined.
1	1	1	Undefined.

Table 64. NICAM control bits 2

NICT0 – Frame Flag Bit – Value is 0 for 8 consecutive frames and 1 for next eight frames.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
51H	SIF AGC Control	AGAT[3:0]				AGDC[3:0]			
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

AGAT[3:0]: AGC attack time control

These bits set the attack time of the Automatic Gain Control.

AGAT[3:0]	Attack Time (ms)	
0H	0.055	(default)
1H	0.075	
2H	0.11	
3H	0.15	
4H	0.22	
5H	0.30	
6H	0.45	
7H	0.9	
8H	1.2	
9H	1.8	
AH	2.4	
BH	7.1	
CH	14.2	
DH	28.5	
EH	56.9	
FH	113.8	

Table 65. AGC attack time

AGDC [3:0]: AGC decay time control

These bits set the decay time of the Automatic Gain Control.

AGDC [3:0]	Decay Time (ms)	
0H	0.9	(default)
1H	1.2	
2H	1.8	
3H	2.4	
4H	3.6	
5H	4.8	
6H	7.1	
7H	14.2	
8H	19.0	
9H	28.5	
AH	38.0	
BH	113.8	
CH	227.6	
DH	455	
EH	910	
FH	1820	

Table 66. AGC decay time

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
52H	AGC Control for AM	AMAT[3:0]				AMDC[3:0]			
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	1	1	0	1	1	1

AMAT[3:0]: AGC attack time control AM

These bits set the attack time of the Automatic Gain Control when the input signal is AM.

AMAT[3:0]	Attack Time (ms)	
0H	0.11	
1H	0.15	
2H	0.22	
3H	0.30	
4H	0.44	
5H	0.59	
6H	0.89	
7H	1.8	(default)
8H	2.4	
9H	3.6	
AH	4.7	
BH	14.2	
CH	28.4	
DH	56.9	
EH	113.8	
FH	227.6	

Table 67. AGC attack time AM

AMDC [3:0]: AGC decay time control AM

These bits set the decay time of the Automatic Gain Control when the input signal is AM. The decay time should always be much slower than the attack time. Best results are obtained if the same value is written to both the attack and decay registers.

AMDC [3:0]	Decay Time (ms)	
0H	1.8	
1H	2.4	
2H	3.6	
3H	4.7	
4H	7.1	
5H	9.5	
6H	14.2	
7H	28.4	(default)
8H	37.9	
9H	56.9	
AH	75.9	
BH	227.6	
CH	455.1	
DH	910.2	
EH	1820	
FH	3640	

Table 68. AGC decay time AM

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
53H	Status	ASDC	BI	IMONO	MONO	SNDST[1:0]		C2DET	C1DET
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

ASDC:

When high, this bit indicates that the Automatic Standard Detection algorithm has completed.

BI:

When high, this bit indicates that a bilingual mode has been detected. It is high under any of the following conditions.

1) SYS[3:0] indicates either EIAJ or A2 and the ID signal (AMOD[1:0]) indicates bilingual (0x2).
2) SYS[3:0] indicates NICAM, NICAM reception is good, and NICT[2:1] indicate bilingual (0x2.)

IMONO

When high, this bit indicates independent mono sound (NICAM only). This bit is set to high when the NICT value is 0xa, 0x2, 0x1 and 0x0.

MONO:

When high, this bit indicates that the received signal has been identified as a stereo signal. When low, this bit indicates that stereo is not available. It is high under any of the following conditions.

1) SYS[2:0] indicates either EIAJ or A2 and the ID signal (AMOD[1:0]) indicates stereo (0x1.)
2) SYS[2:0] indicates NICAM, NICAM reception is good, and NICT[2:1] indicate stereo (0x0.)

SNDST[1:0]:

These bits reflect the sound status of the applicable sound standard.

SNDST[1:0]	Status
00H	Analog Sound Standard (AM/FM) active
01H	Bad reception condition of analog sound
02H	Digital Sound (NICAM) available
03H	Bad reception condition of digital sound

Table 69. Sound Status

C2DET:

When high, this bit indicates that a valid secondary carrier (2^{nd} A2 carrier) has been detected.

C1DET:

When high, this bit indicates that a valid primary carrier has been detected.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
54H	Status Pin Control	0					ASTAT	STAP	STAE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ASTAT

Audio Output Result drives status change. Enabling this bit causes a change in the audio output result register (either LRSL or RRSL) to make the INT pin active (if the INT pin is enabled with STAE.) Reading the status register clears the INT pin.

ASTAT	Status Change Output (only active when STAE = 1)	
0	LRSL or RRSL change does not affect INT pin.	(default)
1	LRSL or RRSL change makes INT pin active.	

Table 70. Status Change Output

STAP

Status change output polarity (INT pin polarity)

STAP	Status Change Output Polarity	
0	Active high	(default)
1	Active low	

Table 71. Status Change Output Polarity

STAE

Status change output enable. The INT pin is enabled or disabled by this bit. When enabled, the INT pin indicates any change in the status register (64H). Reading the status register clears the INT pin.

STAE	Status Change Output	
0	Disabled	(default)
1	Enabled	

Table 72. Status Change Output

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
55H	A/D headroom	0					HDRM[2:0]		
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	0	1

HDRM[2:0]

These bits set the A/D headroom for the Automatic Gain Control to control the input signal to.

HDRM[2:0]	A/D Headroom (dBFS)	
0H	-24	
1H	-21	
2H	-18	
3H	-15	
4H	-12	
5H	-9	(default)
6H	-6	
7H	-3	

Table 73. A/D Headroom

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
56H	AGC Freeze	0							AGFRZ
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

AGFRZ

AGC Freeze. Freezes the current value of the AGC feedback.

AGFRZ	AGC Feedback State	
0	Running	(default)
1	Frozen	

Table 74. AGC Feedback State

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
57H	Stereo Carrier Search Ctrl	0				CHMD[1:0]		SREN[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

CHMD[1:0]

Stereo search system change mode.

CHMD[1:0]	Stereo Search System Change Mode	
0H	SYS[2:0] does not change automatically.	(default)
1H	SYS[2:0] changes when the Stereo Carrier Result Register is read after a stereo carrier is detected.	
2H	SYS[2:0] changes automatically when a stereo carrier is detected.	
3H	SYS[2:0] changes automatically when a stereo carrier is detected.	

Table 75. Stereo Search System Change Mode

SREN[1:0]

Stereo search enable. Whenever the stereo carrier search is enabled (either for one-time search or continuous search), the ASTAT output bit will indicate a status change when the SRCMP bit in the Stereo Carrier Search Result register changes from “0” to “1”, in addition to when the Status register changes.

SREN[1:0]	Stereo Search	
0H	Disabled	(default)
1H	One-time Search Enabled (search disabled and SREN[1:0] returns to 0x0 after stereo carrier detected)	
2H	Continuous Search Enabled (search begins again if stereo carrier is lost after initial detection)	
3H	Continuous Search Enabled (search begins again if stereo carrier is lost after initial detection)	

Table 76. Stereo Search

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
58H	Stereo Carrier Search Result	0	SRIND	SRCMP	SRST	SRRSL[3:0]			
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	1	1	1	1

SRRSL[3:0]

Stereo carrier search result. This is only updated when a new stereo carrier is successfully detected.

SRRSL[3:0]	TV System	Sound Modulation	
0H	B/G	FM-Stereo (A2)	
1H	B/G	FM-Mono/NICAM	
2H	-	reserved	
3H	-	reserved	
4H	D/K	FM-Stereo (A2, D/K1)	
5H	D/K	FM-Stereo (A2, D/K2)	
6H	D/K	FM-Stereo (A2, D/K3)	
7H	D/K	FM-Mono/NICAM (D/K, NICAM)	
8H	--	reserved	
9H	--	reserved	
AH	--	reserved	
BH	--	reserved	
CH	--	reserved	
DH	--	reserved	
EH	--	reserved	
FH	--	No result yet	(default)

Table 77. Stereo Carrier Search TV System Result

SRCMP

SRCMP	Stereo Carrier Search Result (SRRSL) Comparison to SYS	
0	SRRSL and SYS are the same	(default)
1	SRRSL and SYS are different	

Table 78. Stereo Carrier Search Result (SRRSL) Comparison to SYS

SRST

SRST	Stereo Carrier Search Status	
0	Not searching (either search is disabled or a stereo carrier has been detected)	(default)
1	Searching (search is enabled and a stereo carrier is not currently detected)	

Table 79. Stereo Carrier Search Status

SRIND

Stereo carrier search indicator. The SRIND bit indicates that System Select is B/G or D/K with NICAM or A2, Carrier 1 is present, but Carrier 2 is not detected. This bit can be used to determine if Stereo Carrier Search should be enabled.

SRIND	Stereo Carrier Search Indicator	
0	SYS[3:0] is B/G or D/K, NICAM or A2 and Carrier 1 is detected and Carrier 2 is not detected	(default)
1	otherwise	

Table 80. Stereo Carrier Search Indicator

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
59H	Audio Output Result	LOR	ROL	LRSUM	0	LRSL[1:0]		RRSL[1:0]	
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

RRSL[1:0]

Right channel audio output result.

Right Outputs for AUTO = "0"					
RRSL[1:0]	EIA-J	A2	NICAM	FM Radio	
00H	Mono	Mono	AMono	Mono	(default)
01H	R	R	R	R	
02H	A	A	A	Mono	
03H	B	B	B	L-R	

Table 81. Right Output Result

LRSL[1:0]

Left channel audio output result.

Left Outputs for AUTO = "0"					
LRSL[1:0]	EIA-J	A2	NICAM	FM Radio	
00H	Mono	Mono	AMono	Mono	(default)
01H	L	L	L	L	
02H	A	A	A	Mono	
03H	B	B	B	L-R	

Table 82. Left Output Result

LOR, ROL, LRSM

These bits are copied outputs of LOR, ROL and LRSM bits on 4AH. Read only.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
5AH	Mute Control / Status	0	AAOMT	ASDMT	LMT	RMT	MANMT	MUTEL	MUTER
R/W		R/W	R/W	R/W	RD	RD	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MUTER

Mute Control Rch

MUTER	Right Channel	
0	Not Muted	(default)
1	Muted	

Table 83. Mute Control Rch

MUTEL

Mute Control Lch

MUTEL	Left Channel	
0	Not Muted	(default)
1	Muted	

Table 84. Mute Control Lch

MANMT

Manual Mute Control

MANMT	Mute Mode	
0	Mute Determined Automatically	(default)
1	Mute determined by MUTEL,R.	

Table 85. Manual Mute Control

RMT

Mute Result Rch

RMT	Right Channel	
0	Not Muted	(default)
1	Muted	

Table 86. Mute Result Rch

LMT

Mute Result Lch

LMT	Left Channel	
0	Not Muted	(default)
1	Muted	

Table 87. Mute Result Lch

ASDMT

Indicates whether automatic system detection is muting the outputs.

ASDMT	ASD Mute	
0	Not Muting	(default)
1	Muting	

Table 88. ASD Mute

AAOMT

Indicates whether AAOS is muting the outputs.

AAOMT	AAOS Mute	
0	Output is not currently muted by AAOS.	(default)
1	Output is currently muted by AAOS.	

Table 89. AAOS Mute

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
5BH	Auto System Detect Control	0				A6M5	A4M5[2:0]		
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	1

A6M5: Decoder Standard Preference1. This bit is XORed with A6M5 Pin.

A6M5	Decoder Standard Preference1	
00H	SECAM L NICAM	(default)
01H	D/K1, D/K2, D/K3 or D/K NICAM	

Table 90. Decoder Standard Preference 1

A4M5[2:0]: Decoder Standard Preference2. These bits are XORed with A4M52-20 Pins respectively.

A4M5[2:0]	Decoder Standard Preference2	
00H	Reserved	
01H	EIAJ	
02H	M-Korea	
03H	PAL (Chroma Carrier)	(default)
04H	Reserved	
05H	Reserved	
06H	Reserved	
07H	Reserved	

Table 91. Decoder Standard Preference 2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
5CH	Decoder AVC	0			DATK[1:0]		DDEC[1:0]		AVCE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

AVCE: AVC Enable

AVCE	AVC status	
00H	Disabled	(default)
01H	Enabled	

Table 92. AVC Enable

DDEC[1:0]: Decoder AVC Decay time

DDEC[1:0]	AVC Decay time	
0H	85 msec	(default)
1H	1.4 seconds	
2H	2.7 seconds	
3H	5.5 seconds	

Table 93. Decoder AVC Decay time

DATK[1:0]: Decoder AVC Attack time

DATK[1:0]	AVC Attack time	
0H	11 msec	(default)
1H	21 msec	
2H	44 msec	
3H	85 msec	

Table 94. AVC Decay time

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
5DH	Level Prescaler Control	0							PRECTL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

PRECTL

Level prescaler mode. The prescaler is positioned prior to the Automatic Volume control. When in automatic mode, the left and right prescaler levels will be adjusted to output the same level from different standards of normal broad cast's signal.

PRECTL	Level Prescaler Mode	
00H	Automatic	
01H	Manual	(default)

Table 95. Level Prescaler Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
5EH	Prescaler L	PREL[7:0]							
5FH	Prescaler R	PRER[7:0]							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

PREL[7:0]
PRER[7:0]

Prescaler output level for left channel. This register is only used when PRECTL is set to manual mode. Use the following formula to set the desired output level. The gain must be a value from 1/256 to 1.

PREL[7:0], PRER[7:0] = Gain x 256 - 1 (unsigned)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
60H	Manual Output Level L	LEVL[7:0]							
61H	Manual Output Level R	LEVR[7:0]							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

LEVL[7:0]
LEVR[7:0]

Manual output level for left channel. This register is used to set the volume level at the left output. The level adjustment is positioned after the Automatic Volume Control. By using the following formula, set the desired output level. The gain must be a value from 1/256 to 1.

LEVL[7:0], LEVR[7:0] = Gain x 256 - 1 (unsigned)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
62H	Carrier 1 Average Frequency 1	CR1F[15:8]							
63H	Carrier 1 Average Frequency 0	CR1F[7:0]							
R/W		RD							
Default		00000000							

CR1F[15:0]

Carrier 1 average frequency. Represents the difference between the nominal carrier frequency and the actual carrier frequency (2's complement.)

Ferr = CR1F x Fs x 2^{-20} (Hz)

Fac = Fc + Ferr (Hz)

Ferr = Frequency error. Difference between nominal and actual carrier frequencies (Hz)

Fac = Actual frequency of carrier to be demodulated (Hz)

Fc = Nominal carrier frequency set inDM1F (Hz)

Fs = Input sample rate (Hz), see the Sample Rate Register table (Table 45) for the input sample rate that corresponds to the selected output sample rate.

When reading these registers, always read the high byte first. The low byte is only updated when the high byte is read. This ensures that the values read from the two registers come from the same 16-bit word.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
64H	Carrier 1 Phase Noise 1	CR1P[15:8]							
65H	Carrier 1 Phase Noise 0	CR1P[7:0]							
R/W		RD							
Default		00000000							

CR1P[15:0]

Carrier 1 phase noise. Represents the average phase noise in terms of frequency deviation.

CR1P = Fadev / Fs x 2^{16} (in 2's complement)

Fadev = average frequency deviation (in Hz)

Fs = Input sample rate (in Hz), see the Sample Rate Register table (Table 45) for the input sample rate that corresponds to the selected output sample rate.

When reading these registers always read the high byte first. The low byte is only updated when the high byte is read. This ensures that the values read from the two registers come from the same 16-bit word.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
66H	Carrier 1 Average Magnitude 1	CR1M[15:8]							
67H	Carrier 1 Average Magnitude 0	CR1M[7:0]							
R/W		RD							
Default		00000000							

CR1M [15:0]

Carrier 1 average magnitude.

CR1M = Portion of full scale x 1.647^2 x 2^{14} (unsigned)

When reading these registers, always read the high byte first. The low byte is only updated when the high byte is read. This ensures that the values read from the two registers come from the same 16-bit word.

CR1M [15:0]	Average Carrier Magnitude (dBFS)
0xAD9B	0
0x7AE8	-3
0x5702	-6
0x3D99	-9
0x2B9C	-12
0x1EDF	-15
0x15DB	-18
0x0F79	-21
0x0AF4	-24
0x07C1	-27
0x057D	-30

Table 96. Carrier 1 average magnitude

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
68H	Carrier 1 Magnitude Noise 1	CR1N[15:8]							
69H	Carrier 1 Magnitude Noise 0	CR1N[7:0]							
R/W		RD							
Default		00000000							

CR1N [15:0]

Carrier 1 average magnitude noise. An FM carrier has a constant magnitude. This is a measure of its average difference from its average.

CR1N [15:0] = Portion of full scale x 1.647^2 * 2^{14} (unsigned)

When reading these registers, always read the high byte first. The low byte is only updated when the high byte is read. This ensures that the values read from the two registers come from the same 16-bit word.

CR1N[15:8]	Average Carrier Magnitude Noise (dBFS)
0xAD9B	0
0x5702	-6
0x2B9C	-12
0x15DB	-18
0x0AF4	-24
0x057D	-30
0x02C0	-36
0x0161	-42
0x00B1	-48
0x0059	-54
0x002C	-60
0x0016	-66
0x000B	-72

Table 97. Carrier 1 average magnitude noise

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
6AH	Carrier 1 Signal Quality 1	CR1Q[15:8]							
6BH	Carrier 1 Signal Quality 0	CR1Q[7:0]							
R/W		RD							
Default		00000000							

CR1Q[15:0]: Carrier 1 quality.

This is the ratio of CR1M to CR1N. This is an approximation of S/N ratio.

$CR1Q = CR1M / CR1N \times 2^6$ (unsigned)

When reading these registers, always read the high byte first. The low byte is only updated when the high byte is read. This ensures that the values read from the two registers come from the same 16-bit word.

CR1Q [15:0]	Ratio of CR1M to CR1N (dB)
0xFFFF	>60
0x4000	48
0x1000	36
0x0400	24
0x0100	12
0x0040	0
0x0010	-12
0x0004	-24
0x0001	<-36

Table 98. Carrier 1 quality

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
6CH	Carrier 2 Average Frequency 1	CR2F[15:8]							
6DH	Carrier 2 Average Frequency 0	CR2F[7:0]							
R/W		RD							
Default		00000000							

CR2F[15:0]

Carrier 2 average frequency. Represents the difference between the nominal carrier frequency and the actual carrier frequency (2's complement.)

Ferr = CR2F x Fs x 2^{-20} (Hz)

Fac = Fc + Ferr (Hz)

Ferr = Frequency error. Difference between nominal and actual carrier frequencies (Hz)

Fac = Actual frequency of carrier to be demodulated (Hz)

Fc = Nominal carrier frequency set in DM2F (Hz)

Fs = Input sample rate (Hz), see the Sample Rate Register table (Table 45) for the input sample rate that corresponds to the selected output sample rate.

When reading these registers, always read the high byte first. The low byte is only updated when the high byte is read. This ensures that the values read from the two registers come from the same 16-bit word.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
6EH	Carrier 2 Average Magnitude 1	CR2M[15:8]							
6FH	Carrier 2 Average Magnitude 0	CR2M[7:0]							
R/W		RD							
Default		00000000							

CR2M [15:0]

Carrier 2 average magnitude.

CR2M = Portion of full scale x 1.647^2 x 2^{14} (unsigned)

When reading these registers, always read the high byte first. The low byte is only updated when the high byte is read. This ensures that the values read from the two registers come from the same 16-bit word.

CR2M [15:0]	Average Carrier Magnitude (dBFS)
0xAD9B	0
0x7AE8	-3
0x5702	-6
0x3D99	-9
0x2B9C	-12
0x1EDF	-15
0x15DB	-18
0x0F79	-21
0x0AF4	-24
0x07C1	-27
0x057D	-30

Table 99. Carrier 2 average magnitude

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
70H	Carrier 2 Magnitude Noise 1	CR2N[15:8]							
71H	Carrier 2 Magnitude Noise 0	CR2N[7:0]							
R/W		RD							
Default		00000000							

CR2N [15:0]

Carrier 1 average magnitude noise. An FM carrier has a constant magnitude. This is a measure of its average difference from its average.

CR2N [15:0] = Portion of full scale x $1.647^2 * 2^{14}$ (unsigned)

When reading these registers, always read the high byte first. The low byte is only updated when the high byte is read. This ensures that the values read from the two registers come from the same 16-bit word.

CR2N[15:8]	Average Carrier Magnitude Noise (dBFS)
0xAD9B	0
0x5702	-6
0x2B9C	-12
0x15DB	-18
0x0AF4	-24
0x057D	-30
0x02C0	-36
0x0161	-42
0x00B1	-48
0x0059	-54
0x002C	-60
0x0016	-66
0x000B	-72

Table 100. Carrier 2 average magnitude noise

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
72H	Carrier 2 Signal Quality 1	CR2Q[15:8]							
73H	Carrier 2 Signal Quality 0	CR2Q[7:0]							
R/W		RD							
Default		00000000							

CR2Q[15:0]: Carrier 2 quality.

This is the ratio of CR2M to CR2N. This is an approximation of S/N ratio.

CR1Q = CR1M / CR1N x 2^6 (unsigned)

When reading these registers, always read the high byte first. The low byte is only updated when the high byte is read. This ensures that the values read from the two registers come from the same 16-bit word.

CR2Q [15:0]	Ratio of CR2M to CR2N (dB)
0xFFFF	>60
0x4000	48
0x1000	36
0x0400	24
0x0100	12
0x0040	0
0x0010	-12
0x0004	-24

Table 101. Carrier 2 quality

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
74H	Pilot Magnitude	PLTM[7:0]							
R/W		RD							
Default		00000000							

PLTM[7:0]

Pilot magnitude. The pilot is present in EIAJ and FM Radio stereo broadcasts.

PltMag7-0	EIAJ Carrier Deviation
255	6.375kHz
200	5kHz (nominal)
0	0kHz

Table 102. Pilot magnitude

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
75H	FM Subcarrier Magnitude	SUBM[7:0]							
R/W		RD							
Default		00000000							

SUBM[7:0]

FM subcarrier magnitude. The fm subcarrier is present in EIA-J broadcast.

SUBM[7:0]	FM subcarrier magnitude
255	25.5kHz
200	20kHz
150	15kHz
0	0kHz

Table 103. FM subcarrier magnitude

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
76H	FM Subcarrier Noise	SUBN[7:0]							
R/W		RD							
Default		00000000							

SUBNM[7:0]

FM subcarrier noise. The fm subcarrier is present in EIA-J broadcast. In the Table 104, the magnitude of the error is expressed in terms of aural carrier deviation.

SUBM[7:0]	Carrier Deviation
255	25.5kHz
200	20kHz
150	15kHz
0	0kHz

Table 104. FM subcarrier magnitude

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
7BH	Carrier 1 Quality Threshold High	C1QTH[7:0]							
	R/W	R/W							
	Default	00100010							

C1QTH[7:0]

Carrier 1 Quality high threshold. This 8-bit threshold is compared against the top 13 bits of carrier 1 quality (CR1Q[15:3]). The threshold is extended to 13 bits by concatenating five zeros above its MSB.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
7CH	Carrier 1 Quality Threshold Low	C1QTL[7:0]							
	R/W	R/W							
	Default	00010110							

C1QTL[7:0]

Carrier 1 Quality low threshold. This 8-bit threshold is compared against the top 13 bits of carrier 1 quality (CR1Q[15:3]). The threshold is extended to 13 bits by concatenating five zeros above its MSB.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
7DH	Carrier 2 Quality Threshold High	C2QTH[7:0]							
	R/W	R/W							
	Default	00110100							

C2QTH[7:0]

Carrier 2 Quality high threshold. This 8-bit threshold is compared against the top 13 bits of carrier 1 quality (CR2Q[15:3]). The threshold is extended to 13 bits by concatenating five zeros above its MSB.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
7EH	Carrier 2 Quality Threshold Low	C2QTL[7:0]							
	R/W	R/W							
	Default	00100001							

C2QTL[7:0]

Carrier 2 Quality low threshold. This 8-bit threshold is compared against the top 13 bits of carrier 1 quality (CR2Q[15:3]). The threshold is extended to 13 bits by concatenating five zeros above its MSB.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
7FH	Carrier 1 Phase Noise Threshold High	C1PTH[7:0]							
	R/W	R/W							
	Default	10000000							

C1PTH[7:0]

Carrier 1 phase noise high threshold. This 8-bit threshold is compared against the top 11 bits of carrier 1 phase noise (CR1P[15:5]). The threshold is extended to 11 bits by concatenating three zeros above its MSB.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
80H	Carrier 1 Phase Noise Threshold Low	C1PTL[7:0]							
	R/W	R/W							
	Default	00100000							

C1PTL[7:0]

Carrier 1 phase noise low threshold. This 8-bit threshold is compared against the top 11 bits of carrier 1 phase noise (CR1P[15:5]). The threshold is extended to 11 bits by concatenating three zeros above its MSB.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
81H	FM Sub Magnitude Threshold High	FSMTH[7:0]							
	R/W	R/W							
	Default	01111101							

FSMTH[7:0]
FM subcarrier magnitude high threshold. Compared against FM subcarrier magnitude (SUBM[7:0].)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
82H	FM Sub Magnitude Threshold Low	FSMTL[7:0]							
	R/W	R/W							
	Default	01001011							

FSMTL[7:0]
FM subcarrier magnitude low threshold. Compared against FM subcarrier magnitude (SUBM[7:0].)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
83H	FM Sub Noise Threshold High	FSNTH[7:0]							
	R/W	R/W							
	Default	00010100							

FSNTH[7:0]
FM subcarrier noise high threshold. Compared against FM subcarrier noise (SUBN[7:0].)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
84H	FM Sub Noise Threshold Low	FSNTL[7:0]							
	R/W	R/W							
	Default	00001010							

FSNTL[7:0]
FM subcarrier noise low threshold. Compared against FM subcarrier noise (SUBN[7:0].)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
85H	NCM Err Rate Threshold High	NERTH[7:0]							
	R/W	R/W							
	Default	01010000							

NERTH[7:0]
NICAM error rate low threshold. Compared against NICAM error rate (NERR[15:8].)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
86H	NCM Err Rate Threshold Low	NERTL[7:0]							
	R/W	R/W							
	Default	00110000							

NERTL[7:0]
NICAM error rate low threshold. Compared against NICAM error rate (NERR[15:8].)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
8BH	Carrier Magnitude ASD Threshold	ASDMT[7:0]							
R/W		R/W							
Default		00011001							

ASDMT[7:0]

ASD threshold of carrier magnitude. This 8-bit threshold is compared against the top 11 bits of carrier 1 & 2 average magnitude values that are the same as CR1M and CR2M except that their settling times are one-fourth as long. The threshold is extended to 11 bits by concatenating three zeros above its MSB.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
8CH	Carrier Freq ASD Threshold	ASDFT[7:0]							
R/W		R/W							
Default		00011000							

ASDFT[7:0]

ASD threshold of carrier average frequency. This 8-bit threshold is compared against the absolute value of the top 10 bits of carrier 1 & 2 average frequency (CR1F[15:6], CR2F[15:6]). The threshold is extended to 10 bits by concatenating two zeros above its MSB.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
8DH	Carrier FM Quality ASD Threshold	ASQT[7:0]							
R/W		R/W							
Default		00000000							

ASQT[7:0]

Carrier FM quality ASD threshold. This 8-bit threshold is is zero extended to 13 bits by concatenating 5 zeros above its MSB and then it is compared against the top 13 bits of carrier 1 & 2 FM quality values(Figure 29, Table 105)

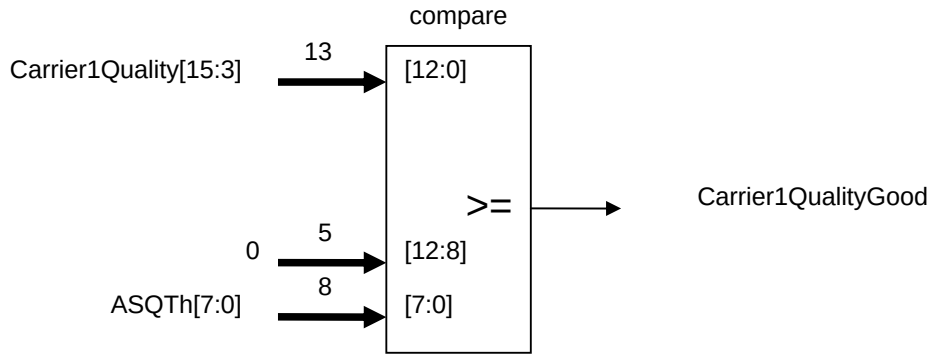


Figure 29. Carrier Quality Threshold

Carrier FM Quality Threshold (dB)= 20*log(ASQTh/8)

Carrier FM Quality Threshold (dB)	ASQT (decimal)	
-INF	0	(default)
10.2	26	(Recommended)
15	45	
20	80	
25	142	
30	253	

Table 105. Table of Typical Carrier FM Quality Threshold Values

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
8EH	Carrier AM Noise ASD Threshold	AANT[7:0]							
R/W		R/W							
Default		1111 1111							

AANT[7:0]

Carrier AM Noise ASD threshold. This 8-bit threshold is compared against the top 8 bits of the carrier 1 phase noise value. The definition of the threshold in terms of carrier frequency deviation is:

$$AANTh = Fadev / Fs * 2^{12}$$

Fadev = average frequency deviation (in Hz)
Fs = Input sample rate (in Hz), see the Sample Rate Register table for the input sample rate that corresponds to the selected output sample rate.

Carrier AM Noise Threshold (kHz) (for Fs = 18.432MSPS)	AANT (decimal)	
0	0	
4.5	1	
40.5	9	(Recommended)
225	50	
450	100	
1147.5	255	(default)

Table 106.Typical Carrier AM Noise Threshold Values

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
8FH	NICAM Noise ASD Threshold	ANNT[7:0]							
R/W		R/W							
Default		1111 1111							

ANNT[7:0]

NICAM Noise ASD threshold. This 8-bit threshold is compared against the top 8 bits of the NICAM noise value.

ANNTh = Average Symbol Phase Error Magnitude (degrees) * 32 / 22.5 (degrees)

Average Symbol Phase Error Magnitude (degrees)	ANNT (decimal)	
0	0	(default)
7.0	10	
21.1	30	(Recommended)
22.5	32	
179	255	

Table 107.Typical NICAM Noise ASD Threshold Values

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
90H	NICAM Noise MSB	NICN[15:8]							
91H	NICAM Noise LSB	NICN[7:0]							
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

ASQT[7:0]

NICAM Average Symbol Phase Error Magnitude. This value represents the average magnitude of the phase error for each NICAM DQPSK symbol.

Average Symbol Phase Error Magnitude = NICNs * 22.5 / 8192 (degrees)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
92H	Carrier FM Quality SCS Threshold	SQLT[7:0]							
R/W		R/W							
Default		00000000							

SQLT[7:0]

The Carrier FM quality SCS threshold is used by the stereo carrier search function to determine the quality of carrier 2. This 8-bit threshold is zero extended to 13 bits by concatenating 5 zeros above its MSB and then it is compared against the top 13 bits of the carrier 2 FM quality value (Figure 30, Table 108).

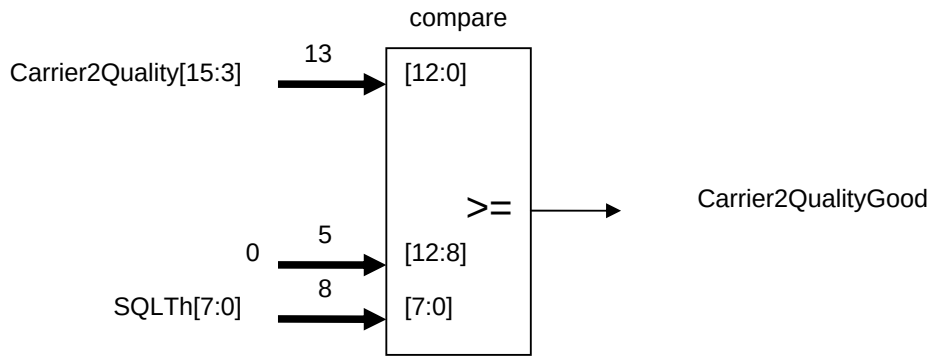


Figure 30. Carrier 2 Quality Threshold

Carrier FM Quality Threshold (dB)= 20*log(SQlTh/8)

Carrier FM Quality Threshold (dB)	SQLT (decimal)	
-INF	0	(default)
6	16	
10.2	26	
15	45	
20	80	
25	142	
30	253	

Table 108.Typical Carrier FM Quality Threshold Values

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
93H	NICAM Noise SCS Threshold	SNST[7:0]							
R/W		R/W							
Default		1111 1111							

SNST[7:0]

The NICAM Noise SCS threshold is used by the stereo carrier search function to determine the quality based on received symbol phase error. This 8-bit threshold is compared against the top 8 bits of the NICAM noise value.

SNSTh = Average Symbol Phase Error Magnitude (degrees) * 32 / 22.5 (degrees)

Average Symbol Phase Error Magnitude (degrees)	SNST (decimal)	
0	0	
7.0	10	
21.1	30	(Recommended)
22.5	32	
179	255	(default)

Table 109.Typical NICAM Noise ASD Threshold Values

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
94H	AVC Level Threshold High	AVCH[7:0]							
R/W		R/W							
Default		0010 0110							

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
95H	AVC Level Threshold Low	AVCL[7:0]							
R/W		R/W							
Default		0001 1011							

AVCH[7:0], AVCL[7:0]

These two thresholds are used to control the target audio level when AVC is active. AVC works by maintaining the combined power of the left and right channels between these high and low level thresholds. The output volume, in dB, relative to full scale is:

20*log10(threshold/128)

The values of these registers should not exceed 128.

SYSTEM DESIGN

Figure 31 shows the system connection diagram. The evaluation board AKD4141 demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

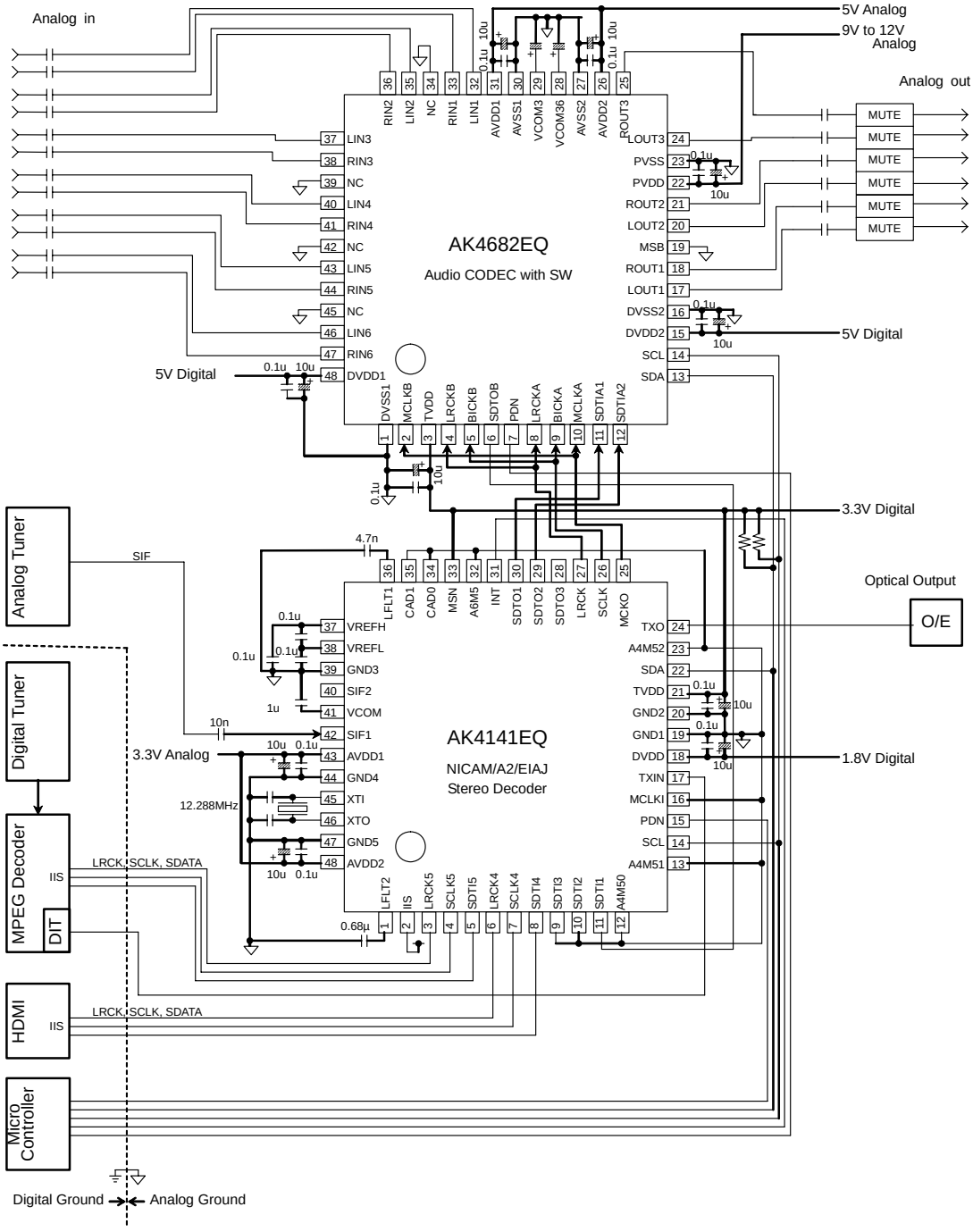


Figure 31. Typical Connection Diagram

1. Grounding and Power Supply Decoupling

The AK4141 requires careful attention to power supply and grounding arrangements. AVDD, DVDD and TVDD are usually supplied from analog supply in system. If AVDD, DVDD and TVDD are supplied separately, the power up sequence is not critical. **All GND pins must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4141 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference Inputs

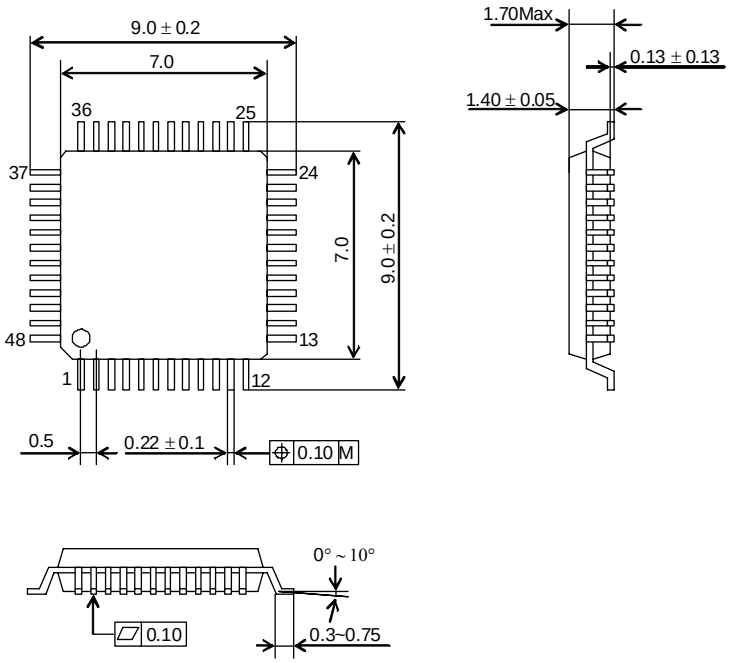
The voltage of AVDD sets the analog input/output range. A 1μF ceramic capacitor attached between VCOM pin and GND4 pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the AVDD and VCOM pins in order to avoid unwanted coupling into the AK4141.

3. Analog Inputs

The AK4141 receives the analog SIF. Each input pins are biased internally.

PACKAGE

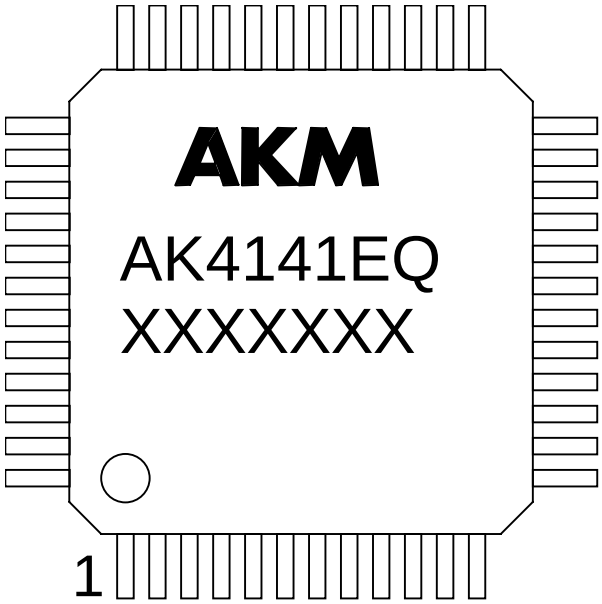
48pin LQFP(Unit:mm)



■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



XXXXXXX: Date code identifier

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
08/05/09	00	First edition		

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