AK4101A
Quad Outputs 192kHz 24-Bit DIT

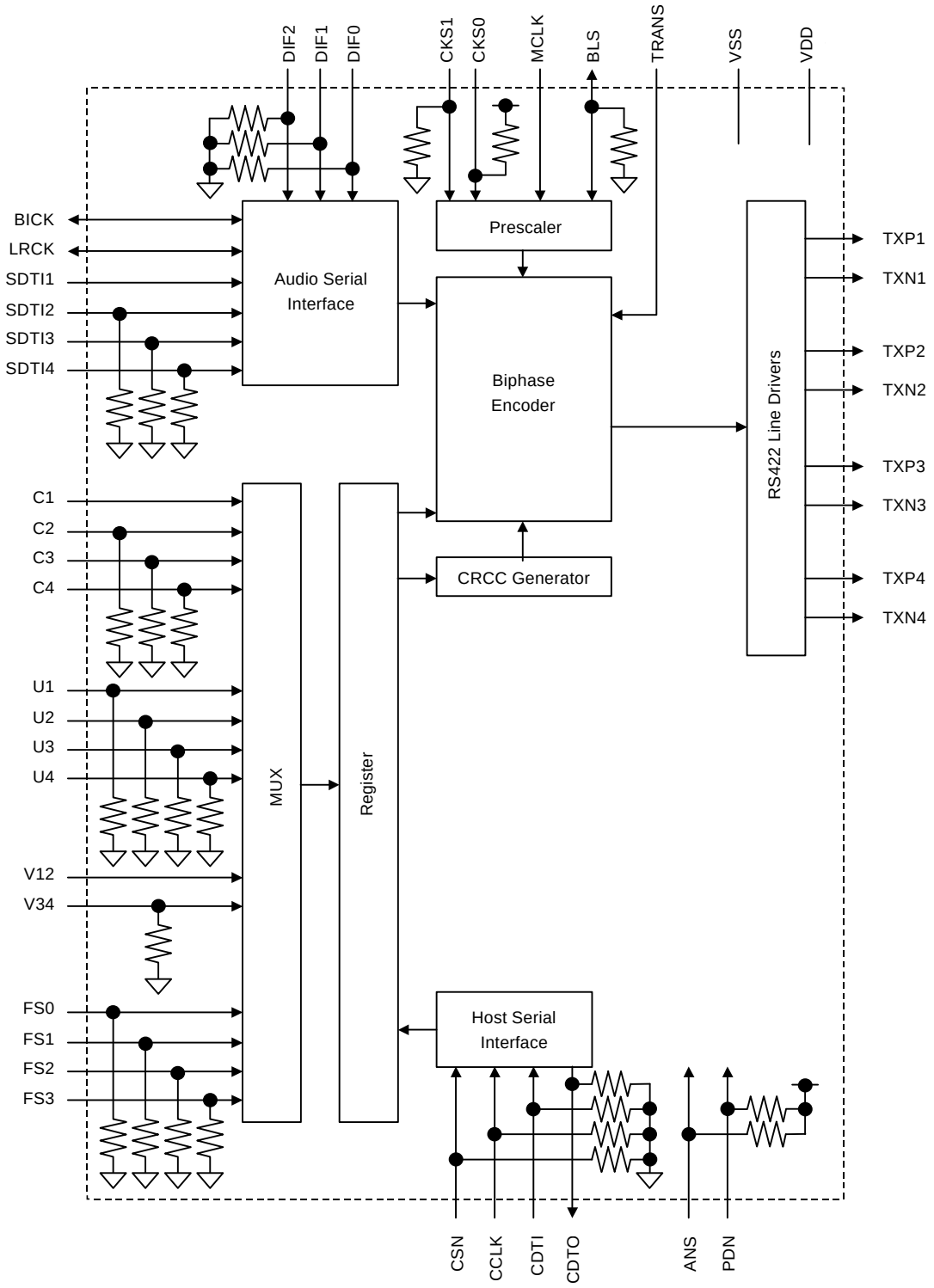
GENERAL DESCRIPTION

The AK4101A is a four outputs digital audio transmitter (DIT) which supports data rate up to 192kHz sample rate operation. The AK4101A supports AES3, IEC60958, S/PDIF & EIAJ CP1201 interface standards. The AK4101A accepts audio data and auxiliary information data and etc, which is then biphase-encoded and driven on to a cable. The audio serial port supports eight formats.

FEATURES

- ☐ **Sampling Rate up to 192kHz**
- ☐ **Support AES3, IEC60958, S/PDIF & EIAJ CP1201 professional and consumer formats**
- ☐ **Generates CRCC codes and parity bits**
- ☐ **Four on-chip RS422 line drivers**
- ☐ **64-byte on-chip buffer memory for Channel Status and User bits**
- ☐ **Supports synchronous/asynchronous access to Channel Status and User bits**
- ☐ **Supports multiple clock frequencies: 128fs, 256fs, 384fs and 512fs**
- ☐ **Supports Left/Right justified and I^2S audio formats**
- ☐ **Easy to use 4 wire, Serial Host Interface**
- ☐ **Audio Routing Mode (Transparent Mode)**
- ☐ **Power supply: 4.75 to 5.25V**
- ☐ **TTL level I/F**
- ☐ **Small Package: 44pin LQFP**
- ☐ **Temperature range of - 40 to 85 °C**

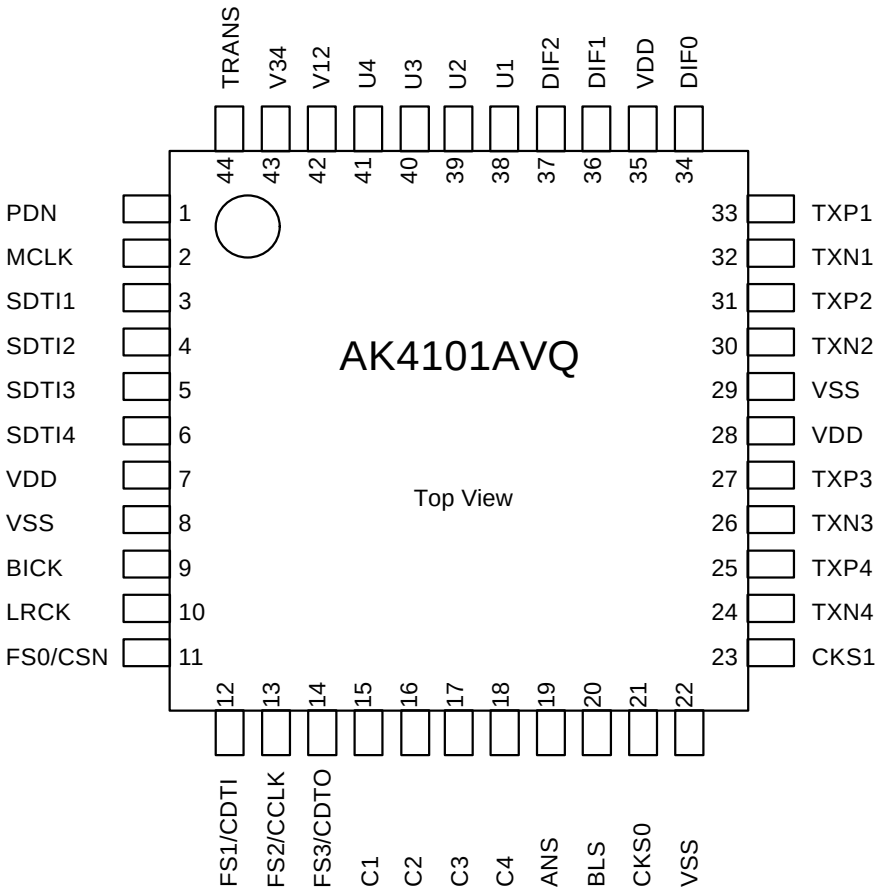
■ Block Diagram



■ Ordering Guide

AK4101AVQ	-40 ~ +85°C	44pin LQFP (0.8mm pitch)

■ Pin Layout



■ Comparison AK4101 with AK4101A

Function		AK4101	**AK4101A**
Ambient Temperature		-10 ~ 70°C	**-40 ~ 85°C**
CRCC generation by FS3-0 pins	Synchronous mode	X	**O**
CRCC generation by FS3-0 bits	Asynchronous mode	X	**O**

O: Input data is reflected to CRCC.
X: Input data is ignored for CRCC.

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	PDN	I	Power Down & Reset Pin (Pull-up Pin) When "L", the AK4101A is powered-down, TXP/N pins are "L" and the control registers are reset to default values.
2	MCLK	I	Master Clock Input Pin
3	SDTI1	I	Audio Serial Data Input 1 Pin
4	SDTI2	I	Audio Serial Data Input 2 Pin (Pull-down Pin)
5	SDTI3	I	Audio Serial Data Input 3 Pin (Pull-down Pin)
6	SDTI4	I	Audio Serial Data Input 4 Pin (Pull-down Pin)
7	VDD	-	Power Supply Pin, 4.75V~5.25V
8	VSS	-	Ground Pin, 0V
9	BICK	I/O	Audio Serial Data Clock Input/Output Pin Serial Clock for SDTI pins which can be configured as an output based on the DIF2-0 inputs.
10	LRCK	I/O	Input/Output Channel Clock Pin Indicates left or right channel, and can be configured as an output based on the DIF2-0 inputs.
11	FS0	I	Sampling Frequency Select 0 Pin at Synchronous mode (Pull-down Pin)
	CSN	I	Host Interface Chip Select Pin at Asynchronous mode (Pull-down Pin)
	AKMODE	I	AK4112B Mode Pin at Audio routing mode (Pull-down Pin) 0: Non-AKM receivers mode, 1: AK4112B mode
12	FS1	I	Sampling Frequency Select 1 Pin at Synchronous mode (Pull-down Pin)
	CDTI	I	Host Interface Data Input Pin at Asynchronous mode (Pull-down Pin)
13	FS2	I	Sampling Frequency Select 2 Pin at Synchronous mode (Pull-down Pin)
	CCLK	I	Host Interface Bit Clock Input Pin at Asynchronous mode (Pull-down Pin)
14	FS3	I	Sampling Frequency Select 3 Pin at Synchronous mode (Pull-down Pin)
	CDTO	O	Host Interface Data Output Pin at Asynchronous mode (Pull-down Pin)
15	C1	I	Channel Status Bit Input Pin for Channel 1
16	C2	I	Channel Status Bit Input Pin for Channel 2 (Pull-down Pin)
17	C3	I	Channel Status Bit Input Pin for Channel 3 (Pull-down Pin)
18	C4	I	Channel Status Bit Input Pin for Channel 4 (Pull-down Pin)
19	ANS	I	Asynchronous/Synchronous Mode Select Pin (Pull-up Pin) 0: Asynchronous mode, 1: Synchronous mode
20	BLS	I/O	Block Start Input/Output Pin (Pull-down Pin) In normal mode, the channel status block output is "H" for the first four bytes. In audio routing mode, the pin is configured as an input. When PDN pin = "L", BLS pin goes "H" at Normal mode.
21	CKS0	I	Clock Mode Select 0 Pin (Pull-up Pin)
22	VSS	-	Ground Pin, 0V

No.	Pin Name	I/O	Description
23	CKS1	I	Clock Mode Select 1 Pin (Pull-down Pin)
24	TXN4	O	Negative Differential Output Pin for Channel 4
25	TXP4	O	Positive Differential Output Pin for Channel 4
26	TXN3	O	Negative Differential Output Pin for Channel 3
27	TXP3	O	Positive Differential Output Pin for Channel 3
28	VDD	-	Power Supply Pin, 4.75V~5.25V
29	VSS	-	Ground Pin, 0V
30	TXN2	O	Negative Differential Output Pin for Channel 2
31	TXP2	O	Positive Differential Output Pin for Channel 2
32	TXN1	O	Negative Differential Output Pin for Channel 1
33	TXP1	O	Positive Differential Output Pin for Channel 1
34	DIF0	I	Audio Serial Interface Select 0 Pin (Pull-down Pin)
35	VDD	-	Power Supply Pin, 4.75V~5.25V
36	DIF1	I	Audio Serial Interface Select 1 Pin (Pull-down Pin)
37	DIF2	I	Audio Serial Interface Select 2 Pin (Pull-down Pin)
38	U1	I	User Data Bit Input Pin for Channel 1 (Pull-down Pin)
39	U2	I	User Data Bit Input Pin for Channel 2 (Pull-down Pin)
40	U3	I	User Data Bit Input Pin for Channel 3 (Pull-down Pin)
41	U4	I	User Data Bit Input Pin for Channel 4 (Pull-down Pin)
42	V12	I	Validity Bit Input Pin for Channel 1 & Channel 2
43	V34	I	Validity Bit Input Pin for Channel 3 & Channel 4 (Pull-down Pin)
44	TRANS	I	Audio Routing Mode (Transparent Mode) Pin at Synchronous mode 0: Normal mode, 1: Audio routing mode (Transparent mode)

Notes:

1. Internal pull-up and pull-down resistors are connected on-chip. The value of the resistors is 43kΩ (typ).
2. All input pins except internal pull-down/pull-up pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(VSS=0V; Note 3)

Parameter	Symbol	min	max	Units
Power Supply	VDD	-0.3	6.0	V
Input Current (All pins except supply pins)	IIN	-	±10	mA
Input Voltage	VIN	-0.3	VDD+0.3	V
Ambient Operating Temperature	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Notes:

3. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supply	VDD	4.75	5.0	5.25	V

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

DC CHARACTERISTICS

(Ta=25°C; VDD=4.75~5.25V)

Parameter	Symbol	min	typ	max	Units
Power Supply Current (fs=108kHz, Note 4)	IDD		10	20	mA
High-Level Input Voltage	VIH	2.4	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
High-Level Output Voltage					
(Except TXP/N pins: Iout=-400µA)	VOH	VDD-1.0	-	-	V
(TXP/N pins: Iout= -8mA)	VOH	VDD-0.8	-	-	V
Low-Level Output Voltage					
(Except TXP/N pins: Iout= 400µA)	VOL	-	-	0.4	V
(TXP/N pins: Iout= 8mA)	VOL	-	-	0.6	V
Input Leakage Current	Iin	-	-	±10	µA

Notes:

4. Power supply current (IDD) is 4mA(typ)@fs=48kHz and 12mA(typ)@fs=192kHz.
IDD increases by 20mA(typ) per channel with professional output driver circuit. IDD is 90mA(typ) if all four channels have professional output driver circuit.
IDD is 150µA(typ) if PDN pin = "L", TRANS pin = "H" and all other input pins except internal pull-up/pull-down pins are held to VSS.

SWITCHING CHARACTERISTICS

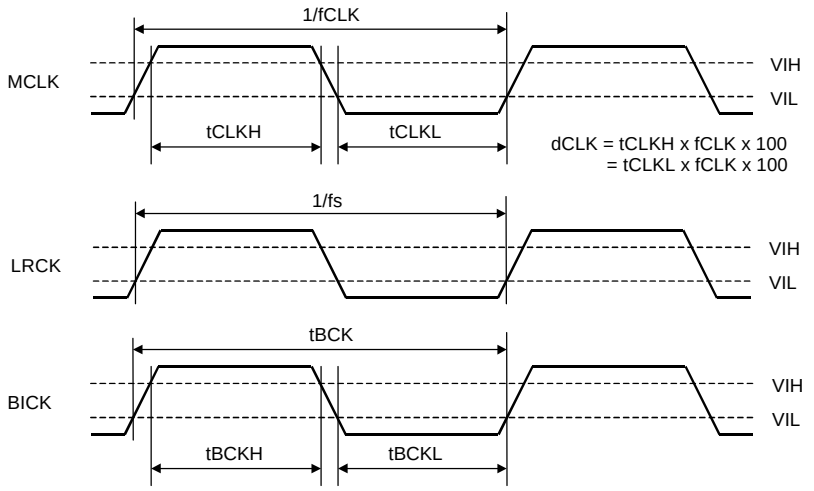
(Ta=25°C; VDD=4.75~5.25V; C_L=20pF)

Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
Frequency		fCLK	3.584		27.648	MHz
Duty Cycle		dCLK	40		60	%
LRCK Timing						
Frequency		fs	28		192	kHz
Duty Cycle at Slave Mode		dLCK	45		55	%
Duty Cycle at Master Mode				50		%
Audio Interface Timing						
Slave Mode						
BICK Period		tBCK	36			ns
BICK Pulse Width Low		tBCKL	15			ns
Pulse Width High		tBCKH	15			ns
LRCK Edge to BICK "↑"	(Note 5)	tLRB	15			ns
BICK "↑" to LRCK Edge	(Note 5)	tBLR	15			ns
SDTI Hold Time		tSDH	8			ns
SDTI Setup Time		tSDS	8			ns
Master Mode						
BICK Frequency		fBCK		64fs		Hz
BICK Duty		dBCK		50		%
BICK "↓" to LRCK		tMBLR	-20		20	ns
SDTI Hold Time		tSDH	20			ns
SDTI Setup Time		tSDS	20			ns
Control Interface Timing						
CCLK Period		tCCK	200			ns
CCLK Pulse Width Low		tCCKL	80			ns
Pulse Width High		tCCKH	80			ns
CDTI Setup Time		tCDS	50			ns
CDTI Hold Time		tCDH	50			ns
CSN "H" Time		tCSW	520			ns
CSN "↓" to CCLK "↑"		tCSS	50			ns
CCLK "↑" to CSN "↑"		tCSH	50			ns
CDTO Delay		tDCD			45	ns
CSN "↑" to CDTO Hi-Z	(Note 6)	tCCZ			70	ns
Power-down & Reset Timing						
PDN Pulse Width		tPDW	150			ns

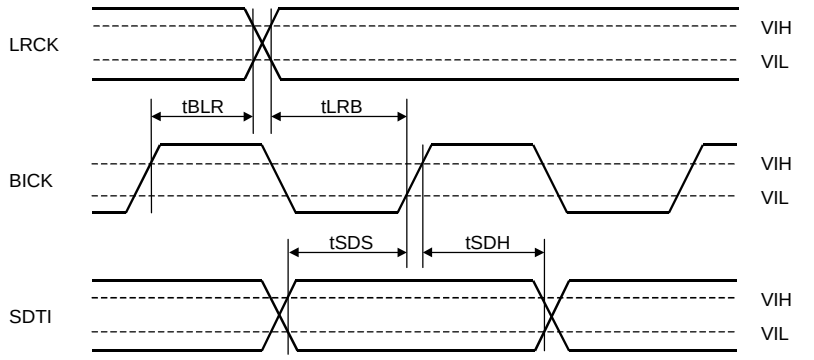
Notes:

5. BICK rising edge must not occur at the same time as LRCK edge.
6. CDTO pin is internally connected to a pull-down resistor.

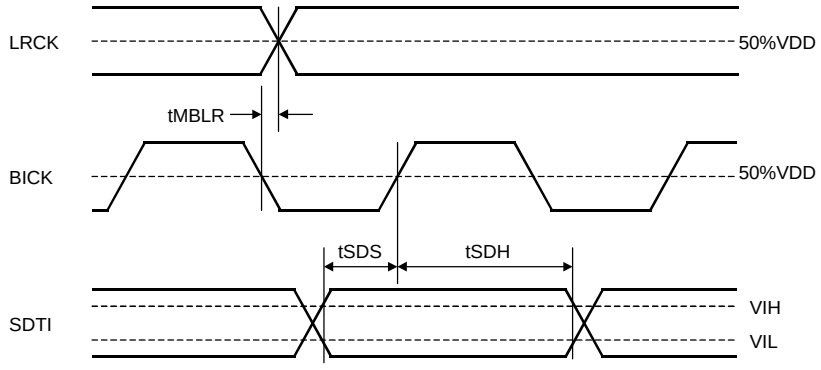
■ Timing Diagram



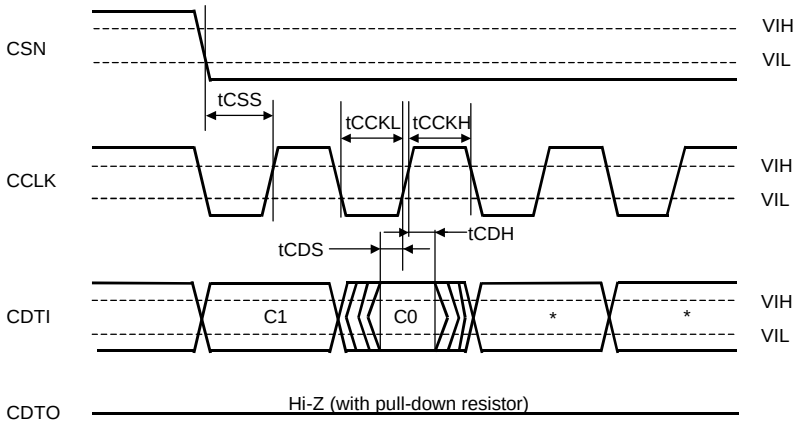
Clock Timing



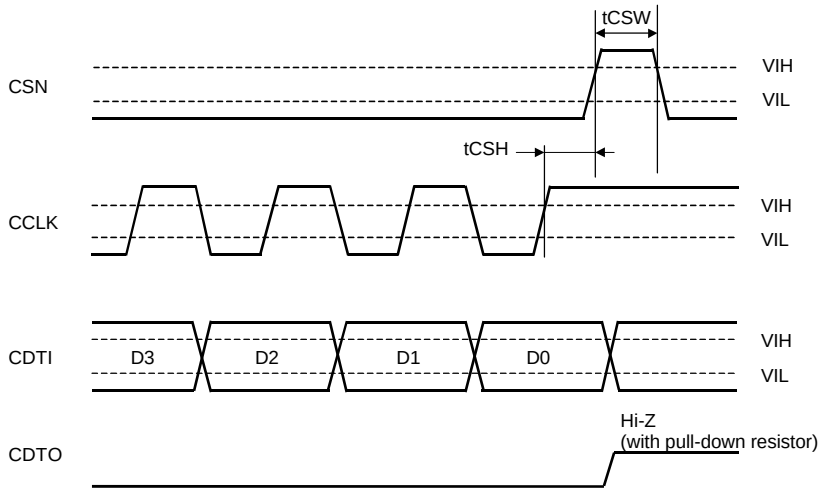
Audio Interface Timing (Slave Mode)



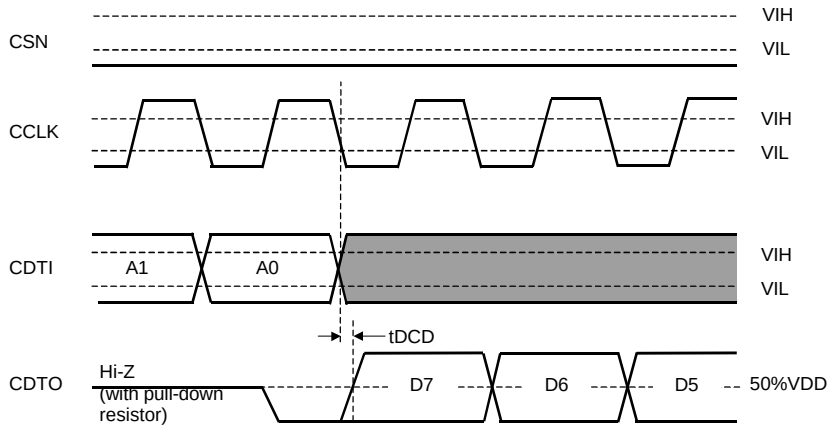
Audio Interface Timing (Master Mode)



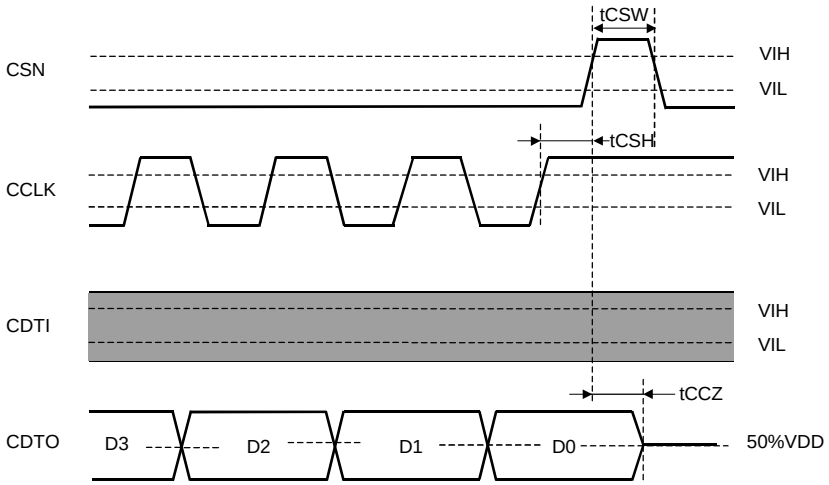
WRITE/READ Command Input Timing



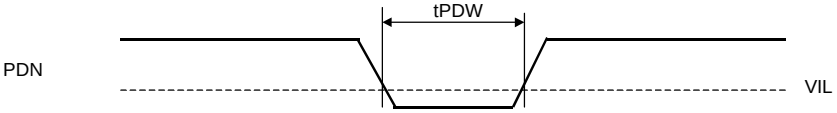
WRITE Data Input Timing



READ Data Output Timing 1



READ Data Output Timing 2



Power-down & Reset Timing

OPERATION OVERVIEW

■ General Description

The AK4101A is a monolithic CMOS circuit that biphase-encodes and transmits audio data, auxiliary information data and etc according to the AES3, IEC60958, S/PDIF and EIAJ CP1201 interface standards. There are four sets of stereo channels that can be transmitted simultaneously. The chip accepts audio data and auxiliary information data separately, multiplexes and biphase-mark encodes the data internally, and drives it directly or through a transformer to a transmission line. There are two modes of operation: asynchronous and synchronous. See section of "Asynchronous Mode/ Synchronous Mode".

■ Initialization

The AK4101A takes 8 bit clock cycles to initialize after PDN pin goes inactive. Also, for correct synchronization, MCLK should be synchronized with LRCK but the phase is not critical.

■ MCLK and LRCK Relationship

For correct synchronization, MCLK and LRCK should be derived from the same clock signal either directly (as through a frequency divider) or indirectly (for example, as through a DSP). The relationship of BICK to LRCK is fixed and should not change. If MCLK or LRCK move such that they are shifted (128fs x 3) or more cycles from their initial conditions, the chip will reset the internal frame and bit counters. However, control registers are not initialized. The following frequencies are supported for MCLK.

CKS1	CKS0	MCLK	fs
0	0	128fs	28k-192kHz
0	1	256fs	28k-108kHz
1	0	384fs	28k-54kHz
1	1	512fs	28k-54kHz

Table 1. MCLK Frequency

■ Asynchronous Mode/ Synchronous Mode

1. Asynchronous Mode (software controlled)

The AK4101A can be configured in the asynchronous mode by connecting the ANS pin to logic "L". In this mode the 16 to 24-bit audio samples are accepted through a configured audio serial port, and the channel status and user data through a serial control host interface (SCI). The SCI allows access to internal buffer memory and control registers which are used to store the channel status and user data. 4bytes per channel of user and channel status is stored. This data is multiplexed with the audio data from the audio serial port, the parity bit is generated, and the bit stream is biphase-mark encoded and driven through the RS422 line drivers. The CRCC code for the channel status is also generated according to the professional mode definition in the AES3 standards. This mode also allows for software control for mute, reset, audio format selection, clock frequency settings and output enables, via the serial host interface.

2. Synchronous Mode (hardware controlled)

The AK4101A when configured in synchronous mode accepts 16 - 24 bit audio samples through the audio serial port and provides dedicated pins for the control data and allows all channel status, user data and validity bits to be serially input through port pins. This data is multiplexed, the parity bit generated, and the bit stream is biphase-mark encoded and driven through an RS422 line driver. The four set of channels have individual channel status and user data pins.

2-1. Audio Routing Mode (Transparent Mode)

The AK4101A can be configured in audio routing mode (transparent mode) by ANS pin = TRANS pin = "1". In this mode, the channel status(C), user data(U) and validity(V) bits must pass through unaltered. The Block Start(B) signal is configured as an input, allowing the transmit block structure to be slaved to the block structure of the receiver. The C, U and V are now transmitted with the current audio sample. In audio routing mode, no CRCC bytes are generated and C bits pass through unaltered. In audio routing mode, the FS0/CSN pin changes definition to AKMODE pin. When set "H" the AK4101A can be configured directly with the AK4112B receiver. When set "L", it may be used with other non-AKM receivers. Setting the part with TRANS pin = "1" and ANS pin = "0" is illegal and places the chip into a test mode.

Pin		Modes		Source for C, U and V bits
ANS	TRANS	Synchronous/Asynchronous	Audio Routing	
0	0	Asynchronous mode	Normal mode	C Pin ORed Control Register U Pin ORed Control Register V Pin ORed Control Register
0	1	(Test mode)		
1	0	Synchronous mode	Normal mode	C,U and V pin
1	1		Audio routing mode	

Table 2. Mode setting

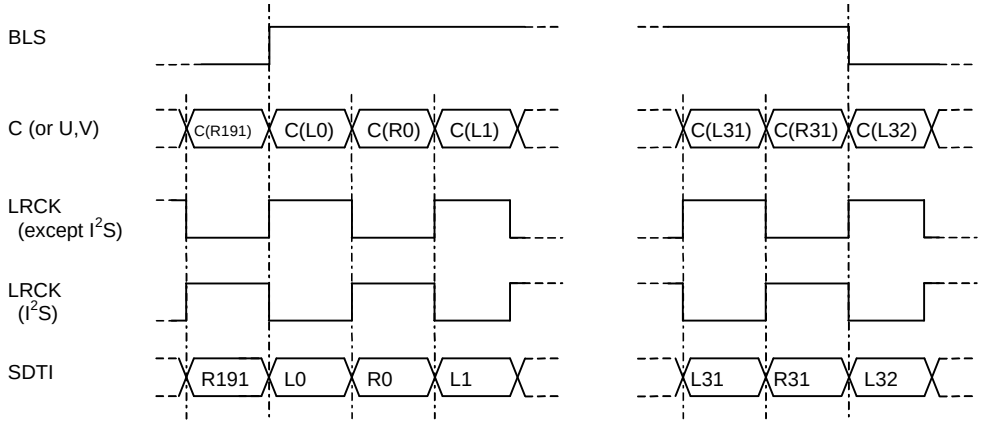


Figure 1. Audio routing mode timing (AKMODE pin = "0")

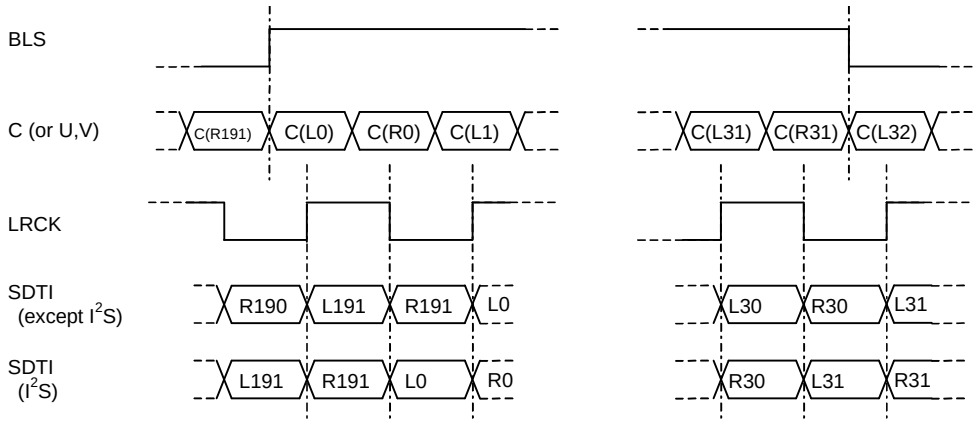


Figure 2. Audio routing mode timing (AKMODE pin = "1")

■ Block Start Timing

Normal mode

In normal mode (TRANS pin = "0"), the block start signal is an output. It goes "H" two bit cycle after the beginning of channel 2 of frame 0 in each block, and stays "H" for the first 32 frames.

Audio routing mode (transparent mode)

In audio routing mode (transparent mode) (ANS pin = TRANS pin = "1"), the block start becomes an input. Except in I^2S mode, a block start signal sampled any time from the first positive BICK edge of the previous left channel to the positive BICK edge preceding the transition of an LRCK indicating the left channel will result in the current left channel being taken as the first sub frame of the current block. See Figure 3 below.

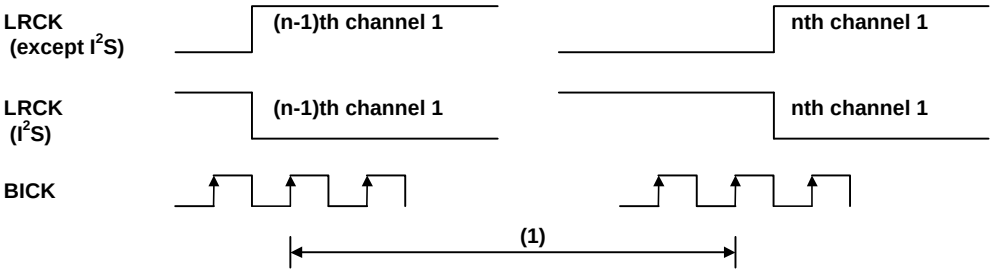


Figure 3. Block start timing in audio routing mode

A block start signal arriving during "(1)" period will result in the usage of "nth channel 1" as the first sub-frame of the block.

■ C, U, V Serial Ports

Normal mode

In normal mode (TRANS pin = "0"), the C, U and V bits are captured (either from the pins, in synchronous mode, or the control registers, in the asynchronous mode) in the sub frame following the audio data. The V bit is set to zero to indicate the audio data is suitable for conversion. The V12 pin indicates validity for Channels 1 & 2 and V34 pin indicates validity for Channels 3 & 4 respectively. See Figure 4 and Figure 5.

Audio routing mode (transparent mode)

In audio routing mode (transparent mode) (ANS pin = TRANS pin = "1"), the C, U and V bits are captured with the same sub-frame as the data to which the C, U and V bits correspond. In all DIF modes except 5 and 7, the C, U and V bits are captured at the first, rising edge of BICK after an LRCK transition. In modes 5 and 7 (I^2S), the C, U and V bits are captured at the second rising edge. See Figure 6 and Figure 7.

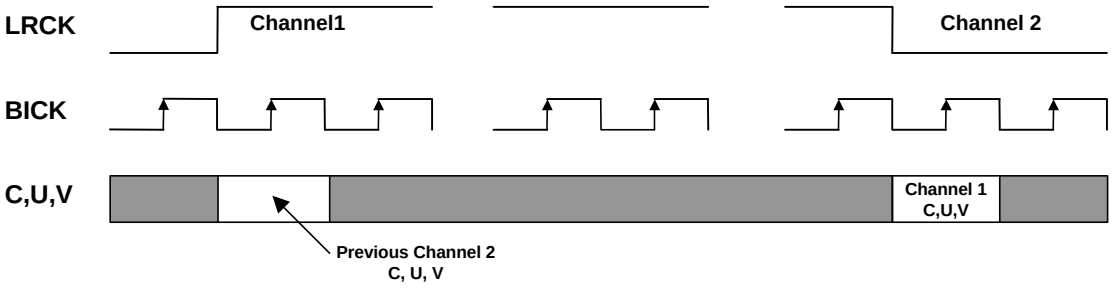


Figure 4. Normal, DIF modes 0, 1, 2, 3, 4, and 6

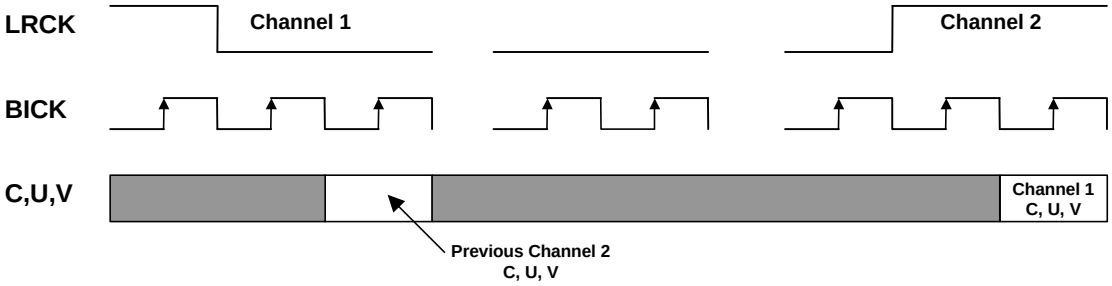


Figure 5. Normal, DIF modes 5 and 7 (I^2S)

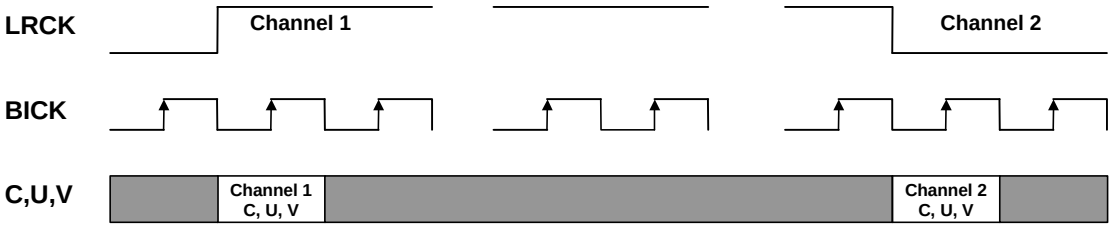


Figure 6. Audio routing, DIF modes 0, 1, 2, 3, 4, and 6

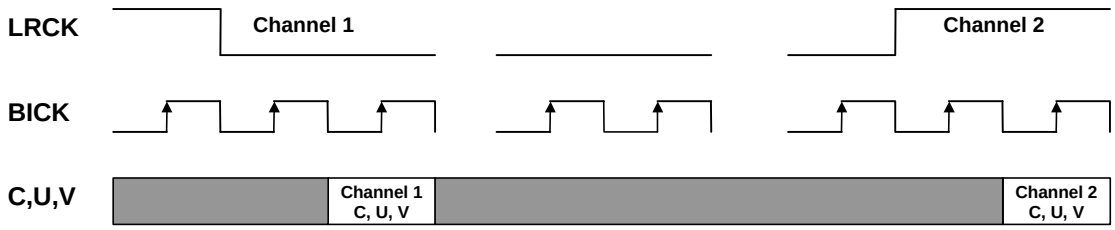


Figure 7. Audio routing, DIF modes 5 and 7 (I^2S)

■ Audio Serial Interface

The audio serial interface is used to input audio data and consists of six pins: Bit Clock (BICK), Word Clock (LRCK) & four Data pins (SDTI 1-4). LRCK indicates the particular channel, left or right. The DIF 2-0 pins in synchronous mode and control registers in asynchronous mode select the particular input mode. In asynchronous mode, DIF2-0 bits are logically ORed with DIF2-0 pins. Audio data format supports 16-24 bits, right justified and left justified modes. The I^2S mode is also supported. The AK4101A can be configured in master and slave modes.

Mode	DIF2	DIF1	DIF0	SDTI	Master / Slave	LRCK	BICK
0	0	0	0	16bit, Right justified	Slave	H/L (I)	32fs-128fs (I)
1	0	0	1	18bit, Right justified	Slave	H/L (I)	36fs-128fs (I)
2	0	1	0	20bit, Right justified	Slave	H/L (I)	40fs-128fs (I)
3	0	1	1	24bit, Right justified	Slave	H/L (I)	48fs-128fs (I)
4	1	0	0	24bit, Left justified	Slave	H/L (I)	48fs-128fs (I)
5	1	0	1	24bit, I^2S	Slave	L/H (I)	50fs-128fs (I)
6	1	1	0	24bit, Left justified	Master	H/L (O)	64fs (O)
7	1	1	1	24bit, I^2S	Master	L/H (O)	64fs (O)

Table 3. Audio Data Format Modes [NOTE; (I): Input, (O): Output]

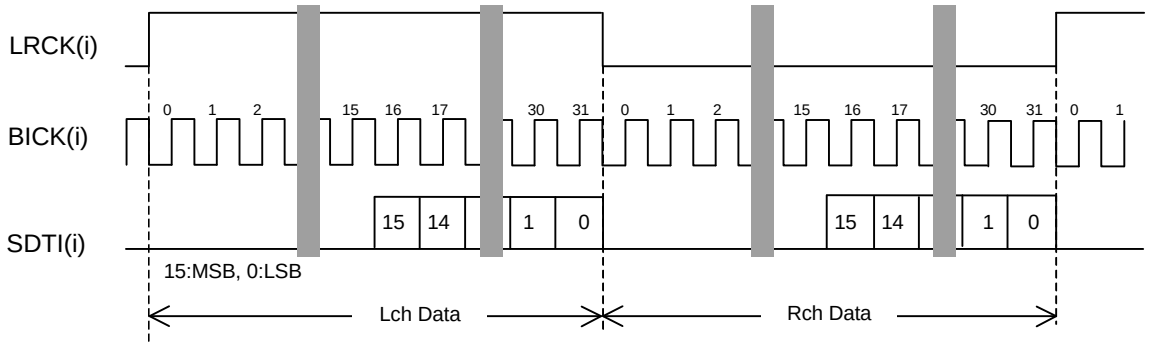


Figure 8. Mode 0 Timing

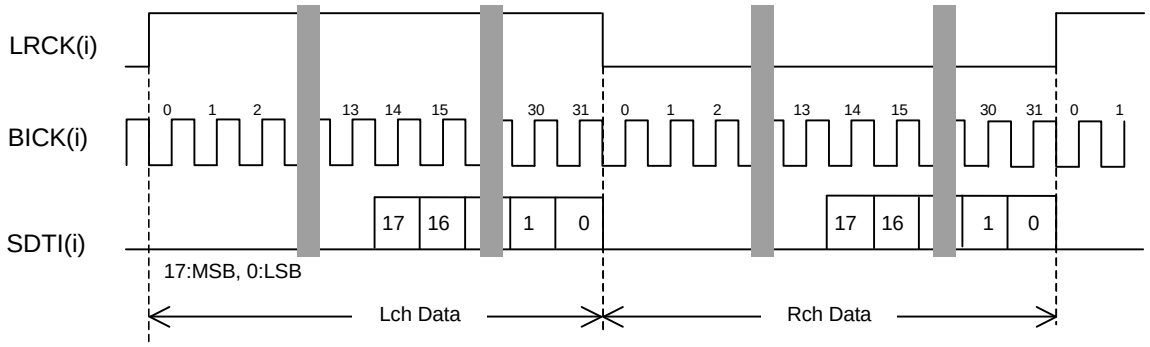


Figure 9. Mode 1 Timing

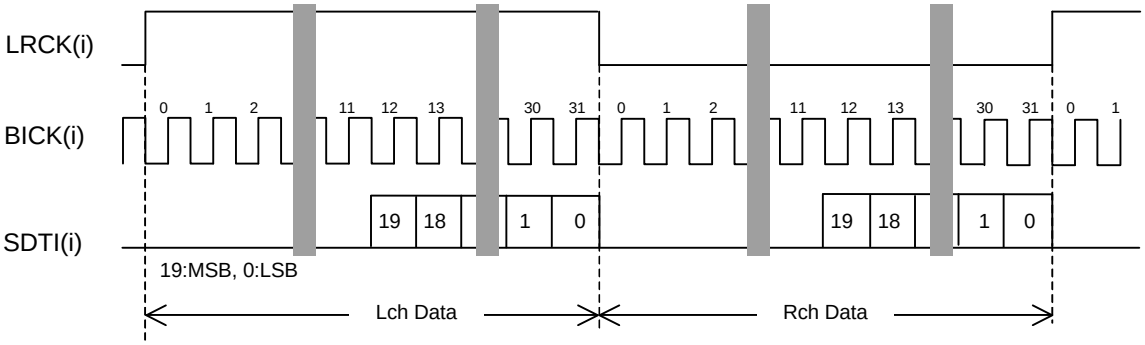


Figure 10. Mode 2 Timing

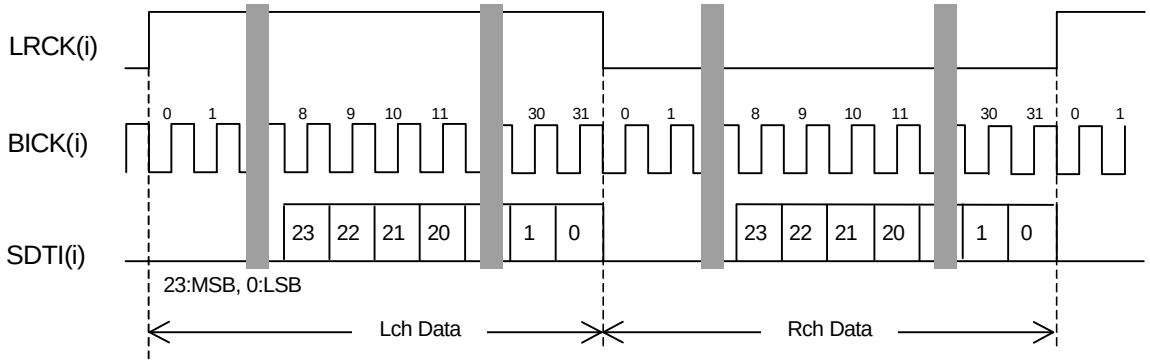


Figure 11. Mode 3 Timing

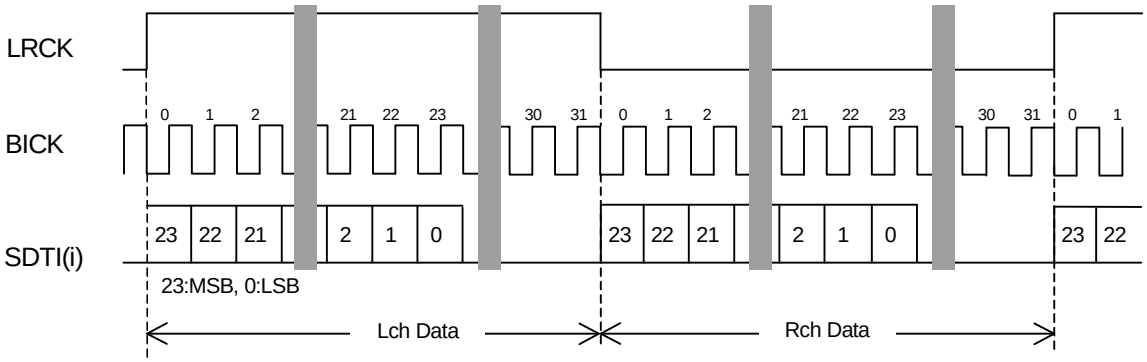


Figure 12. Mode 4, 6 Timing
Mode 4: LRCK, BICK: Input
Mode 6: LRCK, BICK: Output

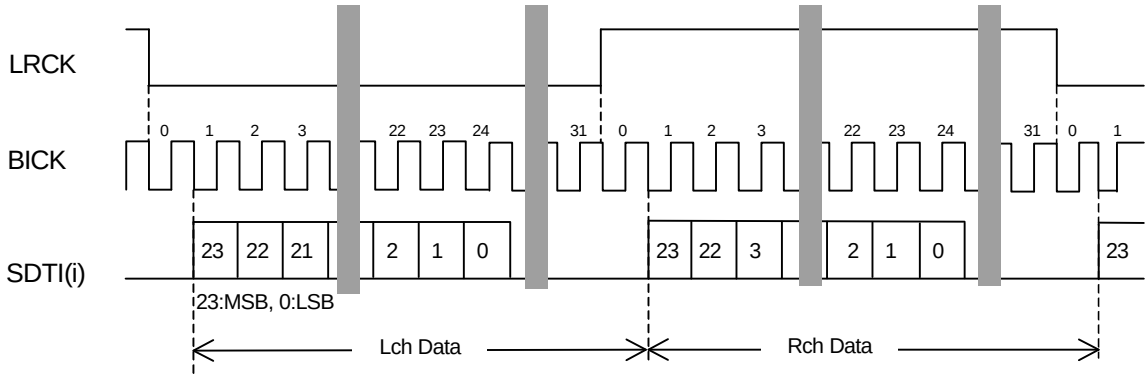


Figure 13. Mode 5, 7 Timing
Mode 5: LRCK, BICK: Input
Mode 7: LRCK, BICK: Output

■ Sampling frequency setting

Bits 3-0 of Channel Status Byte 3 in consumer mode can be set by FS3-0 pins. Also bits 7-6 of Channel Status Byte 0 and bits 6-3 of Channel Status Byte 4 in professional mode can be set by FS3-0 pins.

FS[3:0]	Sampling Frequency	Byte 3 Bits 3-0
0000	44.1kHz	0000
0001	Not Indicated	0001
0010	48kHz	0010
0011	32kHz	0011
0100	22.05kHz	0100
0101	Reserved	0101
0110	24kHz	0110
0111	Reserved	0111
1000	88.2kHz	1000
1001	Reserved	1001
1010	96kHz	1010
1011	Reserved	1011
1100	176.4kHz	1100
1101	Reserved	1101
1110	192kHz	1110
1111	Reserved	1111

Table 4. Sampling frequency setting (Consumer mode)

FS[3:0]	Sampling Frequecny	Byte 0 Bits 7-6	Byte 4 Bits 6-3
0000	Not Defined	00	0000
0001	44.1kHz	01	0000
0010	48kHz	10	0000
0011	32kHz	11	0000
0100	Not Defined	00	0000
0101	Not Defined	00	0000
0110	Not Defined	00	0000
0111	Not Defined	00	0000
1000	For vectoring	00	1000
1001	22.05kHz	00	1001
1010	88.2kHz	00	1010
1011	176.4kHz	00	1011
1100	192kHz	00	0011
1101	24kHz	00	0001
1110	96kHz	00	0010
1111	Not Defined	00	1111

Table 5. Sampling frequency setting (Professional mode)

■ Data Transmission Format

Data transmitted on the TX outputs is formatted in blocks as shown in Figure 14. Each block consists of 192 frames. A frame of data contains two sub-frames. A sub-frame consists of 32 bits of information. Each data bit received is coded using a bi-phase mark encoding as a two binary state symbol. The preambles violate bi-phase encoding so they may be differentiated from data. In bi-phase encoding, the first state of an input symbol is always the inverse of the last state of the previous data symbol. For a logic "0", the second state of the symbol is the same as the first state. For a "1", the second state is the opposite of the first. Figure 15 illustrates a sample stream of 8 data bits encoded in 16 symbol states.

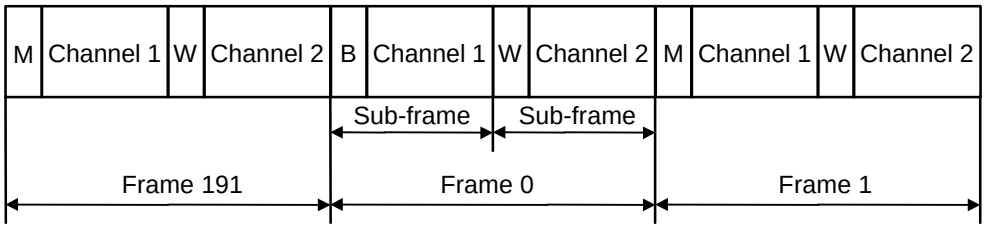


Figure 14. Block format

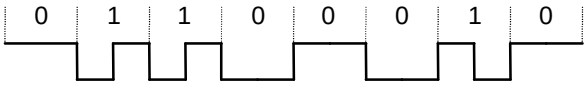


Figure 15. A biphase-encoded bit stream

The sub-frame is defined in Figure 16 below. Bits 0-3 of the sub-frame represent a preamble for synchronization. There are three preambles. The block preamble, B, is contained in the first sub-frame of Frame 0. The channel 1 preamble, M, is contained in the first sub-frame of all other frames. The channel 2 preamble, W, is contained in all of the second sub-frames.
Table 6 below defines the symbol encoding for each of the preambles. Bits 4-27 of the sub-frame contain the 24 bit audio sample in 2's complement format with bit 27 as the most significant bit. For 16 bit mode, Bits 4-11 are all 0. Bit 28 is the validity flag. This is "H" if the audio sample is unreliable. Bit 29 is a user data bit. Frame 0 contains the first bit of a 192 bit user data word. Frame 191 contains the last bit of the user data word. Bit 30 is a channel status bit. Again frame 0 contains the first bit of the 192 bit word with the last bit in frame 191. Bit 31 is an even parity bit for bits 4-31 of the sub-frame.

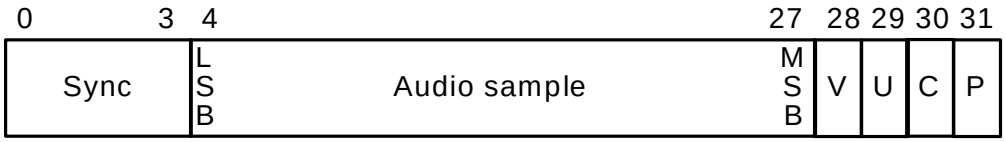


Figure 16. Sub-frame format

The block of data contains consecutive frames transmitted at a state-bit rate of 64 times the sample frequency, fs. For stereophonic audio, the left or A channel data is in channel 1 while the right or B data is in channel 2. For monophonic audio, channel 1 contains the audio data.

Preamble	Preceding state = 0	Preceding state = 1
B	11101000	00010111
M	11100010	00011101
W	11100100	00011011

Table 6. Sub-frame preamble encoding

■ Line Drivers

There are four RS422 line drivers on chip. The AES3 specification states that the line driver shall have a balanced output with an internal impedance of 110 ohms ±20% and also requires a balanced output drive capability of 2 to 7 volts peak-to-peak into 110 ohm load. The internal impedance of the RS422 driver along with a series resistors of 56 ohms realizes this requirement. For consumer use(S/PDIF), the specifications require an output impedance of 75 ohms ±20% and a driver level of 0.5±20% volts peak to peak. A combination of 330 ohms in parallel with 100 ohms realizes this requirement. The outputs can be set to ground by resetting the device or a software mute.

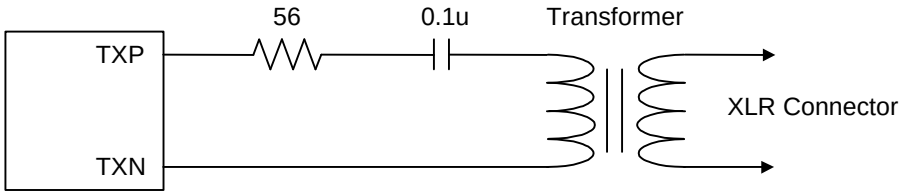


Figure 17. Professional Output Driver Circuit

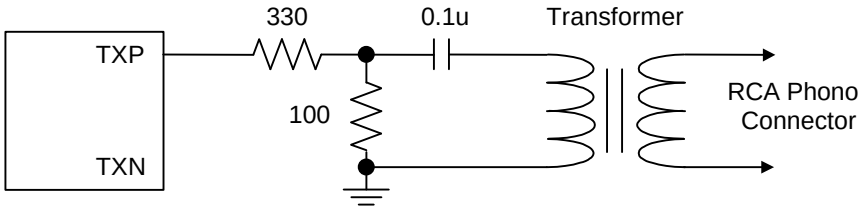
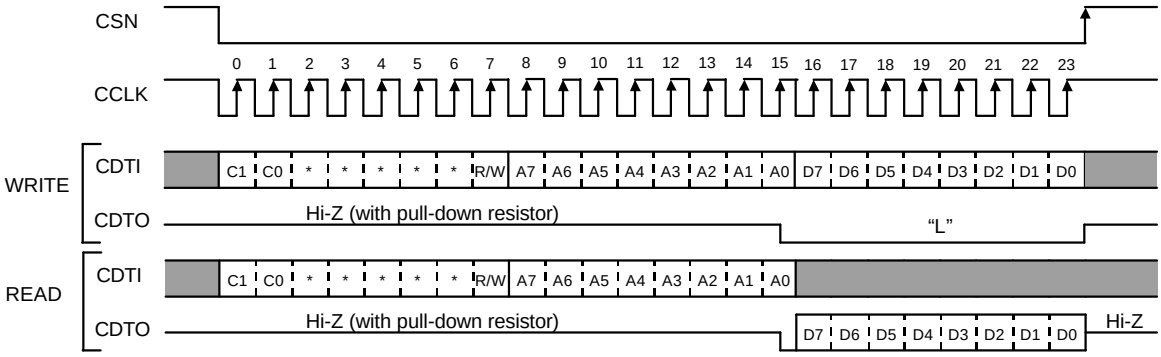


Figure 18. Consumer Output Driver Circuit

■ Serial Control Interface

In asynchronous mode, four of the dual function pins become CSN, CCLK, CDTI and CDTO, a 4 wire microprocessor interface. The internal 66 byte control register can then be read and written. The contents of the control register define, in part, the mode of operation for the AK4101A. Figure 19 illustrates the serial data flow associated with SCI read and write operations. C1-0 bits are the chip address. The AK4101A looks for C1-0 bits to be a "11" before responding to the incoming data. R/W is the Read/Write bit which is "0" for a read operation and "1" for a write operation. The register address contained in A7-0 bits is decoded to select a particular byte of the control register. D7-0 bits on CDTI pin is the control data coming from the microprocessor during a write operation. D7-0 bits on CDTO pin is the contents of the addressed byte from the control register requested during a read operation. The address and data bits are framed by CSN pin = "0". During a write operation, each address and data bit is sampled on the rising edge of CCLK. During a read operation, the address bits are sampled on the rising edge of CCLK while data on CDTO is output on the falling edge of CCLK. CCLK has a maximum frequency of 5 MHz.



C1-C0: Chip Address (Fixed to "11")
R/W: READ/WRITE (0:READ, 1:WRITE)
*: Don't care
A7-A0: Register Address
D7-D0: Control Data

Figure 19. Control I/F Timing

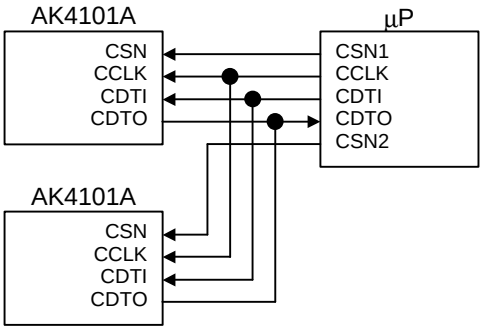


Figure 20. Typical connection with µP
Note: External pull-up resistor should not be attached to CDTO pins since CDTO pin is internally connected to the pull-down resistor.

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Clock/Format Control	CRCE	DIF2	DIF1	DIF0	CKS1	CKS0	MUTEN	RSTN
01H	Validity/fs Control	V4	V3	V2	V1	FS3	FS2	FS1	FS0
02H	Ch 1 A-channel C-bit buffer for Byte 0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
03H	Ch 1 A-channel C-bit buffer for Byte 1	CA15	CA14	CA13	CA12	CA11	CA10	CA9	CA8
04H	Ch 1 A-channel C-bit buffer for Byte 2	CA23	CA22	CA21	CA20	CA19	CA18	CA17	CA16
05H	Ch 1 A-channel C-bit buffer for Byte 3	CA31	CA30	CA29	CA28	CA27	CA26	CA25	CA24
06H-09H	Ch 1 B-channel C-bit buffer for Byte 0-3	CB7 … CB31	… …	… …	… …	… …	… …	… …	CB0 … CB24
0AH-0DH	Ch 1 A-channel U-bit buffer for Byte 0-3	UA7 … UA31	… …	… …	… …	… …	… …	… …	UA0 … UA24
0EH-11H	Ch 1 B-channel U-bit buffer for Byte 0-3	UB7 … UB31	… …	… …	… …	… …	… …	… …	UB0 … UB24
12H-15H	Ch 2 A-channel C-bit buffer for Byte 0-3	…							
16H-19H	Ch 2 B-channel C-bit buffer for Byte 0-3	…							
1AH-1DH	Ch 2 A-channel U-bit buffer for Byte 0-3	…							
1EH-21H	Ch 2 B-channel U-bit buffer for Byte 0-3	…							
22H-25H	Ch 3 A-channel C-bit buffer for Byte 0-3	…							
26H-29H	Ch 3 B-channel C-bit buffer for Byte 0-3	…							
2AH-2DH	Ch 3 A-channel U-bit buffer for Byte 0-3	…							
2EH-31H	Ch 3 B-channel U-bit buffer for Byte 0-3	…							
32H-35H	Ch 4 A-channel C-bit buffer for Byte 0-3	…							
36H-39H	Ch 4 B-channel C-bit buffer for Byte 0-3	…							
3AH-3DH	Ch 4 A-channel U-bit buffer for Byte 0-3	…							
3EH-41H	Ch 4 B-channel U-bit buffer for Byte 0-3	…							

Table 7. Register Map

Notes:

(1) In stereo mode, A indicates Left Channel and B indicates Right Channel.
(2) In asynchronous mode, the DIF2-0 and CKS1-0 bits are logically “ORed” with the DIF2-0 and CKS1-0 pins.
(3) For addresses from 42H to FFH, data is not written.
(4) The PDN pin = “L” resets the registers to their default values.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Clock/Format Control	CRCE	DIF2	DIF1	DIF0	CKS1	CKS0	MUTEN	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	0	0	1	1

RSTN: Timing Reset.
0: Resets the internal frame and bit counters. Control registers are not initialized.
TXP pin is "H" and TXN pin is "L". In normal mode, BLS pin is "H".
1: Normal operation. (Default)

MUTEN: Power Down and Mute for Asynchronous Mode.
0: Power Down Command. Control registers are not initialized.
TXP and TXN pins are "L". In normal mode, BLS pin is "H".
1: Normal operation. (Default)

CKS1-0: Master Clock Frequency Select. (See Table 1.)
Default: "00" (Mode 0: MCLK=128fs)
CKS1-0 bits are logically ORed with CKS1-0 pins.

DIF2-0: Audio Data Format. (See Table 3.)
Default: "000" (Mode 0: 16bit right justified)
DIF2-0 bits are logically ORed with DIF2-0 pins.

CRCE: CRCC Enable at professional mode.
0: CRCC is not generated.
1: CRCC is generated in professional mode. In consumer mode, CRCC is not generated. (Default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Validity/fs Control	V4	V3	V2	V1	FS3	FS2	FS1	FS0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

FS3-0: Sampling Frequency Select. (See Table 4 and Table 5.)
Default: "0000" ("44.1kHz" in consumer mode; "Not defined" in professional mode.)

V1-4: Validity Flag for each channel.
0: Valid (Default)
1: Invalid

V12 pin	V1 bit	V2 bit	V bit on TX1	V bit on TX2
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

Table 8. V bit setting at asynchronous mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Ch 1 A-channel C-bit buffer for Byte 0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
06H	Ch 1 B-channel C-bit buffer for Byte 0	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
12H	Ch 2 A-channel C-bit buffer for Byte 0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
16H	Ch 2 B-channel C-bit buffer for Byte 0	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
22H	Ch 3 A-channel C-bit buffer for Byte 0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
26H	Ch 3 B-channel C-bit buffer for Byte 0	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
32H	Ch 4 A-channel C-bit buffer for Byte 0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
36H	Ch 4 B-channel C-bit buffer for Byte 0	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	0	0

C0-7: Channel Status Byte 0
Default: “00100000”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Ch 1 A-channel C-bit buffer for Byte 1	CA15	CA14	CA13	CA12	CA11	CA10	CA9	CA8
07H	Ch 1 B-channel C-bit buffer for Byte 1	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8
13H	Ch 2 A-channel C-bit buffer for Byte 1	CA15	CA14	CA13	CA12	CA11	CA10	CA9	CA8
17H	Ch 2 B-channel C-bit buffer for Byte 1	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8
23H	Ch 3 A-channel C-bit buffer for Byte 1	CA15	CA14	CA13	CA12	CA11	CA10	CA9	CA8
27H	Ch 3 B-channel C-bit buffer for Byte 1	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8
33H	Ch 4 A-channel C-bit buffer for Byte 1	CA15	CA14	CA13	CA12	CA11	CA10	CA9	CA8
37H	Ch 4 B-channel C-bit buffer for Byte 1	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

C8-15: Channel Status Byte 1
Default: “00000000”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Ch 1 A-channel C-bit buffer for Byte 2	CA23	CA22	CA21	CA20	CA19	CA18	CA17	CA16
14H	Ch 2 A-channel C-bit buffer for Byte 2	CA23	CA22	CA21	CA20	CA19	CA18	CA17	CA16
24H	Ch 3 A-channel C-bit buffer for Byte 2	CA23	CA22	CA21	CA20	CA19	CA18	CA17	CA16
34H	Ch 4 A-channel C-bit buffer for Byte 2	CA23	CA22	CA21	CA20	CA19	CA18	CA17	CA16
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	0	0

CA16-23: Channel Status Byte 2 for A-channel
Default: “00001000”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Ch 1 B-channel C-bit buffer for Byte 2	CB23	CB22	CB21	CB20	CB19	CB18	CB17	CB16
18H	Ch 2 B-channel C-bit buffer for Byte 2	CB23	CB22	CB21	CB20	CB19	CB18	CB17	CB16
28H	Ch 3 B-channel C-bit buffer for Byte 2	CB23	CB22	CB21	CB20	CB19	CB18	CB17	CB16
38H	Ch 4 B-channel C-bit buffer for Byte 2	CB23	CB22	CB21	CB20	CB19	CB18	CB17	CB16
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	0	0	0	0

CB16-23: Channel Status Byte 2 for B-channel
Default: “00000100”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Ch 1 A-channel C-bit buffer for Byte 3	CA31	CA30	CA29	CA28	CA27	CA26	CA25	CA24
09H	Ch 1 B-channel C-bit buffer for Byte 3	CB31	CB30	CB29	CB28	CB27	CB26	CB25	CB24
15H	Ch 2 A-channel C-bit buffer for Byte 3	CA31	CA30	CA29	CA28	CA27	CA26	CA25	CA24
19H	Ch 2 B-channel C-bit buffer for Byte 3	CB31	CB30	CB29	CB28	CB27	CB26	CB25	CB24
25H	Ch 3 A-channel C-bit buffer for Byte 3	CA31	CA30	CA29	CA28	CA27	CA26	CA25	CA24
29H	Ch 3 B-channel C-bit buffer for Byte 3	CB31	CB30	CB29	CB28	CB27	CB26	CB25	CB24
35H	Ch 4 A-channel C-bit buffer for Byte 3	CA31	CA30	CA29	CA28	CA27	CA26	CA25	CA24
39H	Ch 4 B-channel C-bit buffer for Byte 3	CB31	CB30	CB29	CB28	CB27	CB26	CB25	CB24
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

C24-31: Channel Status Byte 3
Default: “01000000”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH-0DH	Ch 1 A-channel U-bit buffer for Byte 0-3	UA7 … UA31	… …	… …	… …	… …	… …	… …	UA0 … UA24
0EH-11H	Ch 1 B-channel U-bit buffer for Byte 0-3	UB7 … UB31	… …	… …	… …	… …	… …	… …	UB0 … UB24
1AH-1DH	Ch 2 A-channel U-bit buffer for Byte 0-3	UA7 … UA31	… …	… …	… …	… …	… …	… …	UA0 … UA24
1EH-21H	Ch 2 B-channel U-bit buffer for Byte 0-3	UB7 … UB31	… …	… …	… …	… …	… …	… …	UB0 … UB24
2AH-2DH	Ch 3 A-channel U-bit buffer for Byte 0-3	UA7 … UA31	… …	… …	… …	… …	… …	… …	UA0 … UA24
2EH-31H	Ch 3 B-channel U-bit buffer for Byte 0-3	UB7 … UB31	… …	… …	… …	… …	… …	… …	UB0 … UB24
3AH-3DH	Ch 4 A-channel U-bit buffer for Byte 0-3	UA7 … UA31	… …	… …	… …	… …	… …	… …	UA0 … UA24
3EH-41H	Ch 4 B-channel U-bit buffer for Byte 0-3	UB7 … UB31	… …	… …	… …	… …	… …	… …	UB0 … UB24
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

U0-31: User Data
Default: all “0”

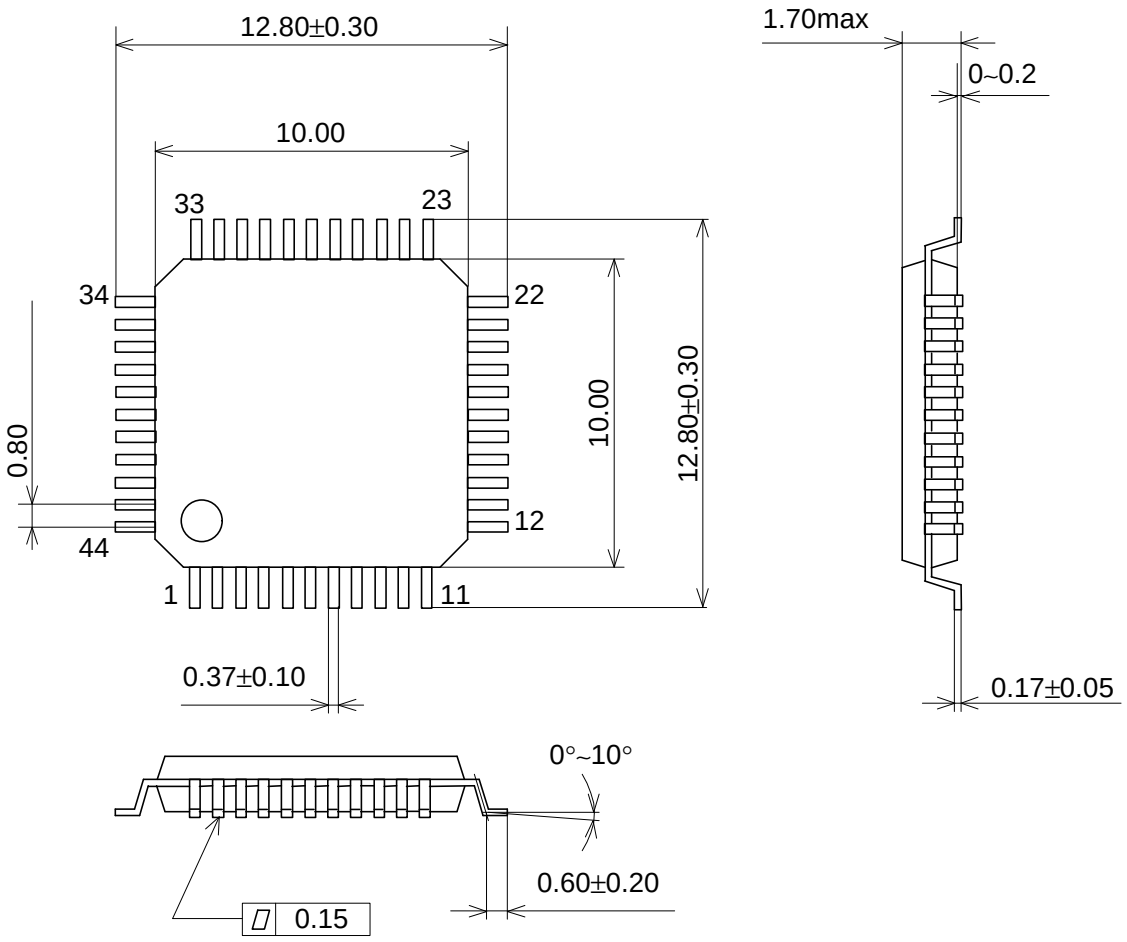
■ Default values of control registers

Bits		Default	
CRCE		1	CRCC is generated.
DIF2-0		000	16bit, Right justified
CKS1-0		00	MCLK=128fs
V4-1		0000	Valid data
FS3-0		0000	fs=44.1kHz
MUTEN		1	Normal Operation
RSTN		1	Normal Operation
Channel Status			
Byte0	- Bit0	0	Consumer Mode
	- Bit1	0	Audio Mode
	- Bit2	1	No Copyright
	- Bit3-5	000	No Emphasis
	- Bit6-7	00	Mode 0
Byte1	- Bit0-7	00000000	General Category Code
Byte2	- Bit0-3	0000	Source Number: Don't care
	- Bit4-7	1000 0100	Channel A Source channel Channel B Source channel
Byte3	- Bit0-3	0100	fs=48kHz
	- Bit4-5	00	Standard Clock Accuracy
	- Bit6-7	00	
User Data		All zeros	

Table 9. Default Values of Control Register

PACKAGE

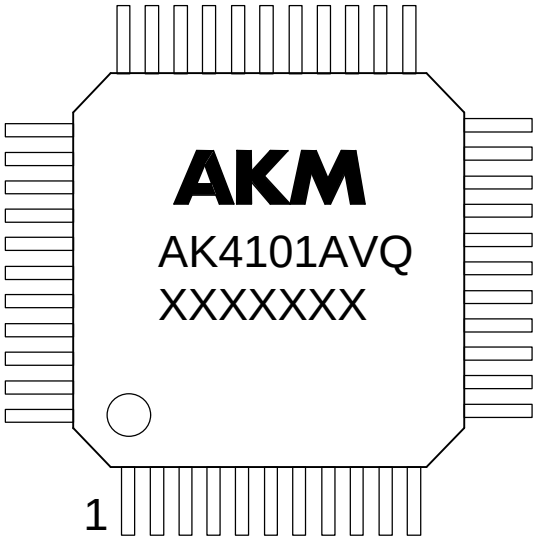
44pin LQFP (Unit: mm)



■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate (Pb free)

MARKING



1) Pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK4101AVQ
4) Asahi Kasei Logo