



AK4120

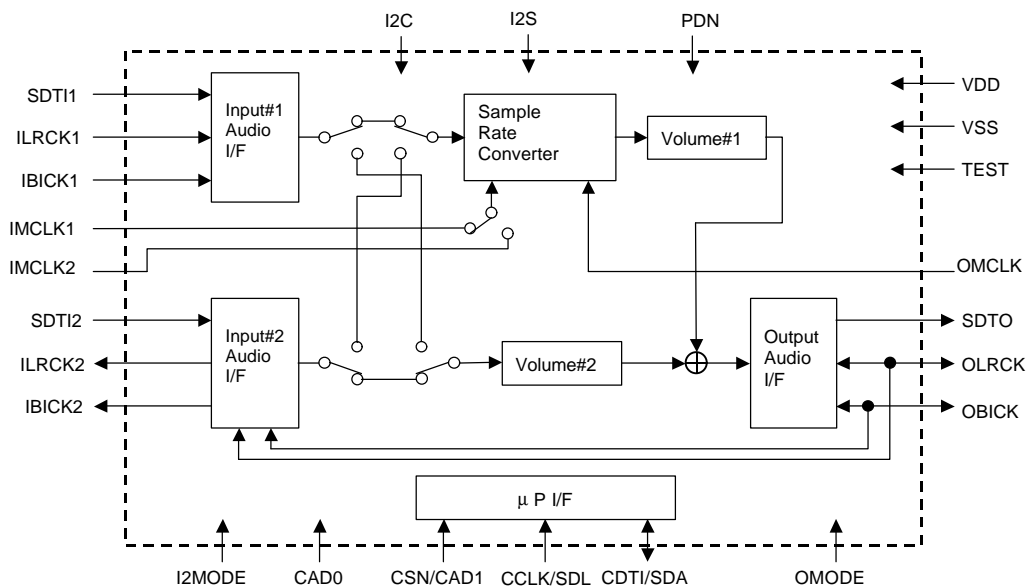
Sample Rate Converter with Mixer and Volume

GENERAL DESCRIPTION

The AK4120 is a stereo asynchronous sample rate converter. The input sample rate range is from 8kHz to 48kHz. The output sample rate is fixed at 32kHz, 44.1kHz, 48kHz or 96kHz. AK4120 includes a digital mixer and digital volume control. Applications for this device include pro audio mastering, consumer format conversion and desktop audio production and playback.

FEATURES

- Stereo Asynchronous Sample Rate Converter
- Digital Mixer
- Digital Volume
- Input Sample Rate Range (FSI): 8kHz to 48kHz
- Output Sample Rate (FSO): 32kHz, 44.1kHz, 48kHz and 96kHz
- Input to Output Sample Rate Ratio: FSO/FSI = 0.667 to 6
- THD+N: -113dB at 1kHz input
- I/F format: MSB justified (20bit), LSB justified (16bit/20bit), I²S
- Master clock: 256/512fs
- 3-wire Serial or I²C Bus μ P I/F for mode setting
- Power Supply: 2.7 to 3.6V



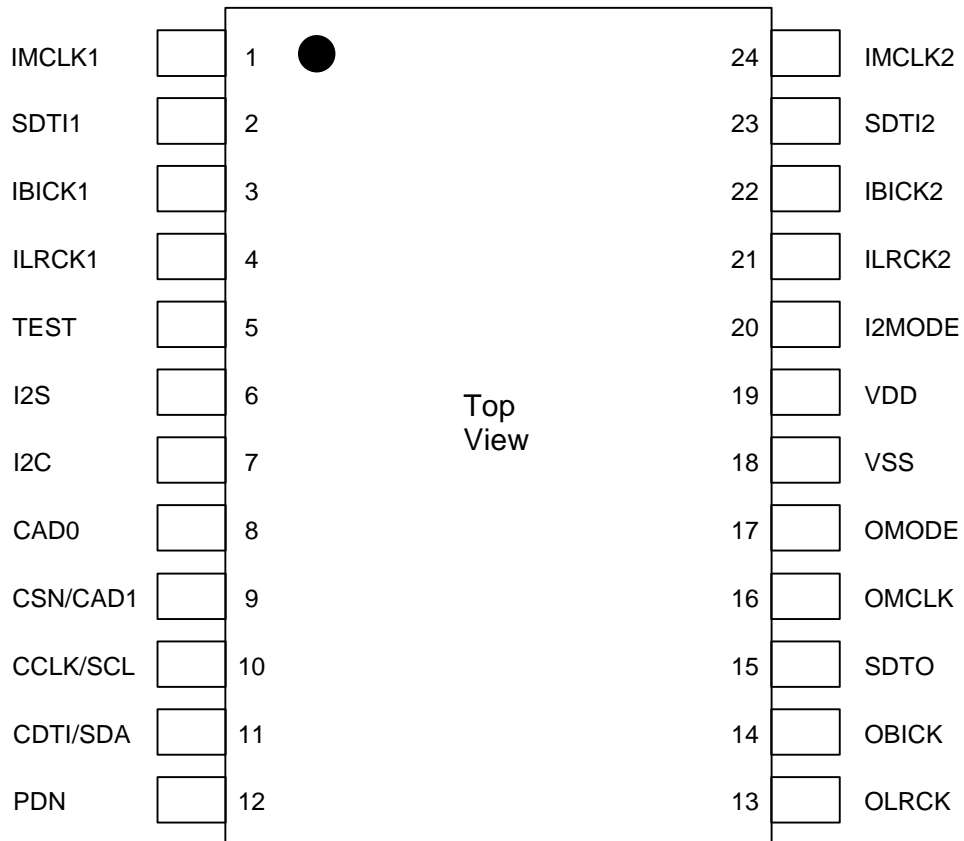
■ Ordering Guide

AK4120VF
AKD4120

-40 ~ +85°C

24pin VSOP (0.65mm pitch)
Evaluation Board for AK4120

■ Pin Layout



| |
|---------------------|
| PIN/FUNCTION |
|---------------------|

| No. | Pin Name | I/O | Function |
|-----|----------|-----|--|
| 1 | IMCLK1 | I | Master Clock Input Pin for Input#1 |
| 2 | SDTI1 | I | Audio Serial Data Input Pin for Input#1 |
| 3 | IBICK1 | I | Audio Serial Data Clock Pin for Input#1 |
| 4 | ILRCK1 | I | L/R Clock Pin for Input#1 |
| 5 | TEST | I | Test Pin. Connect to VSS. |
| 6 | I2S | I | Audio I/F Select Pin “L”: Set by Register, “H”: I ² S |
| 7 | I2C | I | I ² C Select Pin. “L”: 3-wire, “H”: I ² C |
| 8 | CAD0 | I | Chip Address 0 Pin |
| 9 | CSN | I | Chip Select Pin in 3wire serial control mode in 3-wire Serial Control Mode. |
| | CAD1 | I | Chip Address 1 Pin in I ² C control mode. |
| 10 | CCLK | I | Control Data Clock Pin in 3wire serial control mode in 3-wire Serial Control Mode. |
| | SCL | I | Control Data Clock Pin in I ² C control mode. |
| 11 | CDTI | I | Control Data Input Pin in 3wire serial control mode in 3-wire Serial Control Mode. |
| | SDA | I/O | Control Data Pin in I ² C serial control mode in I ² C control mode. |
| 12 | PDN | I | Power-Down pin When “L”, the AK4120 is powered-down and reset. |
| 13 | OLRCK | I/O | L/R Clock Pin for Output |
| 14 | OBICK | I/O | Audio Serial Data Clock Pin for Output |
| 15 | SDTO | O | Audio Serial Data Pin for Output |
| 16 | OMCLK | I | Master Clock Pin for Output |
| 17 | OMODE | I | Master/Slave select pin for Output Audio Data “L”: Slave, “H”: Master |
| 18 | VSS | I | Digital Ground Pin |
| 19 | VDD | I | Digital Power Supply Pin, 3.3V |
| 20 | I2MODE | I | Master/Slave select pin for Input Audio Data #2 “L”: Slave, “H”: Master |
| 21 | ILRCK2 | I/O | L/R Clock Pin for Input#2 |
| 22 | IBICK2 | I/O | Audio Serial Data Clock Pin for Input#2 |
| 23 | SDTI2 | I | Audio Serial Data Input Pin for Input#2 |
| 24 | IMCLK2 | I | Master Clock Input Pin for Input#2 |

| |
|---------------------------------|
| ABSOLUTE MAXIMUM RATINGS |
|---------------------------------|

(VSS=0V; Note 1)

| Parameter | Symbol | min | max | Units |
|--|--------|------|---------|-------|
| Power Supplies | VDD | -0.3 | 4.6 | V |
| Input Current, Any Pin Except Supplies | IIN | - | ±10 | mA |
| Input Voltage | VIN | -0.3 | VDD+0.3 | V |
| Ambient Temperature (Power applied) | Ta | -40 | 85 | °C |
| Storage Temperature | Tstg | -65 | 150 | °C |

Note 1: All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

| |
|---|
| RECOMMENDED OPERATING CONDITIONS |
|---|

(VSS=0V; Note 2)

| Parameter | Symbol | min | typ | max | Units |
|----------------|--------|-----|-----|-----|-------|
| Power Supplies | VDD | 2.7 | 3.3 | 3.6 | V |

Note 2: All voltages with respect to ground.

| |
|------------------------|
| SRC PERFORMANCE |
|------------------------|

(Ta=-40~ 85°C; VDD = 2.7~3.6V; data = 20bit; measurement bandwidth = 20Hz~ FSO/2; unless otherwise specified.)

| Parameter | Symbol | min | typ | max | Units |
|--|---------|-------|------|------|-------|
| Resolution | | | | 20 | Bits |
| Input Sample Rate (Note 3) | FSI | 8 | | 48 | kHz |
| Output Sample Rate (Note 4) | FSO | 32 | | 96 | kHz |
| Dynamic Range (Input= 1kHz, -60dBFS, Note 5) | | | | | |
| FSO/FSI=44.1kHz/48kHz | | - | 115 | - | dB |
| FSO/FSI=48kHz/44.1kHz | | - | 116 | - | dB |
| FSO/FSI=32kHz/48kHz | | - | 114 | - | dB |
| FSO/FSI=96kHz/32kHz | | - | 119 | - | dB |
| Worst Case (FSO/FSI=32kHz/48kHz) | | 112 | - | - | dB |
| Dynamic Range (Input= 1kHz, -60dBFS, A-weighted, Note 5) | | | | | |
| FSO/FSI=44.1kHz/48kHz | | - | 117 | - | dB |
| THD+N (Input= 1kHz, 0dBFS, Note 5) | | | | | |
| FSO/FSI=44.1kHz/48kHz | | - | -112 | - | dB |
| FSO/FSI=48kHz/44.1kHz | | - | -113 | - | dB |
| FSO/FSI=32kHz/48kHz | | - | -111 | - | dB |
| FSO/FSI=96kHz/32kHz | | - | -111 | - | dB |
| Worst Case (FSO/FSI=48kHz/8kHz) | | - | - | -103 | dB |
| Ratio between Input and Output Sample Rate (FSO/FSI, Note 6, Note 7) | FSO/FSI | 0.667 | | 6 | - |

Note 3. 32kHz~96kHz for INPUT#2 at Path Mode 0. 8kHz~96kHz at Path Mode 2 and 3.

Note 4. Min = 8kHz at Path Mode 2 and 3.

Note 5. Measured by Rohde & Schwarz UPD04, Rejection Filter= wide, 8192point FFT. Refer Figure 1 and Figure 2.

Note 6. The "0.667" is the ratio of FSO/FSI when FSI is 48kHz and FSO is 32kHz

Note 7. The "6" is the ratio when FSI is 8kHz and FSO is 48kHz.

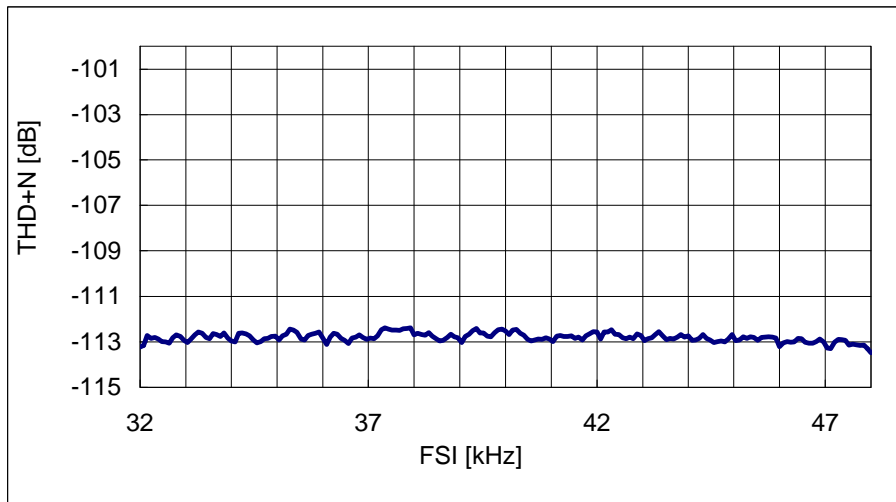


Figure 1: Input Sample Rate (FSI) vs. THD+N (FSO=48kHz)

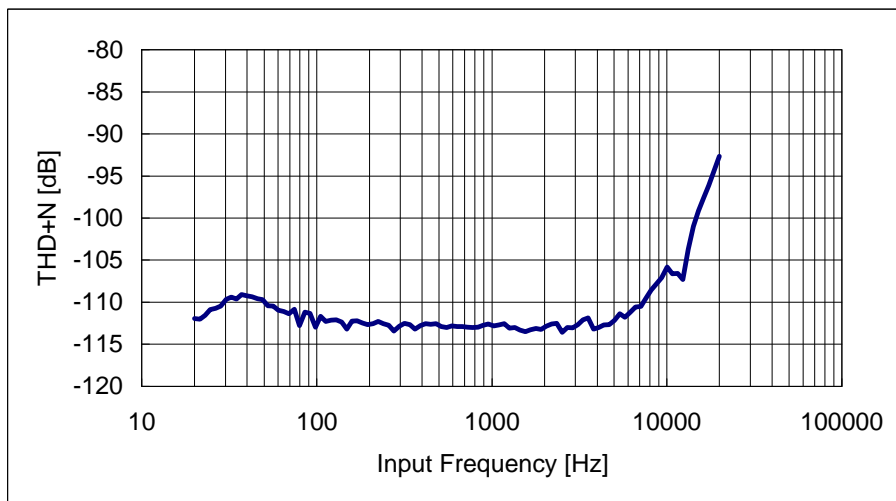


Figure 2: Input Frequency vs. THD+N (FSI=44.1kHz, FSO=48kHz)

DIGITAL FILTER

(Ta=-40~ 85°C; VDD=2.7~3.6V; FSO=FSI=fs)

| Parameter | Symbol | min | typ | max | Units |
|----------------------|----------|-----|----------|----------|-------|
| Digital Filter | | | | | |
| Passband (Note 8) | -0.001dB | PB | 0 | 0.4583fs | kHz |
| Stopband (Note 8) | | SB | 0.5417fs | | kHz |
| Passband Ripple | | PR | | ± 0.01 | dB |
| Stopband Attenuation | | SA | 97 | | dB |
| Group Delay (Note 9) | | GD | - | 56.5 | 1/fs |

Note 8. The passband and stopband frequencies scale with fs (system sampling rate).

Note 9. This value is the time from the rising edge of LRCK after data is input to rising edge of LRCK after data is output, when LRCK for Output data corresponds with LRCK for Input.(at 20bit MSB justified, 16bit and 20bit LSB justified)

DC CHARACTERISTICS

(Ta=-40~85°C; VDD=2.7~3.6V)

| Parameter | Symbol | min | typ | Max | Units |
|--|------------|---------|---------------------------|---------------------|----------------------|
| Power Supply Current Normal operation: (PDN = "H", Path Mode 0) FSI=FSO=48kHz at Slave Mode (I2MODE= OMODE = "L"): VDD=3.3V FSI=48kHz,FSO=96kHz at Master Mode (I2MODE=OMODE= "H") : VDD=3.3V : VDD=3.6V Power down: PDN = "L" (Note 10) | | | 8.5 10.2 11.5 10 | - - 20 100 | mA mA mA μA |
| High-Level Input Voltage | VIH | 0.7xVDD | - | - | V |
| Low-Level Input Voltage | VIL | - | - | 0.3xVDD | V |
| High-Level Output Voltage (Iout=-400μA) | VOH | VDD-0.4 | - | - | V |
| Low-Level Output Voltage (Except SDA pin: Iout=400μA); (SDA pin: Iout= 3mA) | VOL VOL | - - | - - | 0.4 0.4 | V V |
| Input Leakage Current | Iin | - | - | ± 10 | μA |

Note 10. All digital inputs including clock pins are held VSS.

| SWITCHING CHARACTERISTICS | | | | | |
|--|--------|-------|-----|--------|-------|
| (Ta=-40~ 85°C; VDD=2.7~3.6V; CL=20pF) | | | | | |
| Parameter | Symbol | min | typ | max | Units |
| Master Clock Input (IMCLK1) | | | | | |
| Frequency | fCLK | 2.048 | | 24.576 | MHz |
| Duty Cycle (at FSI > 33kHz) | dCLK | 40 | | 60 | % |
| Duty Cycle (at FSI ≤ 33kHz) | dCLK | 28 | | 72 | % |
| Master Clock Input (IMCLK2) | | | | | |
| Frequency | fCLK | 2.048 | | 24.576 | MHz |
| Duty Cycle (at FSI > 33kHz) | dCLK | 40 | | 60 | % |
| Duty Cycle (at FSI ≤ 33kHz) | dCLK | 28 | | 72 | % |
| Master Clock Input (OMCLK) | | | | | |
| Frequency (Note 11) | fCLK | 8.192 | | 24.576 | MHz |
| Duty Cycle (at FSI > 33kHz) | dCLK | 40 | | 60 | % |
| Duty Cycle (at FSI ≤ 33kHz) | dCLK | 28 | | 72 | % |
| L/R clock for Input data #1 (ILRCK1) | | | | | |
| Frequency | fs | 8 | | 48 | kHz |
| Duty Cycle | Duty | 48 | 50 | 52 | % |
| L/R clock for Input data #2 (ILRCK2) | | | | | |
| Frequency (Note 12) | fs | 8 | | 96 | kHz |
| Duty Cycle Slave Mode | Duty | 48 | 50 | 52 | % |
| Duty Cycle Master Mode | Duty | | 50 | | % |
| L/R clock for Output data (OLRCK) | | | | | |
| Frequency (Note 13) | fs | 32 | | 96 | kHz |
| Duty Cycle Slave Mode | Duty | 48 | 50 | 52 | % |
| Duty Cycle Master Mode | Duty | | 50 | | % |
| Audio Interface Timing (Note 14) | | | | | |
| Input#1 at Path Mode 0 and 2 | | | | | |
| Input#2 (Slave Mode) at Path Mode 1 | | | | | |
| BICK Period | tBCK | 325 | | | ns |
| BICK Pulse Width Low | tBCKL | 130 | | | ns |
| BICK Pulse Width High | tBCKH | 130 | | | ns |
| LRCK Edge to BICK “↑” (Note 15) | tBLR | 45 | | | ns |
| BICK “↑” to LRCK Edge (Note 15) | tLRB | 45 | | | ns |
| SDTI1-2, Hold Time from BICK “↑” | tSDH | 40 | | | ns |
| SDTI1-2, Setup Time to BICK “↑” | tSDS | 25 | | | ns |
| Input#2 (Slave Mode) at Path Mode 0 and 3 | | | | | |
| BICK Period | tBCK | 162 | | | ns |
| BICK Pulse Width Low | tBCKL | 65 | | | ns |
| BICK Pulse Width High | tBCKH | 65 | | | ns |
| LRCK Edge to BICK “↑” (Note 15) | tBLR | 45 | | | ns |
| BICK “↑” to LRCK Edge (Note 15) | tLRB | 45 | | | ns |
| SDTI2, Hold Time from BICK “↑” | tSDH | 40 | | | ns |
| SDTI2, Setup Time to BICK “↑” | tSDS | 25 | | | ns |
| Output (Slave Mode) | | | | | |
| OBICK Period | tBCK | 162 | | | ns |
| OBICK Pulse Width Low | tBCKL | 65 | | | ns |
| OBICK Pulse Width High | tBCKH | 65 | | | ns |
| OLRCK Edge to OBICK “↑” (Note 15) | tBLR | 45 | | | ns |
| OBICK “↑” to OLRCK Edge (Note 15) | tLRB | 45 | | | ns |
| OLRCK to SDTO (MSB) | tLRS | | | 40 | ns |
| OBICK “↓” to SDTO | tBSD | | | 40 | ns |

| Parameter | Symbol | min | typ | max | Units |
|--|--------|-----|------|-----|-------|
| Audio Interface Timing | | | | | |
| Input#2(Master Mode) at Path Mode 1 | | | | | |
| BICK Frequency | fBCK | | 64fs | | Hz |
| BICK Duty | dBCK | | 50 | | % |
| BICK “↓” to LRCK | tMBLR | -25 | | 25 | ns |
| BICK “↓” to SDTO | tBSD | -25 | | 40 | ns |
| SDTI2 Hold Time from BICK “↑” | tSDH | 50 | | | ns |
| SDTI2 Setup Time to BICK “↑” | tSDS | 50 | | | ns |
| Input#2 (Master Mode) at Path Mode0 and 3 | | | | | |
| Output (Master Mode) | | | | | |
| BICK Frequency | fBCK | | 64fs | | Hz |
| BICK Duty | dBCK | | 50 | | % |
| BICK “↓” to LRCK | tMBLR | -20 | | 20 | ns |
| BICK “↓” to SDTO | tBSD | -20 | | 30 | ns |
| SDTI2 Hold Time from BICK “↑” | tSDH | 40 | | | ns |
| SDTI2 Setup Time to BICK “↑” | tSDS | 25 | | | ns |

Note 11. Min is 2.048MHz at Path Mode 2 and 3.

Note 12. Max is 48kHz at Path Mode 1

Note 13. Min is 8kHz at Path Mode 2 and 3.

Note 14. BICK means all audio serial data clocks (IBICK1, IBICK2 and OBICK).

LRCK means all L/R clocks (ILRCK1, ILRCK2 and OLRCK).

Note 15. BICK rising edge must not occur at the same time as LRCK edge.

| Parameter | Symbol | min | typ | max | Units |
|---|---------|------|-----|-----|-------|
| Control Interface Timing (3-wire Serial mode): | | | | | |
| CCLK Period | tCCK | 200 | | | ns |
| CCLK Pulse Width Low | tCCKL | 80 | | | ns |
| Pulse Width High | tCCKH | 80 | | | ns |
| CDTI Setup Time | tCDS | 40 | | | ns |
| CDTI Hold Time | tCDH | 40 | | | ns |
| CSN "H" Time | tCSW | 150 | | | ns |
| CSN "↓" to CCLK "↑" | tCSS | 50 | | | ns |
| CCLK "↑" to CSN "↑" | tCSH | 50 | | | ns |
| Control Interface Timing (I²C Bus mode): | | | | | |
| SCL Clock Frequency | fSCL | - | | 100 | kHz |
| Bus Free Time Between Transmissions | tBUF | 4.7 | | - | μs |
| Start Condition Hold Time (prior to first clock pulse) | tHD:STA | 4.0 | | - | μs |
| Clock Low Time | tLOW | 4.7 | | - | μs |
| Clock High Time | tHIGH | 4.0 | | - | μs |
| Setup Time for Repeated Start Condition | tSU:STA | 4.7 | | - | μs |
| SDA Hold Time from SCL Falling (Note 10) | tHD:DAT | 0 | | - | μs |
| SDA Setup Time to SCL Rising | tSU:DAT | 0.25 | | - | μs |
| Rise Time of Both SDA and SCL Lines | tR | - | | 1.0 | μs |
| Fall Time of Both SDA and SCL Lines | tF | - | | 0.3 | μs |
| Setup Time for Stop Condition | tSU:STO | 4.0 | | - | μs |
| Maximum Pulse Width of Spike Noise Suppressed by Input Filter | tSP | | 30 | | ns |
| Power-down & Reset Timing | | | | | |
| PDN Pulse Width (Note 11) | tPD | 150 | | | ns |

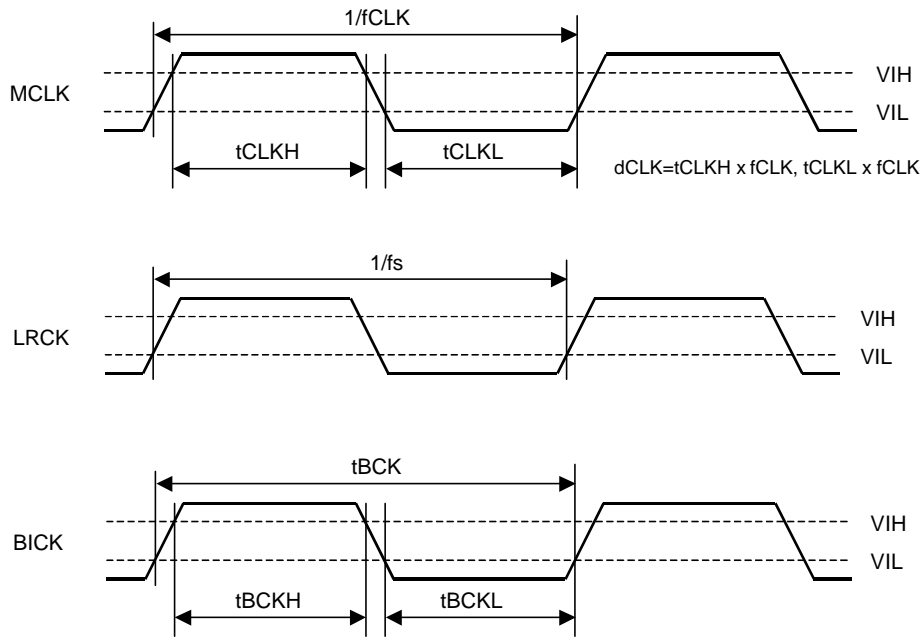
Note 10. Data must be held long enough to bridge the 300 ns transition time of SCL.

Note 11. The AK4120 can be reset by bringing PDN "L" to "H" upon power-up.

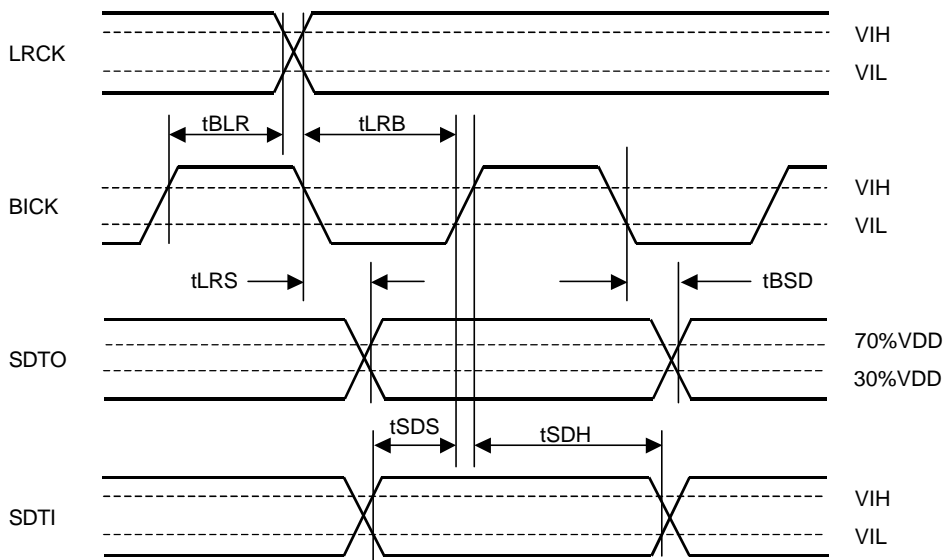
Note 12. I²C is a registered trademark of Philips Semiconductors.

Purchase of Asahi Kasei Microsystems Co., Ltd I²C components conveys a license under the Philips I²C patent to use the components in the I²C system, provided the system conform to the I²C specifications defined by Philips.

■ Timing Diagram

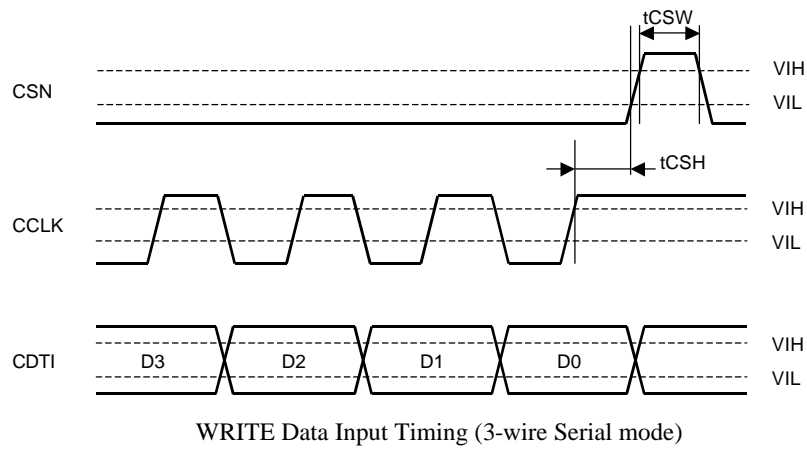
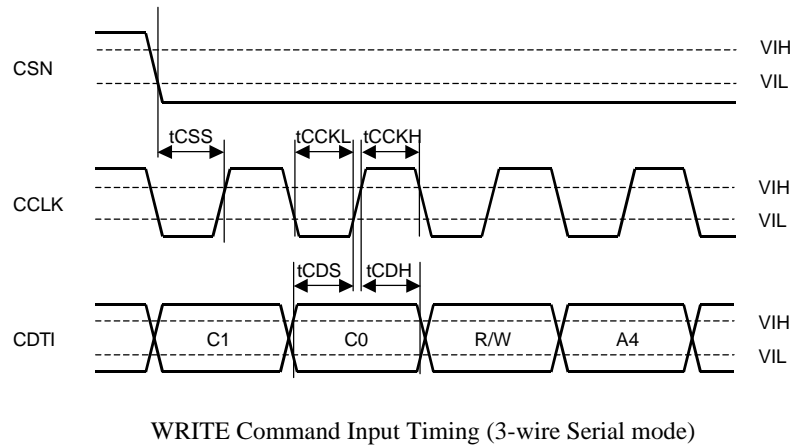
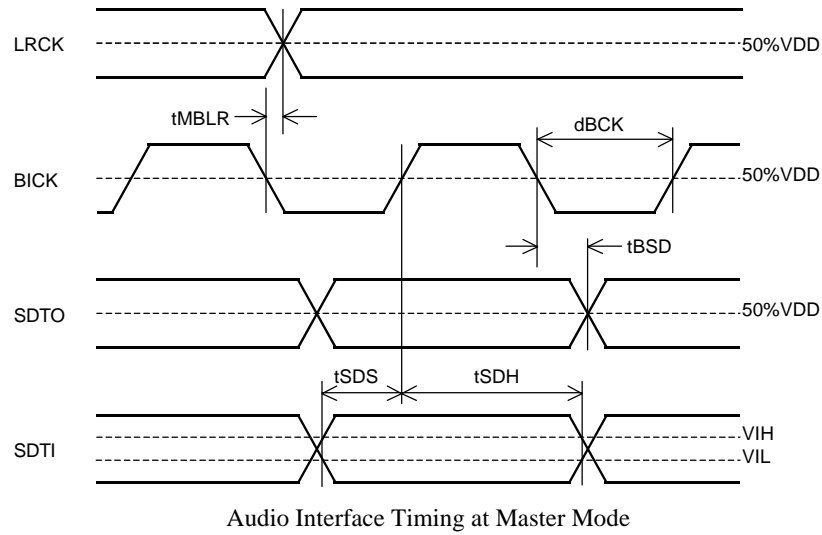


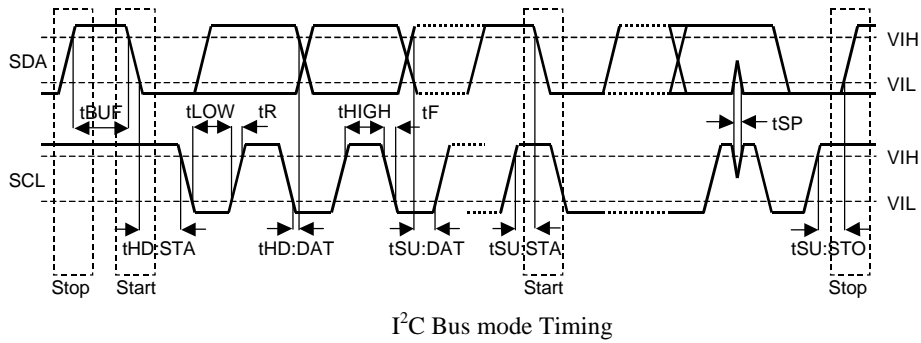
Clock Timing



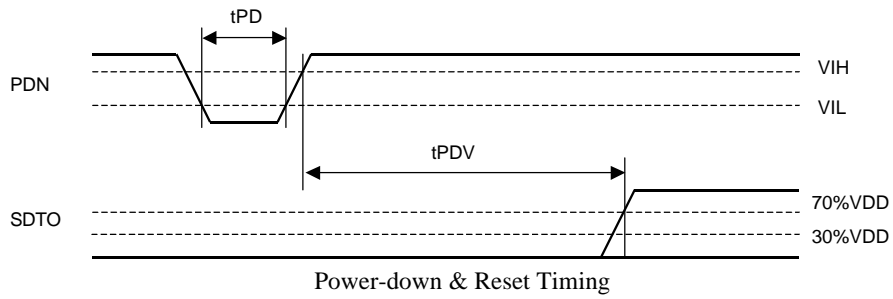
Audio Interface Timing at Slave Mode

Note: MCLK means IMCLK1, IMCLK2 and OCLK.
 BICK means IBICK1, IBICK2 and OBICK.
 LRCK means ILRCK1, ILRCK2 and OLRCK.
 SDTI means SDTI1 and SDTI2.





I²C Bus mode Timing



Power-down & Reset Timing

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|---------------------------|
| OPERATION OVERVIEW |
|---------------------------|

■ I/O Data flow

The AK4120 has two input audio data interfaces (Input#1 and Input#2). The AK4120 has four modes of operation, each corresponding to a different internal audio path as shown in Table 1. These path modes are selected by the PATH1-0 bits.

| Path Mode | PATH1-0 bits | Output Data |
|---------------------|--------------|---|
| 0 (see Figure 3) | “00” | The sample rate of Input#1 data is converted by SRC block. This converted data paths through Volume#1 and Input#2 data is paths through Volume#2. These data are mixed and this mixed data is output. The sample rata of Input#1 is defined by IMCLK1 and the sample rate of Output data is defined by OMCLK. The sample rate of Input#2 should be same as Output data. |
| 1 (see Figure 4) | “01” | The sample rate of Input#2 data is converted by SRC block. This converted data volume is controlled by Volume#1 and this data is output. The sample rata of Input#2 is defined by IMCLK2 and the sample rate of Output data is defined by OMCLK. |
| 2 (see Figure 5) | “10” | Input#1 data paths through Volume#2 and is output. Output data should synchronous with IMCLK. |
| 3 (see Figure 6) | “11” | Input#2 data paths through Volume#2 and is output. Input#2 should synchronous with OMCLK. |

Table 1. Path Mode

Note: When Path Mode is changed, the AK4120 should be powered down using the “PW” bit

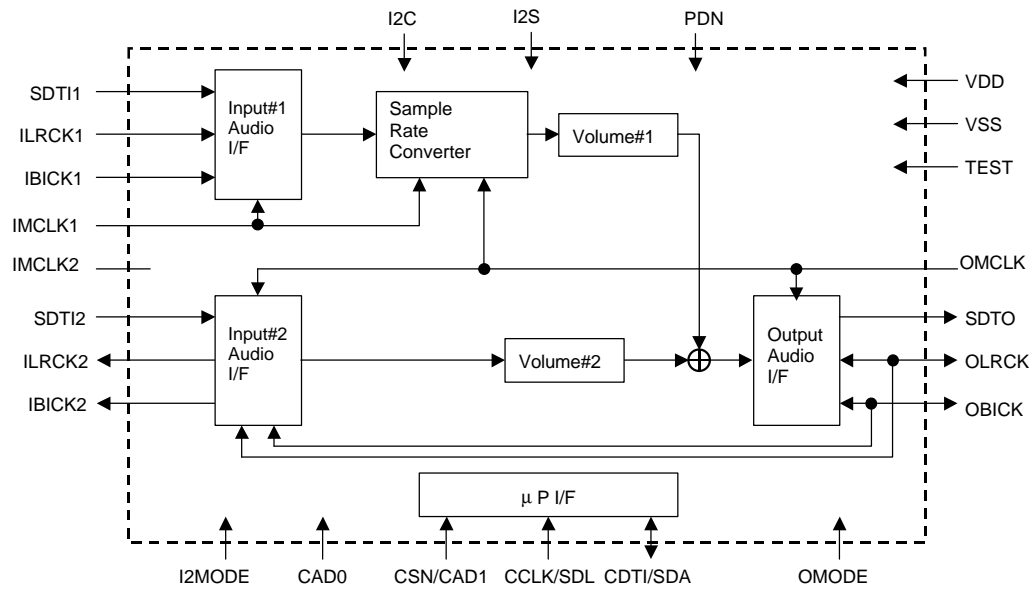


Figure 3. Path Mode 0 (Input#1 SRC + Mixer)

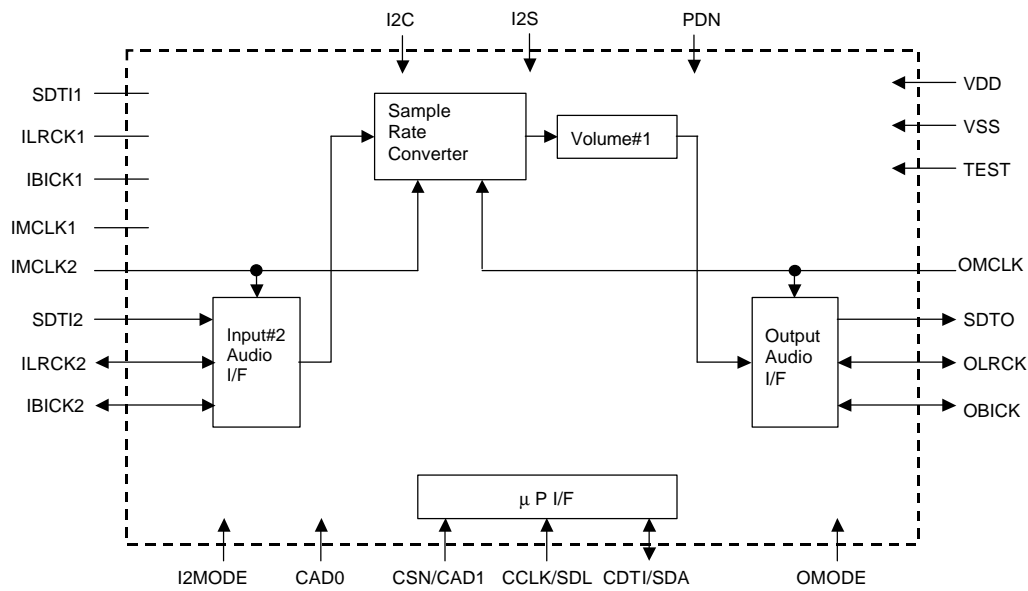


Figure 4. Path Mode 1 (Input#2 SRC)

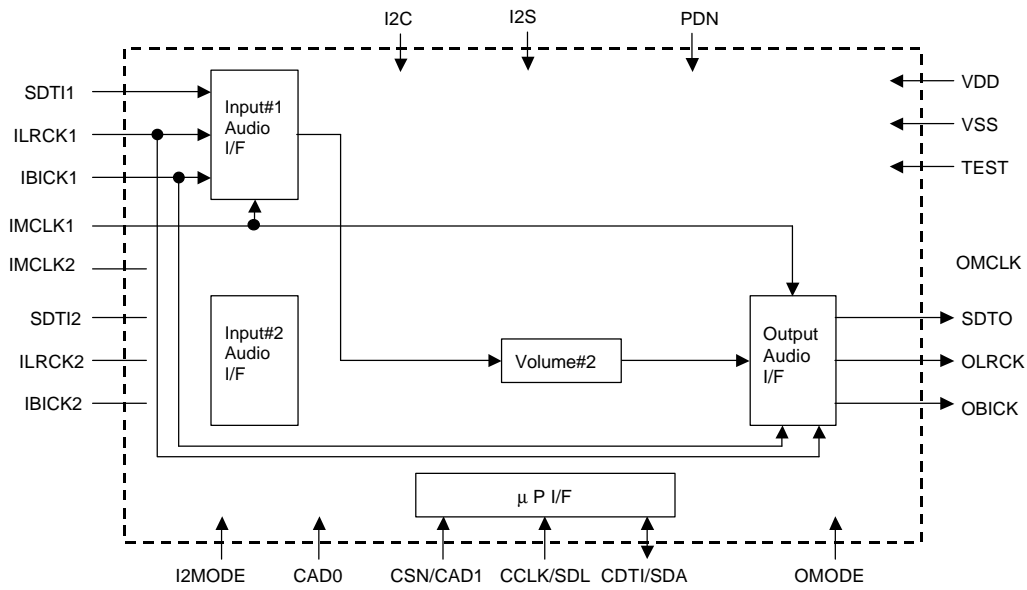


Figure 5. Path Mode 2 (Input#1 through output)

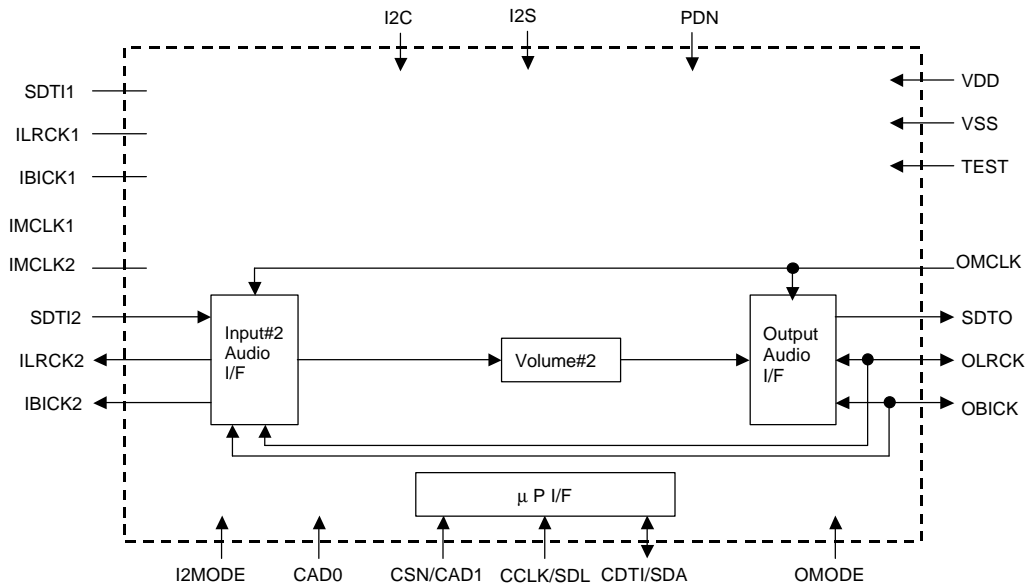


Figure 6. Path Mode 3 (Input#2 through output)

■ System Clock

The external clocks required to operate the AK4120 in each mode are shown in Table 3 and Table 4. The Input#1 port works in slave mode only. The Input#2 and Output ports have both slave and master modes that are selected by the IMODE2 and OMODE pins. The required external clock shown in Table 2 should be always present whenever the AK4120 is in a normal operating mode (PDN="H").

| Path Mode | Synchronizing Group A | SRC | Synchronizing Group B | (Not used) |
|-----------|-----------------------|------------|-----------------------|------------|
| 0 | SDTI1 | Active | SDTI2, SDTO | - |
| 1 | SDTI2 | Active | SDTO | SDTI1 |
| 2 | SDTI1, SDTO | (Not used) | - | SDTI2 |
| 3 | SDTI2, SDTO | (Not used) | - | SDTI1 |

Table 2. Clock Synchronization

| Path Mode | IMCLK1 | IMCLK2 | OMCLK |
|-----------|------------|------------|------------|
| 0 | Input | (Not used) | Input |
| 1 | (Not used) | Input | Input |
| 2 | Input | (Not used) | (Not used) |
| 3 | (Not used) | (Not used) | Input |

Table 3. Master Clock

| Path Mode | ILRCK1, IBICK1 | ILRCK2, IBICK2 | | OLRC, OBICK | |
|-----------|----------------|----------------|--------------|-------------|-----------|
| | | I2MODE = "L" | I2MODE = "H" | OMODE="L" | OMODE="H" |
| 0 | Input | (Not used) | Output | Input | Output |
| 1 | (Not used) | Input | Output | Input | Output |
| 2 | Input | (Not used) | (Not used) | (Not used) | Output |
| 3 | (Not used) | (Not used) | Output | Input | Output |

Table 4. LRCK/BICK

(1) Path Mode 0

IMCLK1 does not need to be synchronized with OMCLK when using Path Mode 1. IMCLK1 should be synchronized with ILRCK1 (clock phase is not important). SDTI2 should be synchronized with OLRCK and OBICK. When the output is slaved, OMCLK should be synchronized with OLRCK (clock phase is not important). When input#2 is in slave mode, OLRCK and OBICK are used while ILRCK2 and IBICK2 are not.

(2) Path Mode 1

IMCLK2 does not need to be synchronized with OMCLK. When Input#2 port is in slave mode, IMCLK2 should be synchronized with ILRCK2 (clock phase is not important). When Output#2 port is in slave mode, OMCLK should be synchronized with OLRCK (clock phase is not important).

(3) Path Mode 2

IMCLK1 should be synchronized with ILRCK1 (clock phase is not important). SDTO should be synchronized with ILRCK1 and IBICK1. When the Output is in slave mode, the OLRCK and OBICK pins are not used. In master mode, ILRCK1 is output through OLRCK and IBICK1 is output through OBICK.

(4) Path Mode 3

OMCLK should be synchronized with OLRCK (clock phase is not important). SDTI2 should be synchronized with OLRCK and OBICK. When Input#2 is in slave mode, ILRCK2 and IBICK2 pins are not used. In master mode, OLRCK is output through ILRCK2 and OBICK is output through IBICK2.

The frequency of IMCLK1, IMCLK2, and OMCLK are fixed based on the sampling rate and clock speed (256fs/512fs). IMCKS1, IMCKS2 and OMCKS bits in register 01H select clock speed.

| LRCK | MCLK (MHz) | | BICK (MHz) |
|---------|------------|---------|------------|
| | 256fs | 512fs | |
| fs | 256fs | 512fs | 64fs |
| 32.0kHz | 8.1920 | 16.384 | 2.0480 |
| 44.1kHz | 11.2896 | 22.5792 | 2.8224 |
| 48.0kHz | 12.2880 | 24.576 | 3.0720 |
| 88.2kHz | 22.5792 | N/A | 5.6448 |
| 96kHz | 24.5760 | N/A | 6.1440 |

Table 5. System Clock Example

■ Volume

AK4120 has two digital volumes (Volume#1 and Volume#2). Volume#1 can control the volume level of data from Input#1 while in Path Mode 0 or from Input#2 while in Path Mode 1. It then passes this data through SRC block. Volume#2 can control the volume level of data from Input#2 while in Path Mode 0 and Path Mode 3, or from Input#1 in Path Mode 2. These volume ranges are from -83.25dB to 12dB in 0.75dB steps. The volume level and mute of each channel can be controlled by register 3-6H.

■ Audio Serial Interface Format

Four serial data modes can be selected by the I2S pin and D5-D0 bits in register 00H as shown in Table 6~8. In all modes the serial audio data is MSB-first, 2's complement format. The SDTO is clocked out on the falling edge of BICKO and the SDTI1 and SDTI2 are latched on the rising edge of BICKI1 and BICKI2.

| I2S pin | DIFI11 | DIFI10 | SDTI1 | LRCK | Default |
|---------|--------|--------|-------------------------|------|---------|
| L | 0 | 0 | 20bit, MSB justified | H/L | |
| L | 0 | 1 | 20bit, I ² S | L/H | |
| L | 1 | 0 | 20bit, LSB justified | H/L | |
| L | 1 | 1 | 16bit, LSB justified | H/L | |
| H | X | X | 20bit, I ² S | L/H | |

Table 6. Audio data formats for Input#1 port

| I2S pin | DIFI21 | DIFI20 | SDTI2 | LRCK | Default |
|---------|--------|--------|-------------------------|------|---------|
| L | 0 | 0 | 20bit, MSB justified | H/L | |
| L | 0 | 1 | 20bit, I ² S | L/H | |
| L | 1 | 0 | 20bit, LSB justified | H/L | |
| L | 1 | 1 | 16bit, LSB justified | H/L | |
| H | X | X | 20bit, I ² S | L/H | |

Table 7. Audio data formats for Input#2 port

| I2S pin | DIFO1 | DIFO0 | SDTO | LRCK | Default |
|---------|-------|-------|-------------------------|------|---------|
| L | 0 | 0 | 20bit, MSB justified | H/L | |
| L | 0 | 1 | 20bit, I ² S | L/H | |
| L | 1 | 0 | 20bit, LSB justified | H/L | |
| L | 1 | 1 | 16bit, LSB justified | H/L | |
| H | X | X | 20bit, I ² S | L/H | |

Table 8. Audio data formats for Output port

Note: When the Audio Serial Interface Mode is changed, the AK4120 should be powered down using the PW bit. ("PW"=0)

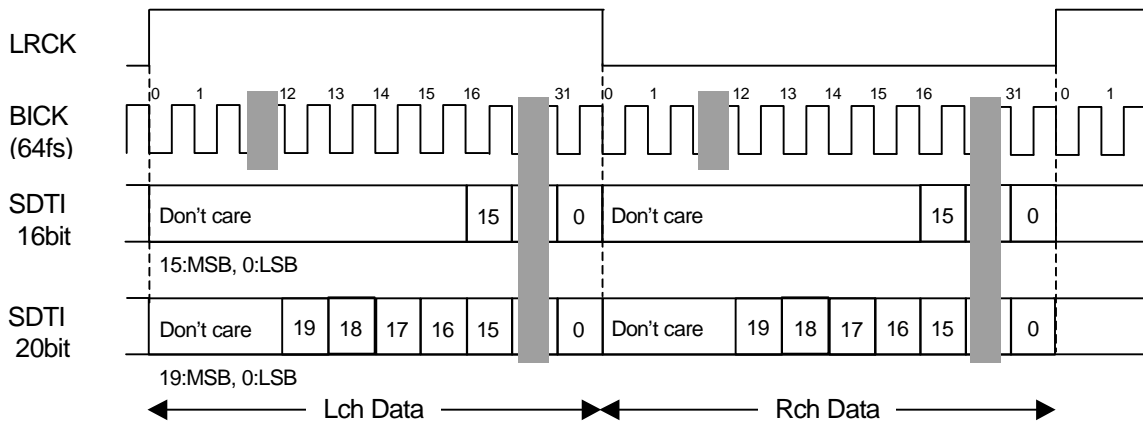


Figure 7. LSB justified Timing

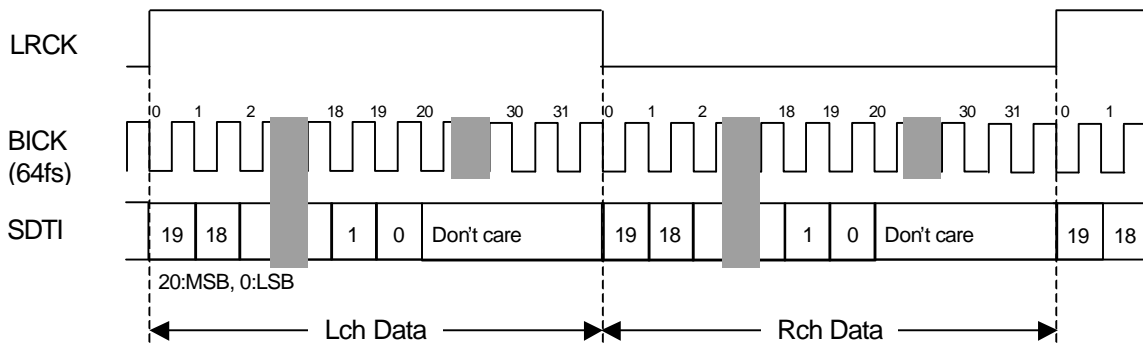


Figure 8. MSB justified Timing

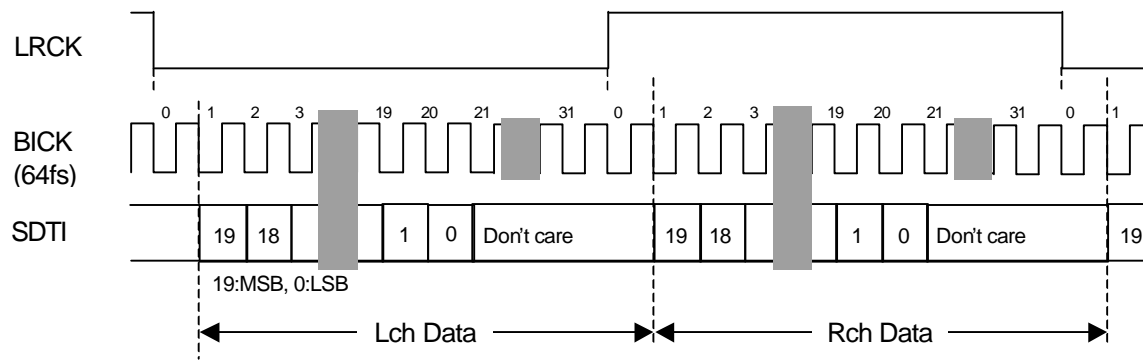


Figure 9. I²S Timing

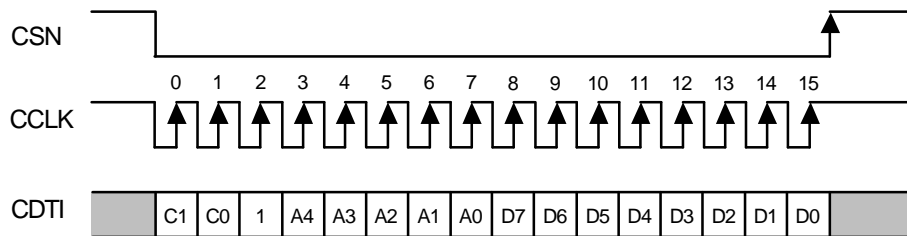
■ Serial Control Interface

The AK4120 is controlled via registers. Internal registers can be written using one of two control modes, I2C or 3-wire, that are selected via I2C pin. PDN = “L” initializes the registers to their default values. When the I2C pin is changed, the AK4120 should be reset using the PDN pin.

- * When PDN= “L”, internal registers cannot be written.
- * The AK4120 does not support the read command while using the 3-wire Serial Control Mode.

(1) 3-wire Serial Control Mode (I2C = “L”)

Internal registers may be written to using the 3 wire μ P interface pins (CSN, CCLK and CDTI). The data on this interface consists of a Chip address that is fixed to “10” and a Read/Write status (1bit, Fixed to “1”; Write only). Also a Register address (MSB first, 5bits) and Control data (MSB first, 8bits) are used. Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after a low-to-high transition of CSN. The clock speed of CCLK is 5MHz(max)



C1-C0: Chip Address (C1:1,C0:CAD0)
 R/W: Read/Write (Fixed to “1” : Write only)
 A4-A0: Register Address
 D7-D0: Control Data

Figure 10. 3-wire Serial Control I/F Timing

Note: Do not write to the address except 00H through 06H.

2) I²C-bus Control Mode (I2C= "H")

The AK4120 supports the standard I²C-bus interface (max:100kHz). Then AK4120 cannot support fast-mode I²C (max: 400kHz).

(2)-1. WRITE Operations

Figure 11 shows the data transfer sequence in I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 17). After the START condition, a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/WN). The most significant five bits of the slave address are fixed as "00100". The next two bits are CAD1 and CAD0 (device address bits). These two bits identify the specific device on the bus. The hard-wired input pins (CAD1 pin and CAD0 pin) set them (Figure 12). If the slave address matches that of the AK4120, the AK4120 generates the acknowledge and the operation is executed. The master must generate an acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 18). A "1" for R/WN bit indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

The second byte is the control register address of the AK4120. The format is MSB first, and three most significant bits are fixed to zero (Figure 13). Subsequent bytes contain control data. The format is MSB first, 8-bits (Figure 14). The AK4120 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 17).

The AK4120 is capable of more than one byte write operation per sequence. After receipt of the third byte, the AK4120 generates an acknowledge, and awaits the next data. The master can transmit multiple bytes rather than terminating the write cycle after the first data byte is transferred. After the receipt of each data, the internal 5-bit address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 06H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten. (If an address greater than 07H is set, this function will not work properly.)

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 19) except for START and STOP conditions.

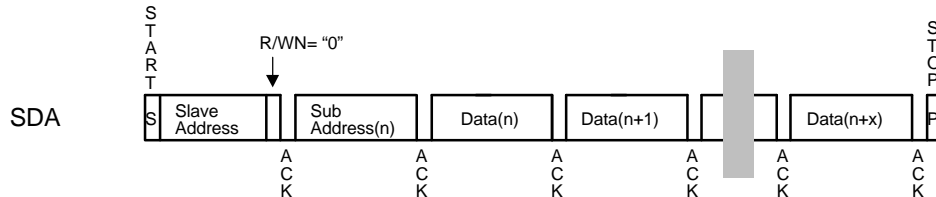


Figure 11. Data transfer sequence at the I²C-bus mode

| | | | | | | | |
|---|---|---|---|---|------|------|------|
| 0 | 0 | 1 | 0 | 0 | CAD1 | CAD0 | R/WN |
|---|---|---|---|---|------|------|------|

(Those CAD1/0 should match with CAD1/0 pins)

Figure 12. The first byte

| | | | | | | | |
|---|---|---|----|----|----|----|----|
| 0 | 0 | 0 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|----|----|----|----|----|

Figure 13. The second byte

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

Figure 14. Byte structure after the second byte

(2)-2. READ Operations

To enable a READ operation in the AK4120, set R/WN bit = "1". After transmission of data, the master can read the next data address by generating an acknowledge instead of terminating the write cycle after the receipt the first data word. After the receipt of each data, the internal 5-bit address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 06H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten. If an address greater than 07H is set, this function will not work properly.)

The AK4120 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4120 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/WN bit set to "1", the AK4120 generates an acknowledge, transmits 1 data byte whose address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a the stop condition, the AK4120 ceases transmission

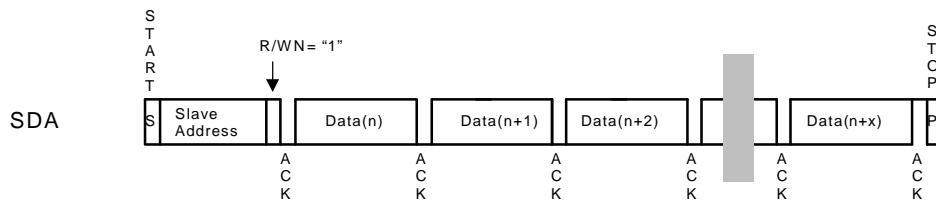


Figure 15. CURRENT ADDRESS READ

(2)-3-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/WN bit set to "1", the master must first perform a "dummy" write operation. The master issues a start request, slave address(R/WN="0") and the register address to read. After the register address's acknowledged, the master immediately reissues the start request and the slave address with the R/WN bit set to "1". The AK4120 generates a stop condition instead of an acknowledge, an acknowledge, 1byte data and increments the internal address counter by 1. If the master generates a stop condition instead of an acknowledge, the AK4120 stops transmitting.

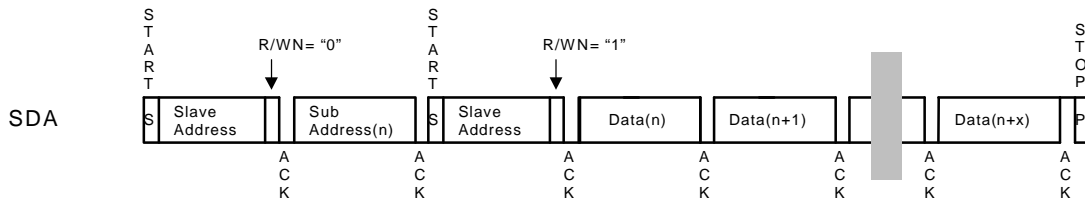


Figure 16. RANDOM ADDRESS READ

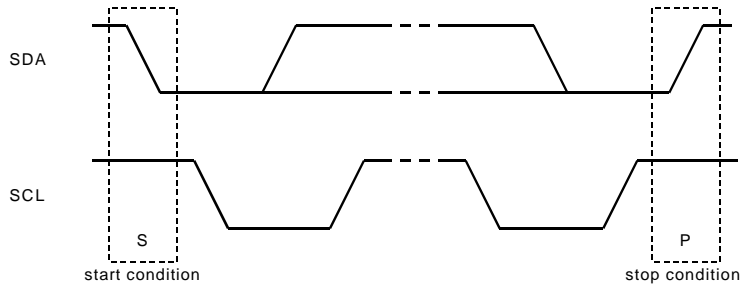


Figure 17. START and STOP conditions

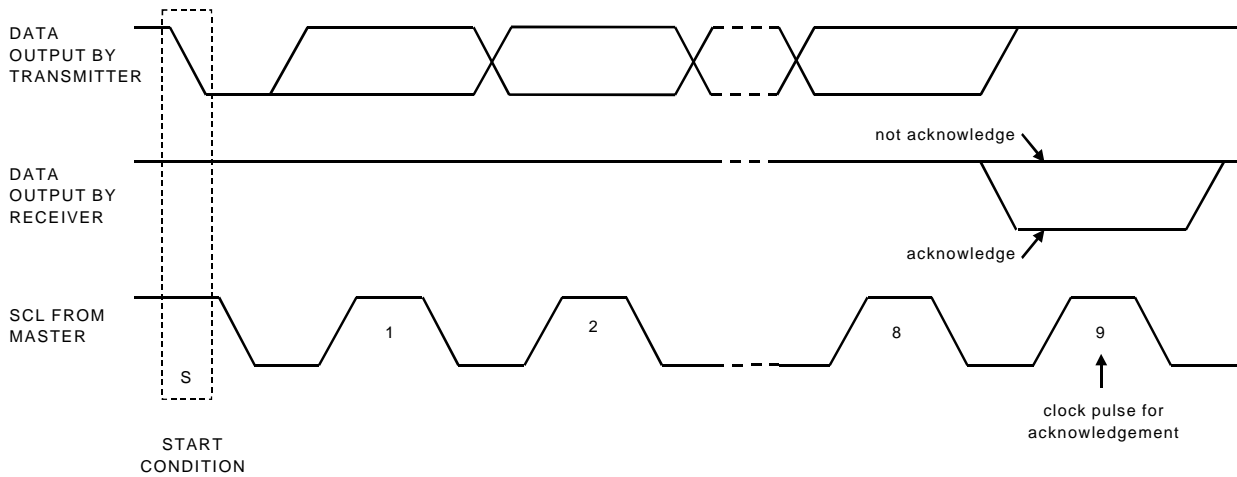


Figure 18. Acknowledge on the I²C-bus

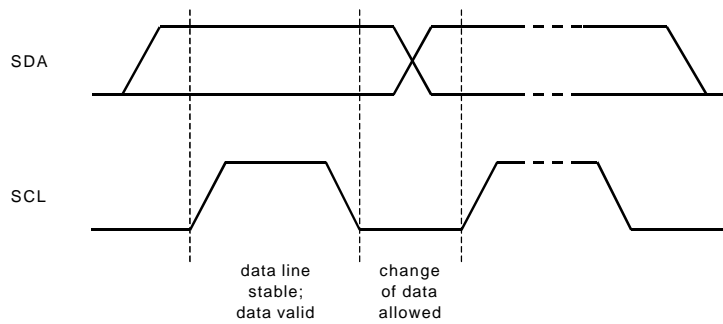


Figure 19. Bit transfer on the I²C-bus

Note: Only addresses 00H through 06H are valid write addresses. All others should not be read from or written to.

■ System Reset

The AK4120 is reset by bringing the power down pin “PDN” =“L”. The digital filters are also reset when this occurs. The AK4120 should be reset once by bringing PDN =“L” upon power-up. After a reset, the required clocks shown in Table 2 must be input.

The SRC block starts $2 \times \text{LRCK1}$ or $2 \times \text{LRCK2}$ after a reset. The SRC block starts outputting data $2053 \times \text{ORCK}$ after a reset occurs. Before $2053 \times \text{ORCK}$, the SRC block outputs “L”.

■ Zero cross detection function of Volume

When ZELM=“0”, the Zero Cross detection function is enabled. Then, if a Volume value is written to the register, the volume will not change until a Zero crossing is detected or this process times out. The ZTM1-0 bits in 01H set this timeout. When ZELM=“1”, Volume changes soon after volume value is written.

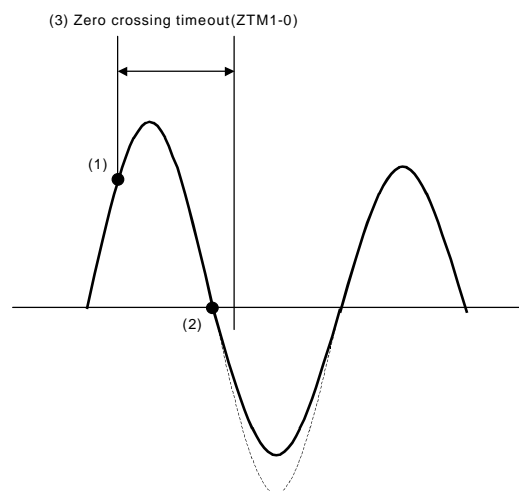


Figure 20. Zero crossing process

- (1) At this point, volume value is written in register.
- (2) This is a zero crossing point. At this point, volume is changed.
- (3) This is time of Zero crossing timeout that is set by ZTM1-0.

■ Mapping of Program Registers

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|------|----------------------|--------|--------|--------|--------|--------|--------|--------|--------|---------|
| 00H | Control 1 | PW | 0 | DIFO1 | DIFO0 | DIFI21 | DIFI20 | DIFI11 | DIFI10 | 80H |
| 01H | Control 2 | 0 | ZELM | ZTM1 | ZTM0 | 0 | OMCKS | IMCKS2 | IMCKS1 | 20H |
| 02H | Control 3 | MUTE2R | MUTE2L | MUTE1R | MUTE1L | 0 | 0 | PATH1 | PATH0 | 00H |
| 03H | Lch Volume#1 Control | 0 | GAIN6 | GAIN5 | GAIN4 | GAIN3 | GAIN2 | GAIN1 | GAIN0 | 10H |
| 04H | Rch Volume#1 Control | 0 | GAIN6 | GAIN5 | GAIN4 | GAIN3 | GAIN2 | GAIN1 | GAIN0 | 10H |
| 05H | Lch Volume#2 Control | 0 | GAIN6 | GAIN5 | GAIN4 | GAIN3 | GAIN2 | GAIN1 | GAIN0 | 10H |
| 06H | Lch Volume#2 Control | 0 | GAIN6 | GAIN5 | GAIN4 | GAIN3 | GAIN2 | GAIN1 | GAIN0 | 10H |

Note: When the PDN goes to “L”, the registers are initialized to their default values.
Data must not be written to the address except 00H through 06H.

■ Register Definitions

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|----|-------|-------|--------|--------|--------|--------|
| 00H | Control 1 | PW | 0 | DIFO1 | DIFO0 | DIFI21 | DIFI20 | DIFI11 | DIFI10 |
| | Default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DIFI11-0: Audio Data Formats for Input#1 port (See Table 6).

DIFI21-0: Audio Data Formats for Input#2 port (See Table 7).

DIFO1-0: Audio Data Formats for Output port (See Table 8).

PW: Power down control

0: Power Down

At PW=“0”, internal registers can be written.

1: Normal Operation (Default)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|------|------|------|----|-------|--------|--------|
| 01H | Control 2 | 0 | ZELM | ZTM1 | ZTM0 | 0 | OMCKS | IMCKS2 | IMCKS1 |
| | Default | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

IMCKS1: Master Clock Speed of the Master Clock for Input#1 (IMCLK1)

0: 256fs(default)

1: 512fs

IMCKS2: Master Clock Speed of the Master Clock for Input#2 (IMCLK2)

0: 256fs(default)

1: 512fs

OMCKS: Master Clock Speed of the Master Clock for Output (OMCLK)

0: 256fs(default)

1: 512fs

Note: Set the PW= “0” when those master clocks are changed.

ZTM1-0:Duration of zero-crossing timeout when ZELM= “0”

| ZTM1 | ZTM0 | | Time of Timeout | | | Default |
|------|------|---------|-----------------|---------|---------|---------|
| | | | 48kHz | 44.1kHz | 32kHz | |
| 0 | 0 | 513/fs | 10.7ms | 11.6ms | 16.0ms | |
| 0 | 1 | 1025/fs | 21.4ms | 23.2ms | 32.0ms | |
| 1 | 0 | 2049/fs | 42.7ms | 46.5ms | 64.0ms | |
| 1 | 1 | 4097/fs | 85.4ms | 92.9ms | 128.0ms | |

Note: Fs is the output sample rate

Table 9. Time of Timeout

ZELM: Select Zero Crossing Enable

0: Enable (Default)

1: Disable

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|--------|--------|--------|--------|----|----|-------|-------|
| 02H | Control 3 | MUTE2R | MUTE2L | MUTE1R | MUTE1L | 0 | 0 | PATH1 | PATH0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PATH1-0: Path Mode Select (See Table 1 and Figure 3-4)

MUTE1L: Mute control for Lch of Volume#1

0: Mute off (Default)

1: Mute On

MUTE1R: Mute control for Rch of Volume#1

0: Mute off (Default)

1: Mute On

MUTE2L: Mute control for Lch of Volume#2

0: Mute off (Default)

1: Mute On

MUTE2R: Mute control for Rch of Volume#2

0: Mute off (Default)

1: Mute On

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|----------------------|----|-------|-------|-------|-------|-------|-------|-------|
| 03H | Lch Volume#1 Control | 0 | GAIN6 | GAIN5 | GAIN4 | GAIN3 | GAIN2 | GAIN1 | GAIN0 |
| 04H | Rch Volume#1 Control | 0 | GAIN6 | GAIN5 | GAIN4 | GAIN3 | GAIN2 | GAIN1 | GAIN0 |
| 05H | Lch Volume#2 Control | 0 | GAIN6 | GAIN5 | GAIN4 | GAIN3 | GAIN2 | GAIN1 | GAIN0 |
| 06H | Rch Volume#2 Control | 0 | GAIN6 | GAIN5 | GAIN4 | GAIN3 | GAIN2 | GAIN1 | GAIN0 |
| Default | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

GAIN6-0: Volume control shown in Table 10 .
 Volume Range: -83.25dB ~12dB(Step 0.75dB)

| GAIN6-0 | Volume Level |
|---------|--------------|
| 00H | 12dB |
| 01H | 11.25dB |
| 02H | 10.5dB |
| : | : |
| 9H | 0.75dB |
| 10H | 0dB |
| 11H | -0.75dB |
| : | : |
| 7DH | -81.75 |
| 7EH | -82.50 |
| 7FH | -83.25 |

Default

Table 10. Output Volume level

Note: |Gain error| < 0.3dB, |Step error| < 0.1dB.

SYSTEM DESIGN

Figure 21 illustrates a typical system connection diagram. An evaluation board is available which demonstrates this application circuit, the optimum layout, power supply arrangement and performance measurement results.

Condition: VDD=3.3V, 3-wire serial control mode, Chip Address = "10"
 Path Mode 0, Input#2 and Output are slave mode

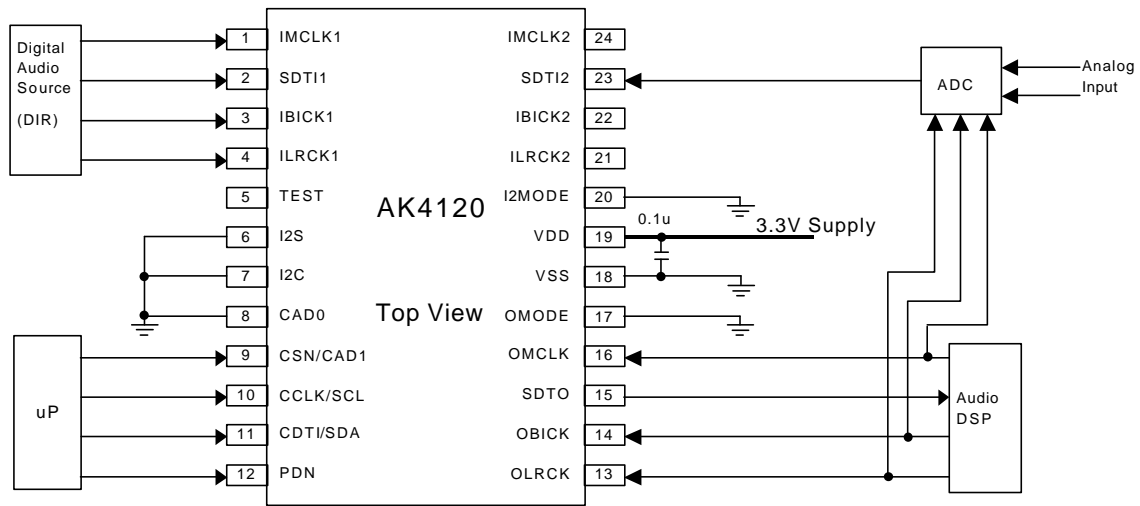
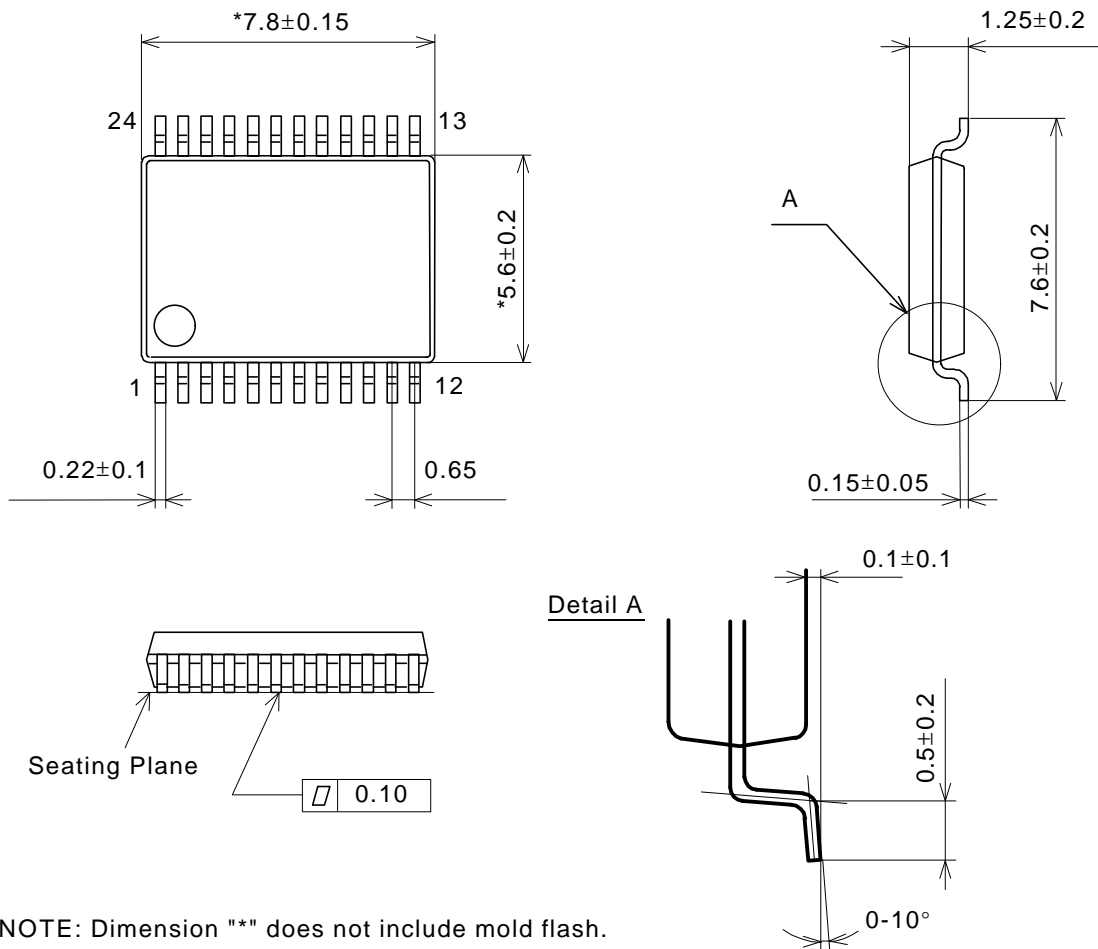


Figure 21. Example of a typical design

PACKAGE

24pin VSOP (Unit: mm)

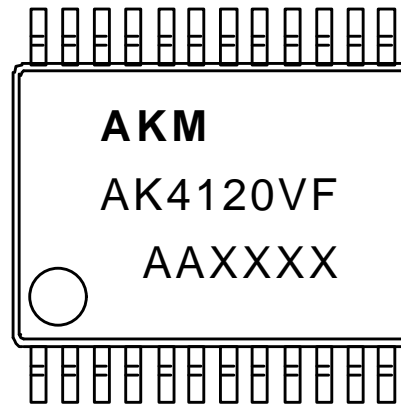


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

| | |
|-------------------------------|------------------------|
| Package molding compound: | Epoxy |
| Lead frame material: | Cu |
| Lead frame surface treatment: | Solder plate (Pb free) |

| |
|----------------|
| MARKING |
|----------------|



Contents of AAXXXX

AA: Lot#
 XXXX: Date Code

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