AK7714

20-Bit Audio Codec with DSP and Delay RAM

General Description

The AK7714 is a highly integrated audio processing IC with 20-bit stereo ADC and 4-channel DAC plus on-chip DSP with 64-kbit delay RAM. The built-in ADC has a dynamic range of 99 dB with S/(N+D) of 92 dB, and the DAC has a dynamic range of 98 dB with S/(N+D) of 89 dB, thereby ensuring high performances. The AK7714 is compatible with each of the sampling frequencies of 48 kHz, 44.1 kHz or 32 kHz, and a program of 512 steps (when sampling at 44.1 kHz or 32 kHz) can be executed in one sampling time. The AK7714 is a programmable audio DSP containing RAM for delay. This allows sound field control programs to be implemented for surround sound, echo 3D, parametric equalizer and the like.
Furthermore, the AK7714 uses a small 100-pin LQFP package, providing the optimum system for the sound field of car audio equipment which is required to meet space saving requirements.

Features

DSP:

- **Word length: 24-bit (Data RAM)**
- **Instruction cycle time: 44.2 ns**
- **Multiplier: 24 x 16 → 40-bit**
- **Divider: 24 / 24 → 16-bit**
- **ALU: 34-bit arithmetic operation (Overflow margin: 4 bits)**
  24-bit arithmetic and logic operation
- **Shift+Register: 1, 2, 3, 4, 8 and 15 bits shifted left**
  1, 2, 3, 4, (6, 14), 8 and 15 bits shifted right
  ( )Numbers in parentheses are restricted.
  Provided with indirect shift function
- **Program RAM: 448 x 32-bit**
- **Coefficient RAM: 384 x 16-bit**
- **Data RAM: 128 x 24-bit**
- **Internal delay memory: 4096 x 16-bit or 2048 x 24-bit**
- **Sampling frequency: 32 kHz to 48 kHz**
- **Serial micro controller interface**
- **Master clock: 512/384/256 fs (512 fs for sampling at 44.1 kHz or 32 kHz)**
- **Master/slave operation**
- **Serial signal input port (2 to 6 ch), output port (2 to 6 ch) : 16/20/24-bit**

ADC: 2 channels

- **20-bit 64 x Over-sampling delta sigma**
- **DR, S/N : 99 dB**
- **S/(N+D) : 92 dB**
- **Digital HPF (fc = 1 Hz)**

DAC: 4 channels

- **20-bit 128 x Over-sampling delta sigma**
- **DR, S/N : 98 dB**
- **S/(N+D) : 89 dB**

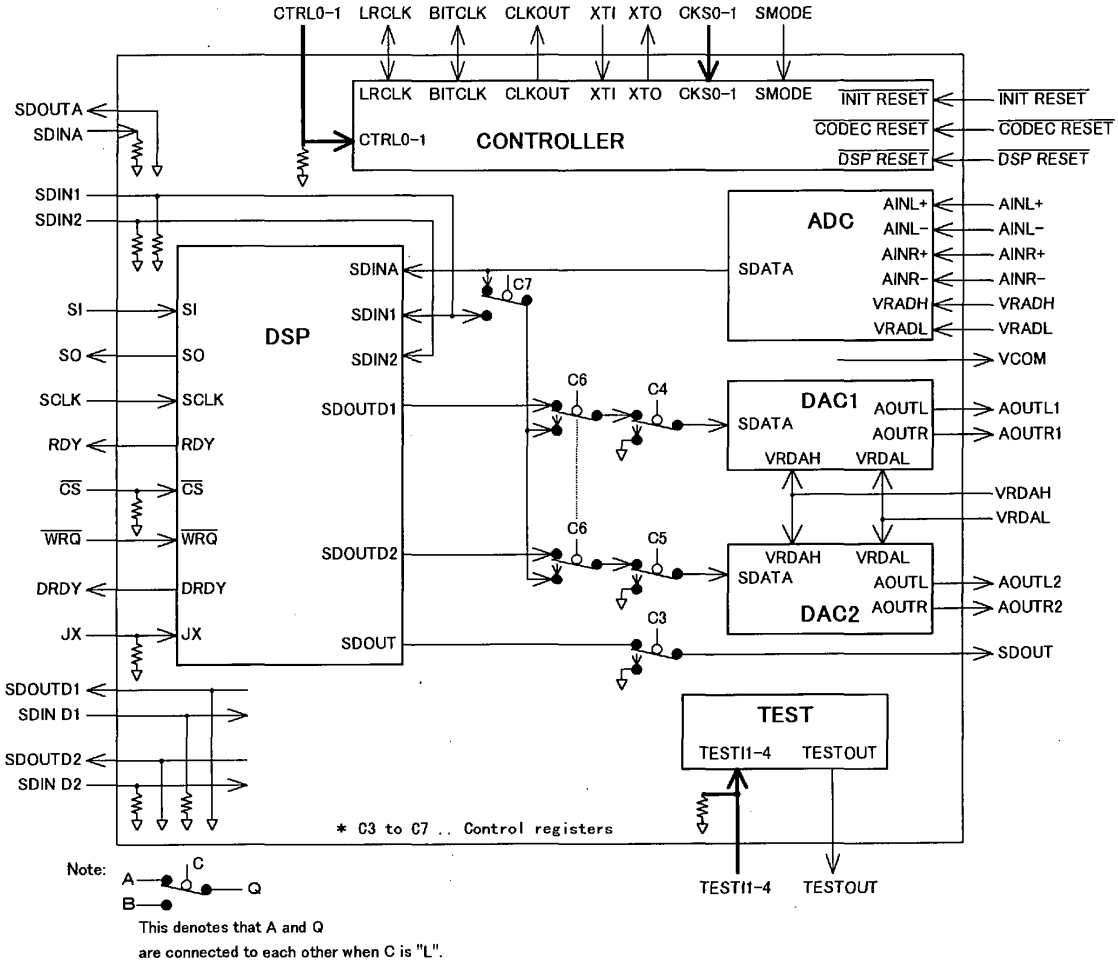
Others

- **Power voltage: + 5 V ±5%**
- **Operating temperature range: -40°C to +85 °C**
  Package: 100-pin LQFP (0.5 mm pitch)

Block diagram

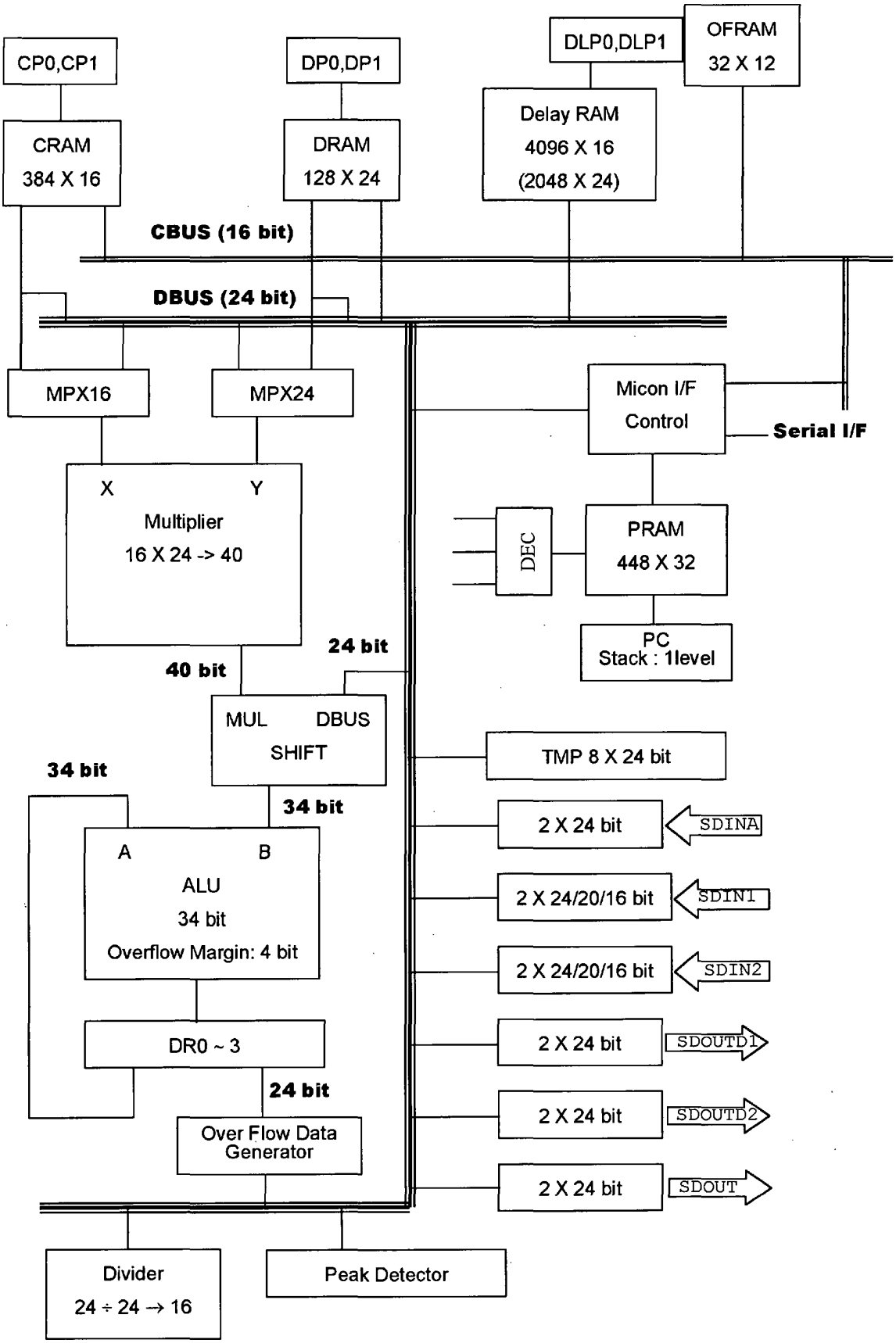
☐ For standard operation (Internal connection mode, C3 to C7: initial settings)

- CPCL :L Internal connection mode
- C3 ~ C7 :All 0 (Initial settings)



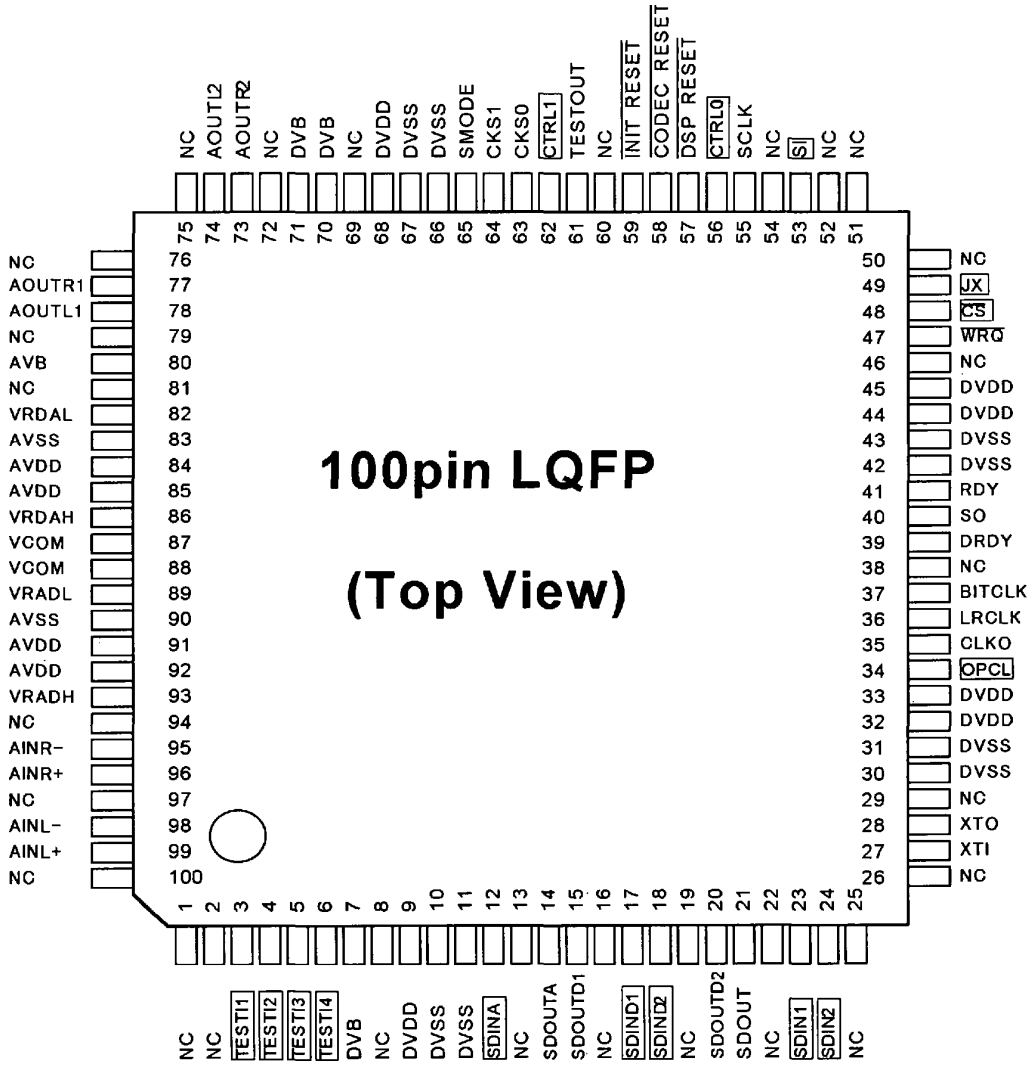
This block diagram is a simplified illustration of the AK7714; it is not a circuit diagram.

☐ Block Diagram of AK7714 DSP Section



Description of Input/Output Pins

(1) Pin layout



Note: ☐ Items enclosed in boxes are provided with pulldown functions.

(2) Pin function

Pin No.	Pin name	I/O	Function	Classification
3	TESTI1	I	**Test pin: Leave open or connect to DVSS. (Pulldown)**	Test
4	TESTI2	I	**Test pin: Leave open or connect to DVSS. (Pulldown)**	
5	TESTI3	I	**Test pin: Leave open or connect to DVSS. (Pulldown)**	
6	TESTI4	I	**Test pin: Leave open or connect to DVSS. (Pulldown)**	
7	DVB	-	**+5 V power supply (Silicon substrate potential)**	Power supply
9	DVDD	-	**+5 V Digital power supply**	
10,11	DVSS	-	**Digital ground**	
12	SDINA	I	**DSP Serial data input pin (Pulldown)** OPCL="L": Disabled. Leave open or connect to DVSS. OPCL="H": Compatible with MSB first 24 bits	Digital section Serial input/output data
14	SDOUTA	O	**ADC Serial data output pin** OPCL="L": Outputs "L". OPCL="H": Outputs MSB first 20-bit data.	
15	SDOUTD1	O	**DSP Serial data output pin** OPCL="L": Outputs "L". OPCL="H": Outputs MSB first 24-bit data.	
17	SDIND1	I	**DAC1 Serial data input pin (Pulldown)** OPCL="L": Disabled. Leave open or connect to DVSS. OPCL="H": Compatible with MSB first 20 bits	
18	SDIND2	I	**DAC2 Serial data input pin (Pulldown)** OPCL="L": Disabled. Leave open or connect to DVSS. OPCL="H": Compatible with MSB first 20 bits	
20	SDOUTD2	O	**DSP Serial data output pin** OPCL="L": Outputs "L". OPCL="H": Outputs MSB first 24-bit data.	
21	SDOUT	O	**DSP Serial data output pin** Outputs MSB first 24-bit data.	

Pin No.	Pin name	I/O	Function	Classification
23	SDIN1	I	**DSP Serial data input pin (Pulldown)** Compatible with MSB first/LSB first 24, 20 and 16 bits	Digital section Serial input data
24	SDIN2	I	**DSP Serial data input pin (Pulldown)** Compatible with MSB first/LSB first 24, 20 and 16 bits	
27	XTI	I	**Master clock input pin** Connect a crystal oscillator between this pin and the XTO pin, or input the external CMOS clock signal XTI pin. The clock frequency can be selected by the CKS0 and CKS1 pins.	System clock
28	XTO	O	**Crystal oscillator output pin** When a crystal oscillator is used, connect it between the XTI pin and this pin. When the external clock is used, keep this pin open.	
30,31	DVSS	-	**Digital Ground**	Power supply
32,33	DVDD	-	**+5 V Digital Power supply**	
34	OPCL	I	**ADC/DAC connection selector pin (Pulldown)** OPCL="L" (Leave open or connect to DVSS.): Connected OPCL="H": Disconnected	Control
35	CLKO	O	**Clock output pin** Outputs the XTI clock. Allows the output to be set to "L" using the CTRL0 and CTRL1 pins.	Others
36	LRCLK	I/O	**LR channel select Clock pin** SMODE="L": Slave mode: Inputs the fs clock. SMODE="H": Master mode: Outputs the fs clock.	System clock
37	BITCLK	I/O	**Serial bit clock pin** SMODE="L": Slave mode: Inputs 64 fs or 48 fs clocks. SMODE="H": Master mode: Outputs 64 fs clocks.	
39	DRDY	O	**Output data ready pin for microcomputer interface.**	Microcomputer interface
40	SO	O	**Serial data output pin for microcomputer interface (compatible with Hi-Z)** Hi-Z state is obtained when $\overline{CS}$ ="H".	
41	RDY	O	**Data write ready output pin for microcomputer interface (compatible with Hi-Z)** Hi-Z state is obtained when $\overline{CS}$ ="H".	

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>I/O</th><th>Function</th><th>Classification</th></tr>
<tr><td>42,43</td><td>DVSS</td><td>-</td><td>Digital Ground</td><td>Power supply</td></tr>
<tr><td>44,45</td><td>DVDD</td><td>-</td><td>+5 V Digital power supply</td><td></td></tr>
<tr><td>47</td><td>$\overline{\text{WRQ}}$</td><td>I</td><td>Microcomputer interface Write Request pin</td><td>Microcomputer interface</td></tr>
<tr><td>48</td><td>$\overline{\text{CS}}$</td><td>I</td><td>Microcomputer interface chip selector input pin (Pulldown)
Also used for SO control in addition to chip selection.
When only one AK7714 is used and SO is not used, $\overline{\text{CS}}$="L" may be used unchanged. SO and RDY will be Hi-z when $\overline{\text{CS}}$ ="H".</td><td></td></tr>
<tr><td>49</td><td>JX</td><td>I</td><td>External condition jump pin (Pulldown)</td><td>Program control</td></tr>
<tr><td>53</td><td>SI</td><td>I</td><td>Microcomputer interface serial data input pin (Pulldown)</td><td>Microcomputer interface</td></tr>
<tr><td>55</td><td>SCLK</td><td>I</td><td>Microcomputer interface serial data clock input pin</td><td></td></tr>
<tr><td>56</td><td>CTRL0</td><td>I</td><td>Clock output control pin (Pulldown)
Use of CTRL0 and CTRL1 allows the CLKO output and LRCLK/BITCLK outputs
in the master mode to be fixed to “L” or “H”. See Function Description.
<table>
<tr><th>CTRL1</th><th>CTRL0</th><th>CLKO</th><th>LRCLK</th><th>BITCLK</th></tr>
<tr><td>0</td><td>0</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>1</td><td>0</td><td>“L”</td><td>Output</td><td>Output</td></tr>
<tr><td>1</td><td>1</td><td>“L”</td><td>“H”(“L”)</td><td>“L”</td></tr>
</table></td><td>Control</td></tr>
<tr><td>57</td><td>$\overline{\text{DSP RESET}}$</td><td>I</td><td rowspan="2">Reset pin
Normally, $\overline{\text{DSP RESET}}$ and $\overline{\text{CODEC RESET}}$ are simultaneously controlled for use.</td><td rowspan="3">Reset</td></tr>
<tr><td>58</td><td>$\overline{\text{CODEC RESET}}$</td><td>I</td></tr>
<tr><td>59</td><td>$\overline{\text{INIT RESET}}$</td><td>I</td><td>Reset pin (for initialization)
Used to input “L” to initialize the AK7714 at power-on.</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>I/O</th><th>Function</th><th>Classification</th></tr>
<tr><td>61</td><td>TESTOUT</td><td>O</td><td>Test pin: Leave open.</td><td>Test</td></tr>
<tr><td>62</td><td>CTRL1</td><td>I</td><td>Clock output control pin (Pulldown)
Use of CTRL0 and CTRL1 allows the CLKO output and LRCLK/BITCLK outputs
in the master mode to be fixed to “L” or “H”.
See CTRL0 (pin 56) & Function Description.</td><td rowspan="3">Control</td></tr>
<tr><td>63
64</td><td>CKS0
CKS1</td><td>I</td><td>Clock selector pin
<table>
<tr><th>CKS1</th><th>CKS0</th><th>XTI</th><th>DSP</th></tr>
<tr><td>0</td><td>0</td><td>384fs</td><td>384fs</td></tr>
<tr><td>0</td><td>1</td><td>512fs</td><td>512fs</td></tr>
<tr><td>1</td><td>0</td><td>256fs</td><td>256fa</td></tr>
<tr><td>1</td><td>1</td><td colspan="2">Test mode (disabled)</td></tr>
</table></td></tr>
<tr><td>65</td><td>SMODE</td><td>I</td><td>Slave/master mode selector pin
Set LRCLK and BITCLK to input or output mode.
SMODE="L": Slave mode (LRCLK and BITCLK are set to input mode.)
SMODE="H": Master mode (LRCLK and BITCLK are set to output mode.)</td></tr>
<tr><td>66,67</td><td>DVSS</td><td>-</td><td>Digital ground</td><td rowspan="3">Power supply</td></tr>
<tr><td>68</td><td>DVDD</td><td>-</td><td>Power supply pin for digital section 5 V (typ)
+5 V Digital power supply</td></tr>
<tr><td>70,71</td><td>DVB</td><td>-</td><td>+5 V Power supply (normally analog) (Silicon substrate potential)</td></tr>
<tr><td>73</td><td>AOUTR2</td><td>O</td><td>DAC2 Rch analog output pin</td><td rowspan="4">Analog section</td></tr>
<tr><td>74</td><td>AOUTL2</td><td>O</td><td>DAC2 Lch analog output pin</td></tr>
<tr><td>77</td><td>AOUTR1</td><td>O</td><td>DAC1 Rch analog output pin</td></tr>
<tr><td>78</td><td>AOUTL1</td><td>O</td><td>DAC1 Lch analog output pin</td></tr>
<tr><td>80</td><td>AVB</td><td>-</td><td>+5 V power supply (Silicon substrate potential)</td><td>Power supply</td></tr>
<tr><td>82</td><td>VRDAL</td><td>I</td><td>DAC Reference voltage input pin
Normally, connect to AVSS (pin 83).</td><td>Analog section</td></tr>
</table>

Pin No.	Pin name	I/O	Function	Classification
83	AVSS	-	**Analog ground 0V**	Power supply
84,85	AVDD	-	**Power supply pin for analog section 5 V (typ) (Silicon substrate potential)** **+5 V Analog power supply**	
86	VRDAH	I	**DAC Reference voltage input pin** Normally, connect to AVDD (pin 84,85), and connect 0.1 μF and 10 μF capacitors between this and VRDAL.	Analog section
87,88	VCOM	O	**Common voltage pin for analog section** Connect 0.1 μF and 10 μF capacitors between this and AVSS. Do not use for the external circuit.	
89	VRADL	I	**ADC Reference voltage input pin** Normally, connect to AVSS (pin 90).	
90	AVSS	-	**Analog Ground 0V**	Power supply
91,92	AVDD	-	**+5 V Analog Power supply (Silicon substrate potential)**	
93	VRADH	I	**ADC Reference voltage input pin** Normally, connect to AVDD (pin 91,92), and connect 0.1 μF and 10 μF capacitors between this and VRADL.	Analog section
95	AINR-	I	**ADC Rch analog inverted input pin**	
96	AINR+	I	**ADC Rch analog non-inverted input pin**	
98	AINL-	I	**ADC Lch analog inverted input pin**	
99	AINL+	I	**ADC Lch analog non-inverted input pin**	

Pin No.	Pin name	I/O	Function	Classification
1,2,8,13,16,19,22,25,26,29,38 46,50,51,52,54,60,69,72,75,76 79,81,94,97,100	NC	-	**NC (No connection)** These pins should be left floating.	NC

Absolute maximum rating

(AVSS, DVSS = 0 V: All voltages indicated are relative to the ground.)

Item	Symbol	Min	Max	Unit
Power supply voltage				
Analog (AVDD), Boards (DVB and AVB)	VA	-0.3	6.0	V
Digital (DVDD) (Note 1)	VD	-0.3	6.0 or (VA+0.3)	V
Input current (except for power supply pin)	IIN	-10	+10	mA
Analog input voltage AINL+, AINL-, AINR+, AINR-, VRADH, VRADL, VRDAH, VRDAL	VINA	-0.3	VA+0.3	V
Digital input voltage (Note 1)	VIND	-0.3	VA+0.3	V
Operating ambient temperature	Ta	-40	85	°C
Storage temperature	Tstg	-65	150	°C

Note: 1. Must not exceed the maximum rating of 6.0 V (namely, VD ≤ (VA+0.3 V) ≤ 6.0 V).
(VA is a power supply to supply silicon substrate potential.)

WARNING: Operation at or beyond these limits may result in permanent damage of the device.
Normal operations are not guaranteed under these critical conditions in principle.

Recommended operating conditions

(AVSS, DVSS = 0 V: All voltages indicated are relative to the ground.)

Items	Symbol	Min	Typ	Max	Unit
Power supply voltage					
Board (AVB, DVB), AVDD	VA	4.75	5.0	5.25	V
DVDD	VD	4.75	5.0	VA	V
Reference voltage (VREF)					
VRADH, VRDAH	VRH		VA		V
VRADL, VRDAL	VRL		0.0		V

Note: 1. Start up VA simultaneously with or earlier than VD, and stop VD simultaneously with or earlier than VA.
2. When starting and stopping the power supply, meet the absolute maximum rating condition: VD ≤ (VA+0.3 V).
It is generally recommended to use at VD ≤ VA. However, the VD must be 4.75 volts or more.
3. The analog input voltage and output voltage are proportional to the VRADH and VRDAH voltages.

Electric characteristics

(1) Analog characteristics

(Unless otherwise specified, Ta = 25°C; AVDD, DVDD, AVB, DVB = 5.0 V; VRADH = AVDD, VRADL = AVSS, VRDAH = AVDD, VRDAL = AVSS; fs = 44.1 kHz; BITCLK = 64 fs ; XTI = 256 fs;
Signal frequency 1 kHz; measuring frequency = 10 Hz to 20 kHz; 20 bits; DSP section in the reset state; ADC with all ifferential inputs)

	Parameter	Min	Typ	Max	Unit
ADC section	Resolution			20	Bits
	Dynamic characteristics				
	S/(N+D) (-0.5 dB) (Note 1)	86	92		dB
	Dynamic range (A filter) (Note 2)	94	99		dB
	S/N (A filter)	94	99		dB
	Inter-channel isolation (f =1 kHz)	90	105		dB
	DC accuracy				
	Inter-channel gain mismatching		0.1	0.3	dB
	Gain drift		50		ppm/°C
	Analog input				
	Input voltage (Note 3)	±1.9	±2.0	±2.1	Vp-p
	Input impedance		220		kΩ
DAC section	Resolution			20	Bits
	Dynamic characteristics				
	S/(N+D) (0 dB)	83	89		dB
	Dynamic range (-60 dB) (A filter) (Note 2)	93	98		dB
	S/N (A filter)	93	98		dB
	Inter-channel isolation (f = 1 kHz) (Note 4)	90	105		dB
	DC accuracy				
	Inter-channel gain mismatching (Note 4)		0.2	0.5	dB
	Gain drift		50		ppm/°C
	Analog output				
	Output voltage (Note 5)	2.70	2.95	3.20	Vp-p
	Load resistance	5			kΩ

Note:
1. Single end input will result in poorer characteristics.
2. Indicates S/(N+D) when -60 dB signal is input.
3. The full scale for analog input voltage (ΔAIN = (AIN+) - (AIN-)) can be represented By (±FS = ±(VRADH-VRADL) × 0.4).
4. Specified for L and R of each DAC.
5. The full-scale voltage (0 dB) and output voltage are proportional to VRDAH voltage. Analog output voltage (Typ. @ 0 dB) = 2.95 Vpp*VRDAH/5

(2) DC characteristics

(VDD = AVDD = DVDD = AVB = DVB = 5.0 V ±5%, Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
High level input voltage (Note 1)	VIH				V
Input pins other than XTI and test pins		2.4			V
XTI and test pins		70% VDD			
Low level input voltage (Note 1)	VIL				
Input pins other than XTI and test pins				0.6	
XTI and test pins				30% VDD	
High level output voltage Iout=-100μA	VOH	VDD-0.5			V
Low level output voltage Iout=100μA	VOL			0.5	V
Input leak current (Note 2)	Iin	-10		±10	μA
Input leak current Pulldown pins (Note 3)	Iid		100		μA

Note: 1. The test pins are as follows: TESTI1, TESTI2, TESTI3, TESTI4
2. The pulldown pins are not included.
3. The pulldown pins are as follows (Typ 50 kΩ):
TESTI1, TESTI2, TESTI3, TESTI4, SDINA, SDIND1, SDIND2, SDIN1, SDIN2, OPCL,
CS, JX, SI, CTRL0, CTRL1

Note: Regarding the input/output levels in the text, the low level is represented as "L" or 0, and the high level as "H" or 1. In principle, "0" and "1" are used for the bus (serial/parallel), such as registers.

(3) Current consumption

(AVDD = AVB, DVB, DVDD = 5.0 V±5%, Ta = 25°C; master clock (XTI) = 22.5792MHz = 512 fs [fs = 44.1kHz]; when operating for DAC 4 channel with 1 kHz sinusoidal wave full-scale input to each of ADC 2 ch analog input pins)

Power supply				
Parameter	Min	Typ	Max	Unit
Power supply current				
1) During operation				
a) AVDD + AVB + DVB		41		mA
b) DVDD (Note 1)		87		mA
c) Total (a+b)		128	162	mA
2) When INIT RESET= "L"(reference value)		7		mA
Note 2				
Power consumption				
1) During operation				
a) AVDD+AVB+DVB		205		mW
b) DVDD (Note 1)		435		mW
c) Total(a+b)		640	850	mW
2) When INIT RESET ="L" (reference value)				mW
Note 2		35		

Note: 1. Varies slightly according to the frequency used and contents of the DSP program.
Note: 2. This is a reference value in case of using the crystal oscillator.
But, varies slightly according to the types of crystal oscillators.

(4) Digital filter characteristics

Values described below are design values cited as references. These are not for guaranteeing the characteristics.

1) ADC Section:

(Ta = 25°C; AVDD, DVDD, AVB, DVB = 5.0 V ±5%; fs = 44.1 kHz)

Parameter	Symbol	Min	Typ	Max	Unit
Pass band (-0.02 dB) (-6.0 dB)	PB	0 0		20.00 22.05	kHz kHz
Stop band (Note 1)	SB	24.35			kHz
Pass band ripple (Note 2)	PR			±0.005	dB
Stop band attenuation (Notes 3,4)	SA	80			dB
Group delay distortion	ΔGD			0	μs
Group delay (Ts = 1/fs)	GD		29.3		Ts

Note: 1. These frequencies scale with the sampling frequency (fs).
2. The pass band is from DC to 19.75 kHz when fs = 44.1 kHz.
3. The stop band is from 27.56 kHz to 2.795 MHz when fs = 44.1 kHz.
4. When fs = 44.1 kHz, the analog modulator samples analog input at 2.8224 MHz. The input signal is not attenuate dBy the digital filter in the multiple bands (n x 2.8224 MHz ± 20.21 kHz ; n = 0, 1, 2, 3...) of the sampling frequency.

2) DAC section

(Ta = 25°C; AVDD, DVDD, AVB, DVB = 5.0 V ±5%; fs = 44.1 kHz)

Parameter	Symbol	Min	Typ	Max	Unit
Digital filter					
Pass band ±0.07 dB (Note 1) (-6.0 dB)	PB	0 -	 22.05	20.0 -	kHz kHz
Stop band (Note 1)	SB	24.1			kHz
Pass band ripple	PR			±0.07	dB
Stop band attenuation	SA	47			dB
Group delay (Ts = 1/fs) (Note 2)	GD	-	15.3		Ts
Digital filter + Analog filter					
Amplitude characteristics 0 to 20.0 kHz			±0.5		dB

Note: 1. The pass band and stop band frequencies are proportional to "fs" (system sampling rate), and are represente PB = 0.4535 fs(@ -0.06 dB) and SB = 0.546 fs, respectively.
2. The caluculating delay time which occurred by digital filtering. This time is from setting the 20-bit data of both channels on input register to the output of analog signal.

(5) Switching characteristics

1) System clock

(AVDD = AVB, DVB, DVDD = 5.0 V±5%, Ta = 25°C, CL = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Master clock (XTI)					
a) With a crystal oscillator:					
256 fs: Frequency	fMCLK	11.0	11.2896	12.288	MHz
384 fs: Frequency	fMCLK	12.288	16.9344	18.432	MHz
512 fs: Frequency	fMCLK	16.384	22.5792	22.5792	MHz
b)With an external clock input:					
Duty factor (≤ 18.432 MHz) (> 18.432MHz)		40 45	50 50	60 55	%
256 fs: Frequency : High level width : Low level width	fMCLK tMCLKH tMCLKL	11.0 30 30	11.2896	12.288	MHz
384 fs: Frequency : High level width : Low level width	fMCLK tMCLKH tMCLKL	12.288 20 20	16.9344	18.432	MHz
512 fs: Frequency : High level width : Low level width	fMCLK tMCLKH tMCLKL	16.384 17 17	22.5792	22.5792	MHz
Clock rise time Clock fall time	tCR tCF			6 6	ns ns
LRCLK Sampling frequency	fs	32	44.1 1	48	kHz fs
Slave mode: Clock rise time Slave mode: Clock fall time	tLR tLF			10 10	ns ns
BITCLK	fBCLK	48	64		fs
Slave mode: High level width Slave mode: Low level width	tBCLKH tBCLKL	100 100			
Slave mode: Clock rise time Slave mode: Clock fall time	tBR tBF			6 6	ns ns

2) Reset

(AVDD = AVB, DVB, DVDD = 5.0 V ±5%, Ta = 25°C, CL = 20 pF)

Parameter		Symbol	Min	Typ	Max	Unit
$\overline{\text{INIT RESET}}$	(Note 1)	tRST	150			ns
$\overline{\text{DSP RESET}}$	(Note 1)	tRST	150			ns
$\overline{\text{CODEC RESET}}$	(Note 1)	tRST	150			ns

Note 1. "L" is acceptable when power is turned on.

3) Audio interface

(AVDD = AVB, DVB, DVDD = 5.0 V ±5%,Ta = 25°C, CL = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Slave mode					
BITCLK frequency	fBCLK	48	64		fs
BITCLK low level width	tBCLKL	100			ns
BITCLK high level width	tBCLKH	100			ns
Delay time from BITCLK"↑" to LRCLK	tBLRD	40			ns
Delay time from LRCLK to BITCLK "↑"	tLRBD	40			ns
Delay time from LRCLK to serial data output	tLRD			70	ns
Delay time from BITCLK to serial data output	tBSOD			70	ns
Serial data input latch hold time	tBSIDS	40			ns
Serial data input latch setup time	tBSIDH	40			ns
Master mode					
BITCLK frequency	fBCLK		64		fs
BITCLK duty factor			50		
Delay time from BITCLK"↑" to LRCLK	tBLRD	40			ns
Delay time from LRCLK to BITCLK"↑"	tLRBD	40			ns
Delay time from LRCLK to serial data output	tLRD			70	ns
Delay time from BITCLK to serial data output	tBSOD			70	ns
Serial data input latch hold time	tBSIDS	40			ns
Serial data input latch setup time	tBSIDH	40			ns

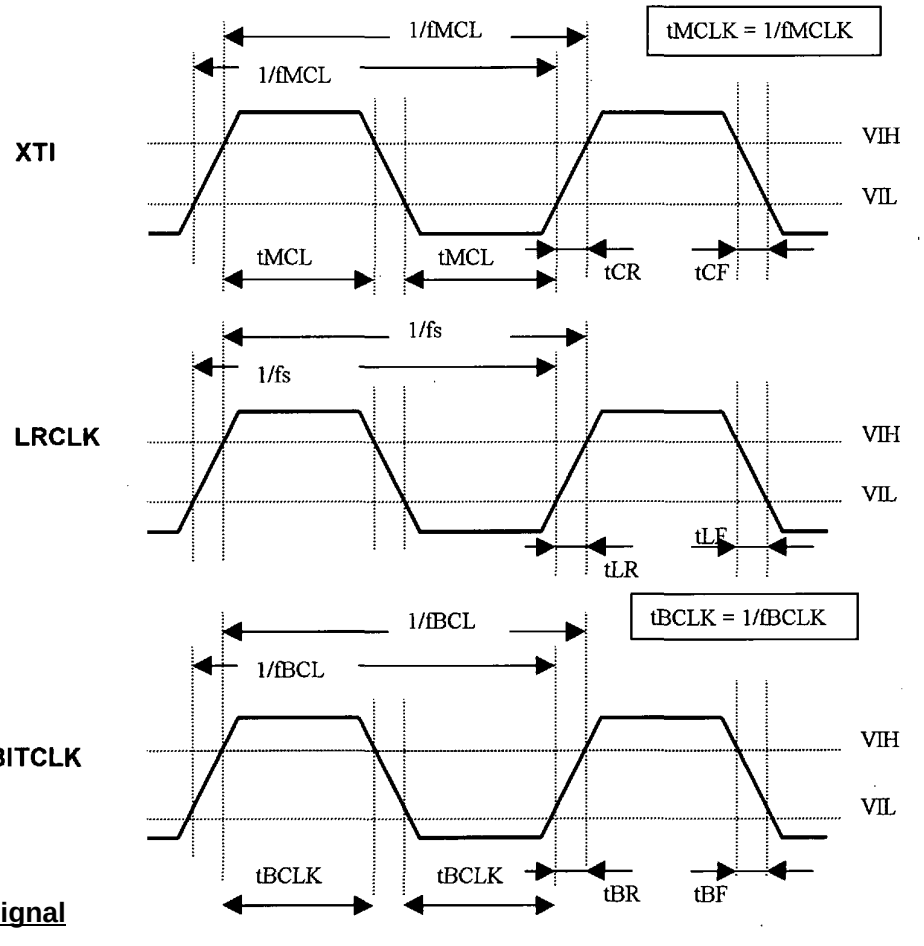
4) Microcomputer interface

(AVDD = AVB, DVB, DVDD = 5.0 V ±5%, Ta = 25°C, CL = 20 pF)

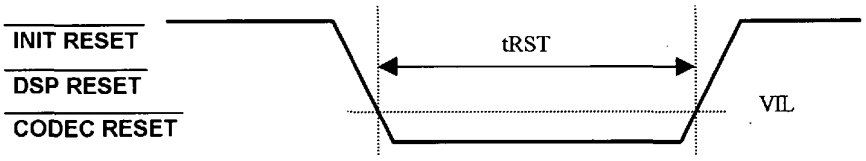
Parameter	Symbol	Min	Typ	Max	Unit
Microcomputer interface signal					
$\overline{CS}$ Fall time	tCSF			10	ns
$\overline{CS}$ Rise time	tCSR			10	ns
Rest time until RDY and SO Hi-Z states from $\overline{CS}$"↓"	tCSHR			100	ns
Set time until RDY and SO Hi-Z states from $\overline{CS}$"↑"	tCSHS			200	ns
$\overline{WRQ}$ fall time	tWRF			10	ns
$\overline{WRQ}$ rise time	tWRR			10	ns
SCLK fall time	tSF			10	ns
SCLK rise time	tSR			10	ns
SCLK low level width	tSCLKL	150			ns
SCLK high level width	tSCLKH	150			ns
Microcomputer to AK7714					
Time from $\overline{RESET}$"↓" to $\overline{WRQ}$"↓"	tREW	200			ns
Time from $\overline{WRQ}$"↑" to $\overline{RESET}$"↑"	tWRE	200			ns
$\overline{WRQ}$ high level width	tWRQH	200			ns
Time from $\overline{WRQ}$ "↓" to SCLK"↓"	tWSC	200			ns
Time from SCLK"↑" to $\overline{WRQ}$"↑"	tSCW	6×tMCLK			ns
SI latch setup time	tSIS	100			ns
SI latch hold time	tSIH	100			ns
AK7714 to microcomputer					
$\overline{CS}$ high level width	tCSH	200			ns
Time from SCLK"↑" to $\overline{CS}$"V"	tSCS	6×tMCLK			ns
Time from $\overline{CS}$"↓" to SCLK"↓"	tCSC	200			ns
Time from $\overline{CS}$"↑" to DRDY"↑"	tCSDR			100	ns
Delay time from SCLK "↓" to SO output	tSOS			100	ns
AK7714 to microcomputer (RAM DATA read-out)					
SI latch setup time (SI="H")	tRSISH	100			ns
SI latch setup time (SI="L")	tRSISL	100			ns
SI latch hold time	tRSIH	100			ns
Time from SCLK "↓" to SO (PRAM)	tSOPD			100	ns
Time from SCLK "↓" to SO (CRAM, OFRAM)	tSOCOD			100	ns

(6) Timing Diagram

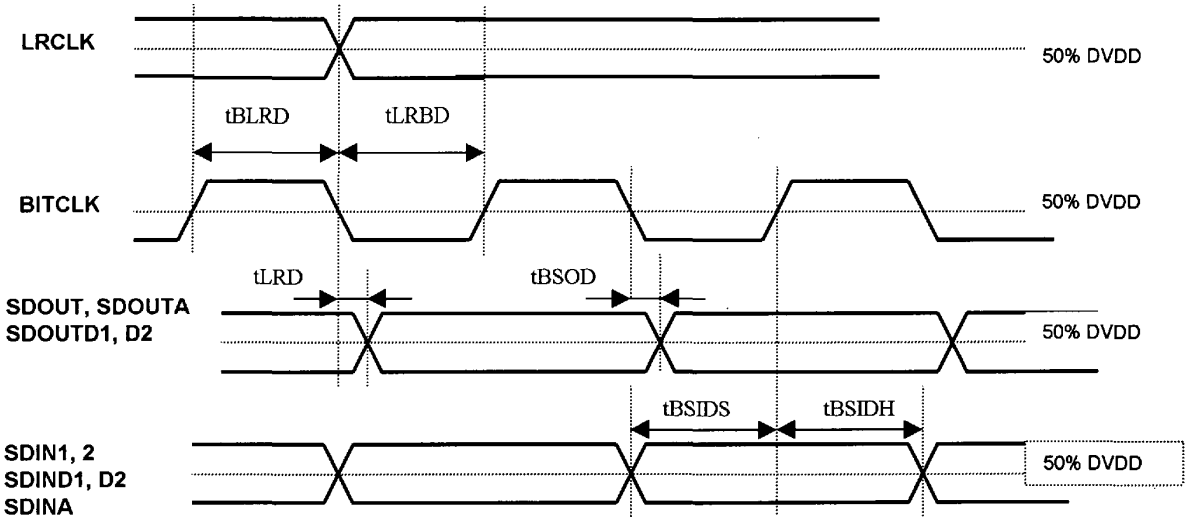
1) System clock



2) Reset signal

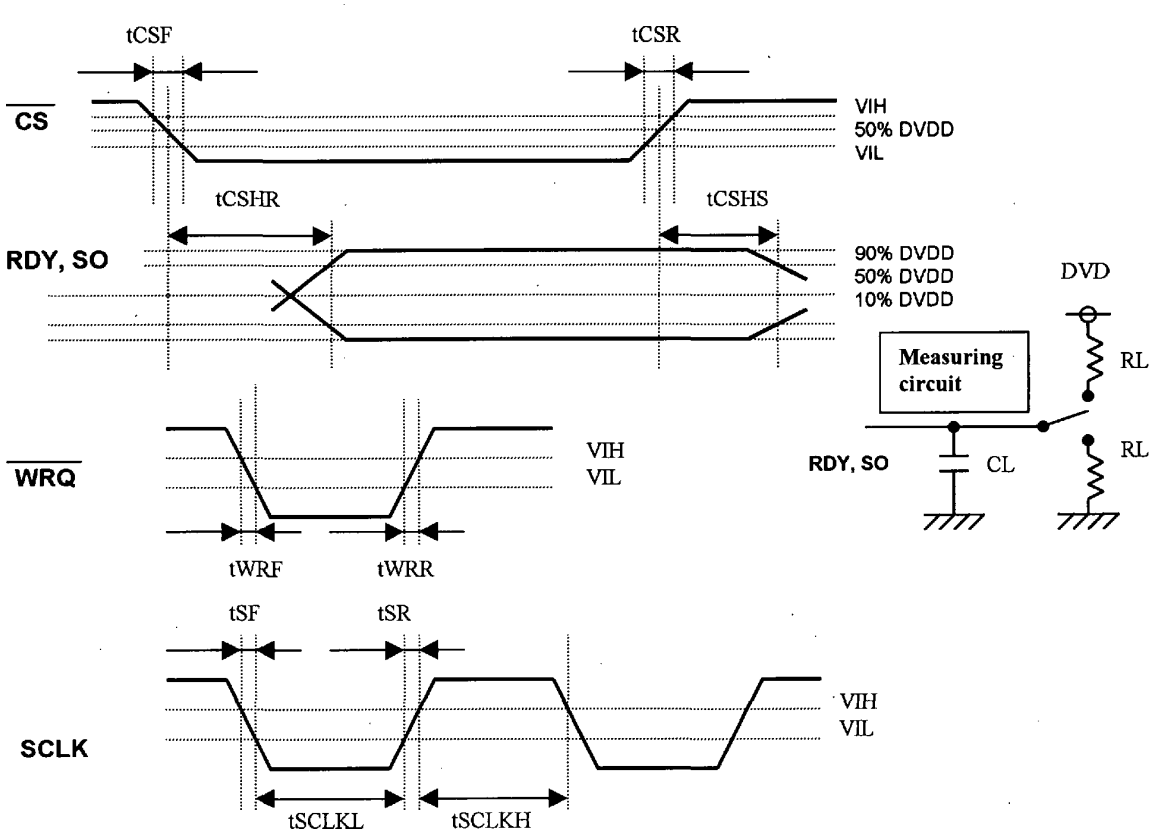


3) Audio interface

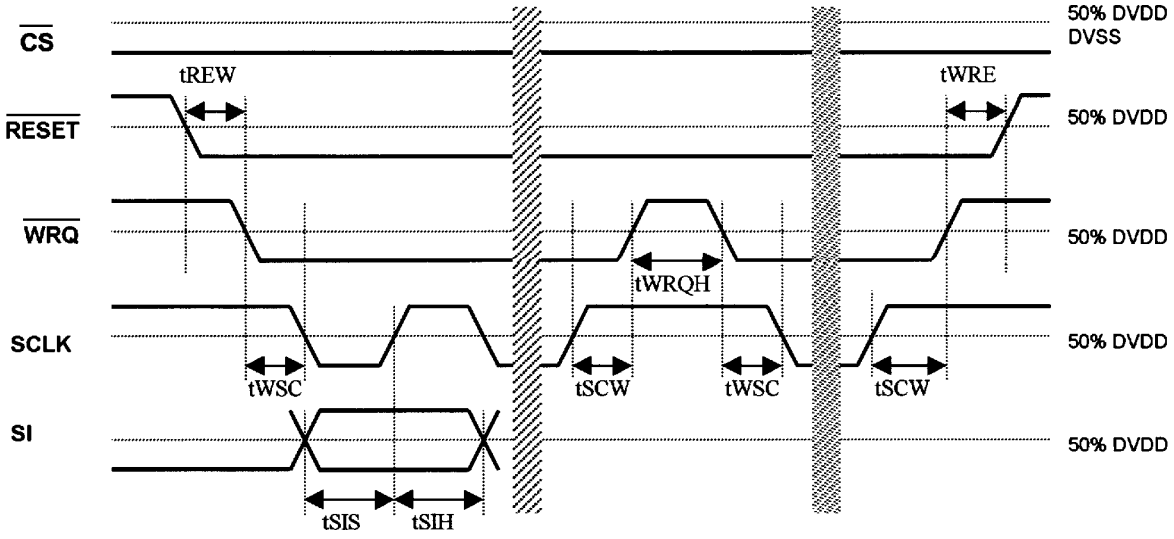


4) Microcomputer interface

■ Microcomputer interface signals

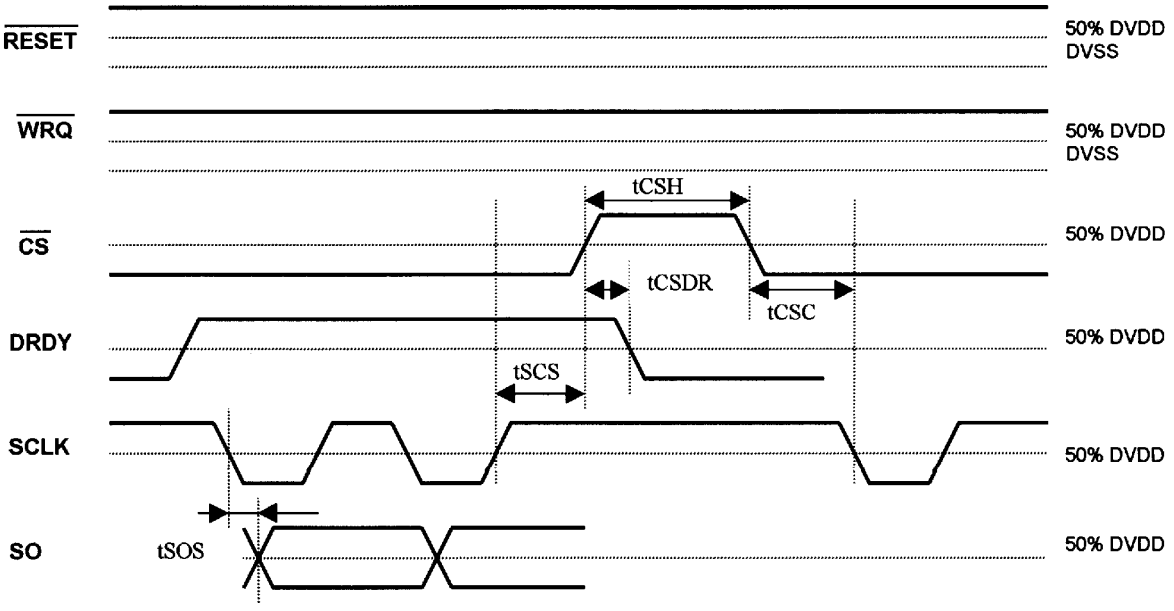


■ Microcomputer to AK7714

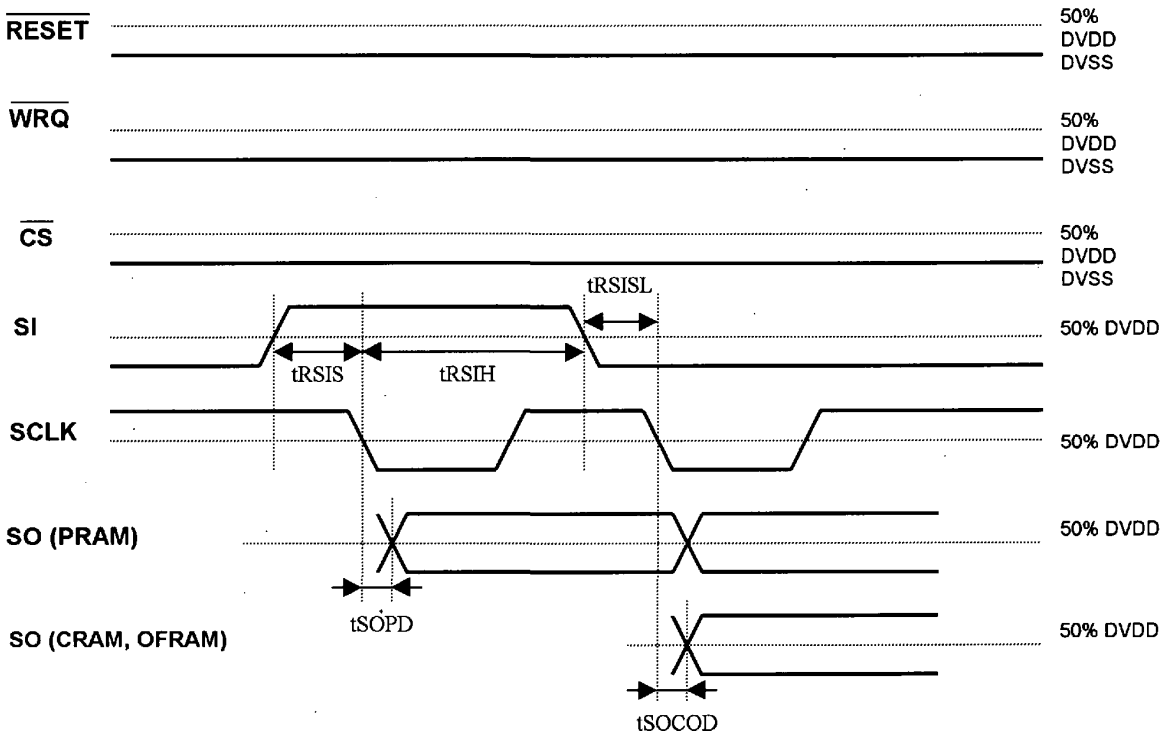


Note : Timing for RUN state is the same except that $\overline{\text{RESET}}$ is set to "H"
$\overline{\text{RESET}}$ represents system reset in normal use.

■ AK7714 to Microcomputer



■ AK7714 to Microcomputer (RAM data read-out)



Function Description

(1) Various settings

1) OPCL (pin 34): ADC and DAC connection selector pin (See Block Diagram on page 2.)

- Normally, OPCL is used in "L" or open. (Internal connection mode)
  In this case, ADC output and DAC1/DAC2 inputs are directly connected to the DSP internally. At this time, leave the SDINA (pin 12), SDIND1 (pin 17) and SDIND2 (pin 18) open or set to "L".
  It should be noted that "L" is output from the SDOUTA (pin 14), SDOUTD1 (pin 15) and SDOUTD2 (pin 20).
- When the OPCL is set to "H", the ADC output and DAC1/DAC2 inputs can be used independently from the DSP. (Input/output formats are restricted.)
  Note: SDINA supports only MSB-first 24-bit input (including I^2S compatibility).
  SDOUTA supports only MSB-first 20-bit output (including I^2S compatibility).
  SDIND1 and SDIND2 support only MSB-first 20-bit inputs (including I^2S compatibility).

2) CTRL1 (pin 62) and CTRL0 (pin 56): clock output control pins

CLKO output and LRCLK and BITCLK outputs in the master mode can be fixed to "L" or "H" by setting these two pins.

Mode	CTRL1	CTRL0	CLKO	Master mode LRCLK	Master mode BITCLK
1	0	0	Output	Output	Output
2	0	1	Disabled (This is a test mode, so do not use it.)		
3	1	0	"L"	Output	Output
4	1	1	"L"	"H" (For "L", see Note.)	"L"

Note: When CTRL1 and CTRL0 are used in the open state, Mode 1 will be selected.
Output is set to "L" when I^2S compatible.
Mode 4 can be used only when the AK7714 is used "Analog to Analog".

3) CKS1 (pin 64) and CKS0 (pin 63): Clock selector pin

CKS1	CKS0	XTI	DSP
0	0	384fs	384fs
0	1	512fs	512fs
1	0	256fs	256fs
1	1	Test mode (disabled)	

fs: Sampling frequency

4) SMODE (pin 65): Slave and master mode selector pin

Sets LRCLK (pin 36) and BITCLK (pin 37) to either input or output.

a) Slave mode: SMODE = "L"
   LRCLK (1 fs) and BITCLK (48 fs or 64 fs) become input.
b) Master mode: SMODE = "H"
   LRCLK (1 fs) and BITCLK (64 fs) become output.

5) Control registers

The control registers (16 bits) can be set via the microcomputer interface in addition to the control pins. For the value to be written in the control registers, see the description of the microcomputer interface. The following describes the control register map.

Control register map ([ ] indicates the default values.)

Code	Function		
C15	Selects the data reset function after reset is released.	[0: Used]	1: Unused
C14	Selects delay RAM sampling	[0: 1Sampling]	1: 2 Sampling
C13	Selects DRAM addressing method	[0: Ring addressing]	1: Linear addressing
C12	Random number generator circuit	[0: Unused]	1: Used
C11	Test mode (Use at 0)	[0: Normal operation]	1: Test mode
C10	Test mode (Use at 0)	[0: Normal operation]	1: Test mode
C9	Test mode (Use at 0)	[0: Normal operation]	1: Test mode
C8	Resets ADC section	[0: Normal operation]	1: Reset
C7	Sets internal path	[0: ADC serial data selected]	1: SDIN1 selected
C6	Sets internal path	[0: Normal setting]	1: Sets the path selected by C7
C5	DAC2 section reset control	[0: Normal operation]	1: DAC2 section reset
C4	DAC1 section reset control	[0: Normal operation]	1: DAC1 section reset
C3	SDOUT output enable	[0: SDOUT = Output]	1: SDOUT = "L"
C2 C1	Selects SDIN1 and SDIN2 input mode. Mode 1 (C2=0, C1=0): [MSB first (24 bits)] Mode 2 (C2=0, C1=1): LSB first (24 bits) Mode 3 (C2=1, C0=0): LSB first (20 bits) Mode 4 (C2=1, C1=1): LSB first (16 bit) Note: When CØ = 1, the state is I²S compatible independent of mode setting; however, set to Mode 1.		
C0	Select I²S compatible. [0: Normal setting] 1: I²S compatible (In this case, all input/output pins are I²S compatible.)		

Data can be loaded into the control registers only when $\overline{\text{DSP RESET}}$ = "L" and $\overline{\text{CODEC RESET}}$ = "L". If used otherwise, an operation error will occur. To avoid an operation error, do not use it.

a) C0, C1, C2

See (5) Audio data interface (internal connection mode)

b) C3

In case of not using the SDOUT, if this code is set "1" then the SDOUT outputs "L" level.

c) C4

In case of using only DAC2, this code can set to "1" and DAC1 will RESET. It can useful for saving the power consumption of DAC1. The output signals of AOUTL1 and AOUTR1 will be Hi-z.

d) C5

In case of using only DAC2, this code can set to "1" and DAC1 will RESET. It can useful for saving the power consumption of DAC1. The output signals of AOUTL1 and AOUTR1 will be Hi-z.

e) C6, C7

Normally C6 and C7 are "0" setting. In detail, please see (8) Special use, 2) Use as ADC and DAC (mainly for test).

f) C8

In case of not using the ADC part, this code can RESET the ADC part. In this case, the digital output from ADC will be "00000h" and it will save the power consumption of the ADC part.

g) C9, C10, C11

This is test mode. C9, C10 and C11 should be "0".

h) C12

This DSP has a single feedback type shift-register [24,21,19,18,17,16,15,14,14,19,9,5,1]s independently from calculation block.
This register change the data in every sampling time. And its output connected with DBUS, so in case of selected MSRG command at program code, then 24-bit random data will appear in every sampling .
In case of using this register, please set this code to "1".

i) C13

This code sets the addressing method of DRAM (Data Ram).
C13 = 0 : Ring addressing
C13 = 1 : Linear addressing.
DRAM has 128-word x 24-bit and has 2 addressing pointers (DP0, DP1).
The Ring addressing mode : Its start address increments 1 by every sampling time.
The Linear addressing mode : Its start address is always same , DP0 = 00h and DP1 = 40h.

j) C14

This code is setting for DLYRAM (internal 4k-word x 16-bit Delay RAM)sampling method.
Normally C14 = 0, this means its address pointer will work as ring addressing by every sampling.
If it set C14 = 1, this means the address pointer will work as ring addressing by every 2 sampling.
This is a decimation mode and it can extend delay time. But, it will appear aliasing.
When it is C14=1 mode, the Delay Ram area will consist 3 banks.
The bank 1 is from 000h to 3FFh : (The address of this area is always 1 sampling ring addressing.)
The bank 2 , bank 3 and bank 4 (400h to 7FFh, 8FFh to BFFh and C00h to FFFh) can set to decimation mode.

k) C15

Normally it should be C15=0. At this time after release the system reset, DRAM (Data Ram) and DLYRAM (Internal delay Ram) will be clear to "0" .
It takes 8LRCLK at 512fs mode, 11LRCLK at 384fs mode and 16LRCLK at 256fs mode after the Reset pulse comes out. The Reset pulse comes out at first rising point of LRCLK at master mode and in case of slave mode, it comes out about after 3LRCLK.

(2) Power supply startup sequence

Turn on the power by setting to $\overline{\text{INIT RESET}}$ = "L",$\overline{\text{DSP RESET}}$ = "L" and $\overline{\text{CODEC RESET}}$ = "L".
Then the AK7714 is initialized by setting to $\overline{\text{INIT RESET}}$ = "H". Note 1)
Initialization by $\overline{\text{INIT RESET}}$ is sufficient if it is done only when the power is turned on.

Note1: Set to $\overline{\text{INIT RESET}}$ = "H" after setting the oscillation when a crystal oscillator is used.
This setting time may differ depending on the crystal oscillator and its external circuit.

2: Do not stop the system clock (slave mode: XTI, LRCLK, BITCLK, master mode: XTI) except when $\overline{\text{INIT RESET}}$ = "L".
If these clock signals are not supplied, too much current will flow because the dynamic logic is used internally, and an operation failure may result.

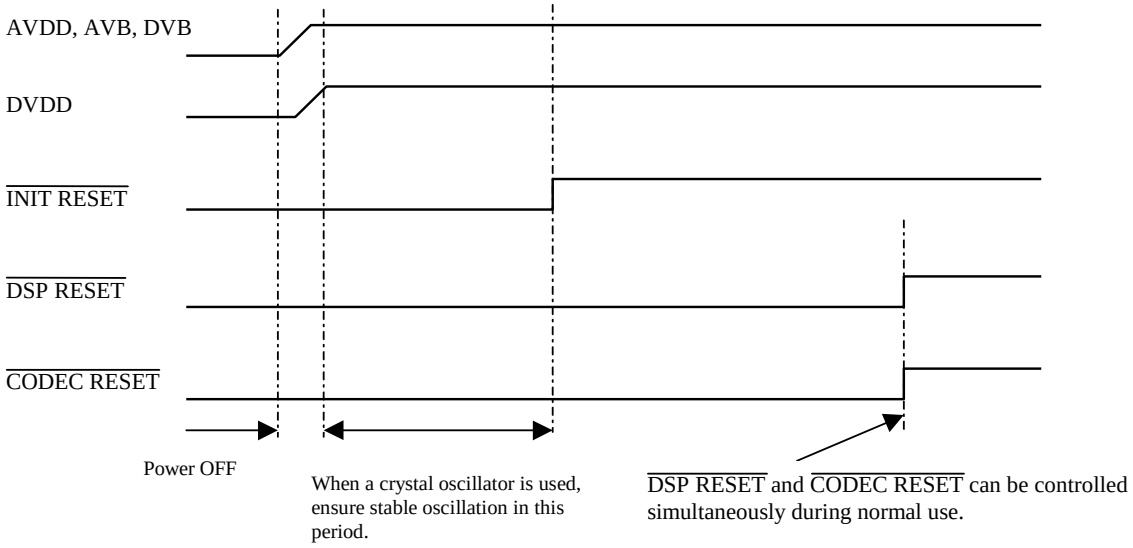


Fig. Power supply startup sequence

(3) Resetting

The AK7714 has three reset pins: $\overline{\text{INIT RESET}}$,$\overline{\text{DSP RESET}}$ and $\overline{\text{CODEC RESET}}$.
The $\overline{\text{INIT RESET}}$ pin is used to initialize the AK7714, as shown in "Power supply startup sequence above."
$\overline{\text{DSP RESET}}$ and $\overline{\text{CODEC RESET}}$ are normally controlled simultaneously. The system is reset when
$\overline{\text{DSP RESET}}$ = "L" and $\overline{\text{CODEC RESET}}$ = "L". (Description of "reset" is for "system reset".)
Under the condition of this system reset, the program write operation is performed (except for write operation during running).
During the system reset phase, the ADC and DAC sections are also reset. (The digital section of ADC output is MSB first 00000h and the analog section of DAC output is Hi-z.)
CLKO is output even during the system reset phase if CTRL (1:0) = 0h (Mode 1), but LRCLK and BITCLK in the master mode will stop.
The system reset is released by setting either $\overline{\text{DSP RESET}}$ or $\overline{\text{CODEC RESET}}$ to "H", and this will activate the internal counter. LRCLK and BITCLK in the master mode are generated by this counter: however, a hazard may occur when a clock signal is generated. When the system reset is released in the slave mode, internal timing will be actuated in synchronization with "↑" of LRCLK (when the standard input format is used). Timing between the external and internal clocks is adjusted at this time. If the phase difference in LRCLK and internal timing is within about -1/16 to 1/16 of the input sampling cycle (1/fs) during the operation, the operation is performed with internal timing remaining unchanged. If the phase difference exceeds the above range, the phase is adjusted by synchronization with "↑" of LRCLK (when the standard input format is used). This is a circuit to prevent failure of synchronization with the external circuit owing to noise and the like. For some time after returning to the normal state after loss of synchronization, normal data will not be output. If you want to change the clock, do so while the system is reset.
The ADC section can output 516-LRCLK after its internal counter started. (The internal counter starts at the first rising edge of LRCLK at master mode. In case of slave mode, it starts end of 2LRCLK after release of system reset.)
The AK7714 performs normal operation when both $\overline{\text{DSP RESET}}$ and $\overline{\text{CODEC RESET}}$ are set to "H".

(4) System clock

The required system clock is XTI (256 fs/384 fs/512 fs), LRCLK (fs) and BITCLK (64 fs) in the slave mode, and is XTI (256 fs/384 fs/512 fs) in the master mode.
LRCLK corresponds to the standard digital audio rate (32 kHz, 44.1 kHz, 48 kHz).

fs	XTI (Master clock)			BITCLK
	256 fs	384 fs	512 fs	64 fs
32.0 kHz	- Note	12.2880 MHz	16.3840 MHz	2.0480 MHz
44.1 kHz	11.2896 MHz	16.9344 MHz	22.5792 MHz	2.8224 MHz
48.0 kHz	12.2880 MHz	18.4320 MHz	- Note	3.0720 MHz

Note: 256 fs is not supported at fs = 32.0 kHz. 512fs is not supported at fs = 48.0 kHz.

SMODE	CKS1	CKS0	XTI	LRCLK, BITCLK
L	L	L	384 fs	Input
L	L	H	512 fs	Input
L	H	L	256 fs	Input
H	L	L	384 fs	Output
H	L	H	512 fs	Output
H	H	L	256 fs	Output

1) Master clock (XTI pin)

The master clock is obtained by connecting a crystal oscillator between the XTI pin and XTO pin or by inputting an external clock into the XTI pin while the XTO pin is open.
CLKO outputs a clock having the same frequency as the XTI. (The phase is different. Also, the phase difference varies slightly according to the product. When a crystal oscillator is used, the same frequency is obtained after the oscillation of the crystal oscillator has settled.)
In the AK7714, CLKO will be output when power is turned on and oscillation has occurred.
If CLKO is not required, set to CTRL1 = "H".

2) Slave mode

The required system clock is XTI (256 fs/384 fs/512 fs), LRCLK (1 fs) and BITCLK (48/64 fs).
The master clock (XTI) and LRCLK must be synchronized, but the phase does not have to be adjusted.

3) Master mode

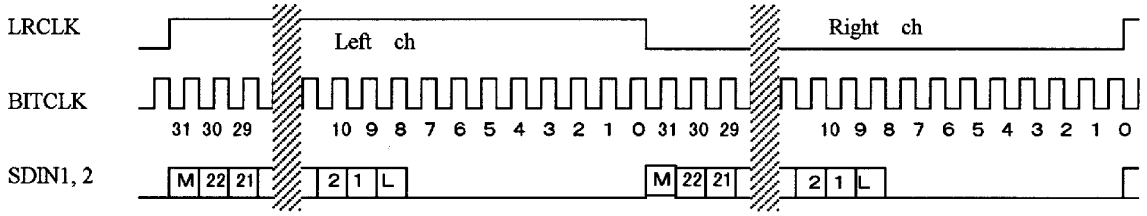
The required system clock is XTI (256 fs/384 fs/512 fs). When the master clock (XTI) is input, LRCLK (1 fs) and BITCLK (64 fs) will be output from the internal counter synchronized with the XTI. (CTRL0 = "L" during normal operation.)
LRCLK and BITCLK will not be output during initial reset ($\overline{\text{INIT RESET}}$ = "L") and system reset ($\overline{\text{DSP RESET}}$ = $\overline{\text{CODEC RESET}}$ = "L").

(5) Audio data interface (internal connection mode)

The serial audio data pins SDIN1, SDIN2 and SDOUT (OPCL = L: Internal connection mode) are interfaced with the external system, using LRCLK and BITCLK. The data format is the first MSB of the 2's complement. Normally, the input/output format, in addition to the standard format used by AKM, can be changed to the I^2S compatible mode by setting the control register C0 to 1. (In this case, all input/output audio data pin interface is in the I^2S compatible mode.)
The input SDIN1 and SDIN2 formats are adjusted (24 bits) at initialization. Setting the control registers C2 and C1 will cause them to be compatible with 24 bits, 20 bits and 16 bits. (Note: C0 = 0)
However, inidividul setting of SDIN1 and SDIN2 is not allowed.
The output SDOUT is fixed at 24 bits.
At slave mode BITCLK corresponds to not only 64fs but also 48fs. But, we recommend 64fs. Following formats describe 64fs examples.

1) Standard input format (C0 = 0: initial set value)

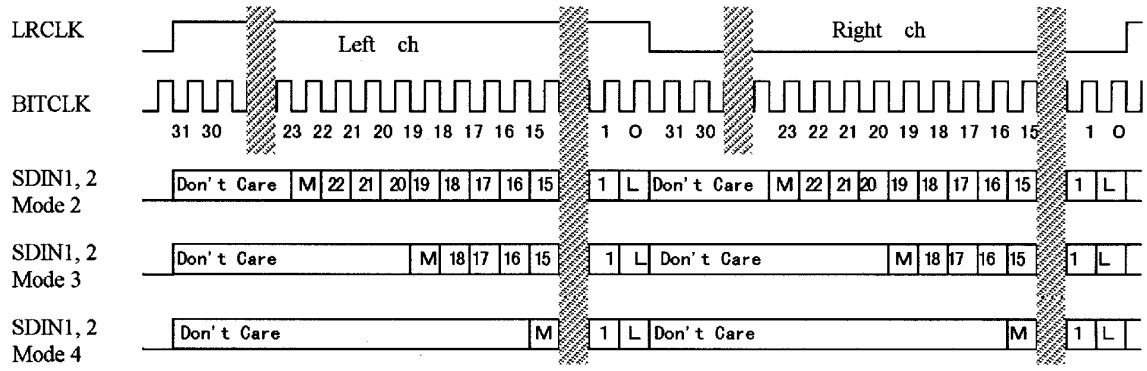
a) Mode 1 (C2, C1 = 0, 0: Initial set value)



M: MSB, L: LSB

• When you want to input the MSB-first 20-bit data into SDIN1 and 2, input four "0s" following the LSB.

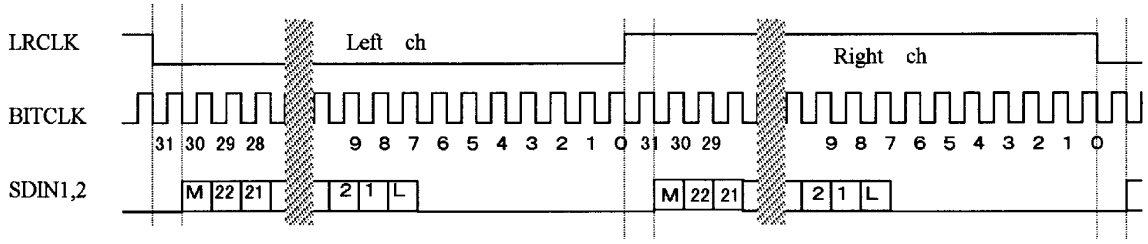
b) Mode 2, Mode 3 and Mode 4



M : MSB, L : LSB

SDIN1 and 2 Mode 2: (C2, C1) = (0, 1) 24 bits
SDIN1 and 2 Mode 3: (C2, C1) = (1, 0) 20 bits
SDIN1 and 2 Mode 4: (C2, C1) = (1, 1) 16 bits

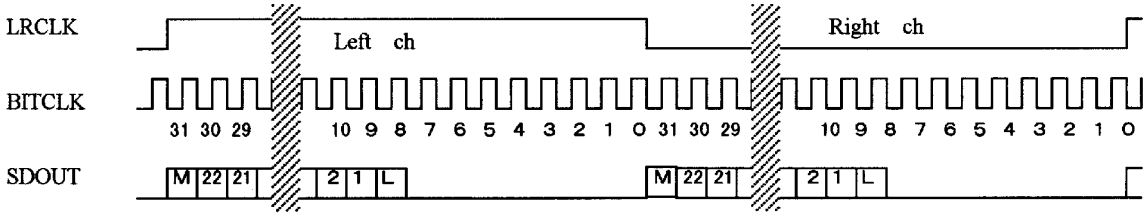
2) I²S compatible input format (C0 = 1)



M: MSB, L: LSB

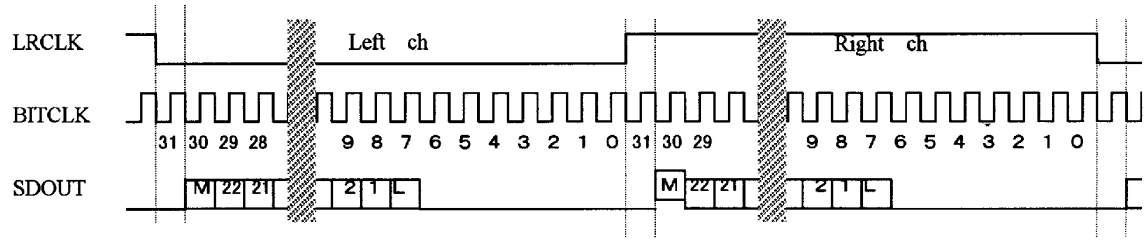
Mode 1: (C2, C1) = (0, 0) must be set.

3) Standard output format (C0 = 0: initial set value)



M: MSB, L: LSB

4) I²S compatible output format (C0 = 1)



M: MSB, L: LSB

(6) Interface with microcomputer

Interface with the microcomputer is provided by 7 control signals: $\overline{CS}$ (Chip Select Bar), $\overline{WRQ}$ (Write ReQuest Bar), SCLK (Serial data input CLocK), SI (Serial data Input), SO (Serial data Output), RDY (ReaDY) and DRDY (Data ReaDY).
In the AK7714, two types of operations are provided; writing and reading during the reset phase (namely, system reset) and those during the run phase. During the reset phase, data can be written to the control register, program RAM,coefficient RAM, offset RAM, and external conditional jump code, and data can be read from the program RAM,coefficient RAM and offset RAM. During the run phase, data can be written to the coefficient RAM,offset RAM and external conditional jump code, and data on the DBUS (data bus) can be read from SO.
$\overline{CS}$ is used also for SO control in addition to the chip selection. When only one AK7714 is used without SO, $\overline{CS}$ = "L" is allowed at all times.
If there is no communication with the microcomputer, set SCLK to "H" and SI to "L" for use.

Data is serially input and output with the MSB first. The following 8-bit command data is sent first, and the specified work is performed.

Command code list

Contents of command	Conditions for use:	Code (C7C6C5C4C3C2C1C0)	
Program RAM write	[RSPW]	During reset phase:	Code (11000000)
External conditional JMP code write	[JCON]	both reset and run phases:	Code (11000100)
Coefficient RAM write	[RSCW]	during reset phase:	Code (10100000)
Coefficient RAM write	[RNCW]	during run phase:	Code (10100100)
Offset RAM write	[RSOW]	during reset phase:	Code (10010000)
Offset RAM write	[RNOW]	during run phase:	Code (10010100)
CRAM/OFFRAM rewrite preparation	[BNBW]	during run phase:	Code (10001000)
Control register write	[CONW]	during reset phase:	Code (00000110)
Program RAM read		during reset phase:	Code (11000011)
Program CRAM read		during reset phase:	Code (10100001)
Program OFRAM read		during reset phase:	Code (10010001)

NOTE: Do not send codes other than the above command codes. Otherwise, an operation error may occur.

1) Write during reset phase

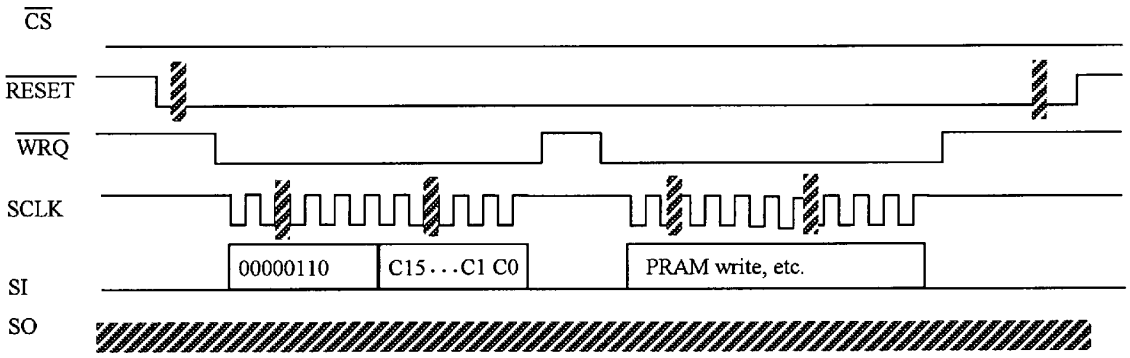
a) Control register write (during reset phase)

Data comprising a set of three bytes is used to perform the control register write operation (during the reset phase). When all data has been transferred, the RDY terminal goes to "L". It goes to "H" upon completion of the write operation.

Data transfer procedure

①	Command code	(00000110)
②	Control data	(C15.....C8)
③	Control data	(C7 .....C0)

The register to control the operation mode of this LSI comprises 16 bits. For the function of each bit, see the description of 5) "Control registers" on page 22.



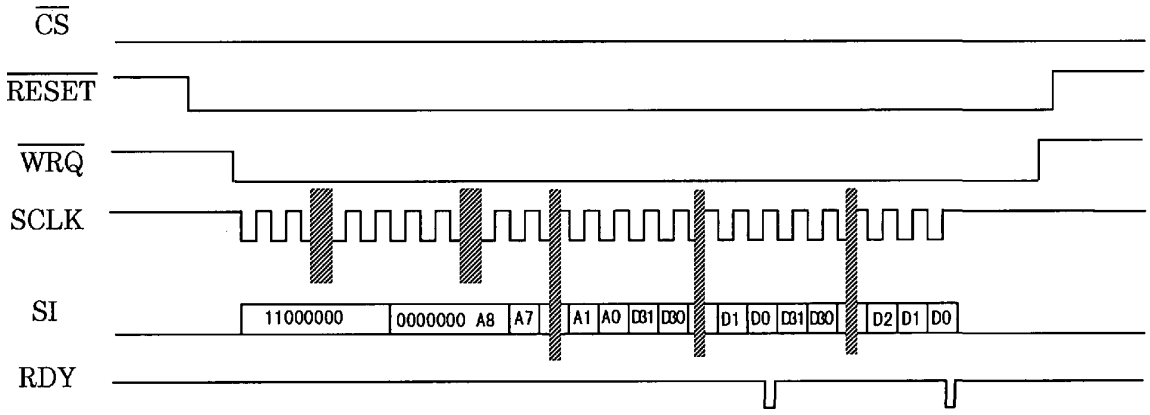
Control register write operation

b) Program RAM write (during reset phase)

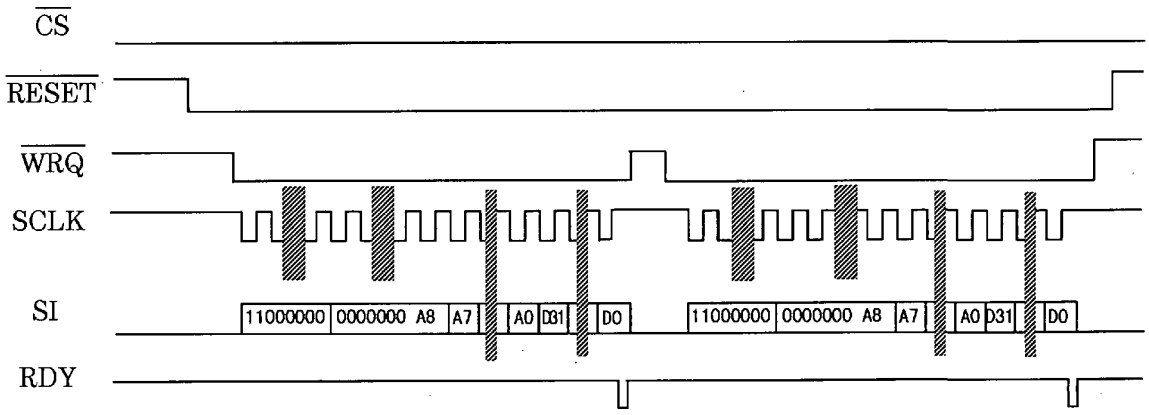
The program RAM write operation is performed during the reset phase according to data comprising a set of 7 bytes (in case of 1-word program RAM writting). When all data has been transferred, the RDY terminal is set to "L". Upon completion of writing into PRAM, it goes to "H" to allow the next data to be input. When data of continuous addresses is written, input the data(④ to ⑦) of after the next address as is. (No command code or address is required and $\overline{\text{RESET}}$ and $\overline{\text{WRQ}}$ hold to "L".) To write discontinuous data, shift the $\overline{\text{WRQ}}$ terminal from "H" to "L" again. Then input the command code, address and data in that order. (For $\overline{\text{RESET}}$, operate both $\overline{\text{CODEC RESET}}$ and $\overline{\text{DSP RESET}}$ simultaneously.)

Data transfer procedure

①	Command code	(11000000)
②	Address upper	(0000000A8)
③	Address lower	(A7.....A0)
④	Data	(D15 .....D8)
⑤	Data	(D23 .....D16)
⑥	Data	(D15 .....D8))
⑦	Data	(D7.....D0)



Input of continuous address data into PRAM



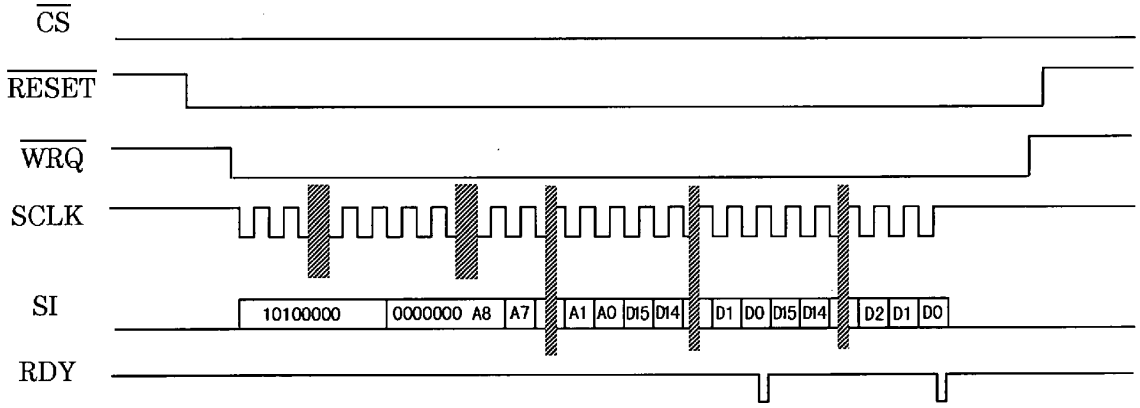
Input of discontinuous address data into PRAM

c) Coefficient RAM write (during reset phase)

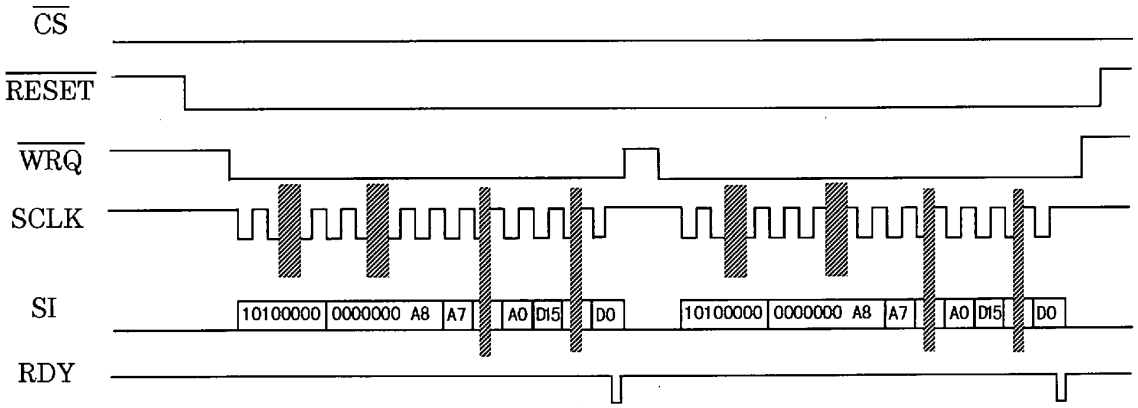
Data comprising a set of 5 bytes (in case of 1-word CRAM writting) is used to perform the coefficient RAM write operation (during the reset phase). When all data has been transferred, the RDY terminal goes to "L". Upon completion of writing into CRAM, it goes to "H" to allow the next data to be input. When data of continuous addresses is written, input the data(④ to ⑤) of after the next address as is. (No command code or address is required and $\overline{\text{RESET}}$ and $\overline{\text{WRQ}}$ hold to "L".) To write discontinuous data, shift the $\overline{\text{WRQ}}$ terminal from "H" to "L". Then input the command code, address and data in that order.
(For $\overline{\text{RESET}}$, operate both $\overline{\text{CODEC RESET}}$ and $\overline{\text{DSP RESET}}$ simultaneously.)

Data transfer procedure

①	Command code	(10100000)
②	Address upper	(0000000A8)
③	Address lower	(A7.....A0)
④	Data	(D15 ..... D8)
⑤	Data	(D7.....D0)



Input of continuous address data into CRAM



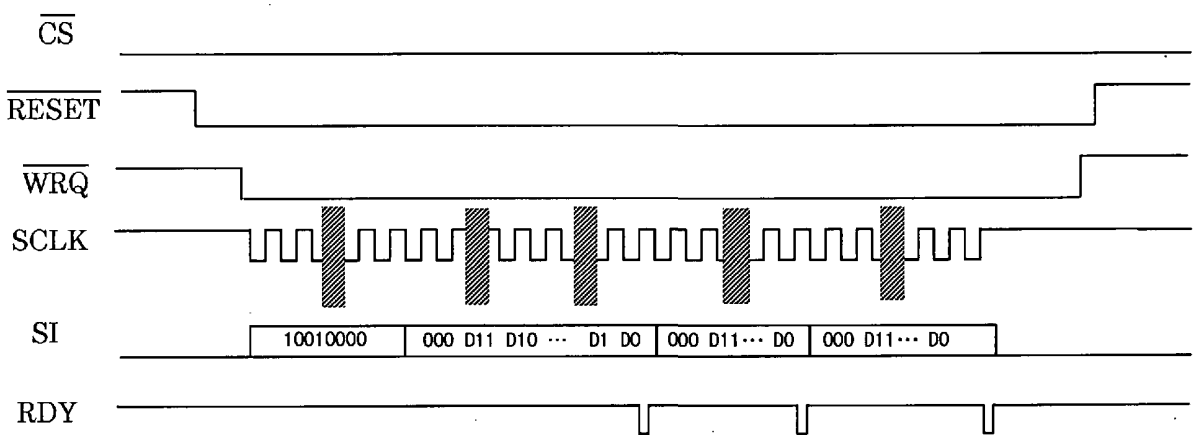
Input of discontinuous address data into CRAM

d) Offset RAM write (during reset phase)

Data comprising a set of 3 bytes (in case of 1-word Offset RAM writting) is used to perform offset RAM write operation (during the reset phase). In this case the operation must be started from address 0. When data of continuous addresses is written, input the data(② to ③) of after the next address as is. (No command code is required and $\overline{\text{RESET}}$ and $\overline{\text{WRQ}}$ hold to "L".) When all data has been transferred, the RDY terminal goes to "L". Upon completion of writing into the OFFRAM, it goes to "H" to allow the next data to be input.
(For $\overline{\text{RESET}}$, operate both $\overline{\text{CODEC RESET}}$ and $\overline{\text{DSP RESET}}$ simultaneously.)

Data transfer procedure

① Command code	(10010000)
② Data	(0000 D11 D10 D9 D8)
③ Data	(D7.....D0)

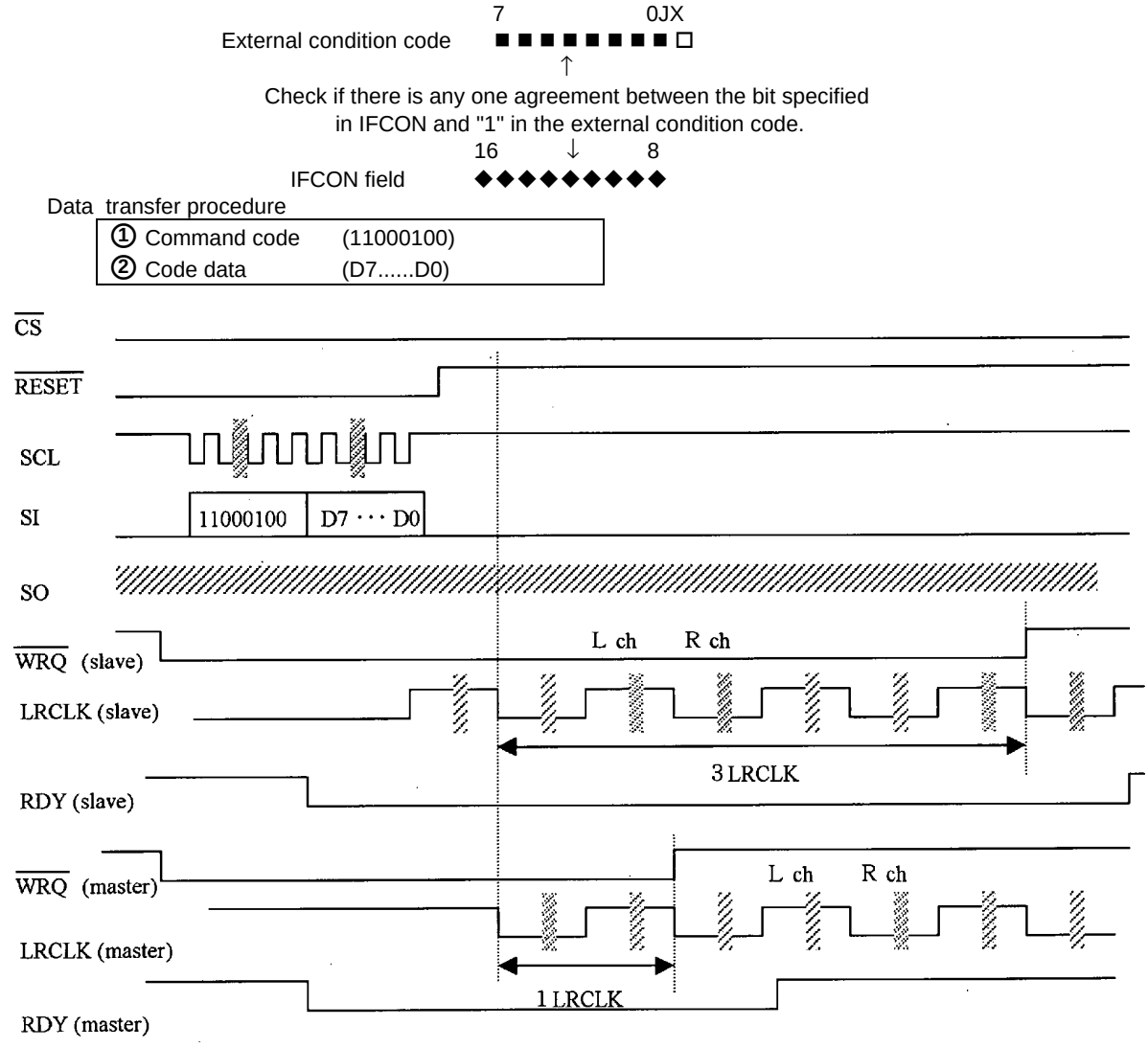


Input of data into OFFRAM

e) External conditional jump code write (during reset phase)

Data comprising a set of two bytes is used to perform the external conditional jump code write operation. The data can be input during both the reset and operation phases, and the input data is set to the specified register at the leading edge of LRCLK. When all data has been transferred, the RDY terminal goes to "L". Upon completion of writing, it goes to "H". A jump command will be executed if there is any one agreement between "1" of each bit of the external condition code 8 bits (soft set) plus 1 bit (hard set) at the external input terminal JX and "1" of each bit of the IFCON field. The data during the reset phase can be written only before release of the reset, after all data has been transferred. $\overline{WRQ}$ transition from "L" to "H" in the write operation during the reset phase must be executed after three LRCLK in the slave mode and one LRCLK in master mode, respectively, from the falling edge of LRCLK after release of the reset. Then RDY goes to "H" after capturing the rise of the next LRCLK. Write operation from the microcomputer is disabled until RDY goes to "H". The IFCON field provides external conditions written on the program.

Note: The LRCLK phase is inverted in the I2S-compatible state.



Timing for external conditional jump write operation (during reset phase)

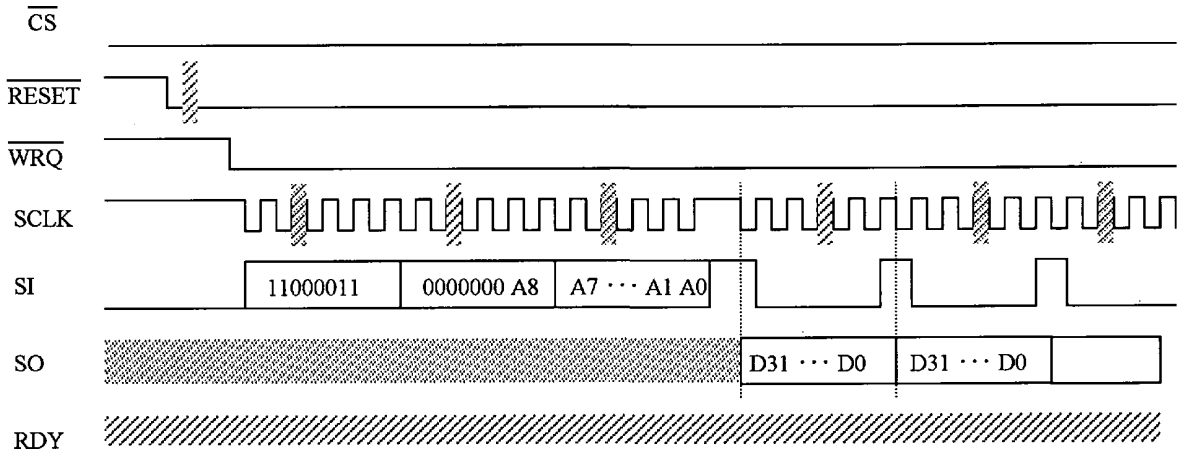
2) Read during reset phase

a) Program RAM read (during reset phase)

To read data written into PRAM, input the command code and the address you want to read out. After that, set SI to "H" and SCLK to "L". Then the data is output from SO in synchronization with the falling edge of SCLK. (Ignore the RDY operation that will occur in this case.)
If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to "H".

Data transfer procedure

①	Command code input	(11000011)
②	Read address input	(0.....A8)
		(A7.....A0)



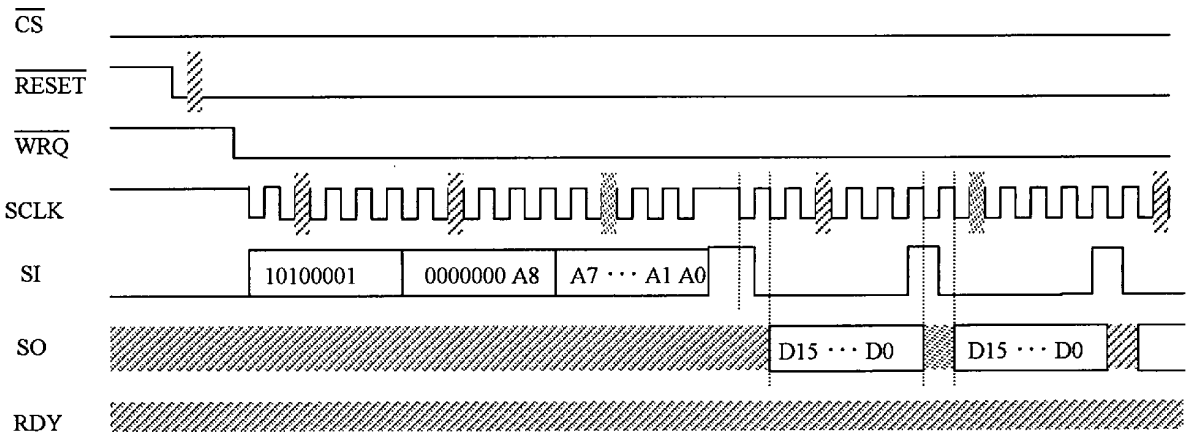
Reading of PRAM data

b) CRAM data read (during reset phase)

To read out the written coefficient data, input the command code and the address you want to read out. After that, set SI to "H" and SCLK to "L" as preparation. Then, when SI is set to "L", the data is output from SO in synchronization with the falling edge of SCLK.
If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to "H".

Data transfer procedure

① Command code	(10100001)
② Address	(0.....A8)
	(A7.....A0)



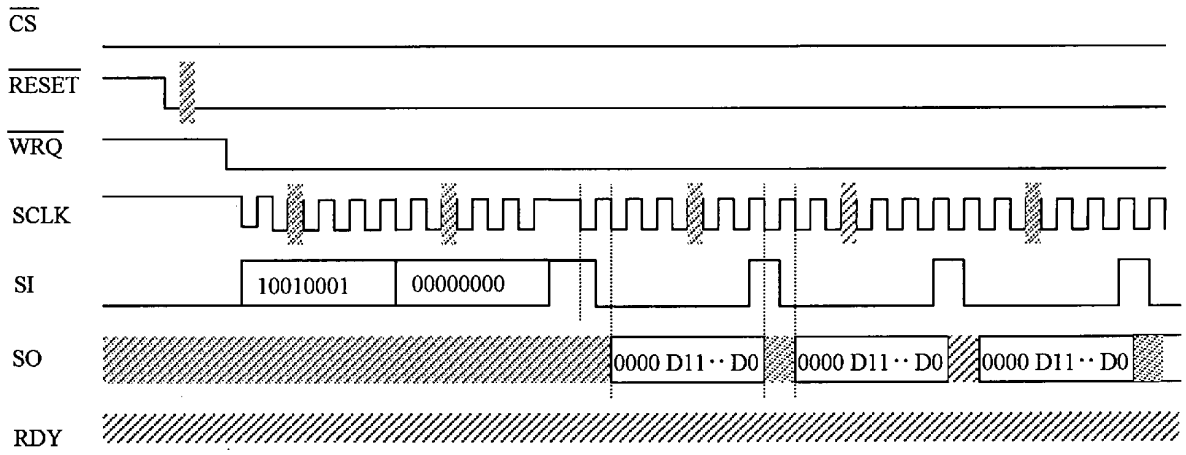
Reading of CRAM data

c) OFRAM data read (during reset phase)

The written offset data can be read out during the reset phase. To read it, input the command code and 8-bit "0". After that, set SI to "H" and SCLK to "L". This completes preparation for outputting the data. Then set SI to "L", and the data is output in synchronization with the falling edge of SCLK. In this case, OFRAM can be output only from the address data at address 0.

Data transfer procedure

① Command code	(10010001)
② Data input	(00000000)



Reading of OFRAM data

3) Write during RUN phase

a) CRAM/OFRAM rewrite preparation and write (during RUN phase)

This function is used to rewrite CRAM (coefficient RAM) and OFRAM (offset RAM) during program execution. After inputting the command code, you can input a maximum of 16 data of the continuous addresses you want to rewrite. Then input the write command code and rewrite the leading address. Every time the RAM address to be rewritten is specified, the contents of RAM are rewritten. The following is an example to show how five data from address "10" of the coefficient RAM are rewritten:

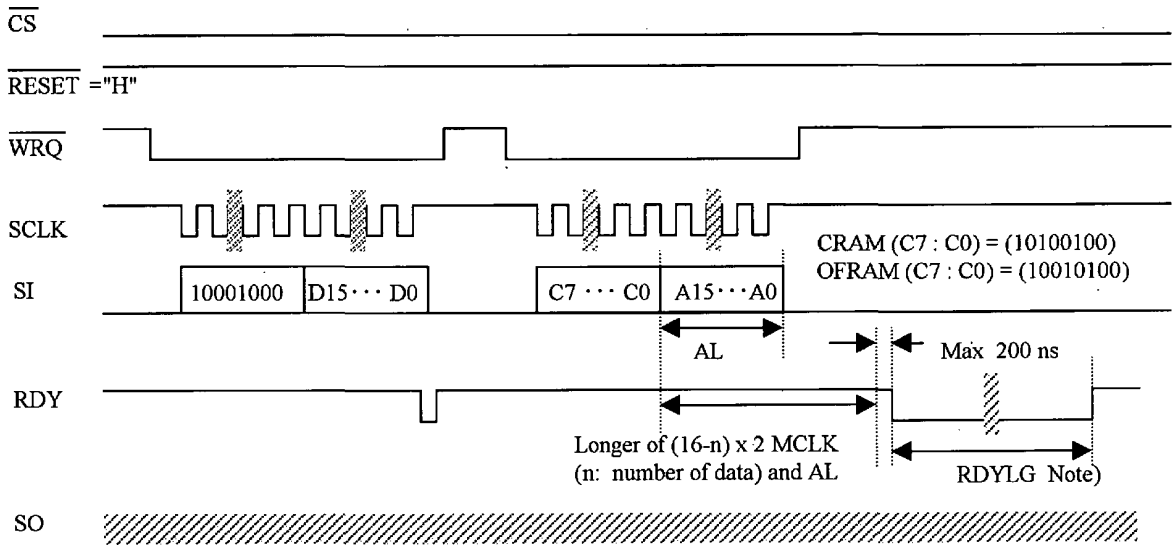
Coefficient RAM execution address	7	8	9	10	11	13	16	11	12	13	14	15
			↓	↓				↓	↓	↓		
Rewrite position			○	○	↑			○	○	○		

Note that address "13" is not executed until address "12" is rewritten.

Data transfer procedure

*Preparation for rewrite		① Command code	(10001000)
		② Data	(D15 .....D8)
		③ Data	(D7.....D0)
*Rewrite	1) CRAM	① Command code	(10100100)
		② Address upper	(0000000A8)
		③ Address lower	(A7000...A0)
	2) OFRAM	① Command code	(10010100)
		② Address upper	(00000000)
		③ Address lower	(000A4...A0)

Note: CRAM ranges from A8 to A0.
OFRAM ranges from A4 to A0.



Note: The RDY signal will go to high within the maximum of two LRCLKs if the RDYLG width is programmed to ensure a new address to be rewritten within one sampling cycle.

CRAM and OFRAM rewriting preparation and writing

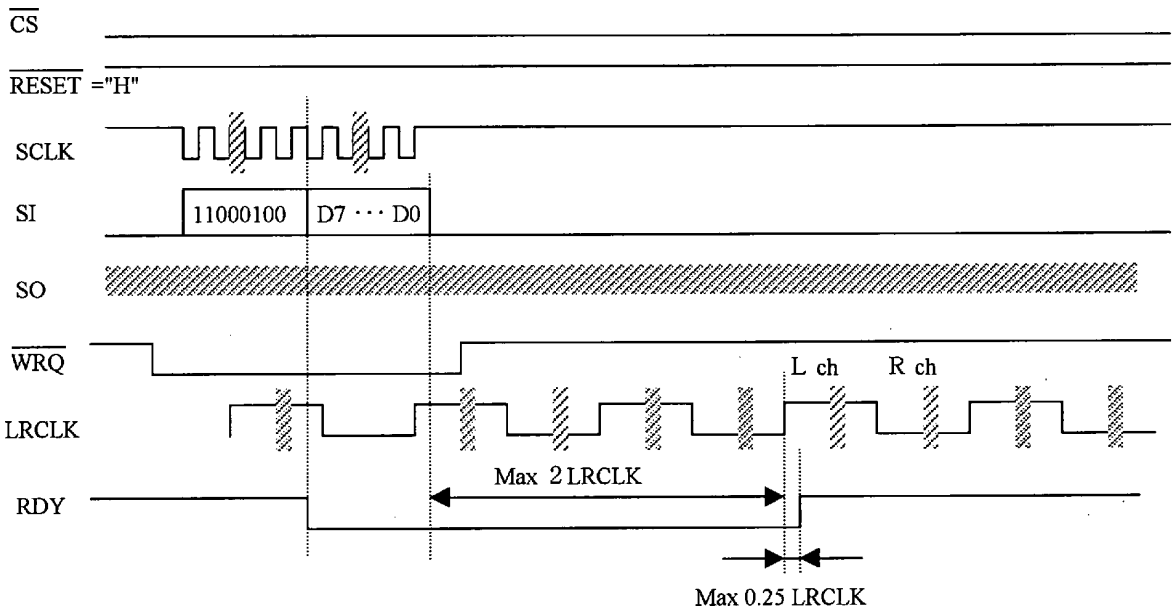
b) External conditional jump code rewrite (during RUN phase)

Data comprising a set of two bytes is used to write the external conditional jump code. Data can be input during both the reset and operation phases, and input data is set to the specified register at the rising edge of LRCLK. When all data has been transferred, the RDY terminal goes to "L". Upon completion of writing, it goes to "H". A jump command will be executed if there is any one agreement between each bit of the 8-bit external condition code and "1"of each bit of the IFCON field. A write operation from the microcomputer is disabled until RDY goes to "H".

Note: The LRCLK phase is inverted in the I2S-compatible state.

Data transfer procedure

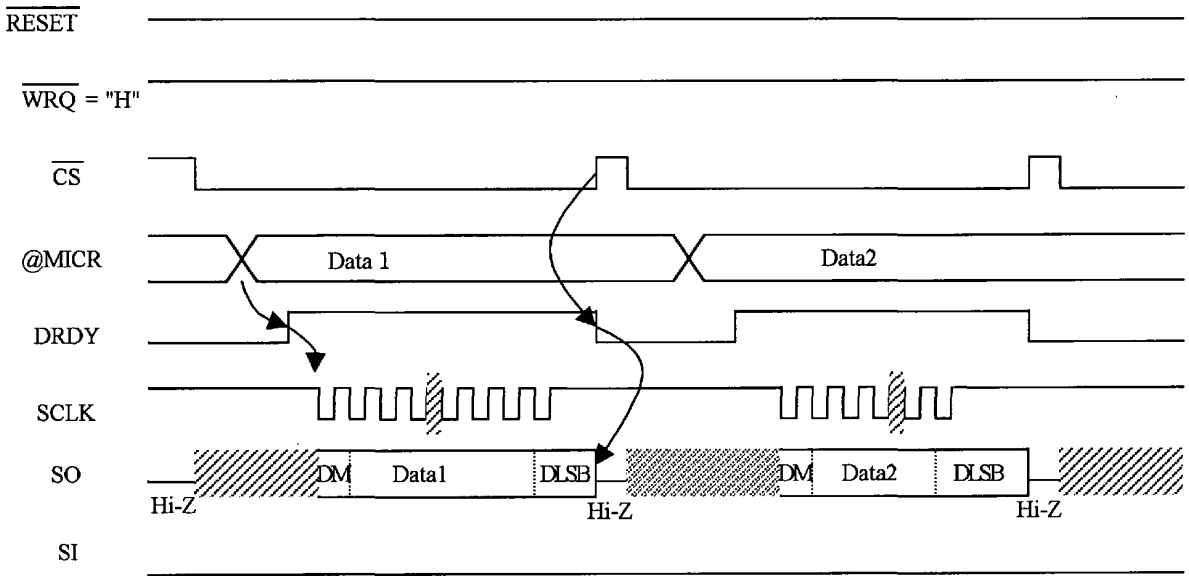
①	Command code	(11000100)
②	Code .data	(D7.....D0)



External condition jump write timing (during RUN phase)

4) Read-out during RUN phase (SO output)

SO outputs data on DBUS (data bus) of the DSP section. Data is set when @MICR is specified by the DST field. Setting of data allows DRDY to go to "H", and data is output synchronized with the falling edge of SCLK. When $\overline{CS}$ goes to "H", DRDY goes to "L" to wait for the next command. Once DRDY goes to "H", the data of the last @MICR command immediately before DRDY goes to "H" will be held until $\overline{CS}$ goes to "H", and subsequent commands will be rejected.
A maximum of 24 bits are output from SO. After the required number of data (not exceeding 24 bits) is taken out by SCLK, the next data can be output by setting $\overline{CS}$ to "H".



SO read (during RUN phase)

(7) ADC section high-pass filter

The AK7714 incorporates a digital high-pass filter (HPF) for cancelling the section DC offset in the ADC section. The HPF cut-off frequency is about 1 Hz (fs = 48 kHz). This cut-off frequency is proportional to the sampling frequency (fs).

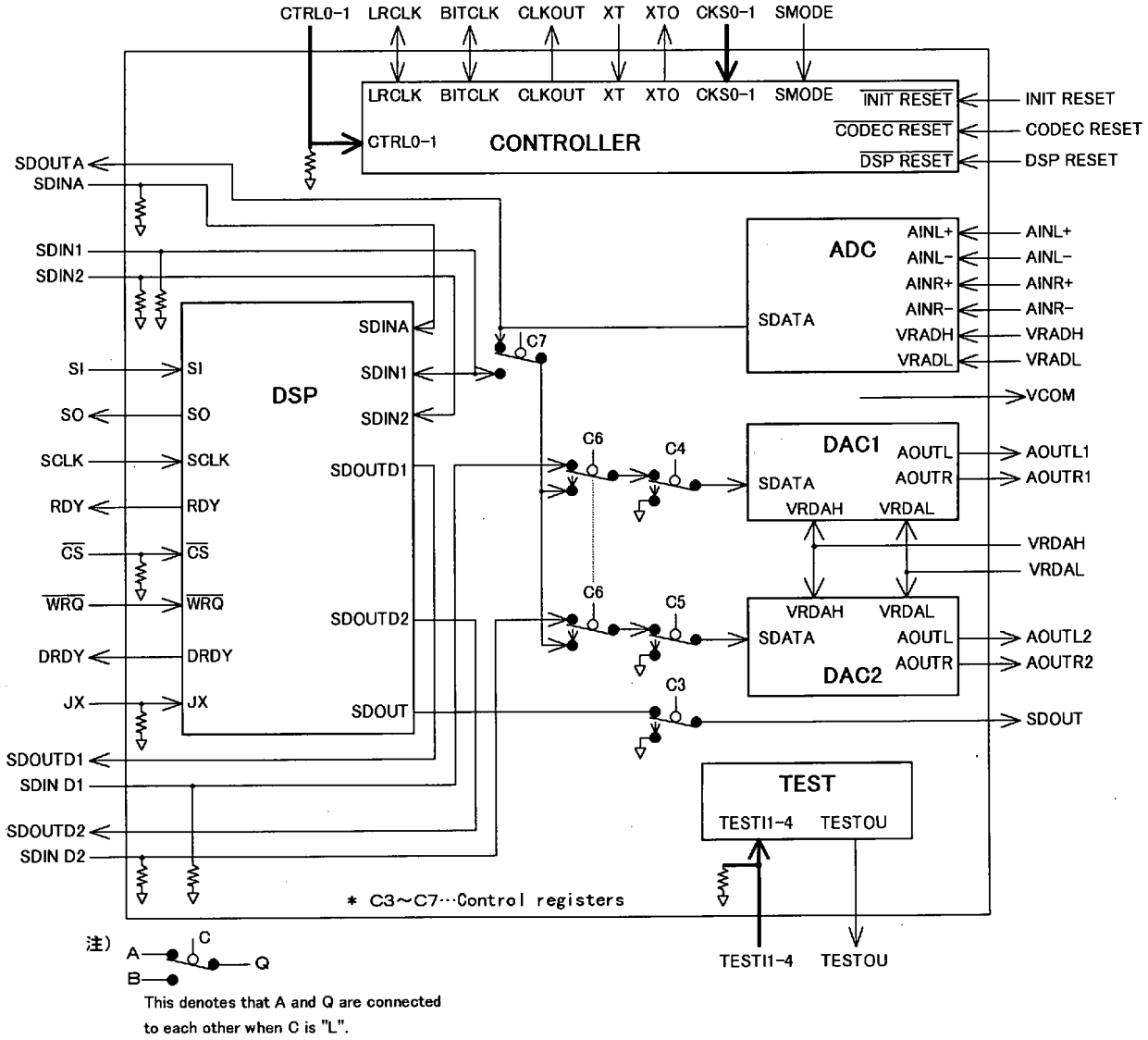
	48 kHz	44.1 kHz	32 kHz
Cut-off frequency	0.93 Hz	0.86 Hz	0.62 Hz

(8) Special use

1) External connection mode

Normally, OPCL is used at "L" (internal connection mode), but when OPCL is set to "H", the ADC output and DAC1/DAC2 inputs can be used independently form DSP. (External connection mode)

OPCL = "H": External connection mode



The following shows the input/output interface in external connection mode:

- SDINA for MSB-first 24-bit input (including I^2S compatibility)
- SDOUTA for MSB-first 20-bit output (including I^2S compatibility)
- SDOUTD1 and SDOUTD2 for MSB-first 24-bit outputs (including I^2S compatibility)
- SDIND1 and SDIND2 for MSB-first 20-bit inputs (including I^2S compatibility)

Conversion between the input/output standard format and I^2S is interlocked with the control register C0, similar to the case for internal connection mode.

2) Use as ADC and DAC (mainly for test)

Only the ADC and DAC sections can be operated while keeping the DSP section in the reset state with the independent control of $\overline{\text{DSP RESET}}$ and $\overline{\text{CODEC RESET}}$. (When no DSP processing is required, power saving and noise reduction can be expected. However, the ADC data cannot be output in internal connection mode. In external connection mode, it is output from SDOUTA.)

In internal connection mode, setting of the control registers allows the following operations to be performed:

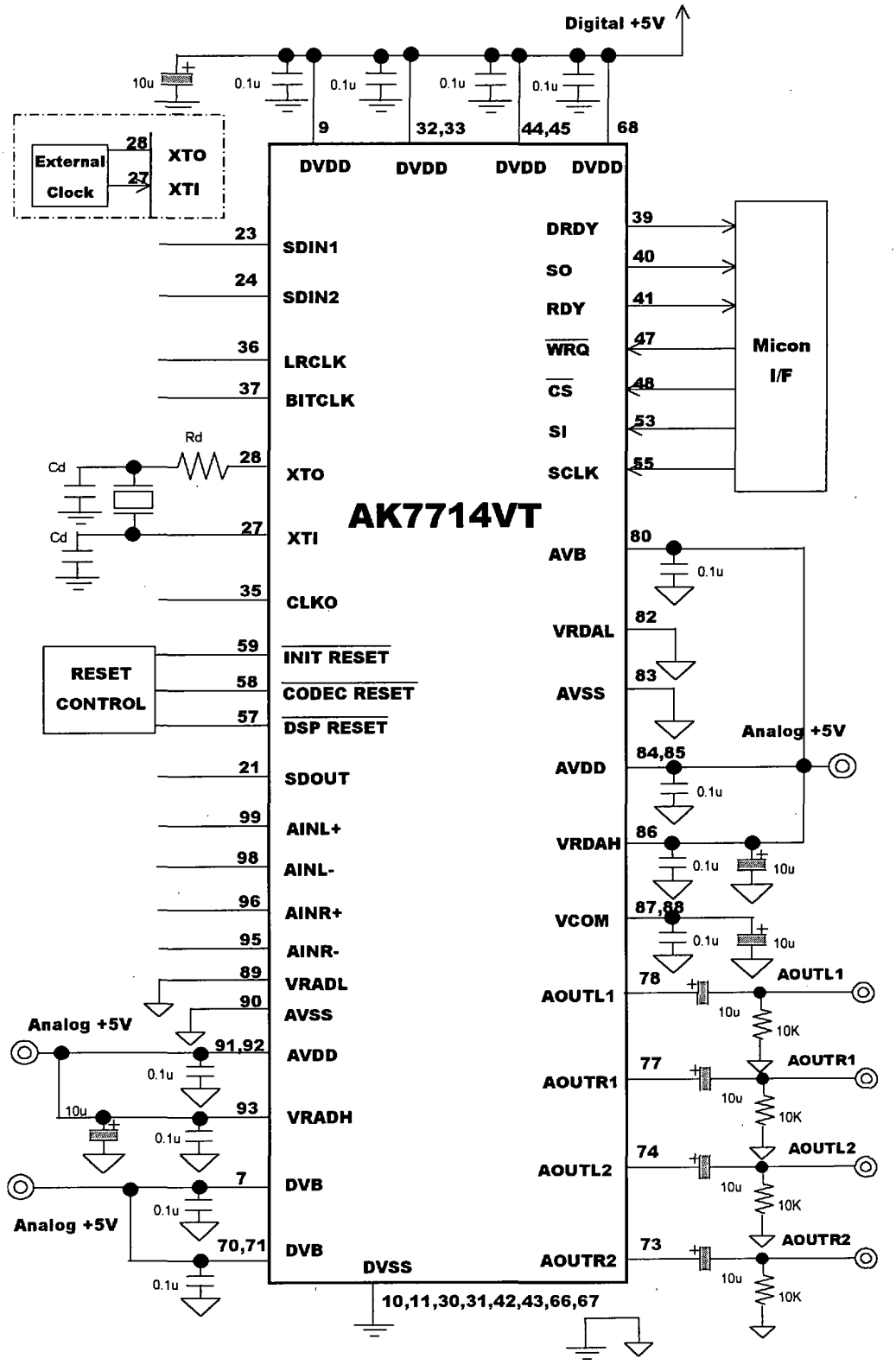
a) ADC to DAC1 and DAC2 (Analog to Analog)
The ADC output data is directly connected over to DAC1 and DAC2. (C6 = 1, C7 = 0)
When input to the DAC2 is not required, set C5 = 1.
(When input to the DAC1 is not required, set C4 = 1.)

b) SDIN1 to DAC1 and DAC2
SDIN1 input data is directly connected to DAC1 and DAC2. (C6 = 1, C7 = 1)
In this case, only the MSB-first 20-bit input (including I^2S compatibility: C0 = 1) is supported.
When input to DAC2 is not required, set C5 = 1.
(When input to DAC1 is not required, set C4 = 1.)

For this operation, set only $\overline{\text{CODEC RESET}}$ to "H" after setting the control registers during the system reset phase ($\overline{\text{DSP RESET}}$ = $\overline{\text{CODEC RESET}}$ = "L"). To make a new setting, be sure to perfom the system reset.

System Design

(1) Example circuit



(2) Peripheral circuit

1) Ground and power supply

To minimize digital noise coupling, AVDD and DVDD are individually decoupled in AK7714. System analog power is supplied to AVDD, AVB and DVB. AVB and DVB are connected to each other through the IC board, and eventually have several ohms of resistance. If the set of AVDD, AVB and DVB and DVDD are driven by individual power sources, start up AVDD, AVB and DVB simultaneously with DVDD, or start up AVDD, AVB and DVB first.
Generally, power supply and ground wires must be connected separately according to the analog and digital systems. Connect them at a position close to the power source on the PC board. Decoupling capacitors, and ceramic capacitors of small capacity in particular, should be connected at positions as close as possible to the AK7714.
If the absolute maximum rating conditions of a power supply cannot be maintained depending on the system, it is recommended to supply the AK7714 power from the same regulator. Power patterns must be separated into analog and digital patterns. For a digital pattern, connection must be made through an appropriate one-ohm resistor from the regulator. In this case, the capacitor with the larger capacity must be connected to the analog side.

2) Reference voltage

The input voltage difference between the VRADH pin and the VRADL pin determines the full scale of analog input, while the potentials difference between the VRDAH pin and the VRDAL pin determines the full scale of the analog output. Normally, connect AVDD to VRADH and VRDAH, and connect 0.1μF ceramic capacitors from them to AVSS. VCOM is used as the common voltage of the analog signal.
To shut out high frequency noise, connect a 0.1μF ceramic capacitor in parallel with an appropriate 10μF electrolytic capacitor between this pin and AVSS. The ceramic capacitor in particular should be connected at a position as close as possible to the pin. Do not lead current from the VCOM pin. To avoid coupling to the AK7714, digital signals and clock signals in particular should be kept away from the VRADH, VRADL, VRDAH, VRDAL and VCOM pins as far as possible.

3) Analog input

Analog input signals are applied to the modulator through the differential input pins of each channel. The input voltage is equal to the differential voltage between AIN+ and AIN- (ΔVAIN = (AIN+) - (AIN-)), and the input range is ±FS = ±(VRADH - VRADL) × 0.4.
When VRADH = 5V and VRADL = 0V, the input range is within ±2.0 V. The output code format is given in terms of 2's complements. Table 1 shows the output code relative to input voltage.

Input voltage	Output code (hexadecimal)
	20 bit
> (+FS - 1.5 LSB)	3FFFF
-0.5 LSB	00000 7FFFF
> (-FS + 0.5 LSB)	80000

Table 1. Output code relative to input voltage

When fs = 48 kHz, the AK7714 samples the analog input at 3.072 MHz. The digital filter eliminates noise from 30 kHz to 3.042 MHz. However, noise is not rejected in the bandwidth close to 3.072 MHz. Most audio signals do not have large noise in the vicinity of 3.072 MHz, so a simple RC filter is sufficient.
A/D converter reference voltage is applied to the VRADH and VRADL pins. Normally, connect AVDD to VRADH, and AVSS to VRADL. To eliminate high frequency noise, connect a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic capacitor between the VRADH pin and VRADL.

The analog source voltage to the AK7714 is +5 V. Voltage of AVDD + 0.3 V or more, voltage of AVSS - 0.3 V or less, and current of 10 mA or more must not be applied to analog input pins (AINL and AINR). Excessive current will damage the internal protection circuit and will cause latch-up, thereby damaging the IC. Accordingly, if the surrounding analog circuit voltage is ±15 V, the analog input pins must be protected from signals with the absolute maximum rating or more.

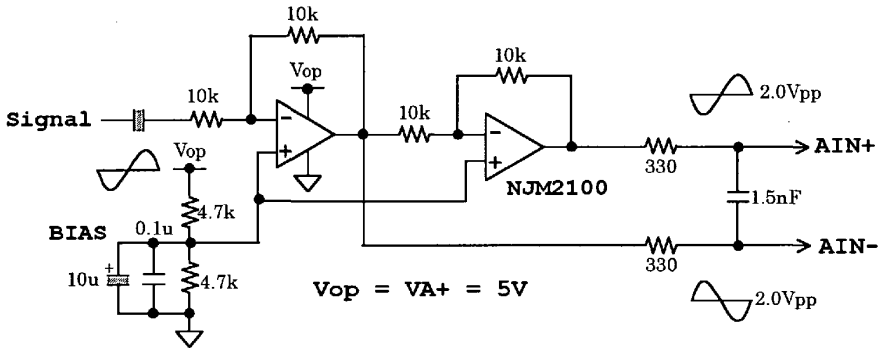


Fig. 1 Example of input buffer circuit (differential input)

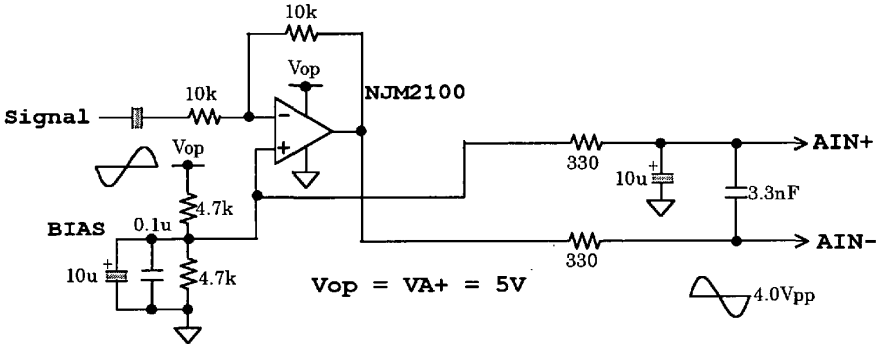


Fig. 2 Example of input buffer circuit (single end input)

An analog signal can be applied to the AK7714 is single end mode. In this case, apply the analog signal (the full scale is 4.0 Vpp when the internal reference voltage is used) to the AIN-input, and bias to the AIN+input. However, use of a low saturated operational amplifier is recommended if the operational amplifier is driven by the 5-volt power supply. The electrolytic capacitor connected to AIN+ is effective for reducing the second harmomics.
(See Fig. 2.)

4) Analog output

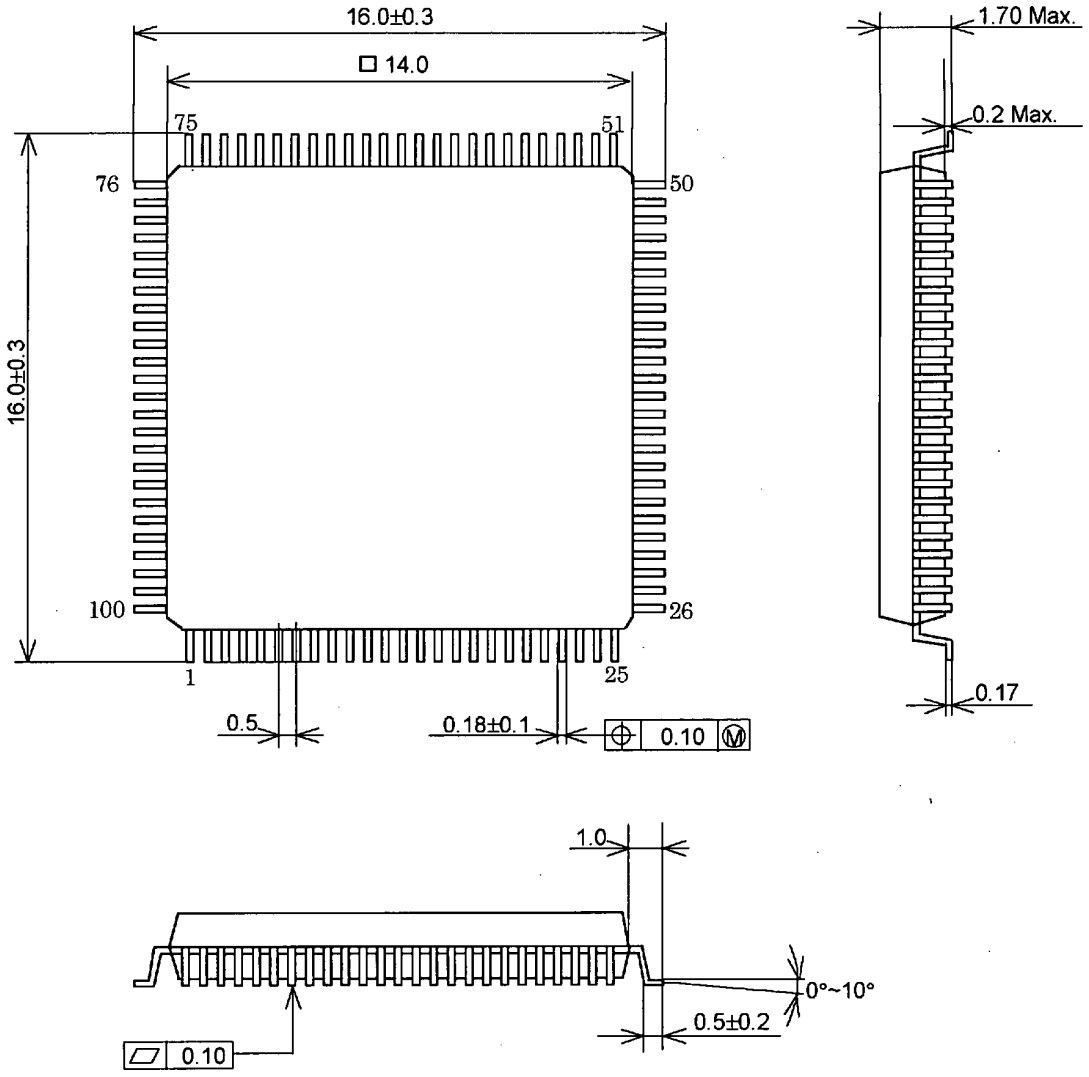
Analog output is single-ended, and the output range is 2.95Vpp (typical) with respect to VCOM voltage. The out-of-band noise (shaping noise) produced by the built-in $\Delta\Sigma$ modulator is reduced by the built-in switched capacitor filter (SCF) and continuous filter (CTF). Therefore, it is not necessary to add an external filter for normal application. The input code format is given in terms of 2's complements with the positive full-scale output for the 3FFFFH(@ 20 bit) input code, and the negative full-scale output for the 80000H (@ 20 bit) input code. VCOM voltage is output as an ideal value for 00000H(@ 20 bit) input code.

5) Connection to digital circuit

To minimize the noise resulting from the digital circuit, connect CMOS logic to the digital output. The applicable logic family includes the 4000B, 74HC, 74AC, 74ACT and 74HCT series.

Package

● 100-pin LQFP (Unit : mm)



● Material & Lead finish

Package:	Epoxy
Lead-frame:	Copper
Lead-finish:	Soldering plate

Marking

Meanings of XXXXAAA
XXXX: Time of manufacture (numeral)
AAA: Lot number (Alphabet)

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