AK4537

16-Bit ΔΣ Stereo CODEC with MIC/HP/SPK-AMP

GENERAL DESCRIPTION

The AK4537 targeted at PDA and other low-power, small size applications. It features a 16-bit stereo CODEC with a built-in Microphone-Amplifier, Headphone-Amplifier and Speaker-Amplifier. Input circuits include a Microphone-Amplifier and an ALC (Auto Level Control) circuit. The AK4537 is available in a 52-QFN, utilizing less board space than competitive offerings.

FEATURES

1. Resolution : 16bits

2. Recording Function
- **Stereo Mic Input**
- **Stereo Line Input**
- **1st MIC Amplifier : +20dB or 0dB**
- **2nd Amplifier with ALC**
  +27.5dB ~ -8dB, 0.5dB Step (MIC input)
  +12dB ~ -23.5dB, 0.5dB Step (LINE input)
- **ADC Performance : S/(N+D) : 79dB, DR, S/N : 83dB (MIC input)**
  S/(N+D) : 88dB, DR, S/N : 91dB (LINE input)

3. Playback Function
- **Digital De-emphasis Filter (tc=50/15μs, fs=32kHz, 44.1kHz, 48kHz)**
- **Digital Volume (0dB ~ -127dB, 0.5dB Step, Mute)**
- **Stereo Headphone-Amp**
  - **S/(N+D) : 70dB, S/N : 90dB**
  - **Output Power : 15mW@16Ω (HVDD=3.3V)**
  - **Click Noise Free at Power ON/OFF**
- **Mono Speaker-Amp with ALC**
  - **S/(N+D) : 64dB@150mW, S/N : 90dB**
  - **BTL Output**
  - **Output Power : 400mW@8Ω (BEEP Input, HVDD=3.3V)**
    300mW@8Ω (MIN Input, ALC2=OFF, HVDD=3.3V)
- **Mono and Stereo Beep Inputs**
- **Mono Line Output**
  - **Differential Output**
  - **Performance : S/(N+D) : 89dB, S/N : 95dB**
- **Stereo Line Output**
  - **Performance : S/(N+D) : 88dB, S/N : 92dB**

4. Power Management

5. Master Clock

(1) PLL Mode
- **Frequencies : 11.2896MHz, 12MHz and 12.288MHz**
- **Input Level : CMOS**

(2) External Clock Mode
- **Frequencies : 2.048MHz ~ 12.288MHz**

6. Output Master Clock Frequencies : 32fs/64fs/128fs/256fs

7. Sampling Rate :

(1) PLL mode
- **8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz**

(2) External Clock mode
- **8kHz ~ 48kHz**

8. Control mode: 4-wire Serial / I2C Bus

9. Master/Slave mode

10. **Audio Interface Format : MSB First, 2's compliment**
    - **ADC : I^2S, 16bit MSB justified**
    - **DAC : I^2S, 16bit MSB justified, 16bit LSB justified**
11. **Ta = -10 ~ 70°C**
12. **Power Supply: 2.4V ~ 3.6V (typ. 3.3V)**
13. **Power Supply Current**
    - **AVDD+DVDD : 19mA**
    - **PVDD : 1.2mA**
    - **HVDD (HP-AMP=ON, SPK-AMP=OFF) : 4mA**
    - **HVDD (HP-AMP=OFF, SPK-AMP=ON) : 7mA**
12. **Package : 52pin QFN (AK4534 pin compatible)**

■ Block Diagram

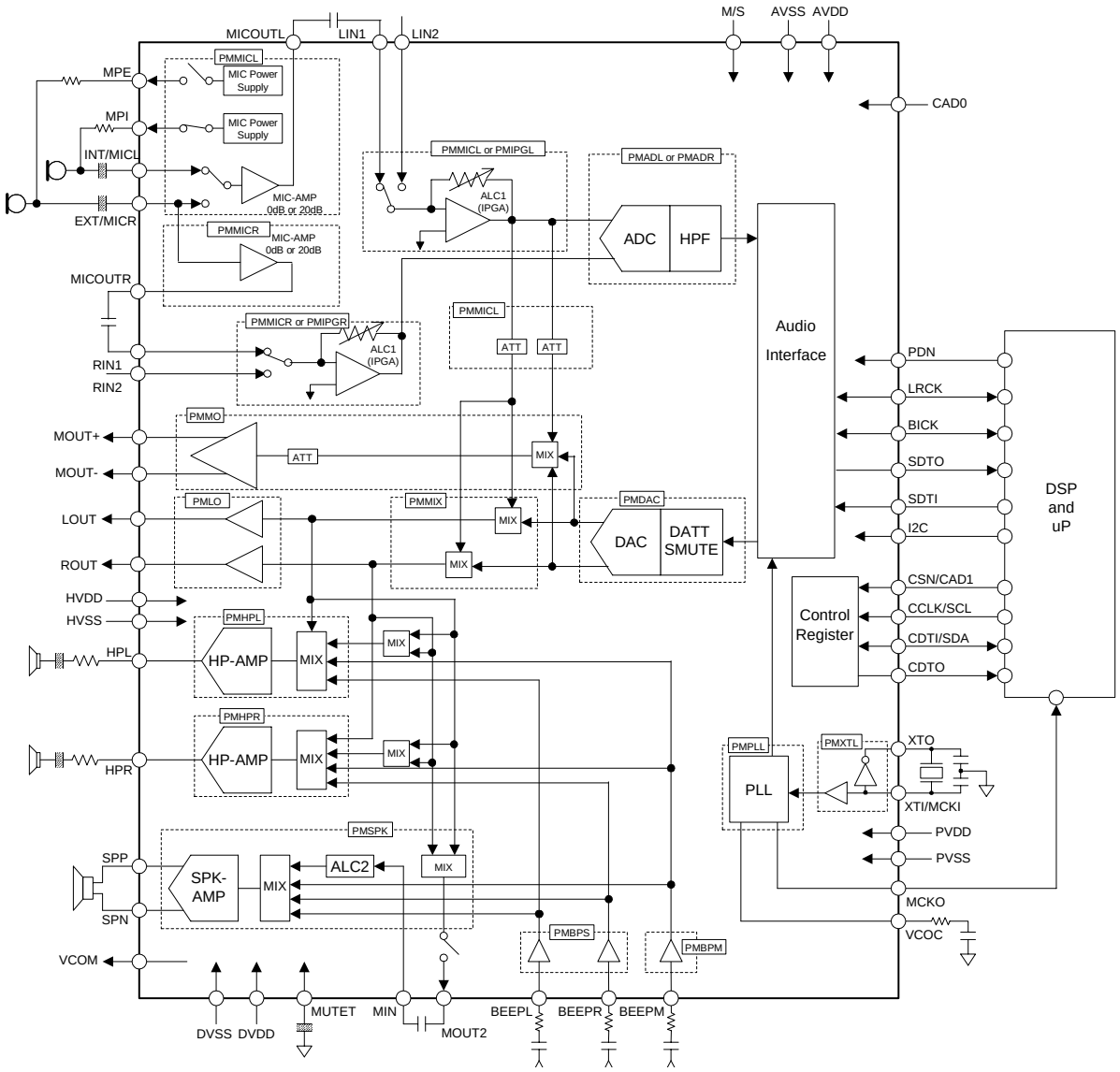
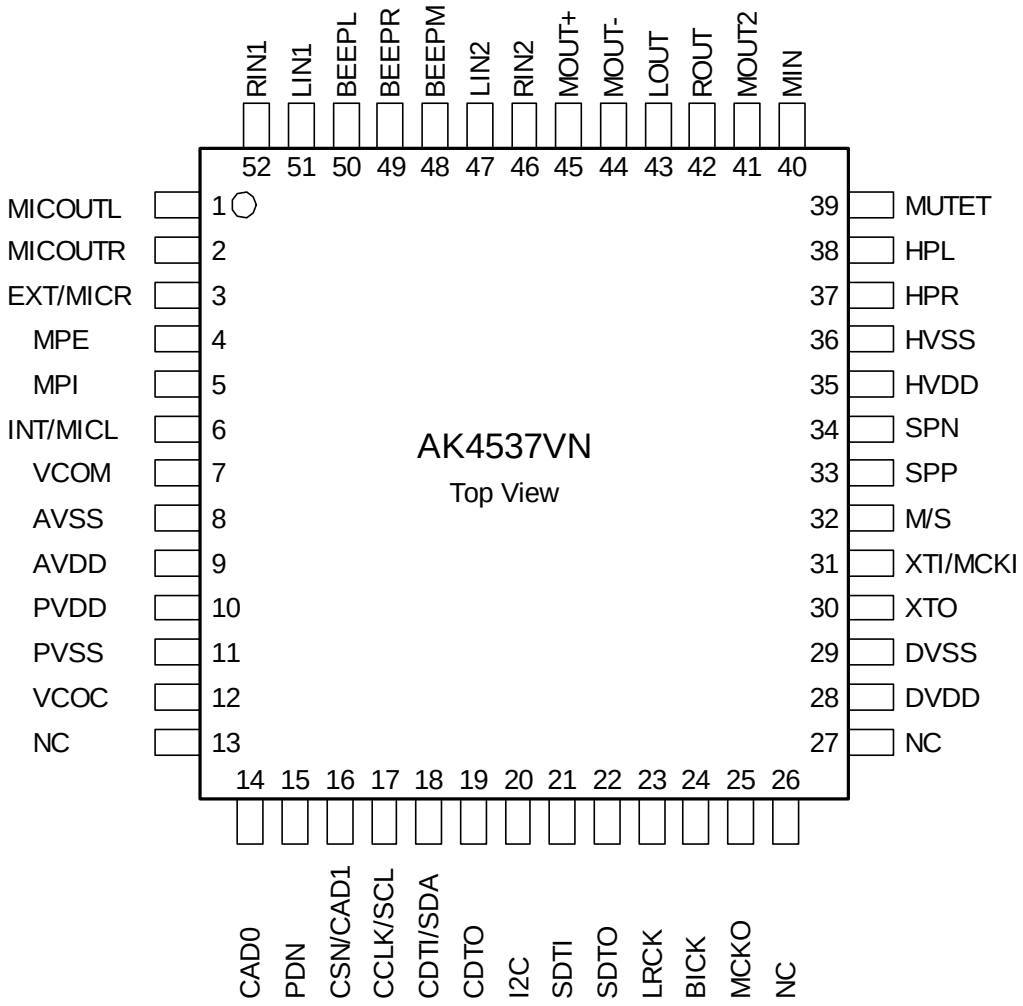


Figure 1. Block Diagram

■ Ordering Guide

AK4537VN	–10 ~ +70°C	52pin QFN (0.4mm pitch)
AKD4537	Evaluation board for AK4537	

■ Pin Layout



■ Comparison with AK4534

1. Function

Function	AK4534	AK4537
Line Input	No	Yes (Stereo)
Mic Input	Mono	Stereo
IPGA	Mono	Stereo
Stereo Line Output	No	Yes
SPK-Amp Gain Select	No	Yes
MOUT Gain Select	No	Yes
Path from IPGA Lch to Analog Output	No	Yes

2. Pin

pin#	AK4534	AK4537
1	MICOUT	MICOUTL
2	TST1	MICOUTR
3	EXT	EXT/MICR
6	INT	INT/MICL
42	TST2	ROUT
43	TST3	LOUT
46	TST4	RIN2
47	TST5	LIN2
51	AIN	LIN1
52	NC	RIN1

3. Register

Addr	Contents
00H	PMIPGL (IPGA Lch Power Control) is added. PMLO (Stereo Line Output Power Control) is added.
01H	SPKG (SPK-Amp Output Power Select) is added.
02H	MOGN (MOUT Gain Select) is added. MICM (IPGA Lch → MOUT) is added
03H	PSLO (Stereo Line Output Power Save Mode Select) is added. MICL (IPGA Lch → LOUT/ROUT, HP-Amp, SPK-Amp) is added.
05H	HPLM, HPRM (HP-Amp Mono Output Select) is deleted. HPM (HP-Amp Mono Output Select) is added.
07H	IPGAC (IPGA Control) is added.
0EH	ATTM (IPGA Lch → MOUT ATT Select) is added. ATTS2-0 (IPGA Lch → LOUT/ROUT, HP-Amp, SPK-Amp ATT Select) is added.
0FH	IPGAR6-0 (Rch IPGA Control) is added.
10H	PMADR (ADC Rch Power Control) is added. PMMICR (MIC-amp Rch Power Control) is added. PMIPGR (IPGA Rch Power Control) is added. INL (IPGA Lch Input Select) is added. INR (IPGA Rch Input Select) is added.

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MICOUTL	O	MIC-Amp Lch Output Pin
2	MICOUTR	O	MIC-Amp Rch Output Pin
3	EXT	I	External Microphone Input Pin (Mono Input) (PMMICR bit = "0")
	MICR	I	Stereo Microphone Rch Input Pin (PMMICR bit = "1")
4	MPE	O	MIC Power Supply Pin for External Microphone / Stereo Microphone Rch
5	MPI	O	MIC Power Supply Pin for Internal Microphone / Stereo Microphone Lch
6	EXT	I	Internal Microphone Input Pin (Mono Input) (PMMICL bit = "0")
	MICR	I	Stereo Microphone Lch Input Pin (PMMICL bit = "1")
7	VCOM	O	Common Voltage Output Pin, 0.45 x AVDD Bias voltage of ADC inputs and DAC outputs.
8	AVSS	-	Analog Ground Pin
9	AVDD	-	Analog Power Supply Pin
10	PVDD	-	PLL Power Supply Pin
11	PVSS	-	PLL Ground Pin
12	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin should be connected to PVSS with one resistor and capacitor in series.
13	NC	-	No Connect. This pin should be left floating.
14	CAD0	I	Chip Address 0 Select Pin
15	PDN	I	Power-Down Mode Pin "H": Power up, "L": Power down reset and initializes the control register.
16	CSN	I	Chip Select Pin (I2C = "L")
	CAD1	I	Chip Address 1 Select Pin (I2C = "H")
17	CCLK	I	Control Data Clock Pin (I2C = "L")
	SCL	I	Control Data Clock Pin (I2C = "H")
18	CDTI	I	Control Data Input Pin (I2C = "L")
	SDA	I/O	Control Data Input Pin (I2C = "H")
19	CDTO	O	Control Data Output Pin (I2C = "L")
20	I2C	I	Control Mode Select Pin "H": I^2C Bus, "L": 4-wire Serial
21	SDTI	I	Audio Serial Data Input Pin
22	SDTO	O	Audio Serial Data Output Pin
23	LRCK	I/O	Input / Output Channel Clock Pin
24	BICK	I/O	Audio Serial Data Clock Pin
25	MCKO	O	Master Clock Output Pin
26	NC	-	No Connect. This pin should be left floating.

No.	Pin Name	I/O	Function
27	NC	-	No Connect. This pin should be left floating.
28	DVDD	-	Digital Power Supply Pin
29	DVSS	-	Digital Ground Pin
30	XTO	O	X'tal Output Pin
31	XTI	I	X'tal Input Pin
	MCKI	I	External Master Clock Input Pin
32	M/S	I	Master / Slave Mode Pin "H" : Master Mode, "L" : Slave Mode
33	SPP	O	Speaker Amp Positive Output Pin
34	SPN	O	Speaker Amp Negative Output Pin
35	HVDD	-	Headphone Amp Power Supply Pin
36	HVSS	-	Headphone Amp Ground Pin
37	HPR	O	Rch Headphone Amp Output Pin
38	HPL	O	Lch Headphone Amp Output Pin
39	MUTET	O	Mute Time Constant Control Pin Connected to HVSS pin with a capacitor for mute time constant.
40	MIN	I	ALC Input Pin
41	MOUT2	O	Analog Mixing Output Pin
42	ROUT	O	Rch Stereo Line Output Pin
43	LOUT	O	Lch Stereo Line Output Pin
44	MOUT–	O	Mono Line Negative Output Pin
45	MOUT+	O	Mono Line Positive Output Pin
46	RIN2	I	Rch Analog Input 2 Pin (LINE Input)
47	LIN2	I	Lch Analog Input 2 Pin (LINE Input)
48	BEEPM	I	Mono Beep Signal Input Pin
49	BEEPR	I	Rch Stereo Beep Signal Input Pin
50	BEEPL	I	Lch Stereo Beep Signal Input Pin
51	LIN1	I	Rch Analog Input 1 Pin (MIC Input)
52	RIN1	I	Lch Analog Input 1 Pin (MIC Input)

Note: All input pins except analog input pins (INT, EXT, LIN1, RIN1, MIN, BEEPM, BEEPL, BEEPR, LIN2 and RIN2) should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS, PVSS, HVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	–0.3	4.6	V
	Digital	DVDD	–0.3	4.6	V
	PLL	PVDD	–0.3	4.6	V
	Headphone-Amp / Speaker-Amp	HVDD	–0.3	4.6	V
	|AVSS – PVSS| (Note 2)	ΔGND1	-	0.3	V
	|AVSS – DVSS| (Note 2)	ΔGND2	-	0.3	V
	|AVSS – HVSS| (Note 2)	ΔGND3	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage		VIND	–0.3	DVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–10	70	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS, DVSS, PVSS and HVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS, PVSS, HVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 3)	Analog	AVDD	2.4	3.3	3.6	V
	Digital	DVDD	2.4	3.3	AVDD	V
	PLL	PVDD	2.4	3.3	AVDD	V
	HP / SPK-Amp	HVDD	2.4	3.3	AVDD	V

Note 1. All voltages with respect to ground.
Note 3. The power up sequence between AVDD, DVDD, HVDD and PVDD is not critical.
It is recommended that DVDD and PVDD are the same voltage as AVDD in order to reduce the current at power down mode.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, PVDD, HVDD=3.3V; AVSS=DVSS=PVSS=HVSS=0V; fs=44.1kHz, BICK=64fs; Signal Frequency=1kHz; 16bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

Parameter			min	typ	max	Units
MIC Amplifier:						
Input Resistance			20	30	40	kΩ
Gain	(MGAIN bit = "0")		-	0	-	dB
	(MGAIN bit = "1")		-	20	-	dB
MIC Power Supply:						
Output Voltage	(Note 4)		2.22	2.47	2.72	V
Output Current			-	-	1.25	mA
Input PGA Characteristics:						
Input Resistance	(LIN1, RIN1 pins)		5	10	15	kΩ
(Note 5)	(LIN2, RIN2 pins)		30	60	90	kΩ
Step Size			0.1	0.5	0.9	dB
Gain Control Range	(LIN1, RIN1 pins)		–8	-	+27.5	dB
	(LIN2, RIN2 pins)		–23.5	-	+12	dB
ADC Analog Input Characteristics: ALC1=OFF						
Resolution					16	Bits
Input Voltage	(Note 6)	(Note 7)	0.168	0.198	0.228	Vpp
		(Note 8)	1.68	1.98	2.28	Vpp
S/(N+D)	(–1dBFS)	(Note 7)	71	79	-	dBFS
		(Note 8)	-	88	-	dBFS
D-Range	(–60dBFS, A-weighted)	(Note 7)	75	83	-	dB
		(Note 8)	-	91	-	dB
S/N	(A-weighted)	(Note 7)	75	83	-	dB
		(Note 8)	-	91	-	dB
Interchannel Isolation		(Note 7)	75	90	-	dB
		(Note 8)	-	100	-	dB
Interchannel Gain Mismatch		(Note 7)	-	0.1	0.5	dB
		(Note 8)	-	0.1	0.5	dB
DAC Characteristics:						
Resolution			-	-	16	Bits
Stereo Line Output Characteristics: R_L=10kΩ, DAC → LOUT, ROUT						
Output Voltage	(Note 9)		1.74	1.94	2.14	Vpp
S/(N+D)	(-3dBFS)		78	88	-	dBFS
S/N	(A-weighted)		85	92	-	dB
Interchannel Isolation			-	100	-	dB
Interchannel Gain Mismatch			-	0.1	0.5	dB
Load Resistance			10	-	-	kΩ
Load Capacitance			-	-	30	pF

Note 4. Output voltage is proportional to AVDD voltage. Vout = 0.75 x AVDD.
Note 5. When IPGA Gain is changed, this typical value changes between 8kΩ and 11kΩ (LIN1, RIN1), 48kΩ and 66kΩ (LIN2, RIN2).
Note 6. Input voltage is proportional to AVDD voltage. Vin = 0.06 x AVDD)@Mic In, Vin = 0.6 x AVDD(typ)@Line In.
Note 7. MIC Gain=20dB, IPGA=0dB, ALC1=OFF, INT(MICL)/EXT(MICR) → IPGA → ADC
Note 8. IPGA=0dB, ALC1=OFF, LIN2/RIN2 → IPGA → ADC
Note 9. Output voltage is proportional to AVDD voltage. Vout = 0.588 x AVDD.

Parameter			min	typ	max	Units
Mono Line Output Characteristics: R_L=20kΩ, DAC → MOUT+/MOUT-						
Output Voltage (Note 10)		MOGN=1, -17dB	-	0.31	-	Vpp
		MOGN=0, +6dB	3.56	3.96	4.36	Vpp
S/(N+D) (-3dBFS)		MOGN=1, -17dB	-	76	-	dBFS
		MOGN=0, +6dB	79	89	-	dBFS
S/N (A-weighted)		MOGN=1, -17dB	-	79	-	dB
		MOGN=0, +6dB	85	95	-	dB
Load Resistance		MOGN=1, -17dB	2	-	-	kΩ
		MOGN=0, +6dB	20	-	-	kΩ
Load Capacitance			-	-	30	pF
Headphone-Amp Characteristics: R_L=22.8Ω, DAC → HPL/HPR, DATT=0dB						
Output Voltage (Note 11)			1.54	1.92	2.30	Vpp
S/(N+D) (–3dBFS)			60	70	-	dBFS
S/N (A-weighted)			80	90	-	dB
Interchannel Isolation			70	85	-	dB
Interchannel Gain Mismatch			-	0.1	0.5	dB
Load Resistance			20	-	-	Ω
Load Capacitance	(C1 in Figure 2)		-	-	30	pF
	(C2 in Figure 2)		-	-	300	pF
Speaker-Amp Characteristics: R_L=8Ω, BTL, DAC → MOUT2 → MIN → SPP/SPN, ALC2=OFF						
Output Voltage (Note 12)	SPKG= "0" (Po=150mW)		2.47	3.09	3.71	Vpp
	SPKG= "1" (Po=300mW)		-	4.38	-	Vpp
S/(N+D)	SPKG= "0" (Po=150mW)		50	64	-	dB
	SPKG= "1" (Po=300mW)		-	20	-	dB
	(Po=250mW)		-	60	-	dB
S/N (A-weighted)			82	90	-	dB
Load Resistance			8	-	-	Ω
Load Capacitance			-	-	30	pF

Note 10. Output voltage is proportional to AVDD voltage. Vout = 1.2 x AVDD at Full-differential output.
Vout = 0.6 x AVDD at Single-end Output.
Note 11. Output voltage is proportional to AVDD voltage. Vout = 0.582 x AVDD.
Note 12. Output voltage is proportional to AVDD voltage.
Vout = 0.936 x AVDD(typ)@SPKG= "0", 1.327 x AVDD(typ)@SPKG= "1" at Full-differential output.

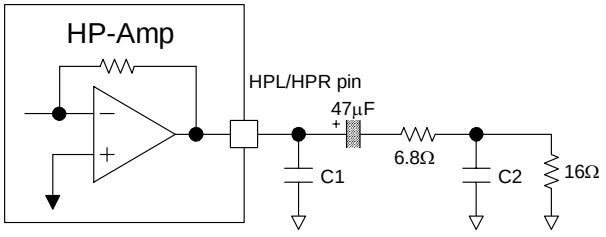


Figure 2. Headphone-amp output circuit

Parameter	min	typ	max	Units
BEEP Input: BEEPL, BEEPR, BEEPM pin				
Maximum Input Voltage (Note 13)	-	-	1.98	Vpp
Feedback Resistance	14	20	26	kΩ
Mono Input: MIN pin				
Maximum Input Voltage (Note 14)	-	-	1.98	Vpp
Input Resistance (Note 15)	12	24	36	kΩ
Mono Output: R_L=10kΩ, DAC → MIX → MOUT2				
Output Voltage (Note 16)	-	1.94	-	Vpp
Load Resistance	10	-	-	kΩ
Load Capacitance (Note 17)	-	-	30	pF
Power Supplies				
Power Up (PDN = "H")				
All Circuit Power-up:				
AVDD+DVDD (Note 18)	-	19	29	mA
PVDD	-	1.2	2	mA
HVDD: HP-AMP Normal Operation No Output (Note 19)	-	4	6	mA
HVDD: SPK-AMP Normal Operation No Output (Note 20)	-	7	18	mA
Power Down (PDN = "L") (Note 21)				
AVDD+DVDD	-	10	100	μA
PVDD	-	10	100	μA
HVDD	-	10	100	μA

Note 13. BEEP-AMP can't output more than this maximum voltage.
Note 14. Maximum Input Voltage is proportional to AVDD voltage. Vin = 0.6 x AVDD.
Note 15. When ALC2 Gain is changed, this typical value changes between 22kΩ and 26kΩ.
Note 16. Output Voltage is proportional to AVDD voltage. Vout = 0.588 x AVDD.
Note 17. When the output pin drives a capacitive load, a resistor should be added in series between the output pin and capacitive load.
Note 18. PMMICL=PMMICR=PMADL=PMADR=PMDAC=PMMO=PMLO=PMSPK=PMHPL=PMHPR=PMVCM=PMPLL=PMXTL=PMBPM=PMBPS= "1", MCKO= "1" and Master Mode. AVDD=13mA (typ.), DVDD=6mA (typ.).
AVDD=10mA(typ.), DVDD=6mA (typ.) at PMMICL=PMADL=PMDAC=PMMO=PMLO=PMSPK=PMHPL=PMHPR=PMVCM=PMPLL=PMXTL=PMBPM=PMBPS= "1", PMMICR=PMADR=PMIPGR= "0", MCKO= "1" and Master Mode.
AVDD=10mA (typ.), DVDD=4mA (typ.) at MCKO= "0" in Slave Mode.
Note 19. PMMICL=PMMICR=PMADL=PMADR=PMDAC=PMMO=PMLO=PMHPL=PMHPR=PMVCM=PMPLL=PMXTL=PMBPM=PMBPS= "1" and PMSPK= "0".
Note 20. PMMICL=PMMICR=PMADL=PMADR=PMDAC=PMMO=PMLO=PMSPK=PMVCM=PMPLL=PMXTL=PMBPM=PMBPS= "1" and PMHPL=PMHPR= "0".
Note 21. All digital input pins are fixed to DVDD or DVSS.

FILTER CHARACTERISTICS

(Ta=−10 ~ 70°C; AVDD, DVDD, PVDD, HVDD=2.4 ~ 3.6V; fs=44.1kHz; DEM=OFF)

Parameter			Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):							
Passband (Note 22)		±0.1dB	PB	0	-	17.4	kHz
		−1.0dB		-	20.0	-	kHz
		−3.0dB		-	21.1	-	kHz
Stopband			SB	27.0	-	-	kHz
Passband Ripple			PR	-	-	±0.1	dB
Stopband Attenuation			SA	65	-	-	dB
Group Delay (Note 23)			GD	-	17.0	-	1/fs
Group Delay Distortion			ΔGD	-	0	-	μs
ADC Digital Filter (HPF):							
Frequency Response (Note 22)		−3.0dB	FR	-	3.4	-	Hz
		−0.5dB		-	10	-	Hz
		−0.1dB		-	22	-	Hz
DAC Digital Filter:							
Passband (Note 22)		±0.1dB	PB	0	-	20.0	kHz
		−6.0dB		-	22.05	-	kHz
Stopband			SB	24.1	-	-	kHz
Passband Ripple			PR	-	-	±0.06	dB
Stopband Attenuation			SA	43	-	-	dB
Group Delay (Note 23)			GD	-	16.8	-	1/fs
DAC Digital Filter + SCF:							
Frequency Response: 0 ~ 20.0kHz			FR	-	±0.5	-	dB
BOOST Filter: (Note 24)							
Frequency Response	MIN	20Hz	FR	-	5.74	-	dB
		100Hz		-	2.92	-	dB
		1kHz		-	0.0	-	dB
	MID	20Hz	FR	-	5.94	-	dB
		100Hz		-	4.71	-	dB
		1kHz		-	0.14	-	dB
	MAX	20Hz	FR	-	16.04	-	dB
		100Hz		-	10.55	-	dB
		1kHz		-	0.3	-	dB

Note 22. The passband and stopband frequencies scale with fs (system sampling rate).
For example, ADC is PB=0.454*fs (@-1.0dB), DAC is PB=0.454*fs (@-0.01dB).

Note 23. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16-bit data of both channels from the input register to the output register of the ADC. This time includes the group delay of the HPF. For the DAC, this time is from setting the 16-bit data of both channels from the input register to the output of analog signal.

Note 24. These frequency responses scale with fs. If a high-level and low frequency signal is input, the analog output clips to the full-scale.

DC CHARACTERISTICS

(Ta=–10 ~ 70°C; AVDD, DVDD, PVDD, HVDD=2.4 ~ 3.6V)

Parameter	Symbol	min	typ	Max	Units
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
Input Voltage at AC Coupling (Note 25)	VAC	50%DVDD	-	-	V
High-Level Output Voltage (Iout=–200μA)	VOH	DVDD–0.2	-	-	V
Low-Level Output Voltage					
(Except SDA pin: Iout=200μA)	VOL	-	-	0.2	V
(SDA pin: Iout=3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA

Note 25. When AC coupled capacitor is connected to MCKI pin.

SWITCHING CHARACTERISTICS

(Ta=–10 ~ 70°C; AVDD, DVDD, PVDD, HVDD=2.4 ~ 3.6V; C_L=20pF)

Parameter			Symbol	min	typ	max	Units
Master Clock Timing							
Crystal Resonator		Frequency		11.2896	-	12.288	MHz
External Clock		Frequency	fCLK	2.048	-	12.288	MHz
		Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
		Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
		AC Pulse Width (Note 26)	tACW	0.4/fCLK	-	-	ns
MCKO Output							
Frequency			fMCK	0.256	-	12.288	MHz
Duty Cycle:	except fs=32kHz		dMCK	40	50	60	%
	fs=32kHz at 256fs (Note 27)		dMCK	-	33	-	%
LRCK Timing							
Frequency			fs	8	-	48	kHz
Duty Cycle		Slave mode	Duty	45	-	55	%
		Master mode	Duty	-	50	-	%
Audio Interface Timing							
Slave mode							
BICK Period			tBCK	312.5	-	-	ns
BICK Pulse Width Low			tBCKL	130	-	-	ns
Pulse Width High			tBCKH	130	-	-	ns
LRCK Edge to BICK "↑"		(Note 28)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge		(Note 28)	tBLR	50	-	-	ns
LRCK to SDTO (MSB) (Except I^2S mode)			tLRS	-	-	80	ns
BICK "↓" to SDTO			tBSD	-	-	80	ns
SDTI Hold Time			tSDH	50	-	-	ns
SDTI Setup Time			tSDS	50	-	-	ns
Master mode							
BICK Frequency		(BF bit = "0")	fBCK	-	64fs	-	Hz
		(BF bit = "1")	fBCK	-	32fs	-	Hz
BICK Duty			dBCK	-	50	-	%
BICK "↓" to LRCK			tMBLR	–80	-	80	ns
BICK "↓" to SDTO			tBSD	–80	-	80	ns
SDTI Hold Time			tSDH	50	-	-	ns
SDTI Setup Time			tSDS	50	-	-	ns

Note 26. Pulse width to ground level when MCKI is connected to a capacitor in series and a resistor is connected to ground (Refer to Figure 4).

Note 27. PMPLL bit = "1".

Note 28. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (4-wire Serial mode):					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN "↓" to CCLK "↑"	tCSS	50	-	-	ns
CCLK "↑" to CSN "↑"	tCSH	50	-	-	ns
CDTO Delay	tDCD	-	-	50	ns
CSN "↑" to CDTO Hi-Z	tCCZ	-	-	70	ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-	-	100	kHz
Bus Free Time Between Transmissions	tBUF	4.7	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	4.0	-	-	µs
Clock Low Time	tLOW	4.7	-	-	µs
Clock High Time	tHIGH	4.0	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	4.7	-	-	µs
SDA Hold Time from SCL Falling (Note 29)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.25	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	4.0	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Reset Timing					
PDN Pulse Width (Note 30)	tPD	150	-	-	ns
PMADL or PMADR "↑" to SDTO valid (Note 31)	tPDV	-	2081	-	1/fs

Note 29. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 30. The AK4537 can be reset by the PDN pin = "L".
Note 31. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1".

■ Timing Diagram

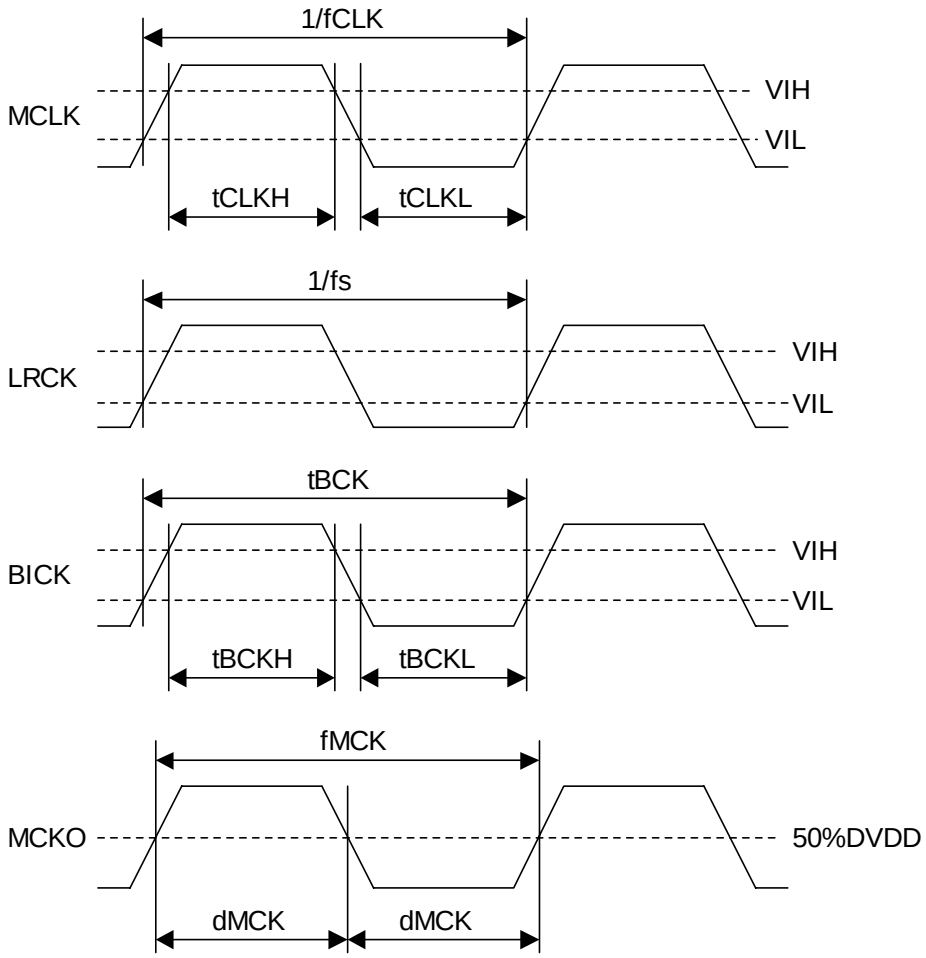


Figure 3. Clock Timing

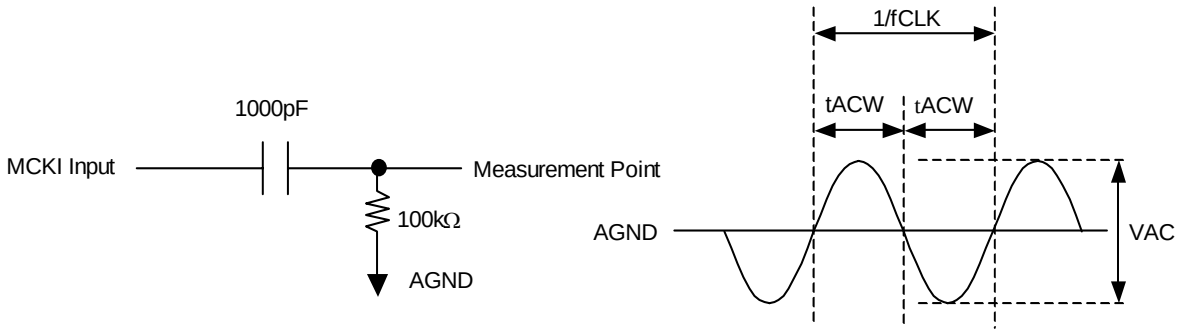


Figure 4. MCKI AC Coupling Timing

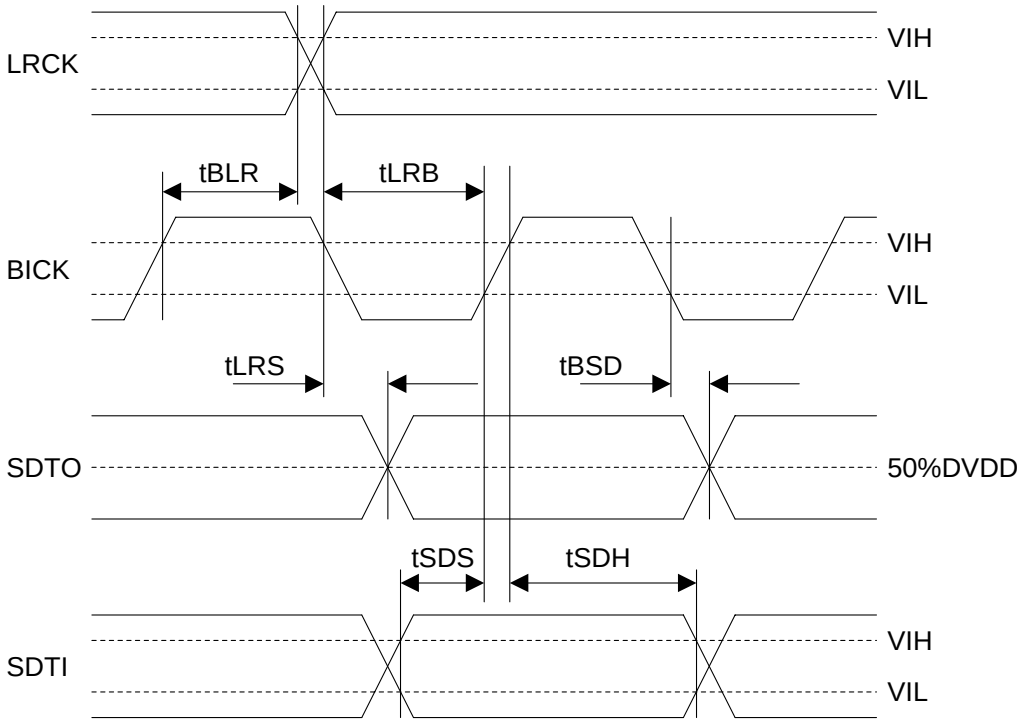


Figure 5. Audio Interface Timing (Slave mode)

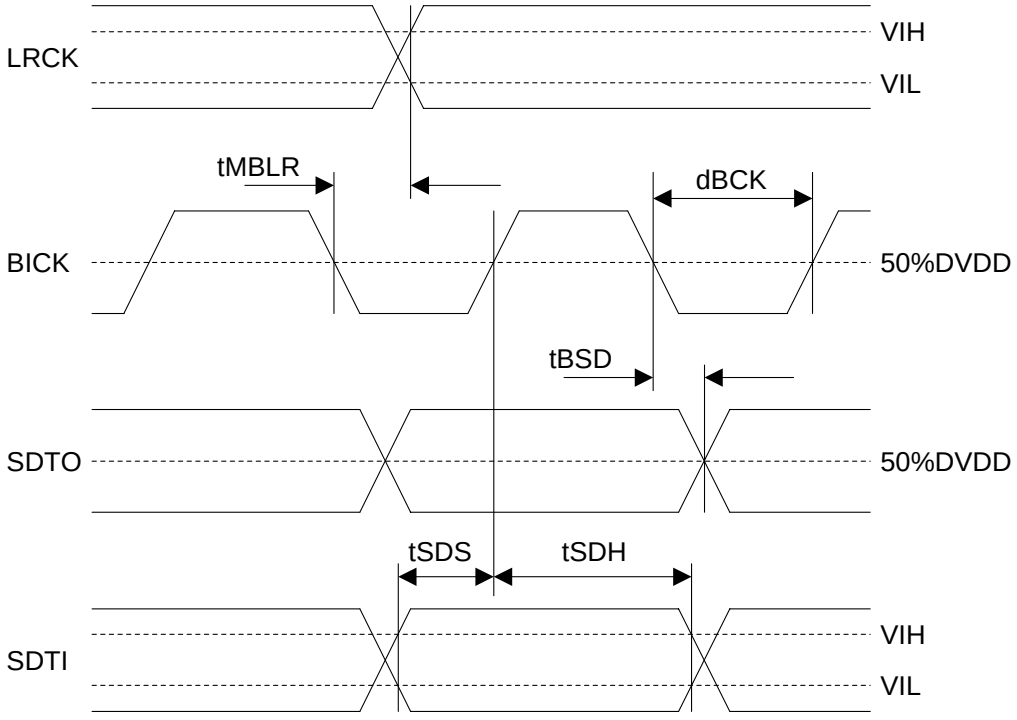


Figure 6. Audio Interface Timing (Master mode)

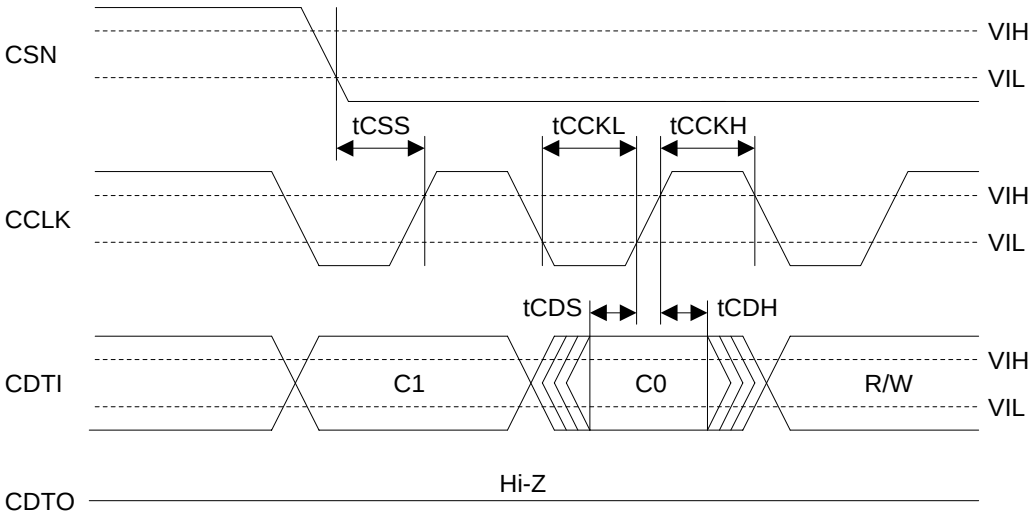


Figure 7. WRITE/READ Command Input Timing

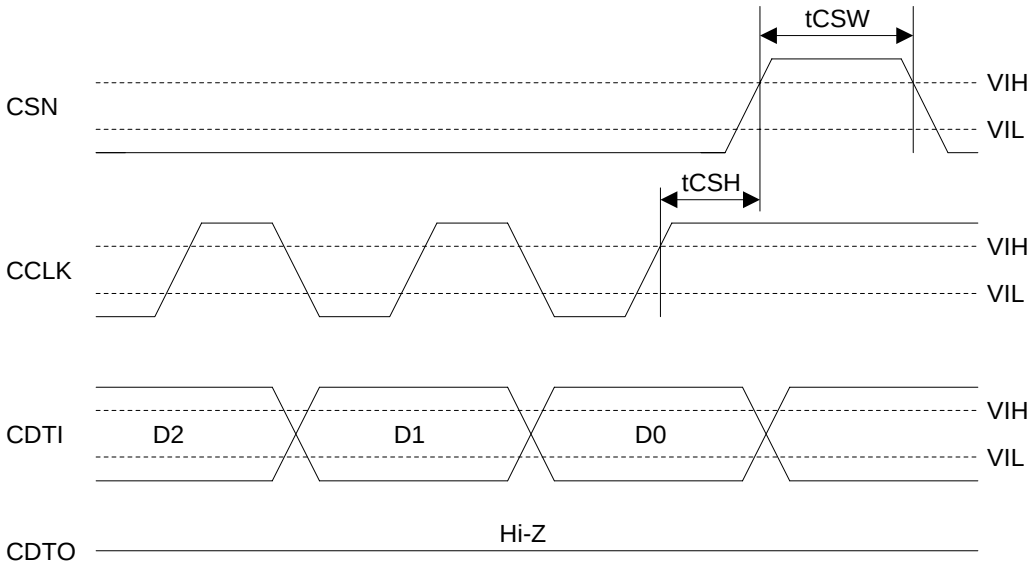


Figure 8. WRITE Data Input Timing

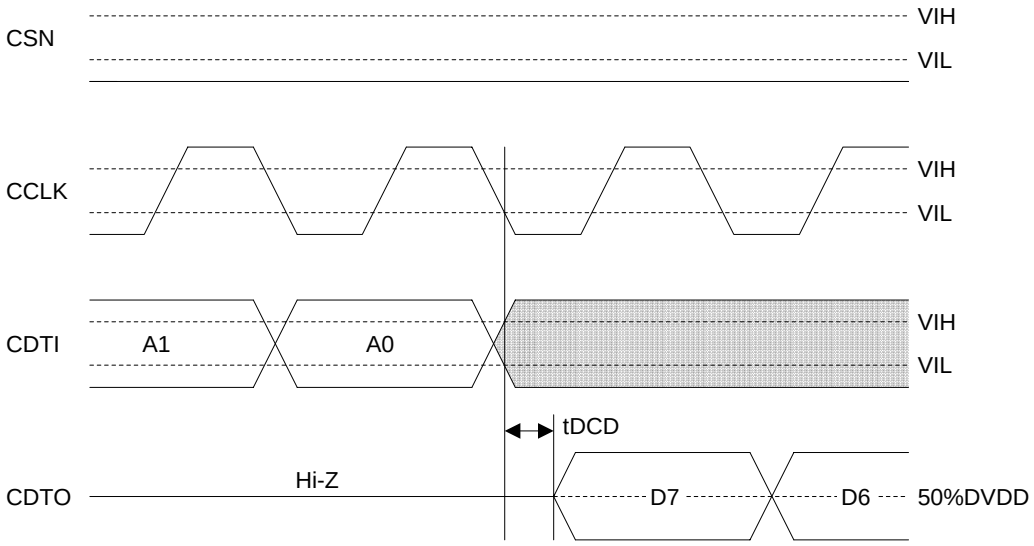


Figure 9. READ Data Output Timing 1

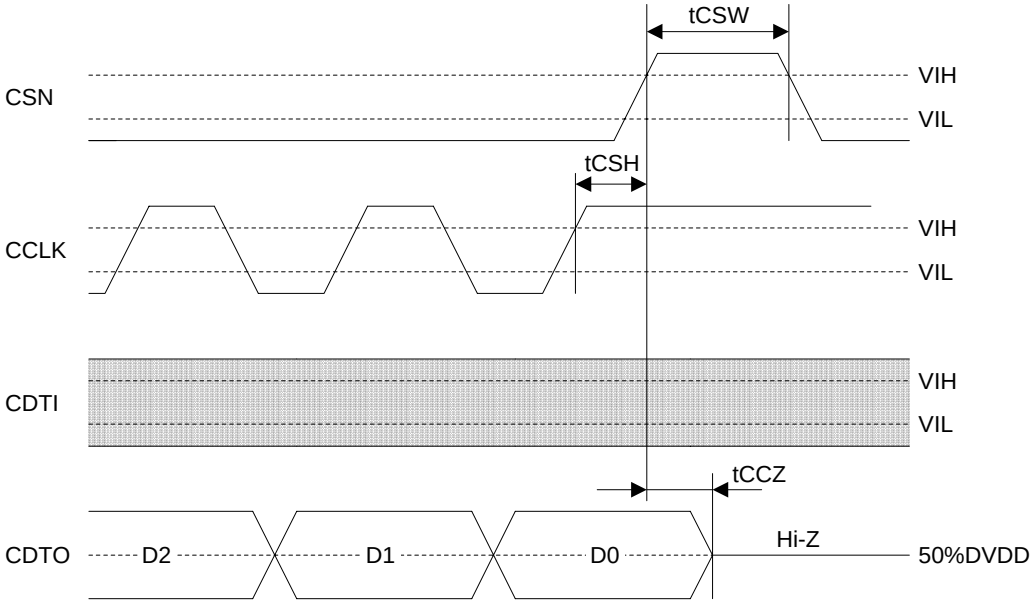


Figure 10. READ Data Output Timing 2

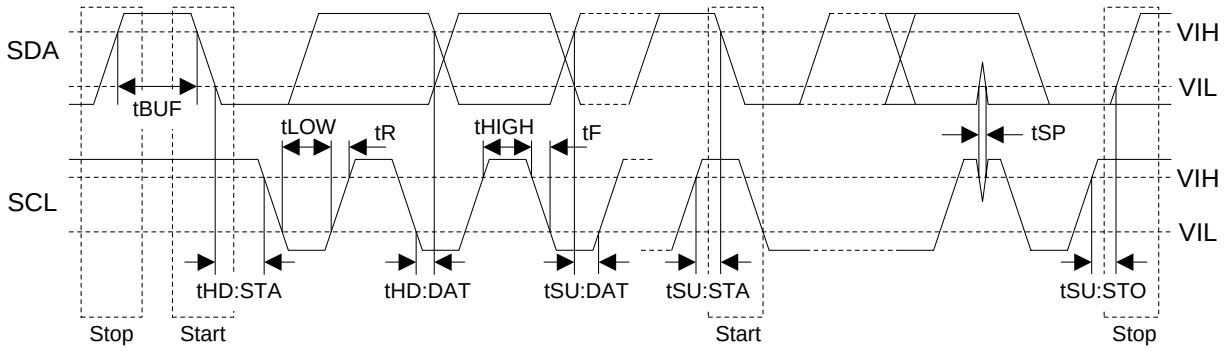


Figure 11. I^{2}C Bus Mode Timing

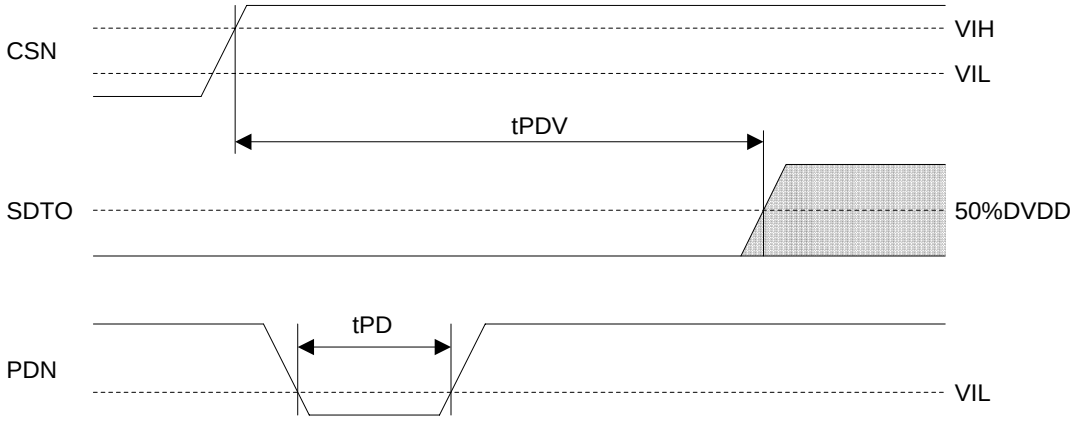


Figure 12. Power Down & Reset Timing

OPERATION OVERVIEW

■ Master Clock Source

The AK4537 requires a master clock (MCLK). This master clock is input to the AK4537 by connecting a X'tal oscillator to XTI and XTO pins or by inputting an external CMOS-level clock to the XTI pin or by inputting an external clock that is greater than 50% of the DVDD level to the XTI pin through a capacitor.

When using a X'tal oscillator, there should be capacitors between XTI/XTO pins and DVSS. When using an external clock, there are two choices: direct, where an external clock is input directly to the XTI pin and indirect, where the external clock is input through a capacitor.

Master Clock		Status	PMXTL bit	MCKPD bit
X'tal Oscillator	(Figure 13)	Oscillator ON	1	0
		Oscillator OFF	0	1
External Clock Direct Input	(Figure 14)	Clock is input to MCKI pin.	0	0
		MCKI pin is fixed to "L".	0	0/1
		MCKI pin is fixed to "H".	0	0
		MCKI pin is Hi-Z	0	1
AC Coupling Input	(Figure 15)	Clock is input to MCKI pin.	1	0
		Clock isn't input to MCKI pin.	0	1

Table 1. Master Clock Status by PMXTL bit and MCKPD bit

(1) X'tal Oscillator

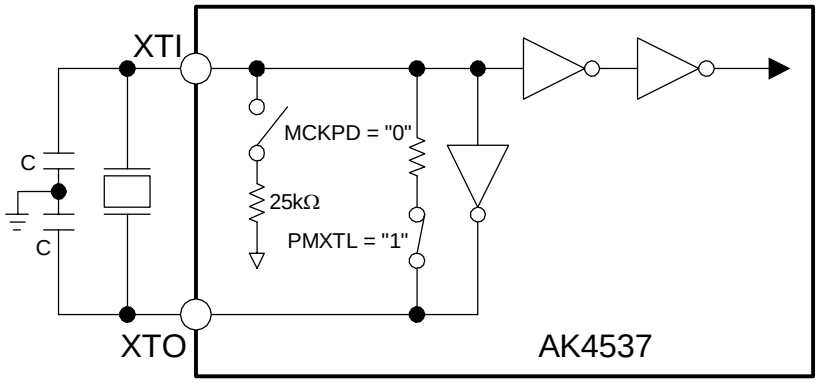


Figure 13. X'tal mode
Note: The capacitor values depend on the X'tal oscillator used. (C : typ. 10 ~ 30pF)

(2) External Clock Direct Input

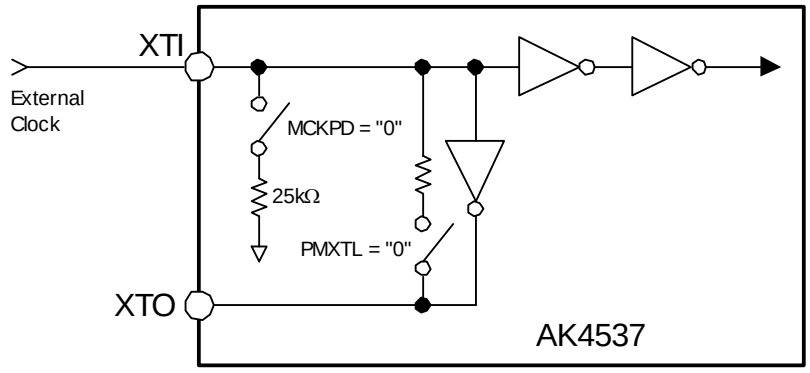


Figure 14. External Clock mode (Input : CMOS Level)
Note: This clock level must not exceed DVDD level.

(3) AC Coupling Input

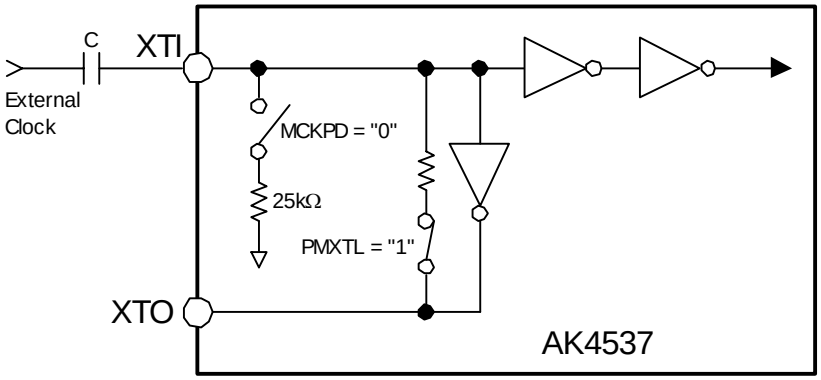


Figure 15. External Clock mode (Input : ≥ 50%DVDD)
Note: This clock level must not exceed DVDD level. (C : 0.1μF)

■ System Clock

(1) PLL Mode (PMPLL bit = "1")

A fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL1-0 and FS2-0 bits (see Table.2 and Table.3). The frequency of the MCKO output is selectable via the PS1-0 bits registers as defined in Table.4 and the MCKO output enable is controlled by the MCKO bit. **If PS1-0 bits are changed before LRCK is input, MCKO is not output. PS1-0 bits should be changed after LRCK is input in slave mode.**

The PLL should be powered-up after the X'tal oscillator becomes stable or external master clock is inputted. It takes X'tal oscillator 20ms(typ) to be stable after PMXTL bit="1". The PLL needs 40ms lock time, whenever the sampling frequency changes or the PLL is powered-up (PMPLL bit="0" → "1").

LRCK and BICK are output from the AK4537 in master mode. When the clock input to MCKI pin stops during normal operation (PMPLL bit = "1"), the internal PLL continues to oscillate (a few MHz), and LRCK and BICK outputs go to "L" (Table 5).

In slave mode, the LRCK input should be synchronized with MCKO. The master clock (MCKI) should be synchronized with sampling clock (LRCK). The phase between these clocks does not matter. LRCK and BICK must be present whenever the AK4537 is operating (PMADL bit = "1", PMADR bit = "1" or PMDAC bit = "1"). If these clocks are not provided, the AK4537 may draw excess current due to its use of internal dynamically refreshed logic. If the external clocks are not present, place the AK4537 in power-down mode (PMADL bit = PMADR bit = PMDAC bit = "0").

Mode	PLL1	PLL0	MCKI	
0	0	0	12.288MHz	Default
1	0	1	11.2896MHz	
2	1	0	12MHz	
3	1	1	N/A	

Table 2. MCKI Input Frequency (PLL Mode)

FS2	FS1	FS0	Sampling Frequency	
0	0	0	44.1kHz	Default
0	0	1	22.05kHz	
0	1	0	11.025kHz	
0	1	1	48kHz	
1	0	0	32kHz	
1	0	1	24kHz	
1	1	0	16kHz	
1	1	1	8kHz	

Table 3. Sampling Frequency (PLL Mode)

Mode	PS1	PS0	MCKO	
0	0	0	256fs	Default
1	0	1	128fs	
2	1	0	64fs	
3	1	1	32fs	

Table 4. MCKO Frequency (PLL Mode, MCKO bit = "1")

	Master Mode (M/S pin = "H")		
	Power up	Power down	PLL Unlock
MCKI pin	Frequency set by PLL1-0 bits (Refer to Table 2)	Refer to Table 1	Frequency set by PLL1-0 bits (Refer to Table 2)
MCKO pin	MCKO bit = "0" : "L" MCKO bit = "1" : Output	"L"	MCKO bit = "0" : "L" MCKO bit = "1" : Unsettling
BICK pin	BF bit = "0" : 64fs Output BF bit = "1" : 32fs Output	"L"	"L"
LRCK pin	Output	"L"	"L"

Table 5. Clock Operation at Master Mode (PLL Mode)

	Slave Mode (M/S pin = "L")		
	Power up	Power down	PLL Unlock
MCKI pin	Frequency set by PLL1-0 bits (Refer to Table 2)	Refer to Table 1	Frequency set by PLL1-0 bits (Refer to Table 2)
MCKO pin	MCKO bit = "0" : "L" MCKO bit = "1" : Output	"L"	MCKO bit = "0" : "L" MCKO bit = "1" : Unsettling
BICK pin	Input	Fixed to "L" or "H" externally	Input
LRCK pin	Input	Fixed to "L" or "H" externally	Input

Table 6. Clock Operation at Slave Mode (PLL Mode)

(2) External mode (PMPLL bit = "0")

When the PMPLL bit = "0", the AK4537 works in external clock mode. The MCKO pin outputs a buffered clock of MCKI input.

For example, when MCKI = 256fs, the sampling frequency is changeable from 8kHz to 48kHz (Table 7). The MCKO bit controls MCKO output enable. The frequency of MCKO is selectable via register the PS1-0 bits as defined in Table 8. **If PS1-0 bits are changed before LRCK is input, MCKO is not output. PS1-0 bits should be changed after LRCK is input in slave mode.** The master clock frequency should be changed only when the PMADL, PMADR and PMDAC bits = "0".

LRCK and BICK are output from the AK4537 in master mode. The clock to the MCKI pin must not stop during normal operation (PMADL bit = "1", PMADR bit = "1" or PMDAC bit = "1"). If this clock is not provided, the AK4537 may draw excess current due to its use of internal dynamically refreshed logic. If the external clocks are not present, place the AK4537 in power-down mode (PMADL bit = PMADR bit = PMDAC bit = "0").

MCKI, BICK and LRCK clocks are required in slave mode. The master clock (MCKI) should be synchronized with sampling clock (LRCK). The phase between these clocks does not matter. LRCK and BICK should always be present whenever the AK4537 is in normal operation (PMADL bit = "1", PMADR bit = "1" or PMDAC bit = "1"). If these clocks are not provided, the AK4537 may draw excess current due to its use of internal dynamically refreshed logic. If the external clocks are not present, place the AK4537 in power-down mode (PMADL bit = PMADR bit = PMDAC bit = "0").

Mode	FS1	FS0	Sampling Frequency (fs)	MCKI	
0	0	0	8kHz ~ 48kHz	256fs	Default
1	0	1	8kHz ~ 24kHz	512fs	
2	1	0	8kHz ~ 12kHz	1024fs	
3	1	1	N/A	N/A	

Table 7. Sampling Frequency Select (EXT Mode)

Mode	PS1	PS0	MCKO	
0	0	0	256fs	Default
1	0	1	128fs	
2	1	0	64fs	
3	1	1	32fs	

Table 8. MCKO Frequency (EXT Mode, MCKO bit = "1")

	Master Mode (M/S pin = "H")	
	Power up	Power down
MCKO pin	MCKO bit = "0" : "L" MCKO bit = "1" : Output	"L"
BICK pin	BF bit = "0" : 64fs Output BF bit = "1" : 32fs Output	"L"
LRCK pin	Output	"L"

Table 9. Clock Operation at Master Mode (EXT Mode)

	Slave Mode (M/S pin = "L")	
	Power up	Power down
MCKO pin	MCKO bit = "0" : "L" MCKO bit = "1" : Output	"L"
BICK pin	Input	Fixed to "L" or "H" externally
LRCK pin	Input	Fixed to "L" or "H" externally

Table 10. Clock Operation at Slave Mode (EXT Mode)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. When the out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through Headphone amp at fs=8kHz is shown in Table 11.

MCLK	S/N (fs=8kHz, A-weighted)
256fs	84dB
512fs	88dB
1024fs	88dB

Table 11. Relationship between MCLK and S/N of HP-AMP

■ Master Mode/Slave Mode

The M/S pin selects either master or slave modes. M/S pin = "H" selects master mode and "L" selects slave mode. The AK4537 outputs MCKO, BICK and LRCK in master mode. The AK4537 outputs only MCKO in slave mode, while BICK and LRCK must be input separately.

Mode	MCKO	BICK / LRCK
Slave Mode	MCKO = Output	BICK = Input LRCK = Input
Master Mode	MCKO = Output	BICK = Output LRCK = Output

Table 12. Master mode/Slave mode

■ System Reset

Upon power-up, reset the AK4537 by bringing the PDN pin = "L". This ensures that all internal registers reset to their initial values.

The ADC enters an initialization cycle that starts when the PMADL or PMADR bit is changed from "0" to "1". The initialization cycle time is 2081/fs, or 47.2ms@fs=44.1kHz. During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2's compliment, "0". The ADC output reflects the analog input signal after the initialization cycle is complete. The DAC does not require an initialization cycle.

■ Audio Interface Format

Three types of data formats are available and are selected by setting the DIF1-0 bits (Table 13). In all modes, the serial data is MSB first, 2's complement format. The SDTO is clocked out on the falling edge of BICK and the SDTI is latched on the rising edge. All data formats can be used in both master and slave modes. LRCK and BICK are output from AK4537 in master mode, but must be input to AK4537 in slave mode. If 16-bit data that ADC outputs is converted to 8-bit data by removing LSB 8-bit, –1 at 16bit data is converted to –1 at 8-bit data. And when the DAC playbacks this 8-bit data, –1 at 8-bit data will be converted to –256 at 16-bit data and this is a large offset. This offset can be removed by adding the offset of 128 to 16-bit data before converting to 8-bit data. When ADC is used as monaural, the output data of powered-down channel is "0".

When LOOP bit = "1", audio interface format of SDTO is fixed to I^2S regardless of DIF1-0 bits setting.

Mode	DIF1	DIF0	SDTO (ADC)	SDTI (DAC)	BICK	Figure	
0	0	0	MSB justified	LSB justified	≥ 32fs	Figure 16	
1	0	1	MSB justified	MSB justified	≥ 32fs	Figure 17	
2	1	0	I^2S	I^2S	≥ 32fs	Figure 18	Default
3	1	1	N/A	N/A	N/A	-	

Table 13. Audio Interface Format

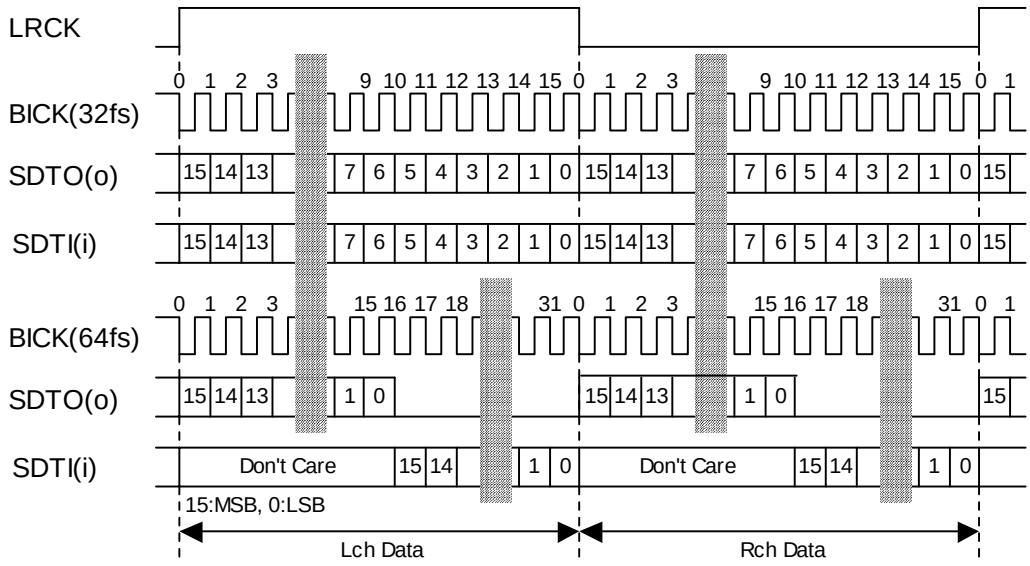


Figure 16. Mode 0 Timing

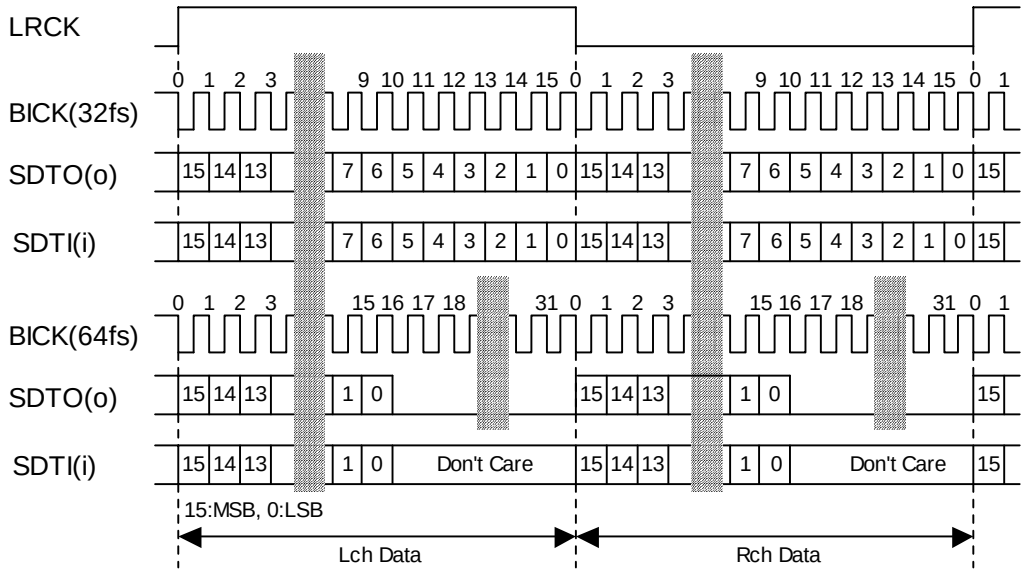


Figure 17. Mode 1 Timing

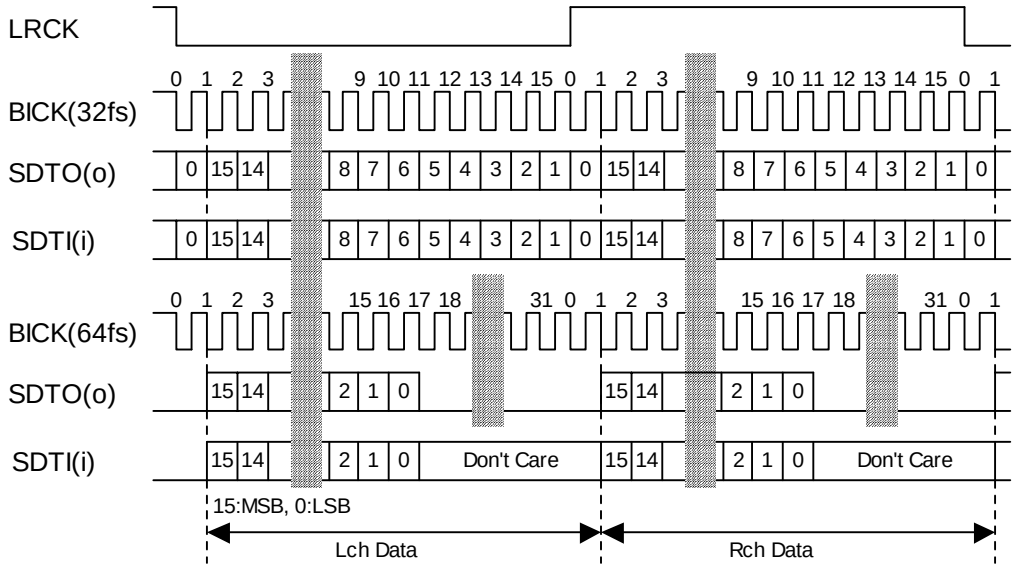


Figure 18. Mode 2 Timing

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 3.4Hz (@fs=44.1kHz) and scales with sampling rate (fs).

■ MIC Gain Amplifier

AK4537 has a Gain Amplifier for Microphone input. This gain is 0dB or 20dB, selected by the MGAIN bit (Table 14). The typical input impedance is 30kΩ.

MGAIN bit	Input Gain	
0	0dB	
1	+20dB	Default

Table 14. MIC Input Gain

The mic gain amp of the AK4537 supports the following three cases:

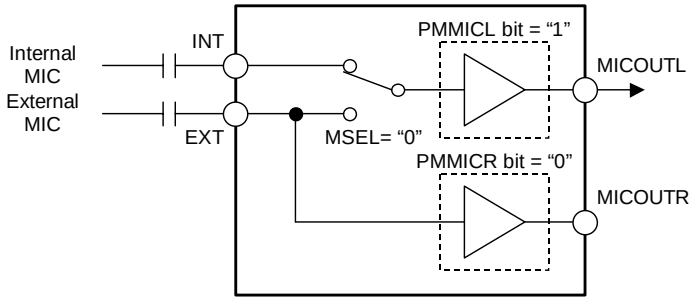


Figure 19. Internal MIC (Mono)

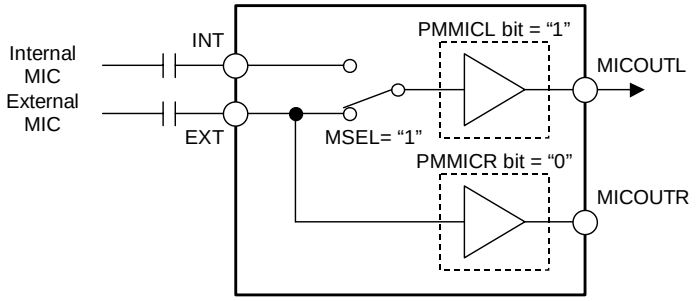


Figure 20. External MIC (Mono)

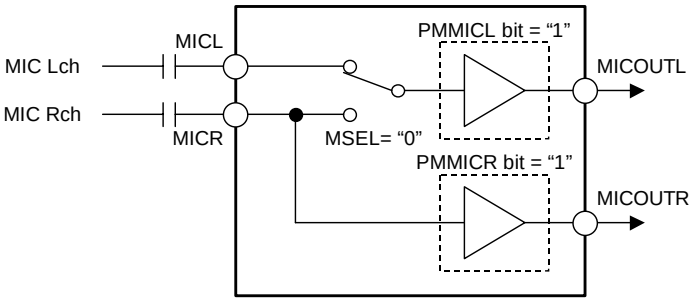


Figure 21. Stereo MIC

■ MIC Power

The MPI and MPE pins supply power for the Microphone. These output voltages are 0.75 x AVDD (typ) and the maximum output current is 1.25mA.

■ Manual Mode

The AK4537 becomes a manual mode at ALC1 bit = "0". This mode is used in the case shown below.

1. After exiting reset state, set up the registers for the ALC1 operation (ZTM1-0, LMTH and etc)
2. When the registers for the ALC1 operation (Limiter period, Recovery period and etc) are changed. For example; When the change of the sampling frequency.
3. When IPGA is used as a manual volume.

When writing to the IPGAL6-0 and IPGAR6-0 bits continually, the control register should be written by an interval more than zero crossing timeout (the write operation interval between IPGAL6-0 and IPGAR6-0 bits also should be more than zero crossing timeout). When IPGAC bit is "0", the write operation interval from IPGAL6-0 bits to IPGAR6-0 bits is no care. Therefore, the auto increment function of I^2C bus is available at IPGAC = "0".

■ MIC-ALC Operation

The ALC (Automatic Level Control) of MIC input is done by ALC1 block when ALC1 bit is "1". When PMMICL bit = "1" and PMMIR bit = "1", the IPGA is set to the same value for both channels.

[1] ALC1 Limiter Operation

When the ALC1 limiter is enabled, and IPGA Lch or Rch output exceeds the ALC1 limiter detection level (LMTH), the IPGA value is attenuated by the amount defined in the ALC1 limiter ATT step (LMAT1-0 bits) automatically.

When the ZELM bit = "1", the timeout period is set by the LTM1-0 bits. The operation for attenuation is done continuously until both Lch and Rch input signal levels become LMTH or less. If the ALC1 bit does not change into "0" after completing the attenuation, the attenuation operation repeats while Lch or Rch input signal level equals or exceeds LMTH.

When the ZELM bit = "0", the timeout period is set by the ZTM1-0 bits. This enables the zero-crossing attenuation function so that the IPGA value is attenuated at the zero-detect points of the waveform.

[2] ALC1 Recovery Operation

The ALC1 recovery refers to the amount of time that the AK4537 will allow both Lch and Rch signal to exceed a predetermined limiting value prior to enabling the limiting function. The ALC1 recovery operation uses the WTM1-0 bits to define the wait period used after completing an ALC1 limiter operation. If Lch or Rch input signals are lower than the "ALC1 Recovery Waiting Counter Reset Level", the ALC1 recovery operation starts. The IPGA value increases automatically during this operation up to the reference level (REF6-0 bits). The ALC1 recovery operation is done at a period set by the WTM1-0 bits. Zero crossing is detected during WTM1-0 period, the ALC1 recovery operation waits WTM1-0 period and the next recovery operation starts.

During the ALC1 recovery operation, when Lch or Rch input signal level exceeds the ALC1 limiter detection level (LMTH), the ALC1 recovery operation changes immediately into an ALC1 limiter operation.

In the case of
(IPGA Lch and Rch Output Level) < (Limiter detection level)
and
(IPGA Lch and Rch Output Level) ≥ (Recovery waiting counter reset level)
during the ALC1 recovery operation, the wait timer for the ALC1 recovery operation is reset. Therefore, in the case of
(IPGA Lch or Rch Output Level) < (Recovery waiting counter reset level),
the wait timer for the ALC1 recovery operation starts.

The ALC1 operation corresponds to the impulse noise. When the impulse noise is input, the ALC1 recovery operation becomes faster than a normal recovery operation.

[3] Example of ALC1 Operation

Table 15 shows the examples of the ALC1 setting. In case of this examples, ALC1 operation starts from 0dB.

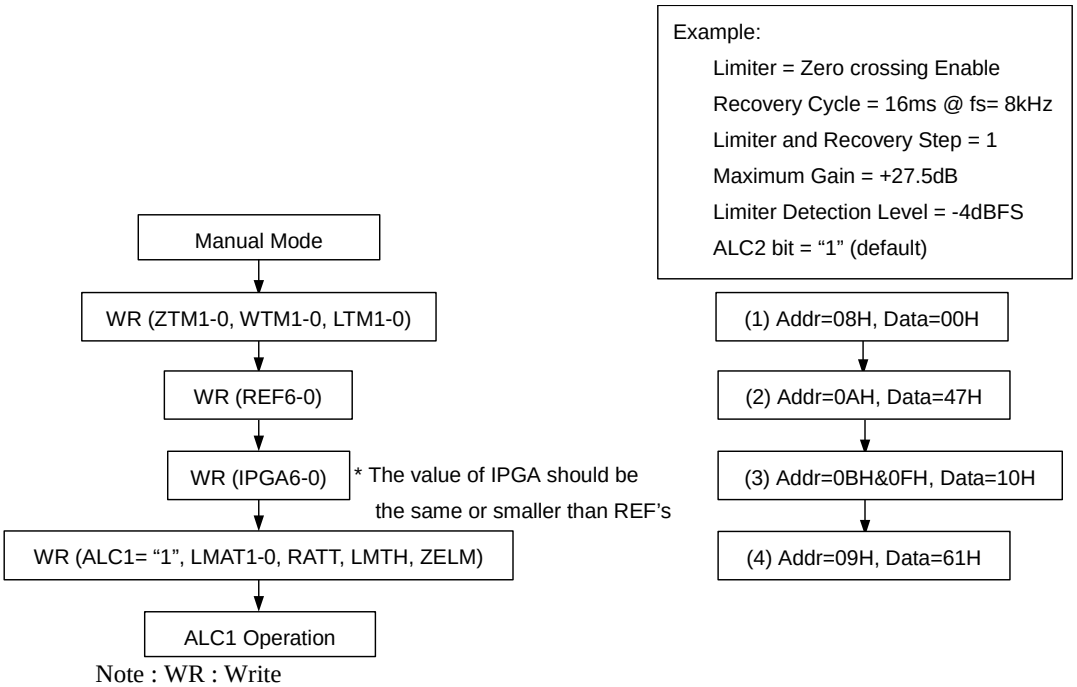
Register Name	Comment	fs=8kHz		fs=16kHz		fs=44.1kHz	
		Data	Operation	Data	Operation	Data	Operation
LMTH	Limiter detection Level	1	-4dBFS	1	-4dBFS	1	-4dBFS
LTM1-0	Limiter operation period at ZELM = 1	00	Don't use	00	Don't use	00	Don't use
ZELM	Limiter zero crossing detection	0	Enable	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	00	16ms	01	16ms	10	11.6ms
WTM1-0	Recovery waiting period *WTM1-0 bits should be the same data as ZTM1-0 bits	00	16ms	01	16ms	10	11.6ms
REF6-0	Maximum gain at recovery operation	47H	+27.5dB	47H	+27.5dB	47H	+27.5dB
IPGAL6-0, IPGAR6-0	Gain of IPGA at ALC1 operation start	10H	0dB	10H	0dB	10H	0dB
LMAT1-0	Limiter ATT Step	00	1 step	00	1 step	00	1 step
RATT	Recovery GAIN Step	0	1 step	0	1 step	0	1 step
ALC1	ALC1 Enable bit	1	Enable	1	Enable	1	Enable

Table 15. Example of the ALC1 setting

The following registers should not be changed during the ALC1 operation. These bits should be changed after the ALC1 operation is finished by ALC1 bit = "0" or PMMIC bit = "0".

- **LTM1-0, LMTH, LMAT1-0, WTM1-0, ZTM1-0, RATT, REF6-0, ZELM bits**

IPGA gain at ALC1 operation start can be changed from the default value of IPGAL6-0 bits while PMMICL, PMMICR, PMIPGL or PMIPGR bit is "1" and ALC1 bit is "0". When ALC1 bit is changed from "1" to "0", IPGA holds the last gain value set by ALC1 operation.



Note : WR : Write

Figure 22. Registers set-up sequence at ALC1 operation

■ De-emphasis Filter

The AK4537 includes the digital de-emphasis filter (tc = 50/15μs) by IIR filter. Setting the DEM1-0 bits enables the de-emphasis filter (Table 16).

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 16. De-emphasis Control

■ Bass Boost Function

The BST1-0 bits control the amount of low frequency boost applied to the DAC output signal (Table 17) . If the BST1-0 bits are set to "10" (MID Level), use a 47μF capacitor for AC-coupling. If the boosted signal exceeds full scale, the analog output clips to the full scale. Figure 10 shows the boost frequency response at –20dB signal input.

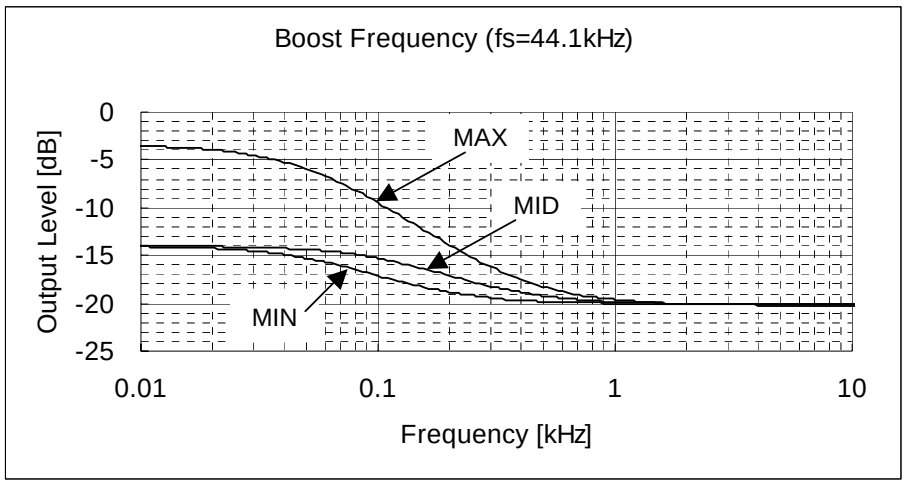


Figure 23. Boost Frequency (fs=44.1kHz)

BST1	BST0	Mode	
0	0	OFF	Default
0	1	MIN	
1	0	MID	
1	1	MAX	

Table 17. Low Frequency Boost Control

■ Digital Attenuator

The AK4537 has a channel-independent digital attenuator (256 levels, 0.5dB step, Mute). The attenuation level of each channel can be set by the ATTL/R7-0 bits. When the DATTC bit = "1", the ATTL7-0 bits control both Lch and Rch attenuation levels. When the DATTC bit = "0", the ATTL7-0 bits control Lch level and ATTR7-0 bits control Rch level. This attenuator has a soft transition function. It takes 1061/fs from 00H to FFH.

ATTL/R7-0	Attenuation	
00H	0dB	Default
01H	–0.5dB	
02H	–1.0dB	
03H	–1.5dB	
:	:	
:	:	
FDH	–126.5dB	
FEH	–127.0dB	
FFH	MUTE (–∞)	

Table 18. DATT Code Table

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit goes to a "1", the output signal is attenuated by -∞ ("0") during the cycle set by the TM1-0 bits. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to 0dB during the cycle set of the TM1-0 bits. If the soft mute is cancelled within the cycle set by the TM1-0 bits after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission (Figure 24).

The soft mute function is independent of output volume and cascade connected between both functions.

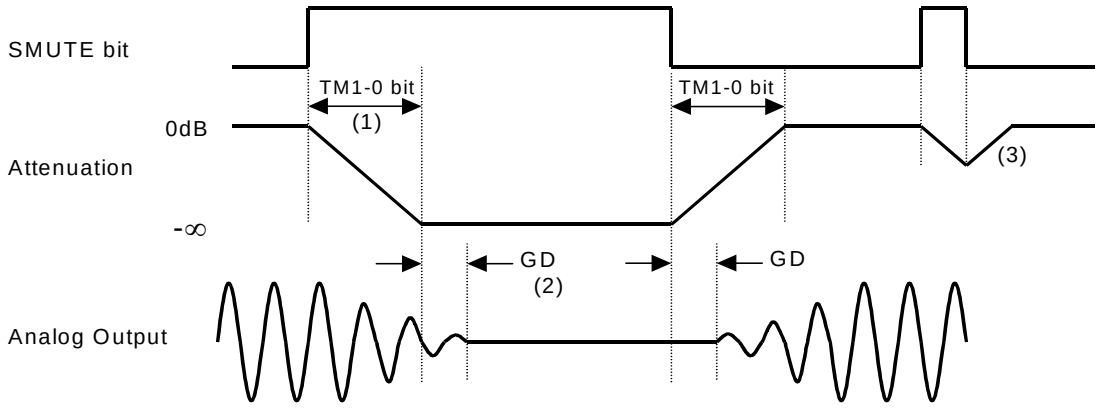


Figure 24. Soft Mute Function

(1) The output signal is attenuated until -∞ ("0") by the cycle set by the TM1-0 bits.
(2) Analog output corresponding to digital input has the group delay (GD).
(3) If the soft mute is cancelled within the cycle of setting the TM1-0 bits, the attenuation is discounted and returned to 0dB(the set value).

■ BEEP Input

When the PMBPS bit is set to “1”, the stereo beep input is powered up. And when the BPSHP bit is set to “1”, the input signals from the BEEPL and BEEPR pins are mixed to Headphone outputs. When the BPSSP bit is set to “1”, the signal of (BEEPL + BEEPR)/2 is input to Speaker-amp. When the PMBPM bit is set to “1”, mono beep input is powered up. And when the BPMHP bit is set to “1”, the input signal from the BEEPM pin to Headphone-amp. When the BPMSP bit is set to “1”, the signal from the BEEPM pin is input to Speaker output. The external resisters Ri adjust the signal level of each BEEP input that are mixed to Headphone and Speaker outputs.

The signal from the BEEPM pin is mixed to the Headphone-amp through a –20dB gain stage. The signal from the BEEPM pin is mixed to the Speaker-amp without gain. The internal feedback resistance is 20k ± 30%Ω.

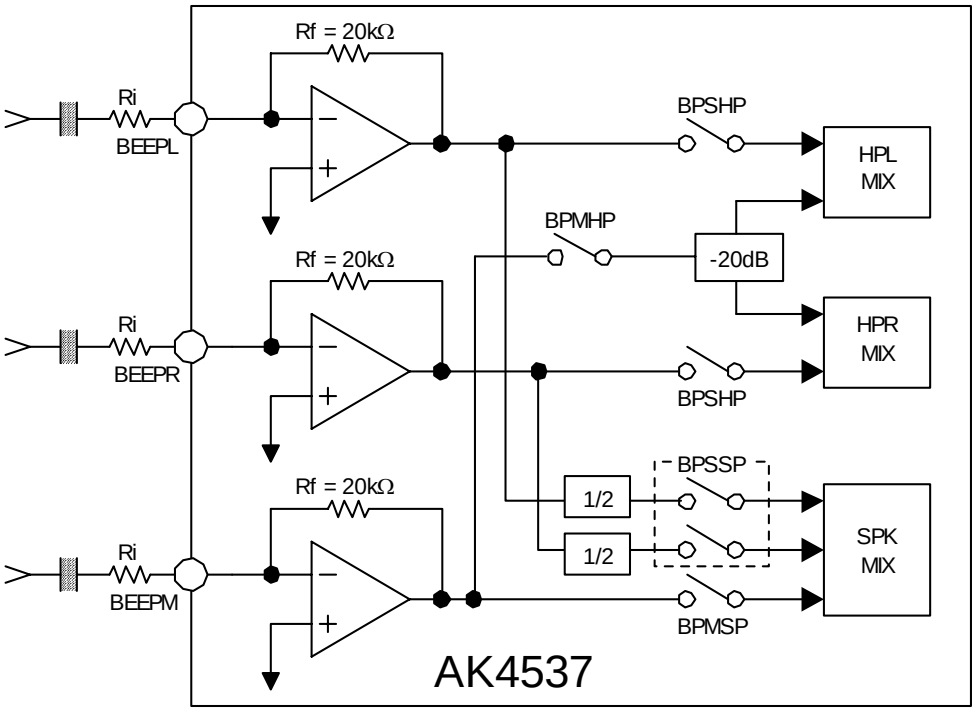


Figure 25. Block Diagram of BEEP pins

■ Headphone Output

Power supply voltage for the Headphone-amp is supplied from the HVDD pin and centered on the HVDD/2 voltage. The Headphone output load resistance is min.20Ω. When the PMHPL and PMHPR bits are "0", the common voltage of Headphone-amp falls and the outputs (HPL and HPR pins) go to "L" (HVSS). When the PMHPL and PMHPR bits are "1", the common voltage rises to HVDD/2. A capacitor between the MUTET pin and ground reduces pop noise at power-up.

[Example] : A capacitor between the MUTET pin and ground = 1.0μF:
Rise/fall time constant: τ = 100ms(typ), 250ms(max)
Time until the common goes to HVSS when PMHPL/R bits = "1" → "0": 500ms(max)

When HPL and HPR bits are "1", the Headphone-amp is powered-down, and the outputs (HPL and HPR pins) go to "L" (HVSS).

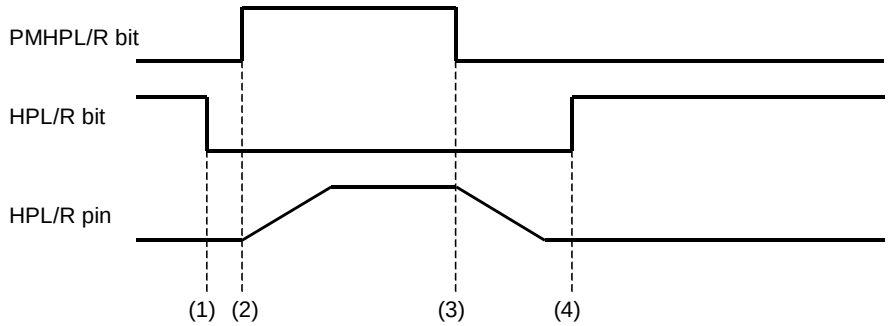


Figure 26. Power-up/Power-down Timing for Headphone-amp

(1) Headphone-amp power-up (HPL, HPR bit= "0"). The outputs are still HVSS.
(2) Headphone-amp common voltage rise up (PMHPL, PMHPR bit= "1"). Common voltage of Headphone-amp is rising. This rise time depends on the capacitor value connected with the MUTET pin. The time constant is τ = 100k x C when the capacitor value on MUTET pin is "C".
(3) Headphone-amp common voltage fall down (PMHPL, PMHPR bit= "0"). Common voltage of Headphone-amp is falling. This fall time depends on the capacitor value connected with the MUTET pin. The time constant is τ = 100k x C when the capacitor value on MUTET pin is "C".
(4) Headphone-amp power-down (HPL, HPR bit= "1"). The outputs are HVSS. If the power supply is switched off or Headphone-amp is powered-down before the common voltage goes to HVSS, some POP noise occurs.

The cut-off frequency of Headphone-amp output depends on the external resistor and capacitor used. Table 19 shows the cut off frequency and the output power for various resistor/capacitor combinations. The headphone impedance R_L is 16Ω. Output powers are shown at HVDD = 2.7, 3.0 and 3.3V. The output voltage of headphone is 0.6 x AVDD (Vpp).
When an external resistor R is smaller than 12Ω, put an oscillation prevention circuit (0.22μF±20% capacitor and 10Ω±20% resistor) because it has the possibility that Headphone-amp oscillates.

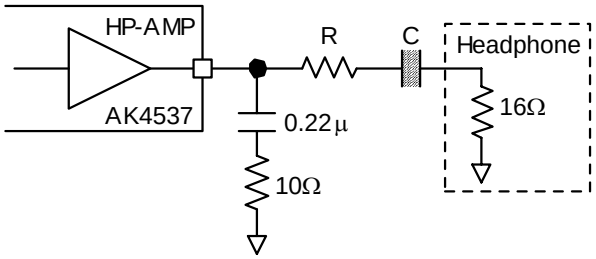


Figure 27. External Circuit Example of Headphone

R [Ω]	C [μF]	fc [Hz] BOOST=OFF	fc [Hz] BOOST=MID	Output Power [mW]		
				2.7V	3.0V	3.3V
6.2	47	152.5	63	10.0	12.4	15.0
16	47	105.8	43	4.8	6.0	7.2
6.2	100	71.2	27	10.0	12.4	15.0
16	100	49.7	20	4.8	6.0	7.2

Table 19. External Circuit Example

■ Speaker Output

The output signal from analog volume is converted into a mono signal [(L+R)/2] and this signal is input to the Speaker-amp via the ALC2 circuit. This Speaker-amp is a mono BTL output. When DAC output signal is input to MIN pin as system design example (Figure 47), Speaker-amp can output a maximum of 300mW@SPKG bit = "0" and ALC2 bit = "0" at 8Ω load when HVDD = 3.3V. When BEEP input is used for DAC output, maximum power becomes 400mW. Figure 29 and Figure 30 indicates connection examples for 400mW output.

SPKG	ALC2	Po(max)	
0	x	150mW	Default
1	0	300mW	
	1	250mW	

Table 20. SPK-Amp Maximum Output Power (x: Don't care)

Speaker blocks (MOUT2, ALC2 and Speaker-amp) can be powered up/down by controlling the PMSPK bit. When the PMSPK bit is "0", the MOUT2, SPP and SPN pins are placed in a Hi-Z state.

When the SPPS bit is "0", the Speaker-amp enters power-save-mode. In this mode, the SPP pin is placed in a Hi-Z state and the SPN pin goes to HVDD/2 voltage. And then the Speaker output gradually changes to the HVDD/2 voltage and this mode can reduce pop noise at power-up. When the AK4537 is powered down, pop noise can be also reduced by first entering power-save-mode.

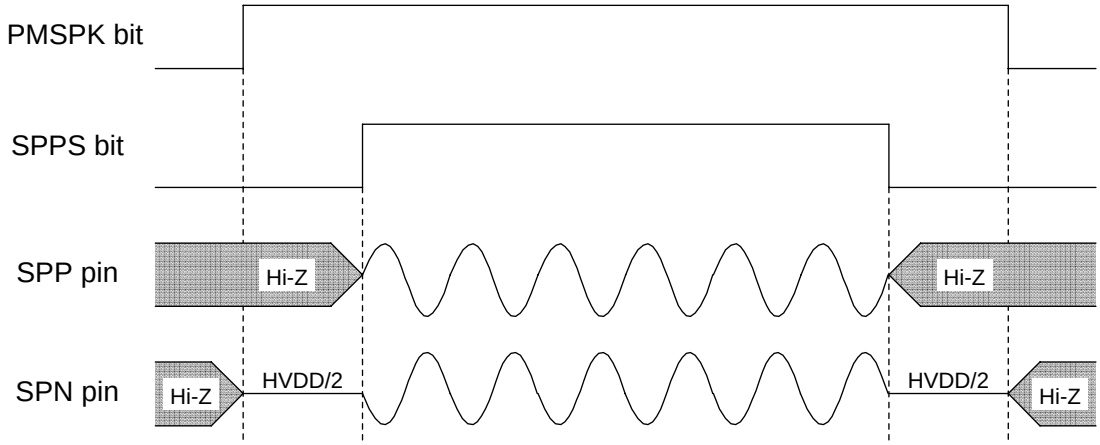


Figure 28. Power-up/Power-down Timing for Speaker-amp

[Connection Example for 400mW output]

1) Using BEEPM pin

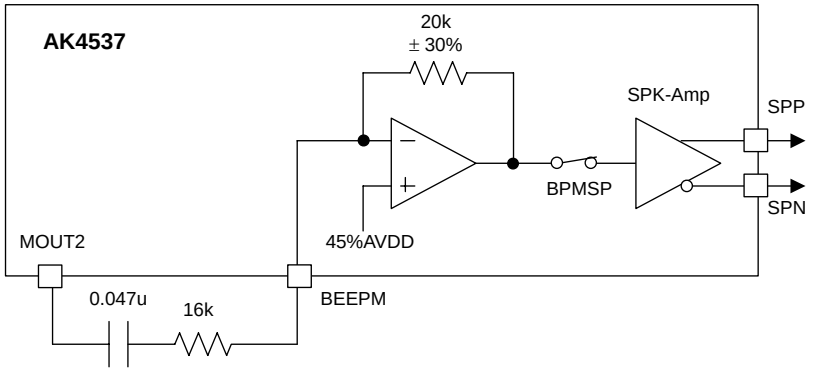


Figure 29. Connection example for 400mW output using BEEPM pin (SPKG bit = "1")

2) Using BEEPL and BEEPR pins

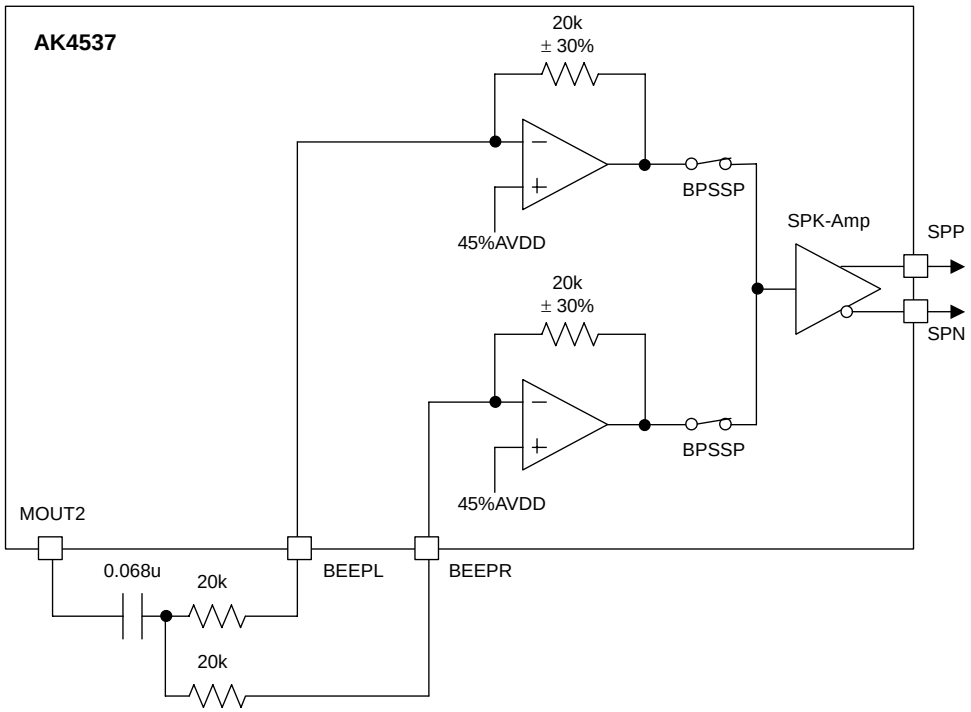


Figure 30. Connection example for 400mW output using BEEPL and BEEPR pins (SPKG bit = "1")

Note)
1. MOUT2 output is recommended to be AC coupled to avoid amplified DC offset of common voltage of MOUT2 and BEEP-Amp is output via BTL Speaker-Amp (that means stand-by current is increased). Capacitor size affects the cut-off frequency of 1st order LPF made by this AC coupling capacitor and series resister in front of BEEP input.
2. Internal feedback resister of BEEP-Amp which determines BEEP-Amp gain has 30% sample variation.

■ Mono Output (MOUT2 pin)

The mixed Lch/Rch signal of DAC is output from the MOUT2 pin. When the MOUT2 bit is "0", this output is OFF and the MOUT2 pin is forced to VCOM voltage. The load impedance is 10kΩ (min.). When the PMSPK bit is "0", the Speaker-amp enters power-down-mode and the output is placed in a Hi-Z state.

■ Stereo Line Output (LOUT/ROUT pins)

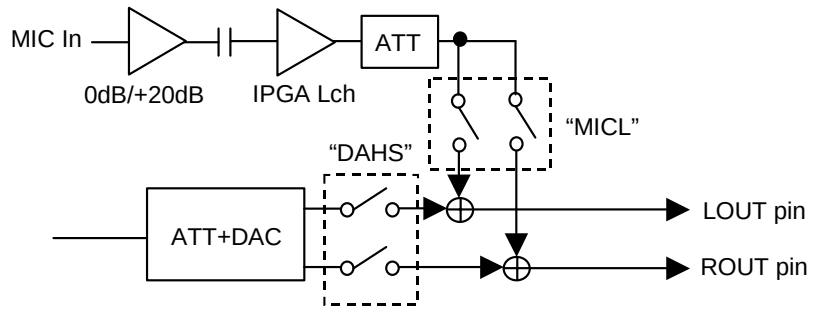


Figure 31. Stereo Line Output

When DAHS bit is "1", Lch/Rch signal of DAC is output from the LOUT/ROUT pins which is single-ended. When MICL bit is "1", Lch signal of IPGA is output from LOUT/ROU pins. The load impedance is 10kΩ (min.). When the PMLO bit is "0", the stereo line output enters power-down-mode and the output is placed in a Hi-Z state. When the PSLO bit is "0" at PMLO bit is "1", stereo line output becomes power-save-mode and the LOUT/ROUT pins are forced to 0.45 x AVDD voltage. When PSLO bit is "1" at PMLO bit is "1", stereo line output is normal operation.

ATTL7-0 and ATTR7-0 bits set the volume control of DAC output. ATTS3-0 bits set the volume control of IPGA Lch output.

■ Mono Output (MOUT+/MOUT- pins)

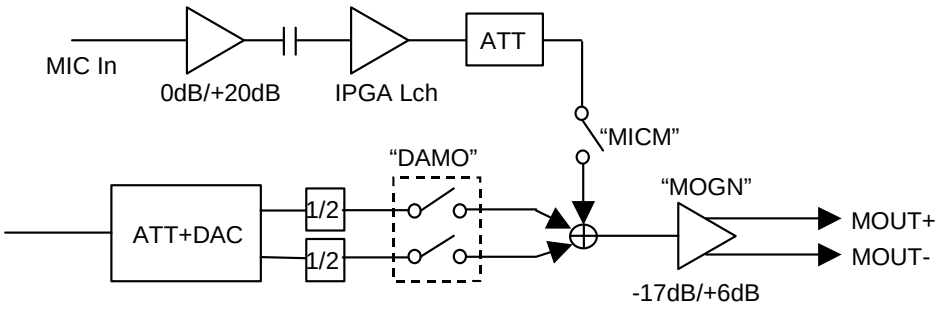


Figure 32. Mono Line Output

When DAMO bit is "1", mono mixer mixes Lch and Rch signal from DAC. This mixed signal is output to mono line output that is differential output. When MICM bit is "1", Lch signal from IPGA is output to mono line output. Either MOUT+ or MOUT- pin can be used as single-ended output pin. The load impedance is 20kΩ (min.). When the PMMO bit is "0", the mono line output enters power-down-mode and the output is placed in a Hi-Z state.

ATTL7-0 and ATTR7-0 bits set the volume control of DAC output. ATTM bit sets the volume control of IPGA Lch output. Amp for mono line output has 6dB gain and -17dB gain that are set by the MOGN bit.

■ **ALC2 Operation** (ALC2 bit = "1")

Input resistance of the ALC2 is 24kΩ (typ) and centered around VCOM voltage, and the input signal level is –3.1dBV. (see Figure 33 and Figure 34. 0dBV=1Vrms=2.828Vpp)

The limiter detection level is proportional to HVDD. The output level is limited by the ALC2 circuit when the input signal exceeds –5.2dBV (=FS-1.9dB@HVDD=3.3V). When a continuous signal of –5.2dBV or greater is input to the ALC2 circuit, the change period of the ALC2 limiter operation is set by the ROTM bit and the attenuation level is 0.5dB/step.

The ALC2 recovery operation uses zero crossings and gains of 1dB/step. The ALC2 recovery operation is done until the input level of the Speaker-amp goes to –7.2dBV(=FS-3.9dB@HVDD=3.3V). The ROTM bit sets the ALC2 recovery operation period.

When the input signal is between –5.2dBV and –7.2dBV, the ALC2 limiter or recovery operations are not done.

When the PMSPK bit changes from "0" to "1", the initilization cycle (2048/fs = 46.4ms @fs=44.1kHz at ROTM bit = "0", 512/fs = 11.4ms @fs=44.1kHz at the ROTM bit = "1") starts. The ALC2 is disabled during the initilization cycle and the ALC2 starts after completing the initilization cycle.

Parameter		ALC2 Limiter operation	ALC2 Recovery operation
Operation Start Level		–5.2dBV	–7.2dBV
Period	ROTM bit = "0"	2/fs = 45μs@fs=44.1kHz	2048/fs = 46.4ms@fs=44.1kHz
	ROTM bit = "1"	2/fs = 181μs@fs=11.025kHz	512/fs = 46.4ms@fs=11.025kHz
Zero-crossing Detection		X	O (Timeout = 2048/fs)
ATT/GAIN		0.5dB step	1dB step

Table 21. Limiter /Recovery of ALC2 at HVDD=3.3V

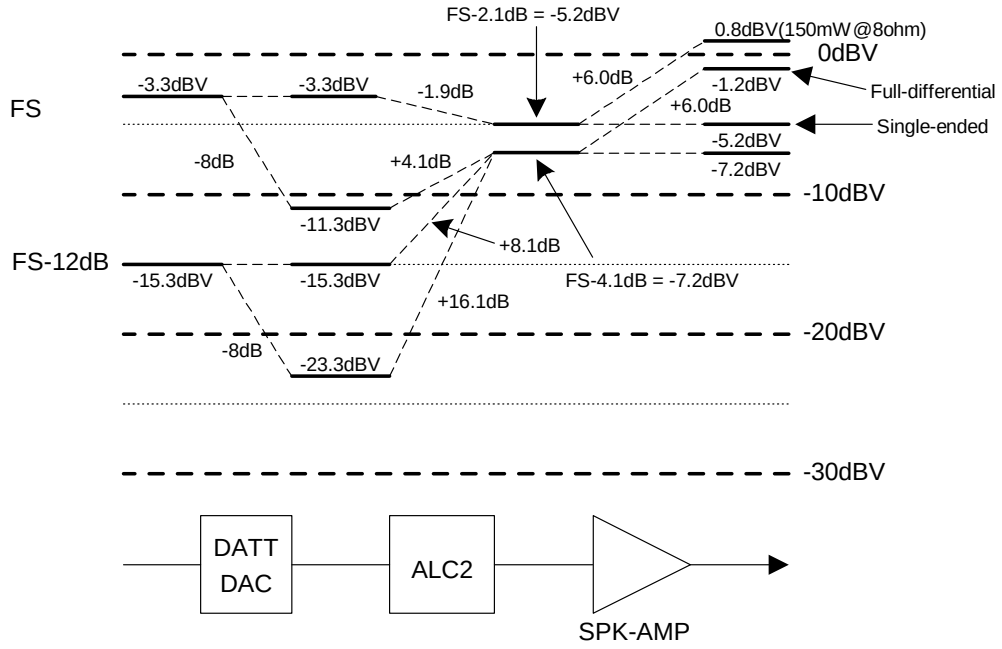


Figure 33. Speaker-amp Output Level Diagram (HVDD=3.3V, DATT=–8.0dB, SPKG bit= "0", ALC2= "1")

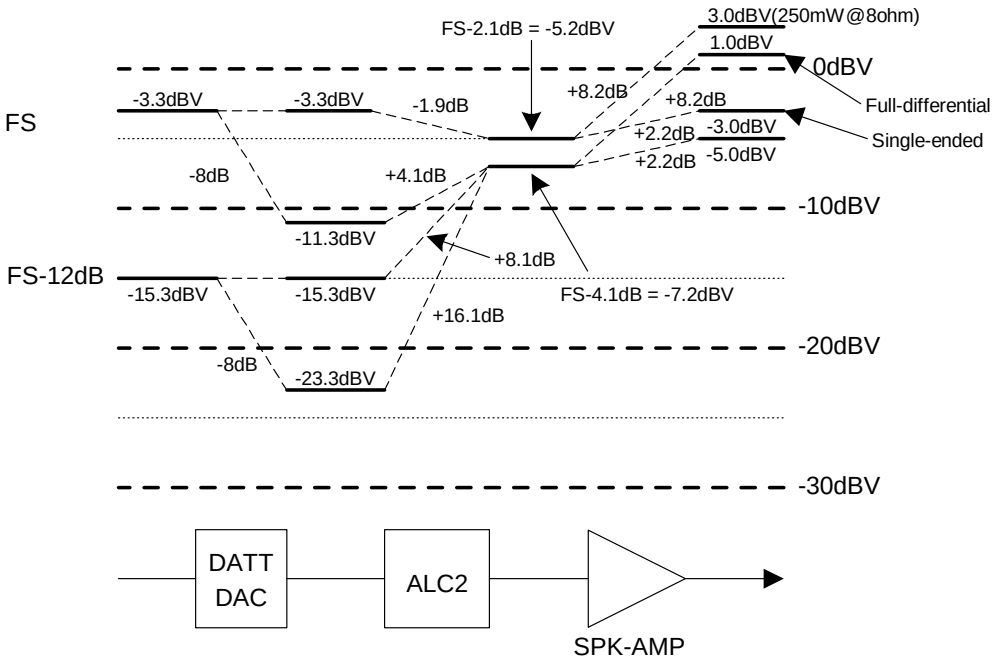
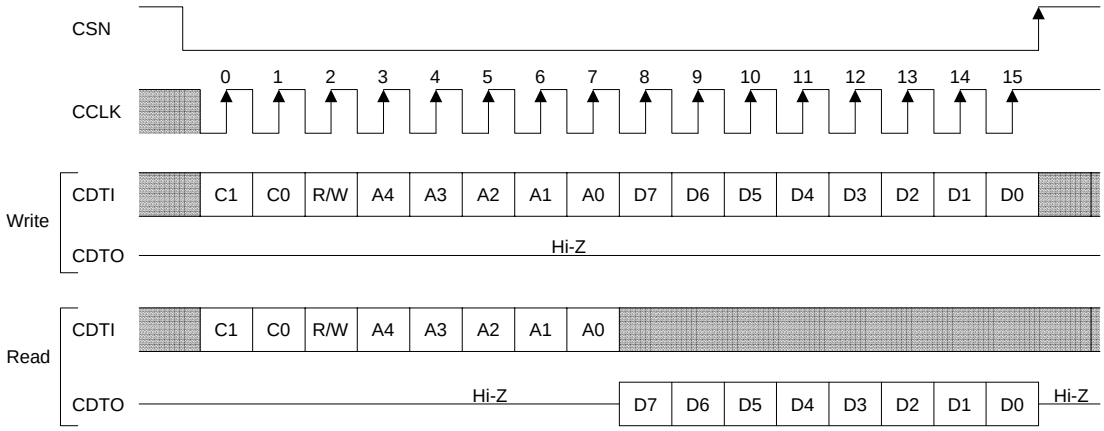


Figure 34. Speaker-amp Output Level Diagram (HVDD=3.3V, DATT=–8.0dB, SPKG bit= “1”, ALC2= “1”)

■ Serial Control Interface

(1) 4-wire Serial Control Mode (I2C pin = “L”)

Internal registers may be written by using the 4-wire µP interface pins (CSN, CCLK, CDTI and CDTO). The data on this interface consists of a 2-bit Chip address, Read/Write, Register address (MSB first, 5bits) and Control data (MSB first, 8bits). The chip address high bit is fixed to “1” and the lower bit is set by the CAD0 pin. Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. After a low-to-high transition of CSN, data is latched for write operations and CDTO bit outputs Hi-Z. The clock speed of CCLK is 5MHz (max). The value of internal registers is initialized at PDN pin = “L”.



C1 - C0 : Chip Address (C1="1", C0=CAD0)
R/W : READ / WRITE ("1" : WRITE, "0" : READ)
A4 - A0 : Register Address
D7 - D0 : Control Data

Figure 35. Serial Control I/F Timing

(2) I²C-bus Control Mode (I2C pin = "H")

The AK4537 supports the standard-mode I²C-bus (max: 100kHz). The AK4537 does not support a fast-mode I²C-bus system (max: 400kHz).

(2)-1. WRITE Operations

Figure 36 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 42). After the START condition, a slave address is sent. This address is 7 bits long followed by an eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next two bits are CAD1 and CAD0 (device address bits). These two bits identify the specific device on the bus. The hard-wired input pins (CAD1 and CAD0 pins) set these device address bits (Figure 37). If the slave address matches that of the AK4537, the AK4537 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 43). A R/W bit value of "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4537. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 38). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 39). The AK4537 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 42).

The AK4537 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4537 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address. Only write to address 00H to 10H.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 44) except for the START and STOP conditions.

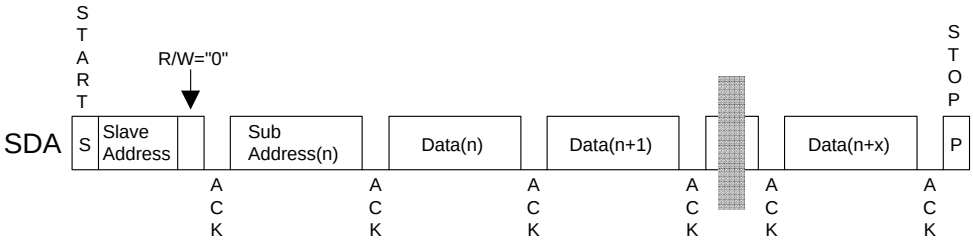


Figure 36. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	CAD1	CAD0	R/W

(Those CAD1/0 should match with CAD1/0 pins)

Figure 37. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 38. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 39. Byte Structure after the second byte

(2)-2. READ Operations

Set the R/W bit = “1” for the READ operation of the AK4537. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 1FH prior to generating a stop condition, the address counter will “roll over” to 00H and the previous data will be overwritten.

The AK4537 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4537 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to “1”, the AK4537 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4537 ceases transmission.

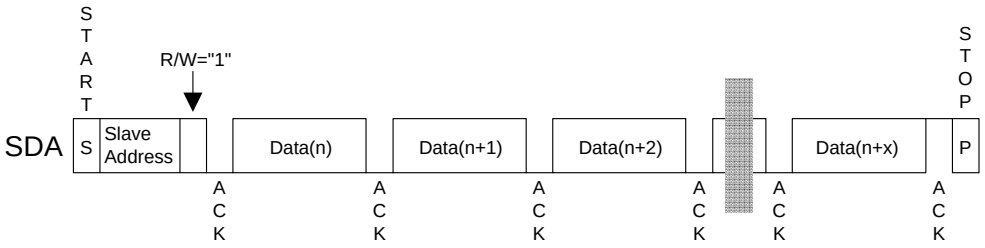


Figure 40. CURRENT ADDRESS READ

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit set to “1”. The AK4537 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4537 ceases transmission.

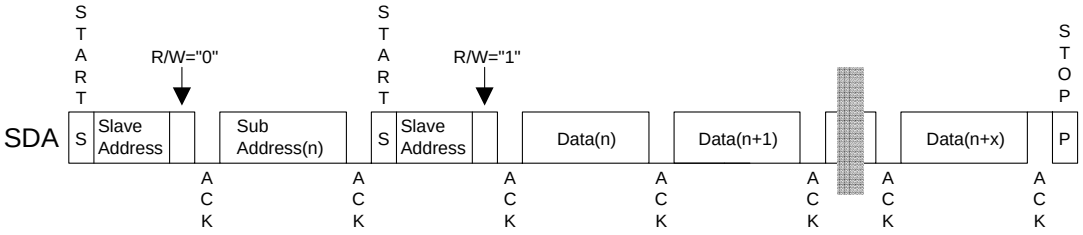


Figure 41. RANDOM ADDRESS READ

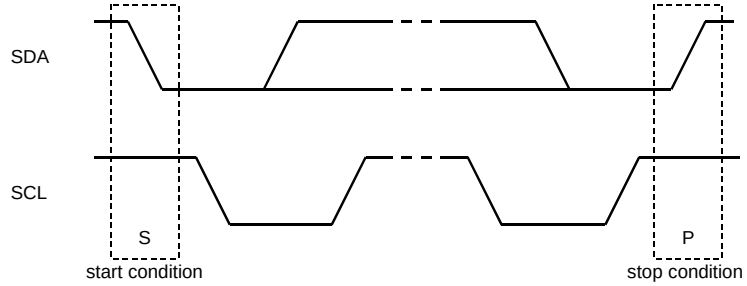


Figure 42. START and STOP Conditions

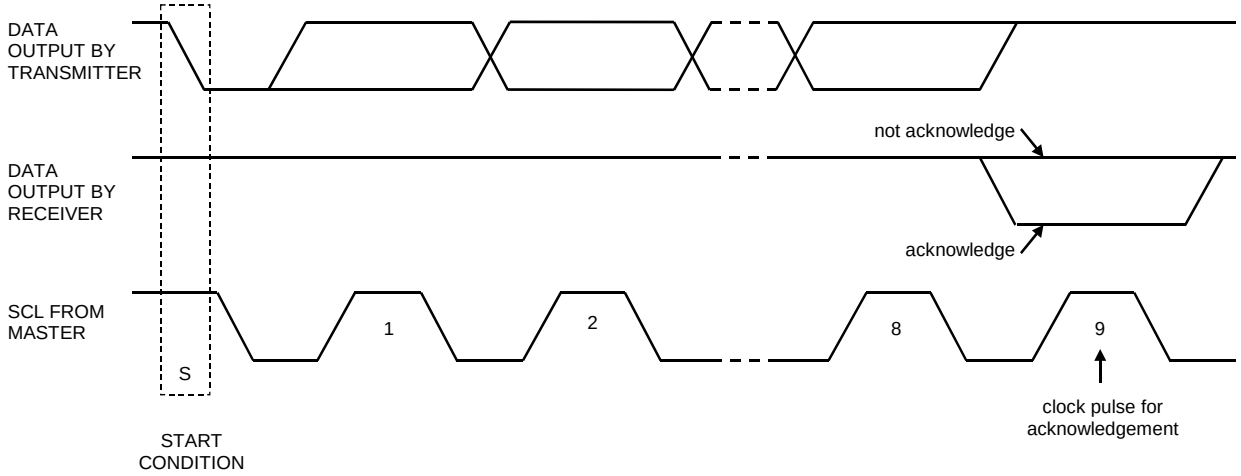


Figure 43. Acknowledge on the I^2C-Bus

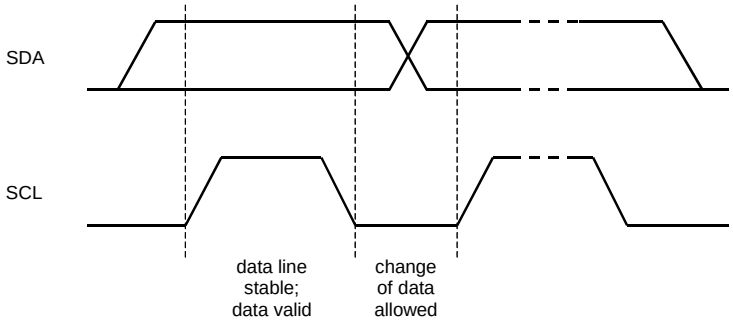


Figure 44. Bit Transfer on the I^2C-Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMVCM	PMBPS	PMBPM	PMLO	PMMO	PMIPGL	PMMICL	PMADL
01H	Power Management 2	MCKPD	PMXTL	PMPLL	SPKG	PMSPK	PMHPL	PMHPR	PMDAC
02H	Signal Select1	MOGN	PSMO	DAMO	MICM	BPSSP	BPMSP	ALCS	MOUT2
03H	Signal Select2	DAHS	PSLO	0	MICL	BPSHP	BPMHP	HPL	HPR
04H	Mode Control 1	PLL1	PLL0	PS1	PS0	MCKO	BF	DIF1	DIF0
05H	Mode Control 2	FS2	FS1	FS0	0	0	HPM	LOOP	SPPS
06H	DAC Control	TM1	TM0	SMUTE	DATTC	BST1	BST0	DEM1	DEM0
07H	MIC Control	0	0	IPGAC	MPWRE	MPWRI	MICAD	MSEL	MGAIN
08H	Timer Select	0	ROTM	ZTM1	ZTM0	WTM1	WTM0	LTM1	LTM0
09H	ALC Mode Control 1	0	ALC2	ALC1	ZELM	LMAT1	LMAT0	RATT	LMTH
0AH	ALC Mode Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0
0BH	Lch Input PGA Control	0	IPGAL6	IPGAL5	IPGAL4	IPGAL3	IPGAL2	IPGAL1	IPGAL0
0CH	Lch Digital ATT Control	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
0DH	Rch Digital ATT Control	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
0EH	Volume Control	ATTM	ATTS2	ATTS1	ATTS0	0	0	0	0
0FH	Rch Input PGA Control	0	IPGAR6	IPGAR5	IPGAR4	IPGAR3	IPGAR2	IPGAR1	IPGAR0
10H	Power Management 3	0	0	0	INR	INL	PMIPGR	PMMICR	PMADR

PDN pin = “L” resets the registers to their default values.

Note: Unused bits must contain a “0” value.
Note: Only write to address 00H to 10H.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMVCM	PMBPS	PMBPM	PMLO	PMMO	PMIPGL	PMMICL	PMADL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMADL: ADC Lch Block Power Control
0: Power down (Default)
1: Power up
When the PMADL or PMADR bit changes from "0" to "1", the initialization cycle (2081/fs=47.2ms @44.1kHz) starts. After initializing, digital data of the ADC is output.

PMADL	PMADR	Analog		Digital
		Lch	Rch	L/R
0	0	Power down	Power down	Power down
0	1	Power down	Power up	Power up
1	0	Power up	Power down	Power up
1	1	Power up	Power up	Power up

Table 22. ADC Block Power Control

PMMICL: MIC Power and IPGA Lch Block Power Control
0: Power down (Default)
1: Power up

PMIPGL: IPGA Lch Block Power Control
0: Power down (Default)
1: Power up
IPGA Lch Block is powered up if PMMICL or PMIPGL bit is "1" (see Table 23).

PMMICL	PMIPGL	MIC-Amp	IPGA
0	0	Power down	Power down
0	1	Power down	Power up
1	0	Power up	Power up
1	1	Power up	Power up

Table 23. MIC-Amp and IPGA Lch Block Power Control

PMMO: Mono Line Out Power Control
0: Power down (Default)
1: Power up

PMLO: Stereo Line Out Power Control
0: Power down (Default)
1: Power up

PMBPM: Mono BEEP In Power Control
0: Power down (Default)
1: Power up
Even if PMBPM= "0", the path is still connected between BEEPM and HP/SPK-Amp. BPMHP and BPMSP bits should be set to "0" to disconnect these paths, respectively.

PMBPS: Stereo BEEP In Power Control
0: Power down (Default)
1: Power up
Even if PMBPS= "0", the path is still connected between BEEPL/R and HP/SPK-Amp. BPSHP and BPSSP bits should be set to "0" to disconnect these paths, respectively.

PMVCM: VCOM Block Power Control
0: Power down (Default)
1: Power up

Each block can be powered down respectively by writing "0" in each bit. When the PDN pin is "L", all blocks are powered down.

When all bits except MCKPD bit are "0" in the 00H, 01H and 10H addresses, all blocks are powered down. The register values remain unchanged. IPGA gain is reset when PMMICL=PMMICR=PMIPGL=PMIPGR= "0" (refer to the IPGAL6-0 and IPGAR6-0 bits description).

When any of the blocks are powered up, the PMVCM bit must be set to "1".

MCLK, BICK and LRCK must always be present unless PMMICL=PMMICR=PMIPGL=PMIPGR=PMADCL =PMADR=PMDAC=PMSPK= "0" or PDN pin = "L". The paths from BEEP to HP-Amp and SPK-Amp can operate without these clocks.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	MCKPD	PMXTL	PMPLL	SPKG	PMSPK	PMHPL	PMHPR	PMDAC
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	0	0	0	0

PMDAC: DAC Block Power Control
0: Power down (Default)
1: Power up

PMHPR: Rch of Headphone-Amp Common Voltage Power Control
0: Power down (Default)
1: Power up

PMHPL: Lch of Headphone-Amp Common Voltage Power Control
0: Power down (Default)
1: Power up

PMSPK: Speaker Block Power Control
0: Power down (Default)
1: Power up

SPKG: Select Speaker-Amp Output Power (8Ω load)
0: 150mW (Default)
1: 300mW(ALC2 = "0") or 250mW(ALC2 = "1")

PMPLL: PLL Block Power Control Select
0: EXT Mode and Power down (Default)
1: PLL Mode and Power up

PMXTL: X'tal Oscillation Block Power Control
0: Power down (Default)
1: Power up

MCKPD: XTI pin pull down control
0: Master Clock input enable
1: Pull down by 25kΩ (Default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Signal Select 1	MOGN	PSMO	DAMO	MICM	BPSSP	BPMSP	ALCS	MOUT2
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MOUT2: MOUT2 Output Enable (Mixing = (L+R)/2)
0: OFF (Default)
1: ON
When the MOUT2 bit = "0", the MOUT2 pin outputs VCOM voltage. The MOUT2 pin outputs signal at the MOUT2 bit = "1". This bit is valid at the PMSPK bit = "1". Hi-Z is output at the PMSPK bit = "0".

ALCS: ALC2 to Speaker-amp Enable
0: OFF (Default)
1: ON
ALC2 output signal is mixed to Speaker-amp at the ALCS bit = "1".

BPMSP: BEEPM to Speaker-amp Enable
0: OFF (Default)
1: ON
Mono BEEP signal (BEEPM pin) is mixed to Speaker-amp at the BPMSP bit = "1".

BPSSP: BEEPL/BEEPR to Speaker-amp Enable
0: OFF (Default)
1: ON
Stereo BEEP signals (BEEPL/BEEPR pins) are mixed to Speaker-amp at the BPSSP bit = "1".

MICM: IPGA Lch to MOUT+/MOUT- Enable
0: OFF (Default)
1: ON
IPGA Lch output signal is output through Mono Line Output (MOUT+/MOUT-pins) at the MICM bit = "1".

DAMO: DAC to MOUT+/MOUT- Enable
0: OFF (Default)
1: ON
DAC output signal is output through Mono Line Output (MOUT+/MOUT-pins) at the DAMO bit = "1".

PSMO: MOUT+/MOUT- Output Enable (Mixing = (L+R)/2)
0: Power Save Mode (Default)
1: Normal Operation
When the PSMO bit = "0", Mono Line Output is in power save mode and the MOUT+ and MOUT- pins output 0.45 x AVDD voltage.

MOGN: Gain control for mono output
0: +6dB (Default)
1: -17dB

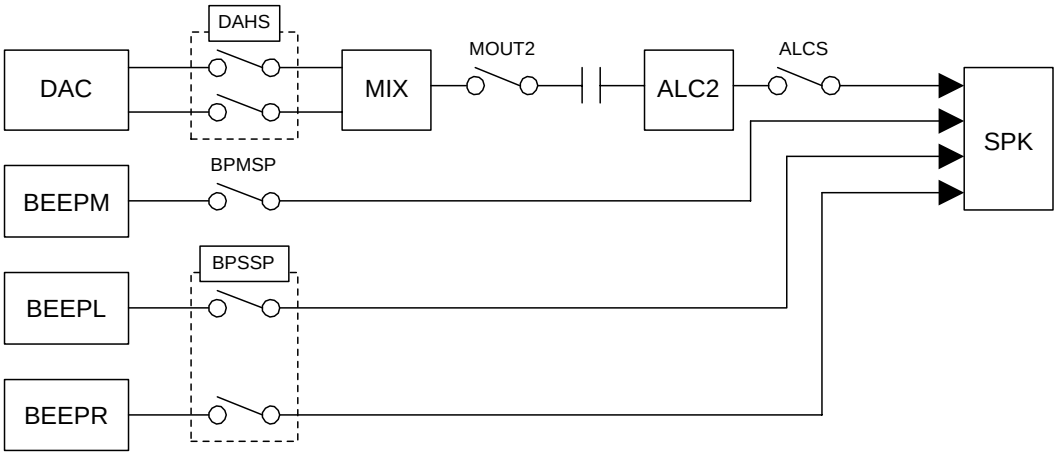


Figure 45. Speaker-amp switch control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Signal Select 2	DAHS	PSLO	0	MICL	BPSHP	BPMHP	HPL	HPR
R/W		R/W	R/W	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	1

HPR: Rch of Headphone-Amp Power Control
0: Normal Operation
1: OFF(Default)

HPL: Lch of Headphone-Amp Power Control
0: Normal Operation
1: OFF(Default)

BPMHP: BEEPM to Headphone-amp Enable
0: OFF (Default)
1: ON
Mono BEEP signal (BEEPM) is mixed to Headphone-amp at the BPMHP bit = "1".

BPSHP: BEEPL/BEEPR to Headphone-amp Enable
0: OFF (Default)
1: ON
Stereo BEEP signals (BEEPL/BEEPR) is mixed to Headphone-amp at the BPSHP bit = "1".

MICL: IPGA Lch to Stereo Line Output, Headphone-amp and MOUT2 Enable
0: OFF (Default)
1: ON
IPGA Lch signal is mixed to Stereo Line Output, Headphone-amp and MOUT2 at the DAHS bit = "1".

PSLO: Select LINEOUT
0: OFF. Power-Save-Mode. Output 0.45 x AVDD voltage. (Default)
1: Normal Operation
PSLO bit is enable when PMLO= "1".

DAHS: DAC to Stereo Line Output, Headphone-amp and MOUT2 Enable
0: OFF (Default)
1: ON
DAC signal is mixed to Stereo Line Output, Headphone-amp and MOUT2 at the DAHS bit = "1".

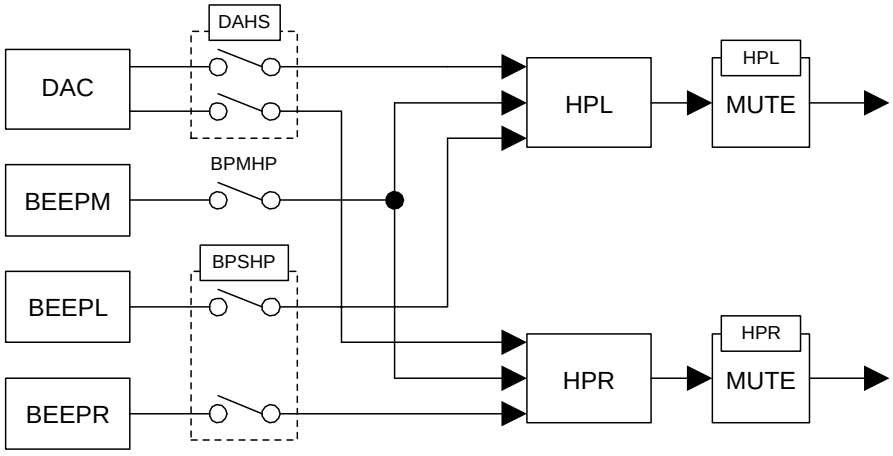


Figure 46. Headphone-amp switch control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Mode Control 1	PLL1	PLL0	PS1	PS0	MCKO	BF	DIF1	DIF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

DIF1-0: Audio Interface Format Select (see Table 13)
Default: "10" (ADC: I^2S, DAC: I^2S)

BF: BICK frequency Select at Master Mode
0: 64fs (Default)
1: 32fs
This bit is invalid in slave mode.

MCKO: Master Clock Output Enable
0: Disable (Default)
1: Enable

PS1-0: Output Master Clock Select (see Table 4, Table 8)
Default: "00" (256fs)

PLL1-0: Input Master Clock Select at PLL Mode (see Table 2)
Default: "00" (12.288MHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Mode Control 2	FS2	FS1	FS0	0	0	HPM	LOOP	SPPS
R/W		R/W	R/W	R/W	RD	RD	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SPPS: Speaker-amp Power-Save-Mode

0: Power Save Mode (Default)

1: Normal Operation

When the SPPS bit = "1", the Speaker-amp is in power-save-mode and the SPP pin becomes Hi-z and SPN pin is set to HVDD/2 voltage. When the PMSPK bit = "1", this bit is valid. After the PDN pin changes from "L" to "H", the PMSPK bit is "0", which powers down Speaker-amp.

LOOP: Loopback ON/OFF

0: OFF (Default)

1: ON

When this bit is "1", the ADC output is passed to the DAC input internally. The external input data to DAC is ignored.

HPM: Mono output select of Headphone

0: Stereo (Default)

1: Mono.

When the HPM bit = "1", (L+R)/2 signals are output to Lch and Rch of the Headphone-amp. Both PMHPL and PMHPR bits should be "1" when HPM bit is "1".

FS2-0: Sampling frequency modes (see Table 3, Table 7)

Default: "000" (fs=44.1kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	DAC Control	TM1	TM0	SMUTE	DATTC	BST1	BST0	DEM1	DEM0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	0	1

DEM1-0: De-emphases response (see Table 16)
Default: “01” (OFF)

BST1-0: Select Low Frequency Boost Function (see Table 17)
Default: “00” (OFF)

DATTC: DAC Digital Attenuator Control Mode Select
0: Independent
1: Dependent (Default)
When DATTC= “1”, ATTL7-0 bits control both Lch and Rch at same time. ATTR7-0 bits are not changed when the ATTL7-0 bits are written.

SMUTE: Soft Mute Control
0: Normal Operation (Default)
1: DAC outputs soft-muted
Soft mute operation is independent of digital attenuator and is performed in the digital domain.

TM1-0: Soft Mute Time Select (see Table 24)
Default: “00” (1024/fs)

TM1	TM0	Cycle	
0	0	1024/fs	Default
0	1	512/fs	
1	0	256/fs	
1	1	128/fs	

Table 24. Soft Mute Time Setting

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	MIC/HP Control	0	0	IPGAC	MPWRE	MPWRI	MICAD	MSEL	MGAIN
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

MGAIN: 1st Mic-amp Gain control
0: 0dB
1: +20dB (Default)

MSEL: Microphone select
0: Internal MIC (Default)
1: External MIC

MICAD: Switch Control from Mic In to ADC
0: OFF (Default)
1: ON
ALC1 output signal is input to ADC when MICAD bit = "1".

MPWRI: Power Supply Control for Internal Microphone
0: OFF (Default)
1: ON
The setting of MPWRI is enabled when PMMICL bit = "1".

MPWRE: Power Supply for External Microphone
0: OFF (Default)
1: ON
The setting of MPWRE is enabled when PMMICL bit = "1".

IPGAC: IPGA Control Mode Select
0: Dependent (Default)
1: Independent
When IPGAC= "1", IPGAL6-0 bits control both Lch and Rch at same time. IPGAR6-0 bits are not changed when the IPGAL6-0 bits are written.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Timer Select	0	ROTM	ZTM1	ZTM0	WTM1	WTM0	LTM1	LTM0
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LTM1-0: ALC1 limiter operation period at zero crossing disable (ZELM bit = "1") (see Table 25)
The IPGA value is changed immediately. When the IPGA value is changed continuously, the change is done by the period specified by the LTM1-0 bits. Default is "00" (0.5/fs).

LTM1	LTM0		ALC1 Limiter Operation Period			
			8kHz	16kHz	44.1kHz	
0	0	0.5/fs	63μs	31μs	11μs	Default
0	1	1/fs	125μs	63μs	23μs	
1	0	2/fs	250μs	125μs	45μs	
1	1	4/fs	500μs	250μs	91μs	

Table 25. ALC1 Limiter Operation Period at zero crossing disable (ZELM bit = "1")

WTM1-0: ALC1 Recovery Waiting Period (see Table 26)
A period of recovery operation when any limiter operation does not occur during the ALC1 operation. Default is "00" (128/fs).

WTM1	WTM0		ALC1 Recovery Operation Waiting Period			
			8kHz	16kHz	44.1kHz	
0	0	128/fs	16ms	8ms	2.9ms	Default
0	1	256/fs	32ms	16ms	5.8ms	
1	0	512/fs	64ms	32ms	11.6ms	
1	1	1024/fs	128ms	64ms	23.2ms	

Table 26. ALC1 Recovery Operation Waiting Period

ZTM1-0: Zero crossing timeout for the write operation by the μP, ALC1 recovery, and zero crossing enable (ZELM bit = "0") of the ALC1 operation. (see Table 27)
When the IPGA of each L/R channels perform zero crossing or timeout independently, the IPGA value is changed by the μP WRITE operation, ALC1 recovery operation or ALC1 limiter operation (ZELM bit = "0"). Default is "00" (128/fs).

ZTM1	ZTM0		Zero Crossing Timeout Period			
			8kHz	16kHz	44.1kHz	
0	0	128/fs	16ms	8ms	2.9ms	Default
0	1	256/fs	32ms	16ms	5.8ms	
1	0	512/fs	64ms	32ms	11.6ms	
1	1	1024/fs	128ms	64ms	23.2ms	

Table 27. Zero Crossing Timeout Period

ROTM: Period time for ALC2 Recovery operation
0: 2048/fs (Default)
1: 512/fs

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	ALC Mode Control 1	0	ALC2	ALC1	ZELM	LMAT1	LMAT0	RATT	LMTH
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	0	0	0	0	0

LMTH: ALC1 Limiter Detection Level / Recovery Waiting Counter Reset Level (see Table 28)

The ALC1 limiter detection level and the ALC1 recovery counter reset level may be offset by about ±2dB. Default is "0".

LMTH	ALC1 Limiter Detection Level	ALC1 Recovery Waiting Counter Reset Level	
0	ADC Input ≥ –6.0dBFS	–6.0dBFS > ADC Input ≥ –8.0dBFS	Default
1	ADC Input ≥ –4.0dBFS	–4.0dBFS > ADC Input ≥ –6.0dBFS	

Table 28. ALC1 Limiter Detection Level / Recovery Waiting Counter Reset Level

RATT: ALC1 Recovery GAIN Step (see Table 29)

During the ALC1 recovery operation, the number of steps changed from the current IPGA value is set. For example, when the current IPGA value is 30H and RATT bit = "1" is set, the IPGA changes to 32H by the ALC1 recovery operation and the output signal level is gained up by 1dB (=0.5dB x 2). When the IPGA value exceeds the reference level (REF6-0 bits), the IPGA value does not increase.

RATT	GAIN STEP	
0	1	Default
1	2	

Table 29. ALC1 Recovery Gain Step Setting

LMAT1-0: ALC1 Limiter ATT Step (see Table 30)

During the ALC1 limiter operation, when either Lch or Rch exceeds the ALC1 limiter detection level set by LMTH, the number of steps attenuated from the current IPGA value is set. For example, when the current IPGA value is 47H and the LMAT1-0 bits = "11", the IPGA transition to 43H when the ALC1 limiter operation starts, resulting in the input signal level being attenuated by 2dB (=0.5dB x 4). When the attenuation value exceeds IPGA = "00" (–8dB), it clips to "00".

LMAT1	LMAT0	ATT STEP	
0	0	1	Default
0	1	2	
1	0	3	
1	1	4	

Table 30. ALC1 Limiter ATT Step Setting

ZELM: Enable zero crossing detection at ALC1 Limiter operation

0: Enable (Default)

1: Disable

When the ZELM bit = "0", the IPGA of each L/R channel perform a zero crossing or timeout independently and the IPGA value is changed by the ALC1 operation. The zero crossing timeout is the same as the ALC1 recovery operation. When the ZELM bit = "1", the IPGA value is changed immediately.

ALC1: ALC1 Enable Flag
0: ALC1 Disable (Default)
1: ALC1 Enable
ALC1 is enabled when ALC1 bit is “1”. Default is “0”(Disable).

ALC2: ALC2 Enable Flag
0: ALC2 Disable
1: ALC2 Enable (Default)
ALC2 is enabled after initialization cycle(2048/fs=46.4ms@fs=44.1kHz). This initialization cycle starts when PMSPK bit is changed from “0” to “1”. Default is “1”(Enable).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	ALC Mode Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	1	0	1	1	0

REF6-0: Reference value at ALC1 Recovery Operation (see Table 31)
During the ALC1 recovery operation, if the IPGA value exceeds the setting reference value by gain operation, then the IPGA does not become larger than the reference value. For example, when REF7-0 = “30H”, RATT = 2step, IPGA = 2FH, even if the input signal does not exceed the “ALC1 Recovery Waiting Counter Reset Level”, the IPGA does not change to 2FH + 2step = 31H, and keeps 30H. Default is “36H”.

DATA (HEX)	GAIN (dB)		STEP	
	MIC Input	LINE Input		
47	+27.5	+12.0	0.5dB	
46	+27.0	+11.5		
45	+26.5	+11.0		
:	:	:		
36	+19.0	+3.5		Default
:	:	:		
2F	+15.5	+0.0		
:	:	:		
10	+0.0	-15.5		
:	:	:		
06	–5.0	–20.5		
05	–5.5	–21.0		
04	–6.0	–21.5		
03	–6.5	–22.0		
02	–7.0	–22.5		
01	–7.5	–23.0		
00	–8.0	–23.5		

Table 31. Setting Reference Value at ALC1 Recovery Operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Lch Input PGA Control	0	IPGAL6	IPGAL5	IPGAL4	IPGAL3	IPGAL2	IPGAL1	IPGAL0
0FH	Rch Input PGA Control	0	IPGAR6	IPGAR5	IPGAR4	IPGAR3	IPGAR2	IPGAR1	IPGAR0
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	0	0

IPGAL6-0: Lch Input Analog PGA (see Table 32)
IPGAR6-0: Rch Input Analog PGA (see Table 32)
Default: "10H" (0dB)
When IPGA gain is changed, IPGAL6-0 and IPGAR6-0 bits should be written while PMMICL, PMMICR, PMIPGL or PMIPGR bit is "1" and ALC1 bit is "0". IPGA gain is reset when PMMICL=PMMICR=PMIPGL =PMIPGR= "0", and then IPGA operation starts from the default value when PMMICL, PMMICR, PMIPGL or PMIPGR bit is changed to "1". When ALC1 bit is changed from "1" to "0", IPGA holds the last gain value set by ALC1 operation. When IPGAL6-0 and IPGAR6-0 bits are read, the register values written by the last write operation are read out regardless the actual gain.

DATA (HEX)	GAIN (dB)		STEP	
	MIC Input	LINE Input		
47	+27.5	+12.0		
46	+27.0	+11.5		
45	+26.5	+11.0		
:	:	:		
36	+19.0	+3.5		
:	:	:		
2F	+15.5	+0.0		
:	:	:		
10	+0.0	-15.5	0.5dB	Default
:	:	:		
06	–5.0	–20.5		
05	–5.5	–21.0		
04	–6.0	–21.5		
03	–6.5	–22.0		
02	–7.0	–22.5		
01	–7.5	–23.0		
00	–8.0	–23.5		

Table 32. Input Gain Setting

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	Lch Digital ATT Control	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
0DH	Rch Digital ATT Control	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATTL/R7-0: Digital ATT Output Control (see Table 18)
Default: "00H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Volume Control	ATTM	ATTS2	ATTS1	ATTS0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

ATTS2-0: Attenuator select of signal from IPGA Lch to Stereo Mixer. (See Table 33)

ATTS2-0	Attenuation	
7H	-6dB	
6H	–9dB	
5H	–12dB	Default
4H	–15dB	
3H	–18dB	
2H	–21dB	
1H	–24dB	
0H	-27dB	

Table 33. Attenuator Table

ATTM: Attenuator control for signal from IPGA Lch to Mono Mixer
0: OFF. 0dB (Default)
1: ON. –4dB

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Power Management 3	0	0	0	INR	INL	PMIPGR	PMMICR	PMADR
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMADR: ADC Rch Block Power Control
0: Power down (Default)
1: Power up

When the PMADL or PMADR bit changes from "0" to "1", the initialization cycle (2081/fs = 47.2ms @44.1kHz) starts. After initializing, digital data of the ADC is output.

PMADL	PMADR	Analog		Digital
		Lch	Rch	L/R
0	0	Power down	Power down	Power down
0	1	Power down	Power up	Power up
1	0	Power up	Power down	Power up
1	1	Power up	Power up	Power up

Table 34. ADC Block Power Control

PMMICR: MIC Power and IPGA Rch Block Power Control
0: Power down (Default)
1: Power up

PMIPGR: IPGA Rch Block Power Control
0: Power down (Default)
1: Power up

IPGA Rch Block is powered up if PMMICR or PMIPGR bit is "1" (see Table 35).

PMMICR	PMIPGR	MIC-Amp	IPGA
0	0	Power down	Power down
0	1	Power down	Power up
1	0	Power up	Power up
1	1	Power up	Power up

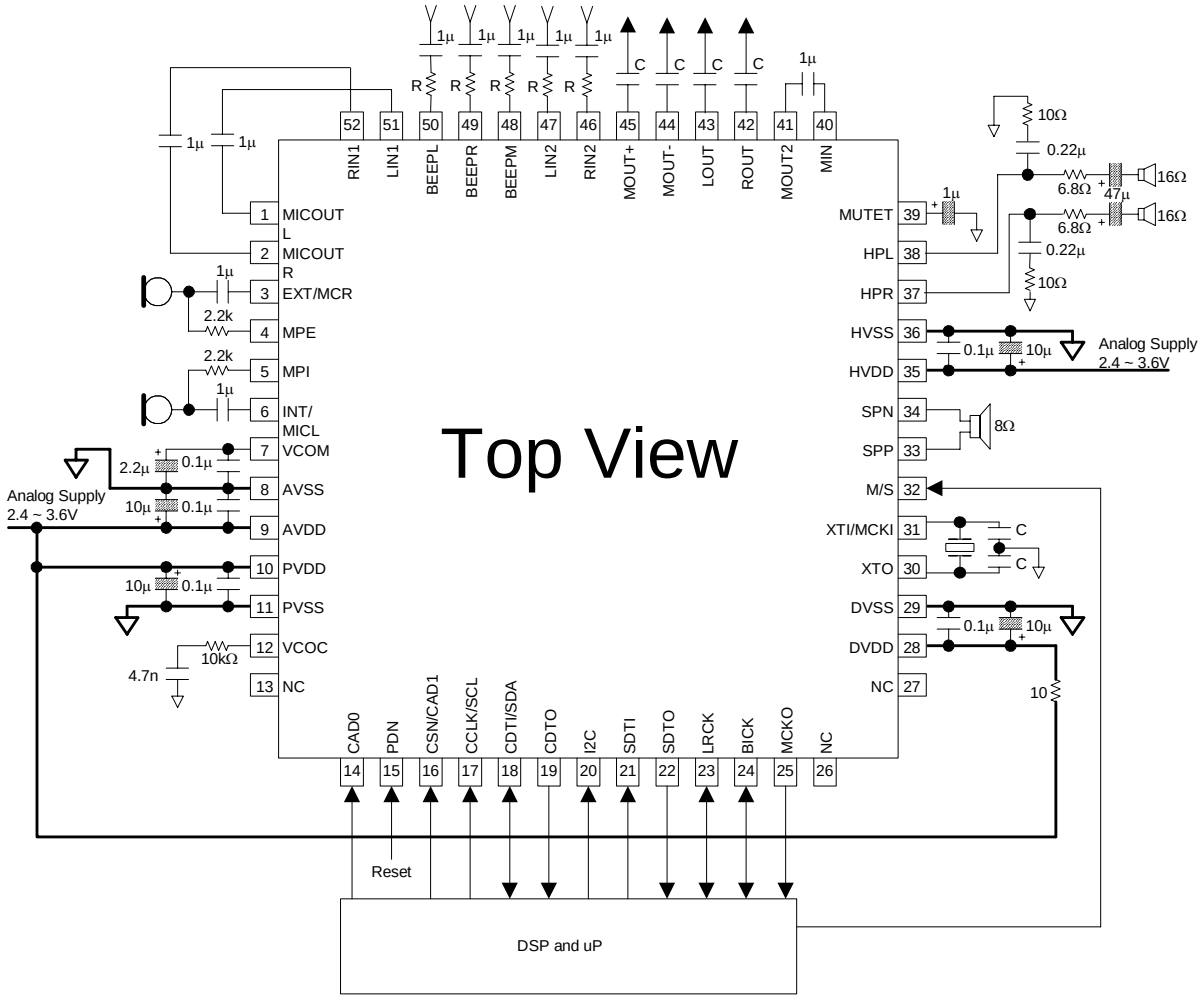
Table 35. MIC-Amp and IPGA Rch Block Power Control

INL: IPGA Lch Input Select
0: MIC input (LIN1: Default)
1: LINE input (LIN2)

INR: IPGA Rch Input Select
0: MIC input (RIN1: Default)
1: LINE input (RIN2)

SYSTEM DESIGN

Figure 47 shows the system connection diagram for the AK4537. An evaluation board [AKD4537] is available which demonstrates the optimum layout, power supply arrangements and measurement results.



Notes:

- AVSS, DVSS, PVSS and HVSS of the AK4537 should be distributed separately from the ground of external controllers.
- Values of R and C in Figure 47 should depend on system.
- All input pins should not be left floating.

Figure 47. Typical Connection Diagram

1. Grounding and Power Supply Decoupling

The AK4537 requires careful attention to power supply and grounding arrangements. AVDD, DVDD, PVDD and HVDD are usually supplied from the system's analog supply. If AVDD, DVDD, PVDD and HVDD are supplied separately, the correct power up sequence should be observed. AVSS, DVSS, PVSS and HVSS of the AK4537 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4537 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4537.

3. Analog Inputs

The Mic, Line and Beep inputs are single-ended. The input signal range scales with nominally at 0.06 x AVDD Vpp for the Mic input and 0.6 x AVDD Vpp for the Beep input, centered around the internal common voltage (0.45 x AVDD). Usually the input signal is AC coupled using a capacitor. The cut-off frequency is $fc = (1/2\pi RC)$. The AK4537 can accept input voltages from AVSS to AVDD.

4. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). Mono output from the MOUT2 pin and Mono Line Output from the MOUT+ and MOUT- pins are centered at 0.45 x AVDD. The Headphone-Amp and Speaker-Amp outputs are centered at HVDD/2.

CONTOROL SEQUENCE

■ Power up

Upon power-up, bring the PDN pin = “L”. Initialize the internal registers to default values after the PDN pin = “H”. Set the following registers to establish the initial condition.

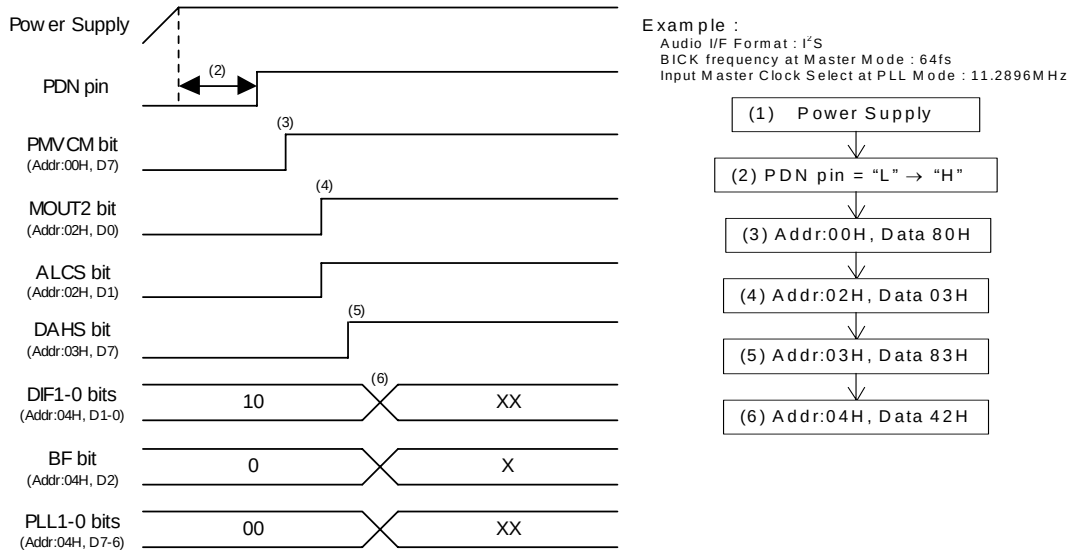


Figure 48. Power Up Sequence

<Example>
(1) Power Supply
(2) PDN pin = “L” → “H”
“L” time of 150ns or more is needed to reset the AK4537.
(3) Power up VCOM : PMVCM bit = “0” → “1”
VCOM should first be powered up before the other block operates.
(4) Set up register 02H : MOUT2 bit = ALCS bit = “0” → “1”
Set the MOUT2 and ALCS bits to “1” when using the Speaker-amp.
(5) Set up register 03H : HPL bit = HPR bit = “1” → “0”, DAHS bit = “0” → “1”
(6) Set up register 04H
- DIF1-0 bits set the audio interface format.
- BF bit sets BICK output frequency in master mode.
- PLL1-0 bits set MCLK input frequency in PLL mode.

■ Clock Set up

When ADC, DAC, ALC1 and ALC2 are used, the clocks (MCLK, BICK and LRCK) must be supplied.

1. When X'tal is used in PLL mode. (Slave mode)

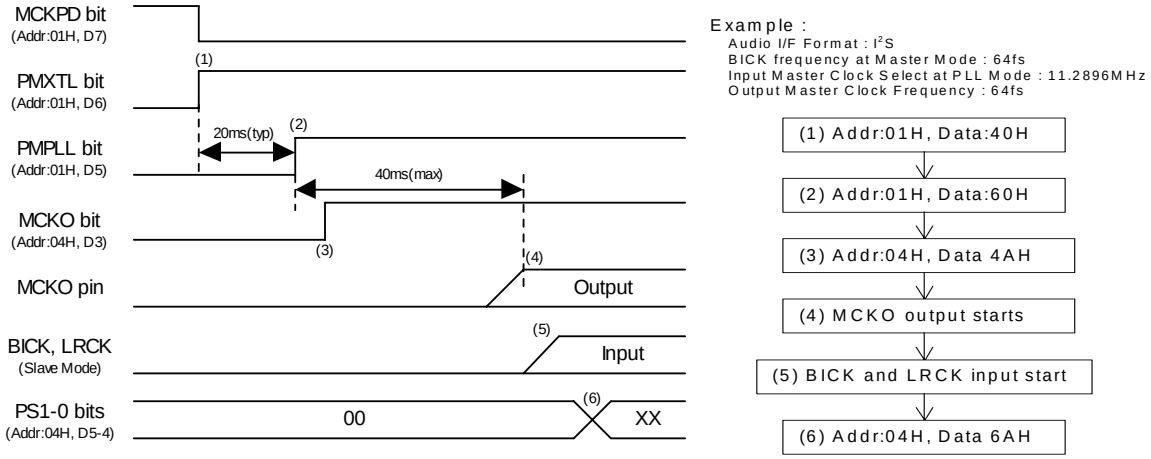


Figure 49. Clock Set Up Sequence(1)

<Example>

(1) Release the pull-down of the XTI pin : MCKPD bit = "1" → "0" and power-up the X'tal oscillator: PMXTL bit = "0" → "1"

(2) Power-up the PLL : PMPLL bit = "0" → "1"
The PLL should be powered-up after the X'tal oscillator becomes stable. It takes X'tal oscillator 20ms(typ) to be stable after PMXTL bit="1". This time depends on X'tal. PLL needs 40ms lock time the PMPLL bit = "0" → "1".

(3) Enable MCKO output : MCKO bit = "0" → "1"

(4) MCKO is output after PLL becomes stable.

(5) Input BICK and LRCK synchronized with the MCKO output.

(6) Set the MCKO output frequency (PS1-0 bits)
If PS1-0 bits are changed before LRCK is input, MCKO is not output. PS1-0 bits should be changed after LRCK is input.

2. When X'tal is used in PLL mode. (Master mode)

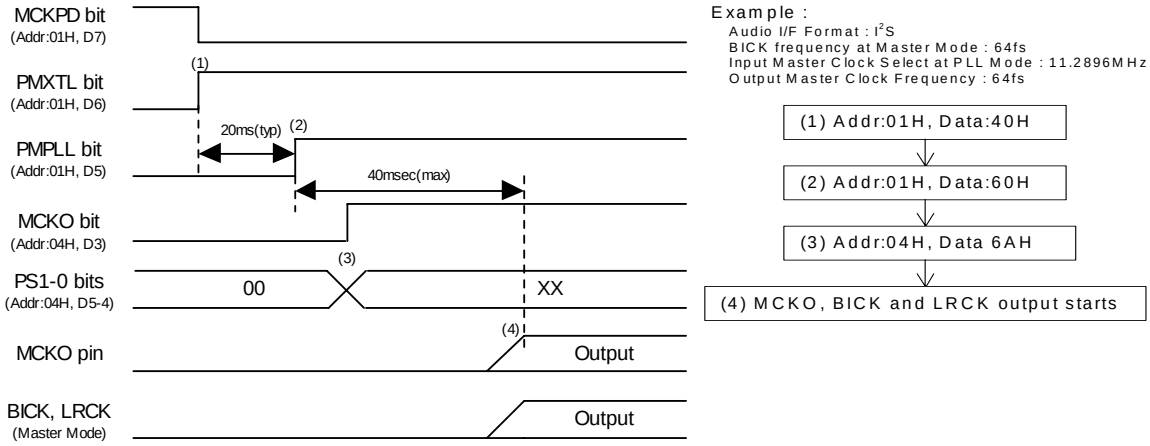


Figure 50. Clock Set Up Sequence(2)

<Example>

(1) Release the pull-down of the XTI pin : MCKPD bit = "1" → "0" and and power-up the X'tal oscillator: PMXTL bit = "0" → "1"

(2) Power-up PLL : PMPLL bit = "0" → "1"

The PLL should be powered-up after the X'tal oscillator becomes stable. It takes X'tal oscillator 20ms(typ) to be stable after PMXTL bit="1". This time depends on X'tal. PLL needs 40ms lock time the PMPLL bit = "0" → "1".

(3) Enable MCKO output : MCKO bit = "0" → "1" and set up MCKO output frequency (PS1-0 bits)

(4) MCKO, BICK and LRCK are output after PLL lock time.

3. When an external clock is used in PLL mode. (Slave mode)

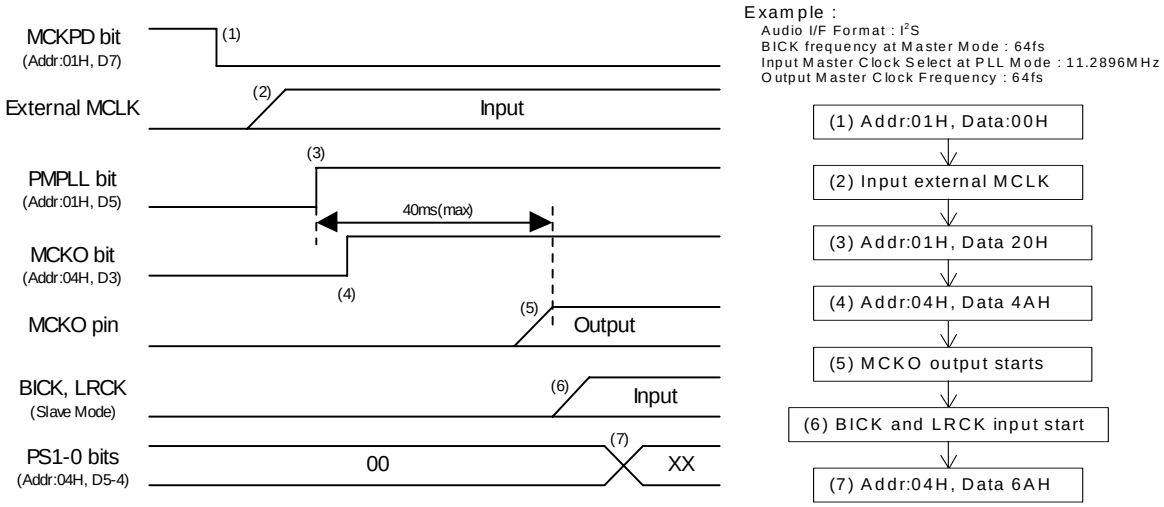


Figure 51. Clock Set Up Sequence(3)

<Example>

(1) Release the pull-down of the XTI pin : MCKPD bit = "1" → "0"
(2) Input an external MCLK
(3) Power-up PLL : PMPLL bit = "0" → "1"
PLL needs 40ms lock time after the PMPLL bit = "0" → "1".
(4) Enable MCKO output : MCKO bit = "0" → "1"
(5) MCKO is output after PLL lock time.
(6) Input BICK and LRCK that synchronized in the MCKO output.
(7) Set up MCKO output frequency (PS1-0 bits)
If PS1-0 bits are changed before LRCK is input, MCKO is not output. PS1-0 bits should be changed after LRCK is input.

4. When an external clock is used in PLL mode. (Master mode)

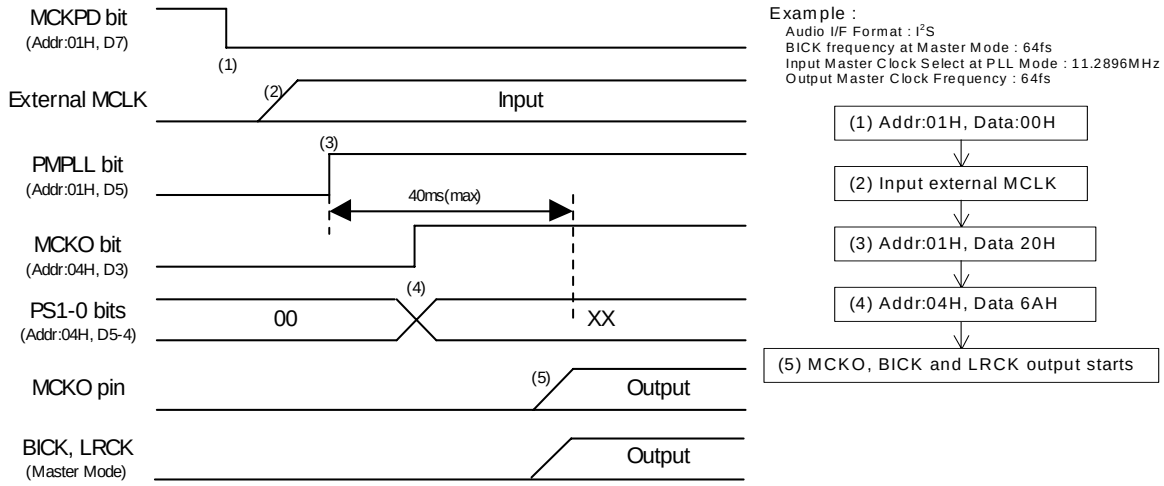


Figure 52. Clock Set Up Sequence(4)

<Example>
(1) Release the pull-down of the XTI pin : MCKPD bit = "1" → "0"
(2) Input an external MCLK
(3) Power-up PLL : PMPLL bit = "0" → "1"
PLL needs 40ms lock time after the PMPLL bit = "0" → "1".
(4) Enable MCKO output : MCKO bit = "0" → "1" and set up MCKO output frequency (PS1-0 bits)
(5) MCKO, BICK and LRCK are output after PLL lock time.

5. External clock mode

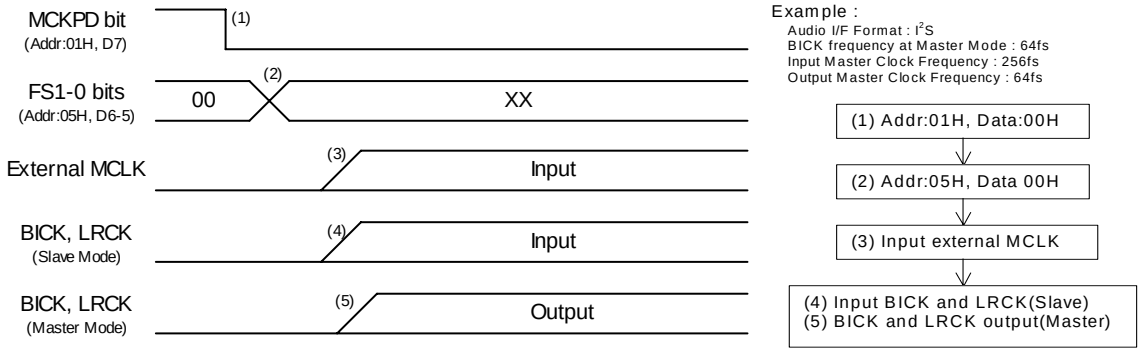


Figure 53. Clock Set Up Sequence(5)

<Example>
(1) Release the pull-down of the XTI pin : MCKPD bit = "1" → "0"
(2) Set up MCLK frequency (FS1-0 bits)
(3) Input an external MCLK
(4) In slave mode, input MCLK, BICK and LRCK.
(5) In master mode, while MCLK is input, BICK and LRCK are output.

■ MIC Input Recording (Mono)

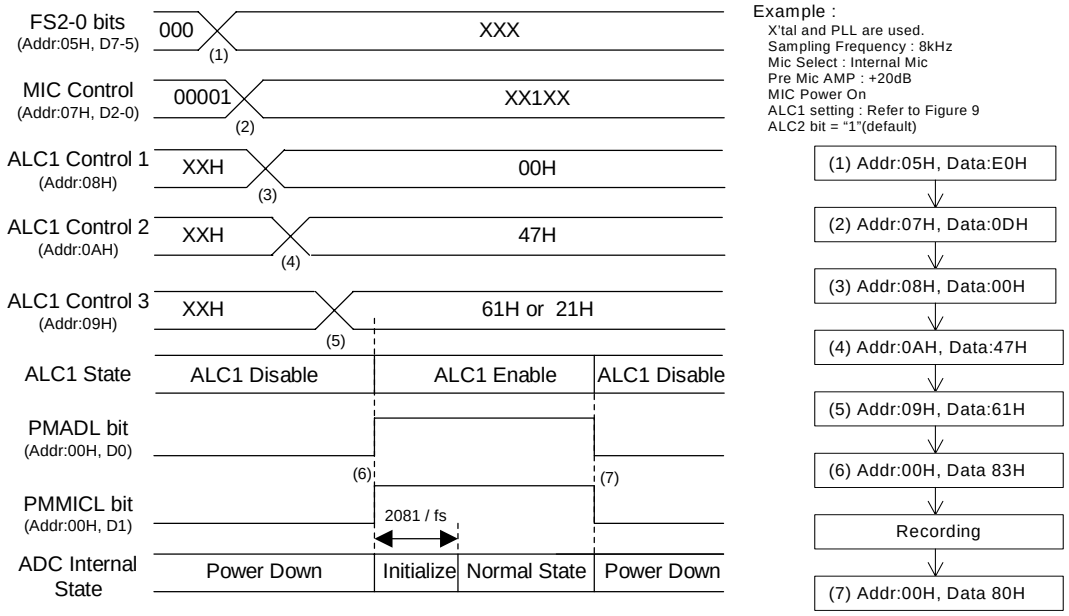


Figure 54. MIC Input Recording Sequence

<Example>

This sequence is an example of ALC1 setting at fs=8kHz. If the parameter of the ALC1 is changed, please refer to "Figure 22. Registers set-up sequence at ALC1 operation"

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS2-0 bits). When the AK4536 is PLL mode, MIC and ADC should be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up MIC input (Addr: 07H)
(3) Set up Timer Select for ALC1 (Addr: 08H)
(4) Set up REF value for ALC1 (Addr: 0AH)
(5) Set up LMTH, RATT, LMAT1-0, ALC1 bits (Addr: 09H)
(6) Power Up MIC and ADC: PMMICL bit = PMADL bit = "0" → "1"
(In case of stereo mic, PMMICR and PMADR bits also should be set to "1".)
The initialization cycle time of ADC is 2081/fs=47.2ms@fs=44.1kHz.
After the ALC1 bit is set to "1" and MIC block is powered-up, the ALC1 operation starts from IPGA initial value (0dB).
(7) Power Down MIC and ADC: PMMIC bit = PMADC bit = "1" → "0"
(In case of stereo mic, PMMICR and PMADR bits also should be set to "0".)
When the registers for the ALC1 operation are not changed, ALC1 bit may be keeping "1". The ALC1 operation is disabled because the MIC block is powered-down. If the registers for the ALC1 operation are also changed when the sampling frequency is changed, it should be done after the AK4537 goes to the manual mode (ALC1 bit = "0") or MIC block is powered-down (PMMICL bit = "0"). IPGA gain is reset when PMMICL =PMMICR=PMIPGL=PMIPGR= "0", and then IPGA operation starts from the default value when PMMICL, PMMICR, PMIPGL or PMIPGR bit is changed to "1".

■ Headphone-amp Output

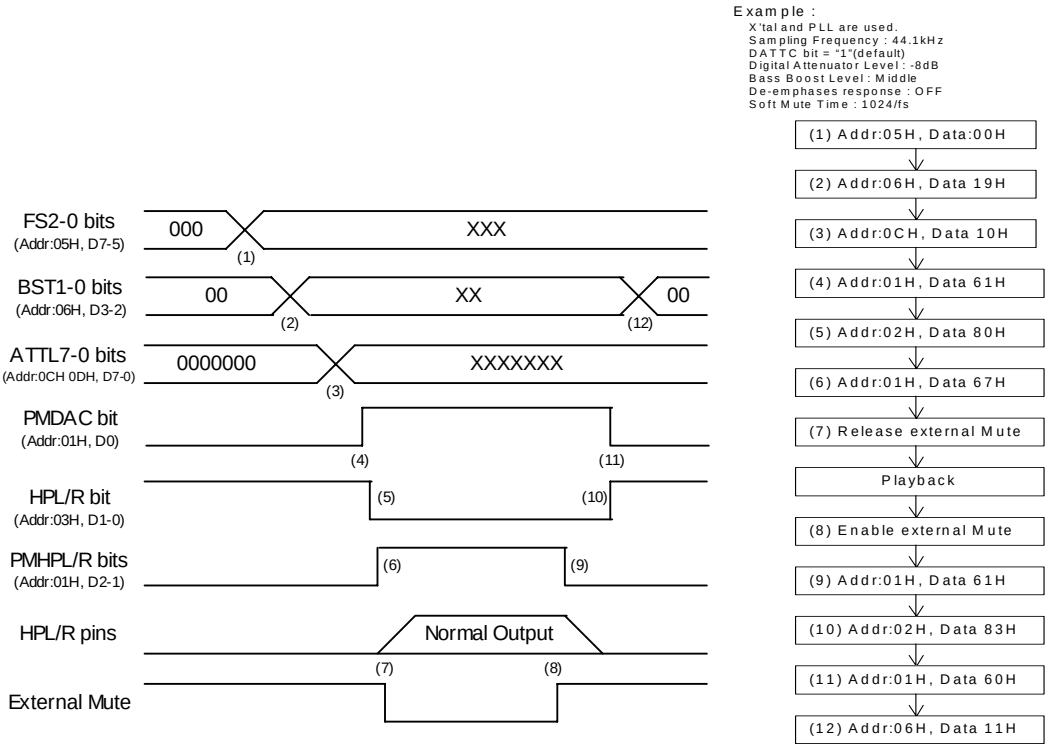


Figure 55. Headphone-Amp Output Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS2-0 bits) if PLL mode is used.

(2) Set up the low frequency boost level(BST1-0 bits)

(3) Set up the digital volume(Addr : 0CH and 0DH)

At DATTC bit = "1"(default), ATTL7-0 bits of Address 0CH control both Lch and Rch attenuation level.

(4) Power up DAC : PMDAC bit = "0" → "1"

(5) Power up headphone-amp : HPL bit = HPR bit = "1" → "0"

Output voltage of headphone-amp is still HVSS.

(6) Rise up the common voltage of headphone-amp : PMHPL bit = PMHPR bit = "0" → "1"

The rising time after power up Headphone-amp depends on the capacitor value connected with the MUTET pin. When this capacitor value is 1.0μF, the time constant is τ_r = 100ms(typ), 250ms(max).

(7) Release the external mute.

(8) Enable the external mute.

(9) Fall down the common voltage of headphone-amp : PMHPL bit = PMHPR bit = "1" → "0"

The rising time after power up Headphone-amp depends on the capacitor value connected with the MUTET pin. When this capacitor value is 1.0μF, the time constant is τ_f = 100ms(typ), 250ms(max).

If the power supply is powered off or Headphone-Amp is powered-down before the common voltage goes to GND, some POP noise occurs. It takes 2times of τ_f that the common voltage goes to GND.

(10) Power down headphone-amp : HPL bit = HPR bit = "0" → "1"

(11) Power down DAC : PMDAC bit = "1" → "0"

(12) Off the low frequency boost level (BST1-0 bits = "00")

■ Speaker-amp Output

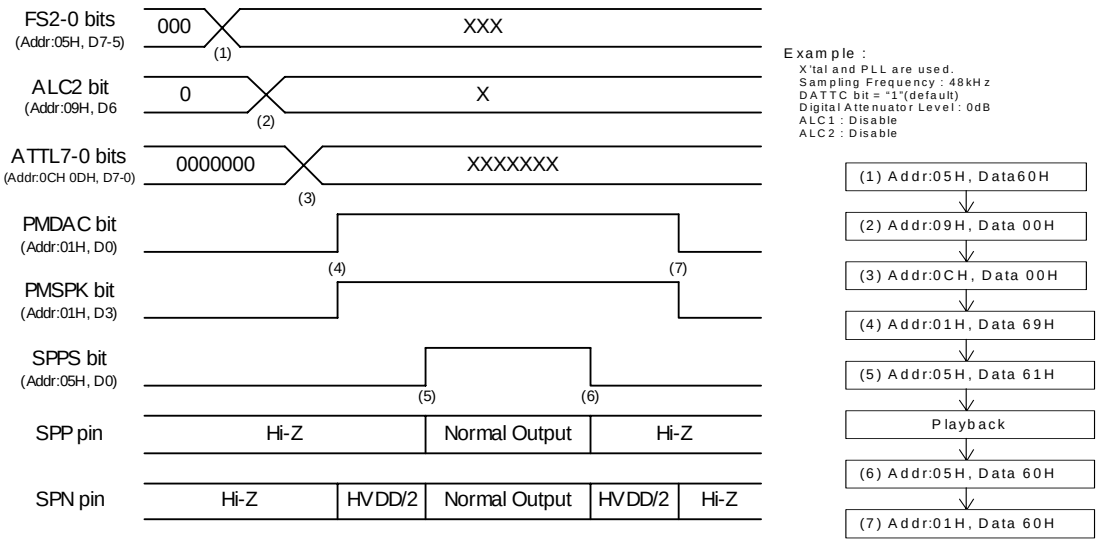


Figure 56. Speaker-Amp Output Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS2-0 bits) if PLL mode is used.

(2) Set up the ALC2 Enable/Disable(ALC2 bit)

(3) Set up the digital volume(Addr : 0CH and 0DH)

At DATTC bit = "1"(default), ATTL7-0 bits of Address 0CH control both Lch and Rch attenuation level.

(4) Power up of DAC and Speaker-amp : PMDAC bit = PMSPK bit = "0" → "1"

The initializing time of Speaker-amp is 2048/fs=46.4ms@fs=44.1kHz.

(5) Exit the power-save-mode of Speaker-amp : SPPS bit = "0" → "1"

(6) Enter the power-save-mode of Speaker-amp : SPPS bit = "1" → "0"

(7) Power down DAC and Speaker-amp : PMDAC bit = PMSPK bit = "1" → "0"

■ Stop of Clock

MCLK can be stopped when PMMIC=PMADC=PMDAC=PMSPK= “0”.

1. When X’tal is used in PLL mode

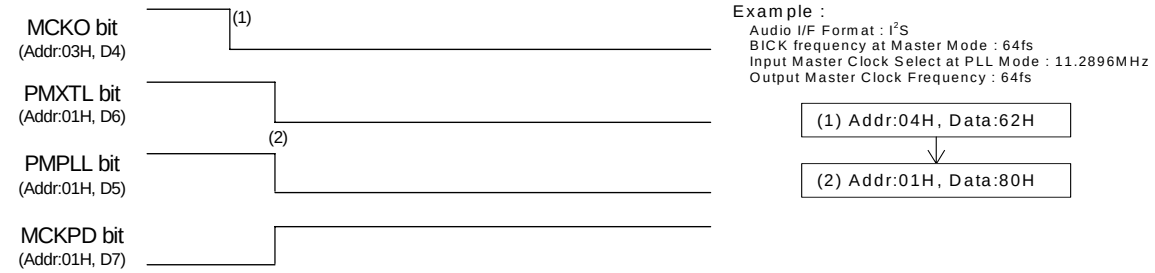


Figure 57. Stop of Clock Sequence(1)

<Example>
(1) Disable MCKO output : MCKO bit = “1” → “0”
(2) Power down X’tal and PLL, Pull down the XTI pin :
PMXTL bit = PMPLL bit = “1” → “0”, MCKPD = “0” → “1”

2. When an external clock is used in PLL mode

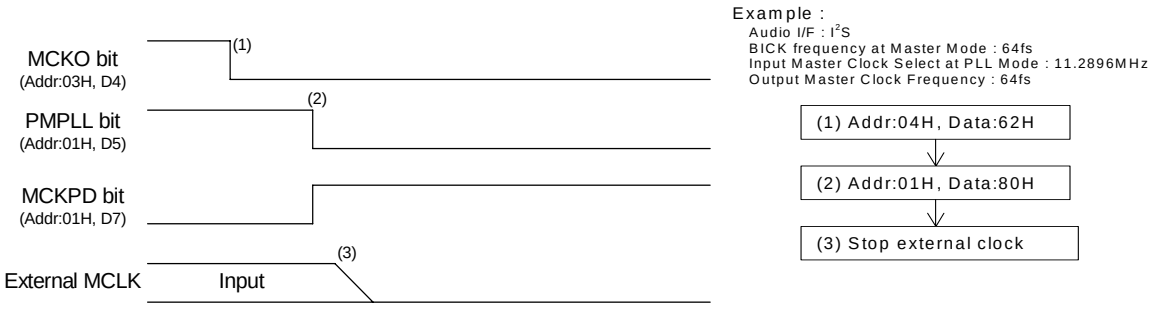


Figure 58. Stop of Clock Sequence(2)

<Example>
(1) Stop MCKO output : MCKO bit = “1” → “0”
(2) Power down PLL, Pull down the XTI pin : PMPLL bit = “1” → “0”, MCKPD = “0” → “1”
When the external MCLK becomes Hi-Z or the external MCLK is input by AC couple, MCKI pin should be pulled down.
(3) Stop an external MCLK

3. External clock mode

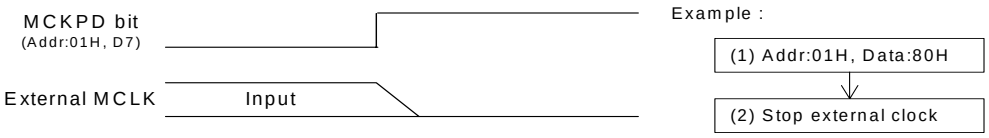


Figure 59. Stop of Clock Sequence(3)

<Example>

(1) Pull down the XTI pin : MCKPD = "0" → "1"
When the external MCLK becomes Hi-Z or the external MCLK is input by AC couple, MCKI pin should be pulled down.

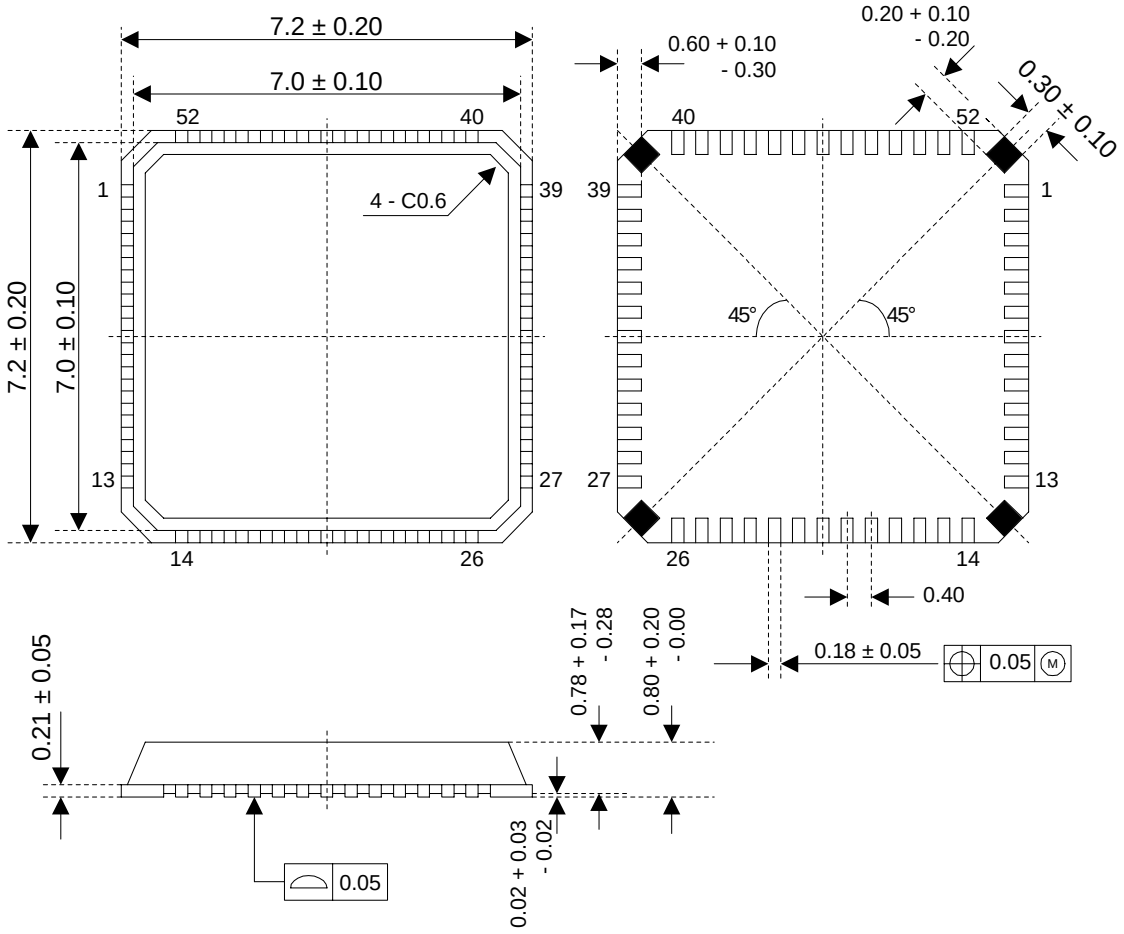
(2) Stop an external MCLK

■ Power down

Power down VCOM(PMVCM= "1" → "0") after all blocks except VCOM are powered down and MCLK stops. The AK4537 is also powered-down by PDN pin = "L". When PDN pin = "L", the registers are initialized.

PACKAGE

52pin QFN (Unit: mm)

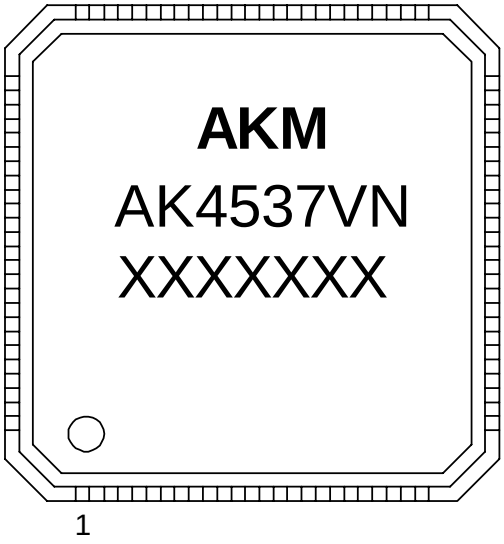


Note) The part of black at four corners on reverse side must not be soldered and must be open.

■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



XXXXXXX : Date code identifier (7 digits)

Revision History

Date (YY/MM/DD)	Revision	Reason	Page	Contents
03/02/03	00	First Edition		
03/03/24	01	Spec change:	33	Headphone amp oscillation prevention circuit 0.22μF+10Ω → 0.22μF±20% capacitor and 10Ω±20% resistor
		Error correct:	5-6	Pin/Function NC pin: "No internal bonding." → "This pin should be left floating."
			22	System Clock The following caution is also added to EXT mode: "If PS1-0 bits are changed before LRCK is input, MCKO is not output. PS1-0 bits should be changed after LRCK is input in slave mode."
			27/21	MIC-ALC Operation (ALC1 Recovery Operation) "If both Lch and Rch input signals are lower than the "ALC1 Recovery Waiting Counter Reset Level", the ALC1 recovery operation starts." → "If Lch or Rch input signals are lower than the "ALC1 Recovery Waiting Counter Reset Level", the ALC1 recovery operation starts."
			56	Register Definitions ATTS2-0 bit: "0(OFF), 1(ON)" is removed.
			59	Analog Input "centered around the internal common voltage (approx. AVDD/2)" → "centered around the internal common voltage (0.45 x AVDD)"
			59	Analog Output "Mono output from the MOUT2 pin and Mono Line Output from the MOUT+ and MOUT- pins are centered at AVDD/2." → "Mono output from the MOUT2 pin and Mono Line Output from the MOUT+ and MOUT- pins are centered at 0.45 x AVDD."
03/05/23	02	Error correct:	21	System Clock "If the sampling frequency is changed and the PLL goes to unlock state when the DAC is operated(PMDAC bit="1"), the DAC data should be soft-muted or "0". In case of the ADC(PMADL bit = "1" or PMADR bit = "1"), the ADC data acquired during the frequency change may be erroneous and therefore should not be used." is deleted.

Date (YY/MM/DD)	Revision	Reason	Page	Contents
03/05/23	02	Explanation addition:	27	Manual Mode "When writing to the IPGAL6-0 and IPGAR6-0 bits continually, the control register should be written by an interval more than zero crossing timeout (the write operation interval between IPGAL6-0 and IPGAR6-0 bits also should be more than zero crossing timeout). When IPGAC bit is "0", the write operation interval from IPGAL6-0 bits to IPGAR6-0 bits is no care. Therefore, the auto increment function of I^2C bus is available at IPGAC = "0"." is added.
			28	Example of ALC1 Operation "IPGA gain at ALC1 operation start can be changed from the default value of IPGAL6-0 bits while PMMICL, PMMICR, PMIPGL or PMIPGR bit is "1" and ALC1 bit is "0". When ALC1 bit is changed from "1" to "0", IPGA holds the last gain value set by ALC1 operation." is added.
			43	Register Definitions (PMBPM bit) "Even if PMBPM= "0", the path is still connected between BEEPM and HP-Amp. BPMHP bit should be set to "0" to disconnect this path." → "Even if PMBPM= "0", the path is still connected between BEEPM and HP/SPK-Amp. BPMHP and BPMSP bits should be set to "0" to disconnect these paths, respectively."
			43	Register Definitions (PMBPS bit) "Even if PMBPS= "0", the path is still connected between BEEPL/R and HP-Amp. BPSHP bit should be set to "0" to disconnect this path." → "Even if PMBPS= "0", the path is still connected between BEEPL/R and HP/SPK-Amp. BPSHP and BPSSP bits should be set to "0" to disconnect these paths, respectively."
			44	Register Definitions (Addr=00H) "IPGA gain is reset when PMMICL=PMMICR=PMIPGL=PMIPGR= "0"." is added. "The paths from BEEP to HP-Amp and SPK-Amp can operate without these clocks." is added.

Date (YY/MM/DD)	Revision	Reason	Page	Contents
03/05/23	02	Explanation addition:	55	Register Definitions (IPGAL6-0 and IPGAR6-0 bits) "When IPGA gain is changed, IPGAL6-0 and IPGAR6-0 bits should be written while PMMICL, PMMICR, PMIPGL or PMIPGR bit is "1" and ALC1 bit is "0". IPGA gain is reset when PMMICL=PMMICR=PMIPGL =PMIPGR= "0", and then IPGA operation starts from the default value when PMMICL, PMMICR, PMIPGL or PMIPGR bit is changed to "1". When ALC1 bit is changed from "1" to "0", IPGA holds the last gain value set by ALC1 operation. When IPGAL6-0 and IPGAR6-0 bits are read, the register values written by the last write operation are read out regardless the actual gain." is added.
			65	MIC Input Recording Sequence Power Up MIC and ADC: "In case of stereo mic, PMMICR and PMADR bits also should be set to "1"." is added. Power Down MIC and ADC: "In case of stereo mic, PMMICR and PMADR bits also should be set to "0"." is added. "IPGA gain is reset when PMMICL =PMMICR=PMIPGL=PMIPGR= "0", and then IPGA operation starts from the default value when PMMICL, PMMICR, PMIPGL or PMIPGR bit is changed to "1"." is added.
		Explanation change:	28	Example of ALC1 Operation Table 15: IPGAL6-0, IPGAR6-0=47H(+27.5dB) → 10H(0dB) Figure 22: Addr=0BH&0FH: Data=47H → 10H
			65	MIC Input Recording Sequence ALC1 Control 3 (Addr: 0BH) Set up IPGA value for ALC1: deleted. "After the ALC1 bit is set to "1" and MIC block is powered-up, the ALC1 operation starts." → "After the ALC1 bit is set to "1" and MIC block is powered-up, the ALC1 operation starts from IPGA initial value (0dB)."
04/11/26	03	Explanation addition:	24	Audio Interface Format [When LOOP bit = "1", audio interface format of SDTO is fixed to I^2S regardless of DIF1-0 bits setting.] is added.
			32	Headphone Output Rise/fall time constant: τ = 250ms(max). Time until the common goes to HVSS when PMHPL/R bits = "1" → "0": 500ms(max).
			66	Headphone Output Sequence (6), (9) Rise/fall time constant: τ = 250ms(max)

Date (YY/MM/DD)	Revision	Reason	Page	Contents
05/04/27	04	Explanation change:	1	Features SPK-AMP Output Power: 300mW → 400mW
			34-35	SPK-AMP "Connection Example for 400mW output" is added.

IMPORTANT NOTICE

- These products and their specifications are subject to change without notice. Before considering any use or application, consult the Asahi Kasei Microsystems Co., Ltd. (AKM) sales office or authorized distributor concerning their current status.
- AKM assumes no liability for infringement of any patent, intellectual property, or other right in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components in any safety, life support, or other hazard related device or system, and AKM assumes no responsibility relating to any such use, except with the express written consent of the Representative Director of AKM. As used here:
  a. A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  b. A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.