AK4569

20-Bit Stereo CODEC with IPGA & HP-AMP

GENERAL DESCRIPTION

The AK4569 is a 20bit CODEC with built-in Input PGA and Headphone Amplifier. The AK4569 includes a microphone/line input selector and an ALC circuit for input, and a Mono line output buffer, analog volume controls and stereo headphone amplifier for output. The AK4569 also features an analog mixing circuit that allows easy interfacing in mobile phone and portable communication designs. The integrated headphone amplifier features "pop-free" power-on/off, a mute control and delivers 8.7mW of power into 16Ω load via 6.8Ω series resistor. The AK4569 is housed in a 28pin QFN package, making it suitable for portable applications.

FEATURE

- ☐ **2ch 20bit ADC**
  - **S/N: 89dB**
  - **Single-ended input**
  - **2 stereo inputs selector**
  - **Analog input PGA: +32dB ~ –19dB, Mute, 0.5dB step (MIC input)**
    +20dB ~ –31dB, Mute, 0.5dB step (LINE input)
  - **Digital HPF for DC-offset cancellation**
  - **I/F format: 20bit MSB justified, I^2S**
- ☐ **2ch 20bit DAC**
  - **I/F Format: I^2S, 20bit MSB justified, 20bit/16bit LSB justified**
  - **Digital ATT: 0dB ~ –127dB, Mute, 0.5dB step (soft transition)**
  - **Soft mute**
  - **Digital De-emphasis Filter: 32kHz, 44.1kHz and 48kHz**
  - **Bass Boost Function**
- ☐ **Sampling Rate: 8kHz ~ 48kHz**
- ☐ **System clock: 256fs/384fs/512fs**
  - **Input level: CMOS or 1Vpp Analog Input**
- ☐ **Analog Mixing Circuit**
- ☐ **Mono Lineout**
  - **Analog volume: 0dB ~ –30dB, Mute, 2dB step**
- ☐ **Headphone Amplifier**
  - **Output Power: 8.7mW x 2ch @16Ω load & 6.8Ω series resistor**
  - **S/N: 90dB**
- ☐ **µP Interface: 3-wire**
- ☐ **Power management**
- ☐ **Power supply: 2.7V ~ 3.6V**
- ☐ **Power dissipation: 15mA**
- ☐ **Ta: –40 ~ 85°C**
- ☐ **Small Package: 28pin QFN (5.2mm x 5.2mm, 0.5mm pitch)**

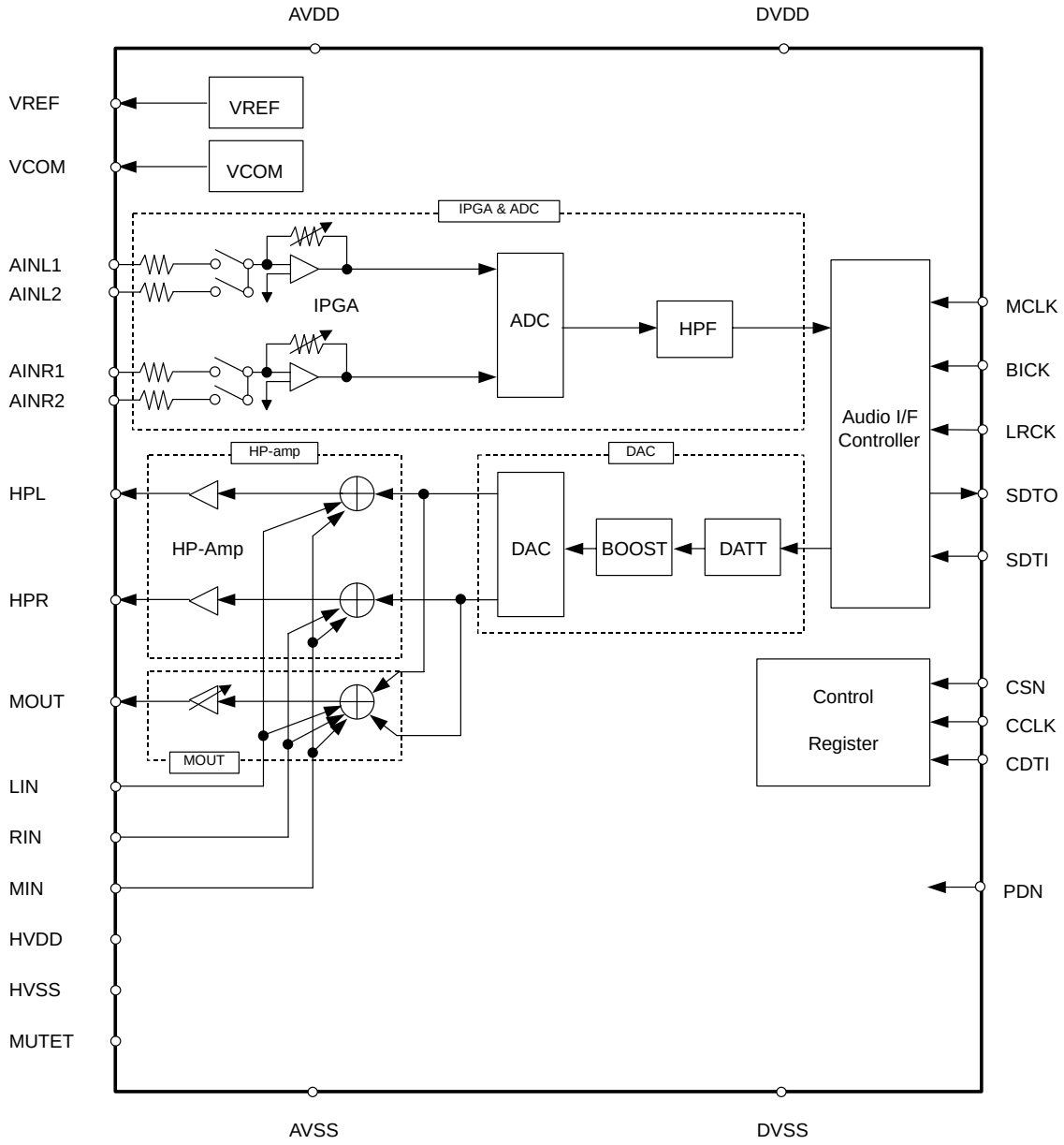
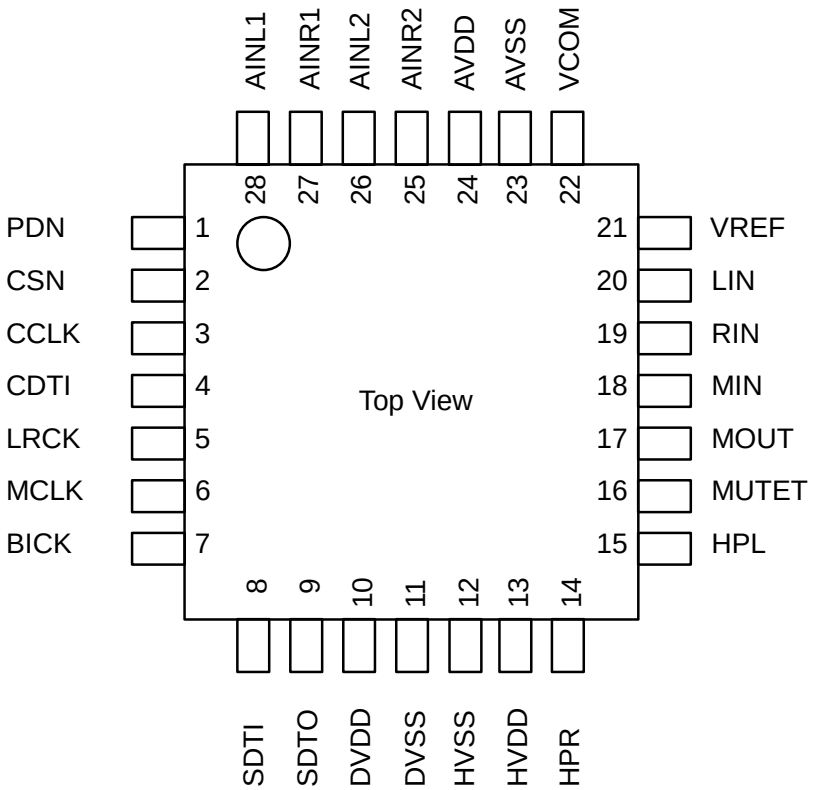


Figure 1. Block diagram

■ Ordering Guide

AK4569VN	–40 ~ +85°C	28pin QFN (0.5mm pitch)
AKD4569	Evaluation board for AK4569	

■ Pin Layout



■ Comparison Table between AK4566 and AK4569

Function	AK4566	AK4569
DAC Digital Filter		
Stopband Attenuation (min)	43dB	59dB
Passband Ripple (max)	±0.06dB	±0.01dB
Frequency Response including Analog Filter (0 ~ 20.0kHz)	±0.5dB	±1.0dB
The condition to stop the external clocks.	PDN pin = “L”	PDN pin = “L” or PMADC=PMDAC bits = “0”

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	PDN	I	Power-down Pin When "L", the AK4569 is in power-down mode and is held in reset. The AK4569 should always be reset upon power-up.
2	CSN	I	Control Data Chip Select Pin
3	CCLK	I	Control Clock Input Pin
4	CDTI	I	Control Data Input Pin
5	LRCK	I	L/R Clock Pin This clock determines which audio channel is currently being output on SDTO pin and input on SDTI pin.
6	MCLK	I	Master Clock Input Pin
7	BICK	I	Serial Bit Clock Pin This clock is used to latch audio data.
8	SDTI	I	Audio Data Input Pin
9	SDTO	O	Audio Data Output Pin SDTO pin goes to DVSS when PDN pin is "L".
10	DVDD	-	Digital Power Supply Pin
11	DVSS	-	Digital Ground Pin
12	HVSS	-	Ground Pin for Headphone Amplifier
13	HVDD	-	Power Supply Pin for Headphone Amplifier
14	HPR	O	Rch Headphone Amplifier Output Pin HPR pin goes to HVSS when PDN pin is "L".
15	HPL	O	Lch Headphone Amplifier Output Pin HPL pin goes to HVSS when PDN pin is "L".
16	MUTET	O	Mute Time Constant Control Pin A capacitor for mute time constant should be connected between MUTET pin and HVSS pin. MUTET pin goes to HVSS when PDN pin is "L".
17	MOUT	O	Mono Analog Output Pin MOUT pin goes to Hi-Z when PDN pin is "L".
18	MIN	I	Mono Analog Input Pin
19	RIN	I	Rch Analog Input Pin
20	LIN	I	Lch Analog Input Pin
21	VREF	O	Reference Voltage Output Pin, 2.1V (typ, respect to AVSS) Normally connected to AVSS pin with 0.1μF ceramic capacitor in parallel with a 4.7μF electrolytic capacitor. VREF pin goes to AVSS when PDN pin is "L".
22	VCOM	O	Common Voltage Output Pin, 1.25V (typ, respect to AVSS) Normally connected to AVSS pin with 0.1μF ceramic capacitor in parallel with a 2.2μF electrolytic capacitor. VCOM pin goes to AVSS when PDN pin is "L".
23	AVSS	-	Analog Ground Pin
24	AVDD	-	Analog Power Supply Pin
25	AINR2	I	Rch Analog Input 2 Pin for ADC (MIC Input)
26	AINL2	I	Lch Analog Input 2 Pin for ADC (MIC Input)
27	AINR1	I	Rch Analog Input 1 Pin for ADC (LINE Input)
28	AINL1	I	Lch Analog Input 1 Pin for ADC (LINE Input)

Note: No digital input pins must be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	HPR, HPL, MOUT, AINR2, AINL2, AINR1, AINL1	These pins should be open.
Digital	SDTO	This pin should be open.
	SDTI	This pin should be connected to DVSS.

ABSOLUATE MAXIMUM RATING

(AVSS, DVSS, HVSS=0V; Note 1)

Parameter			Symbol	min	max	Units
Power Supplies	Analog		AVDD	–0.3	4.6	V
	Digital		DVDD	–0.3	4.6	V
	HP-AMP		HVDD	–0.3	4.6	V
	|AVSS – HVSS|	(Note 2)	ΔGND1	-	0.3	V
	|AVSS – DVSS|	(Note 2)	ΔGND2	-	0.3	V
Input Current (any pins except for supplies)			IIN	-	±10	mA
Analog Input Voltage		(Note 3)	VINA	–0.3	(AVDD+0.3) or 4.6	V
Digital Input Voltage		(Note 4)	VIND	–0.3	(DVDD+0.3) or 4.6	V
Ambient Temperature			Ta	–40	85	°C
Storage Temperature			Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS, DVSS and HVSS must be connected to the same analog ground plane.
Note 3. MIN, RIN, LIN, AINR2, AINL2, AINR1, AINL1 pins.
Max is smaller value between (AVDD+0.3) and 4.6V.
Note 4. PDN, CSN, CCLK, CDTI, LRCK, MCLK, BICK, SDTI pins.
Max is smaller value between (DVDD+0.3) and 4.6V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(AVSS, DVSS, HVSS=0V; Note 1)

Parameter			Symbol	min	typ	max	Units
Power Supplies	Analog		AVDD	2.5	3.0	3.6	V
	Digital	(Note 5)	DVDD	2.5 or (AVDD–0.3)	3.0	3.6 or (AVDD+0.3)	V
	HP-AMP		HVDD	2.5	3.0	3.6	V

Note 1. All voltages with respect to ground.
Note 5. Min is larger value between 2.5V and (AVDD–0.3). Max is smaller value between 3.6V and (AVDD+0.3).

* AKM assumes no responsibility for usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=HVDD=3.0V, AVSS =DVSS=HVSS=0V; fs=44.1kHz; BOOST OFF; Signal Frequency =1kHz; Measurement band width=20Hz ~ 20kHz; unless otherwise specified)

Parameter	min	Typ	max	Units
ADC Resolution			20	bit
IPGA Characteristics: (AINL1, AINR1 pins) (LINE IN)				
Input Voltage	1.35	1.5	1.65	Vpp
Input Resistance	25	50	75	kΩ
Step Size	0.1	0.5	0.9	dB
Gain Control Range	–31		+20	dB
IPGA Characteristics: (AINL2, AINR2 pins) (MIC IN)				
Input Voltage	1.35	1.5	1.65	Vpp
Input Resistance	6	12.5	19	kΩ
Step Size	0.1	0.5	0.9	dB
Gain Control Range	–19		+32	dB
ADC Characteristics: (Note 6)				
S/(N+D) (–1dB Input)	74	84		dB
D-Range (–60dB Input, A-weighted))	82	89		dB
S/N (A-weighted)	82	89		dB
Interchannel Isolation	80	100		dB
Interchannel Gain Mismatch		0.2	0.5	dB
Power Supply Rejection (Note 11)	-	50	-	dB
DAC Resolution			20	bit
Headphone-Amp: (HPL/HPR pins) (Note 7) Load impedance is a serial connection with R_L =22.8Ω and C_L=100μF.				
S/(N+D) (0dBFS Output)	50	70		dB
D-Range (–60dBFS Output, A-weighted)	82	90		dB
S/N (A-weighted)	82	90		dB
Interchannel Isolation	70	90		dB
Interchannel Gain Mismatch		0.2	0.5	dB
Load Resistance (Note 8)	20			Ω
Load Capacitance (C1 in Figure 2) (C2 in Figure 2) (Note 9)			30 300	pF pF
Output Voltage	1.35	1.5	1.65	Vpp
Power Supply Rejection (Note 11)	-	50	-	dB
Mono Output: (MOUT pin) (Note 10)				
S/(N+D) (0dBFS Output)	70	84		dB
S/N (A-weighted)	82	90		dB
Load Resistance (Note 8)	10			kΩ
Load Capacitance			30	pF
Output Voltage	1.35	1.5	1.65	Vpp
Power Supply Rejection (Note 11)	-	50	-	dB
Output Volume: (MOUT pin)				
Step Size	1	2	3	dB
Gain Control Range	–30		0	dB

Note 6. The signal inputs are AINL1/AINR1 or AINL2/AINR2. The value of the IPGA is set to 0dB. On-chip HPF cancels the IPGA and ADC offsets.

Note 7. DACL=DACR= “1”, MINL=MINR=LIN=RIN= “0”, and ATTL=ATTR=0dB.

Note 8. AC Load

Note 9. A resistor greater than 6.8Ω is inserted in series.

Note 10. DACM= “1”, LINM=RINM=MINM= “0”, ATTL=ATTR=ATTM=0dB, and common mode signal is input to L/Rch of DAC.

Note 11. PSR is applied to AVDD, DVDD and HVDD with 1kHz, 50mVpp.

Parameter		min	typ	max	Units
Analog Input: (LIN/RIN/MIN pins)					
Input Resistance		25	50	75	kΩ
Gain					
LIN/RIN→MOUT		–7	–6	–5	dB
MIN→MOUT, LIN/MIN→HPL, RIN/MIN→HPR		–1	0	+1	dB
Power Supplies					
Power Supply Current					
Normal Operation (PDN= “H”)					
AVDD + DVDD + HVDD	(Note 12)		15	24	mA
Power-Down Mode (PDN= “L”)					
AVDD + DVDD + HVDD	(Note 13)		1	100	μA

Note 12. All blocks are powered-up (PMVCM=PMADC=PMDAC=PMHPL=PMHPR=PMMO= “1”), and HP-Amp output is off. AVDD=9mA(typ), DVDD=3mA(typ), HVDD=3mA(typ).
9mA(typ) at playback only (PMVCM=PMDAC=PMHPL=PMHPR=PMMO= “1”, PMADC= “0”).
AVDD=4mA(typ), DVDD=2mA(typ), HVDD=3mA(typ).

Note 13. All digital input pins including clock pins (MCLK, BICK and LRCK) are held at DVDD or DVSS. PDN pin is held at DVSS.

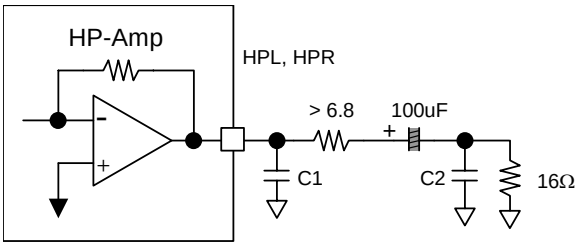


Figure 2. Headphone amp output circuit

FILTER CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, HVDD=2.5 ~ 3.6V; fs=44.1kHz; DEM=OFF; BOOST=OFF)

Parameter			Symbol	min	typ	max	Units
ADC Digital Filter (LPF):							
Passband (Note 15)		±0.1dB	PB	0		17.4	kHz
		–1.0dB		-	20.0	-	kHz
		–3.0dB		-	21.1	-	kHz
Stopband (Note 15)			SB	25.7			kHz
Passband Ripple			PR			±0.1	dB
Stopband Attenuation			SA	65			dB
Group Delay (Note 16)			GD	-	17.0	-	1/fs
Group Delay Distortion			ΔGD		0		μs
ADC Digital Filter (HPF):							
Frequency Response (Note 15)		–3dB	FR		3.4		Hz
		–0.5dB			10		Hz
		–0.1dB			22		Hz
DAC Digital Filter: (Note 14)							
Passband (Note 15)		±0.1dB	PB	0		19.6	kHz
		–0.7dB		-	20.0	-	kHz
		–6.0dB		-	22.05	-	kHz
Stopband (Note 15)			SB	25.2			kHz
Passband Ripple			PR			±0.01	dB
Stopband Attenuation			SA	59			dB
Group Delay (Note 16)			GD	-	16.8	-	1/fs
Group Delay Distortion			ΔGD		0		μs
DAC Digital Filter + Analog Filter: (Note 14)(Note 17)							
Frequency Response 0 ~ 20.0kHz			FR	-	±1.0	-	dB
BOOST Filter: (Note 17) (Note 18)							
Frequency Response	MIN	20Hz	FR	-	5.74	-	dB
		100Hz		-	2.92	-	dB
		1kHz		-	0	-	dB
	MID	20Hz	FR	-	5.94	-	dB
		100Hz		-	4.71	-	dB
		1kHz		-	0.14	-	dB
	MAX	20Hz	FR	-	16.04	-	dB
		100Hz		-	10.55	-	dB
		1kHz		-	0.3	-	dB

Note 14. BOOST OFF (BST1-0 = "00")

Note 15. The passband and stopband frequencies scale with fs.
For example (DAC), PB=0.44*fs(@±0.1dB), SB=0.57*fs(@–59dB).

Note 16. This is the calculated delay time caused by digital filtering. This time is measured from the input of analog signal to setting the 20 bit data of both channels on input register to the output register of ADC. This time also includes group delay of HPF. For DAC, this time is from setting the 20 bit data of both channels on input register to the output of analog signal.

Note 17. DACL → HPL, DACR → HPR, DACL/R → MOUT.

Note 18. These frequency responses scale with fs. If high-level signal is input, the AK4569 clips at low frequency.

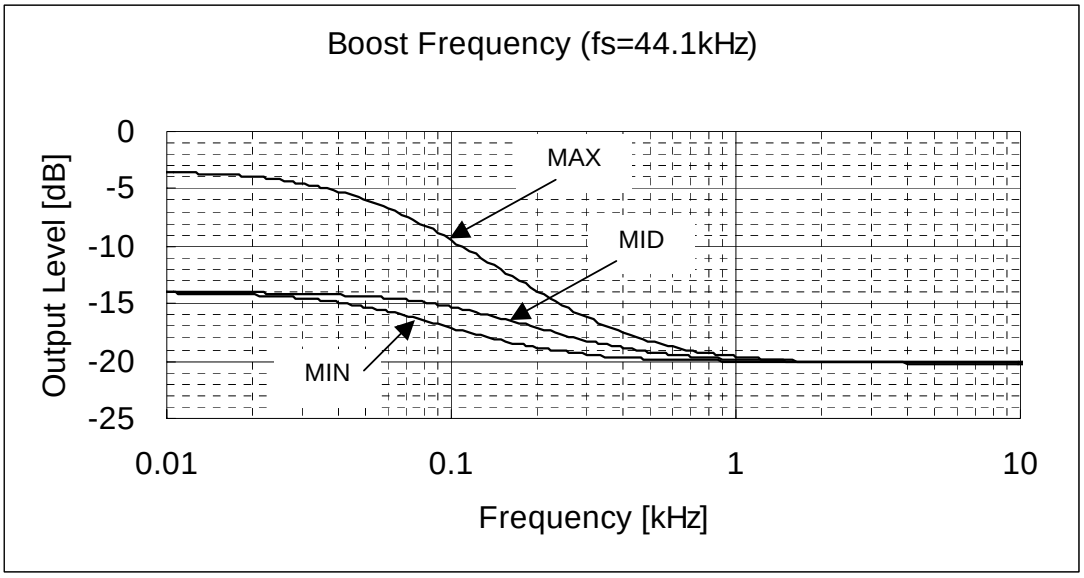


Figure 3. Boost Frequency (fs=44.1kHz)

DC CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, HVDD = 2.5 ~ 3.6V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%DVDD		-	V
Low-Level Input Voltage	VIL	-		30%DVDD	V
Input Voltage at AC Coupling (Note 19)	VAC	1.0			Vpp
High-Level Output Voltage (Iout = –100μA)	VOH	DVDD–0.4	-	-	V
Low-Level Output Voltage (Iout = 100μA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA

Note 19. When AC coupled capacitor is connected to MCLK pin.

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, HVDD = 2.5 ~ 3.6V: CL = 20pF)

Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
Frequency		fCLK	2.048		24.576	MHz
Pulse Width Low	(Note 20)	tCLKL	0.4/fCLK			ns
Pulse Width High	(Note 20)	tCLKH	0.4/fCLK			ns
AC Pulse Width	(Note 21)	tACW	0.4/fCLK			ns
LRCK Timing						
Frequency		fs	8	44.1	48	kHz
Duty Cycle		Duty	45		55	%
Serial Interface Timing (Note 22)						
BICK Period		tBCK	325.5			ns
BICK Pulse Width Low		tBCKL	130			ns
Pulse Width High		tBCKH	130			ns
LRCK Edge to BICK "↑"	(Note 23)	tLRB	50			ns
BICK "↑" to LRCK Edge	(Note 23)	tBLR	50			ns
LRCK to SDTO(MSB)		tLRS			80	ns
BICK "↓" to SDTO		tBSD			80	ns
SDTI Hold Time		tSDH	50			ns
SDTI Setup Time		tSDS	50			ns
Control Interface Timing						
CCLK Period		tCCK	200			ns
CCLK Pulse Width Low		tCCKL	80			ns
Pulse Width High		tCCKH	80			ns
CDTI Setup Time		tCDS	40			ns
CDTI Hold Time		tCDH	40			ns
CSN "H" Time		tCSW	150			ns
CSN "↓" to CCLK "↑"		tCSS	50			ns
CCLK "↑" to CSN "↑"		tCSH	50			ns
Power-down & Reset Timing						
PDN Pulse Width	(Note 24)	tPD	150			ns
PMADC "↑" to SDTO valid	(Note 25)	tPDV		2081		1/fs

Note 20. Except AC coupling.
Note 21. Pulse width to ground level when MCLK is connected to a capacitor in series and a resistor is connected to ground. (Refer to Figure 4.)
Note 22. Refer to "Serial Data Interface".
Note 23. BICK rising edge must not occur at the same time as LRCK edge.
Note 24. The AK4569 can be reset by bringing PDN= "L" to "H" only upon power up.
Note 25. This is the count of LRCK "↑" from PMADC bit="1".

■ Timing Diagram

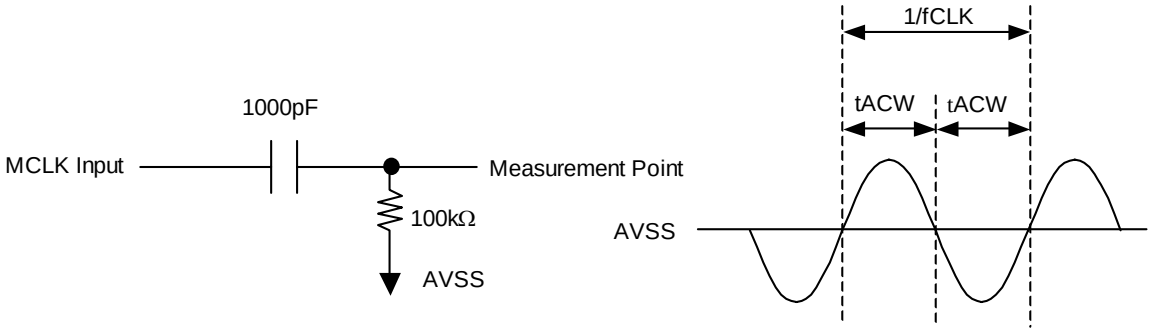


Figure 4. MCLK AC Coupling Timing

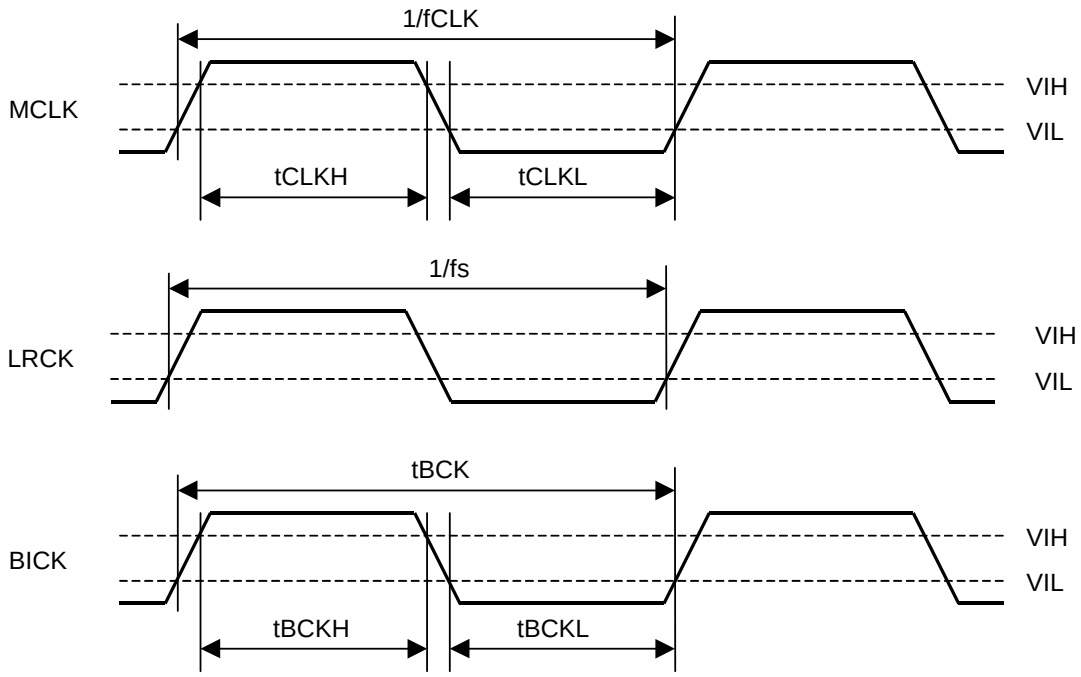


Figure 5. Clock Timing

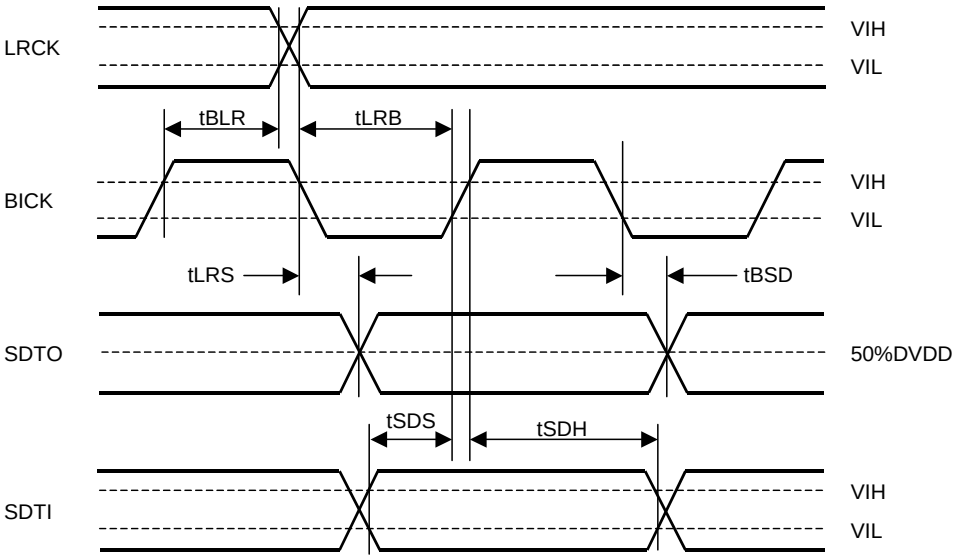


Figure 6. Serial Interface Timing

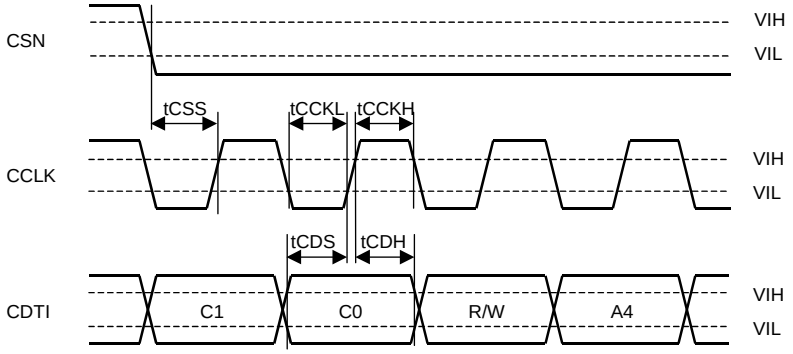


Figure 7. WRITE Command Input Timing

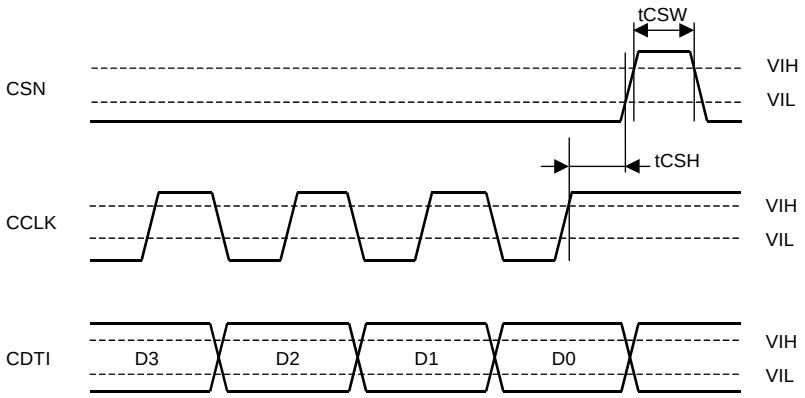


Figure 8. WRITE Data Input Timing

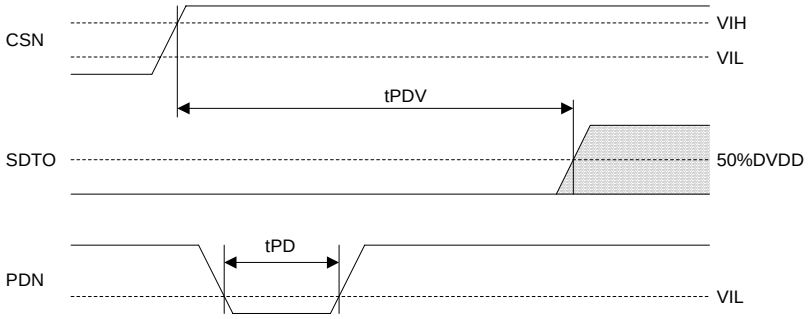


Figure 9. Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock

The external clocks required to operate the AK4569 are MCLK(256fs/384fs/512fs), LRCK(fs) and BICK. The master clock (MCLK) should be synchronized with sampling clock (LRCK). The phase between these clocks does not matter. The frequency of MCLK is detected automatically, and the internal master clock becomes the appropriate frequency. Table 1 shows system clock example.

LRCK	MCLK (MHz)			BICK (MHz)
fs	256fs	384fs	512fs	64fs
8kHz	2.048	3.072	4.096	0.512
11.025kHz	2.8224	4.2336	5.6448	0.7056
12kHz	3.072	4.608	6.144	0.768
16kHz	4.096	6.144	8.192	1.024
22.05kHz	5.6448	8.4672	11.2896	1.4112
24kHz	6.144	9.216	12.288	1.536
32kHz	8.192	12.288	16.384	2.048
44.1kHz	11.2896	16.9344	22.5792	2.8224
48kHz	12.288	18.432	24.576	3.072

Table 1. System Clock Example

External clocks (MCLK, BICK and LRCK) are needed to operate ADC or DAC. All external clocks (MCLK, BICK and LRCK) should always be present whenever the ADC or DAC is in normal operation mode (PMADC bit = “1” or PMDAC bit = “1”). If these clocks are not provided, the AK4569 may draw excess current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, AK4569 should be placed in power-down mode (PDN pin = “L” or PMADC bit = PMDAC bit = “0”). When MCLK is input with AC coupling, the MCKAC bit should be set to “1”. If MCLK with AC coupling stops, MCKPD bit should be set to “1”.

For low sampling rates, outband noise causes both DR and S/N to degrade. DR and S/N are improved by setting DFS bit to “1”. Table 2 shows S/N of DAC output for both the HP-amp and MOUT. When the DFS bit is “1”, MCLK needs 512fs. During normal operation, when the ADC or DAC sampling frequency is changed (PMADC bit = “1” or PMDAC bit = “1”), the DAC output should be soft-muted or “0” data should be input to avoid pop noise.

DFS	fs	MCLK	S/N (fs=8kHz, A-weighted)		
			HP-amp	MOUT	
0	8kHz~48kHz	256fs/384fs/512fs	84dB	84dB	Default
1	8kHz~24kHz	512fs	90dB	88dB	

Table 2. Relationship among fs, MCLK frequency and S/N of HP-amp and MOUT

■ Serial Data Interface

The AK4569 interfaces with external systems via the BICK, LRCK, SDTO and SDTI pins. Four data formats are available and are selected by setting DIF1 and DIF0 bits (Table 3). Mode 0 of SDTI is compatible with existing 16bit DACs and digital filters. Mode 1 of SDTI is a 20bit version of Mode 0. Mode 2 of SDTI is similar to AKM ADCs and many DSP serial ports. Mode 3 is compatible with the I^2S serial data protocol. In SDTI Modes 2 and 3, the following formats are also valid: 16-bit data followed by four zeros and 18-bit data followed by two zeros. In all modes, the serial data is MSB first and 2's complement format.

Mode	DIF1	DIF0	SDTO	SDTI	BICK	LRCK	
0	0	0	20bit, MSB justified	16bit, LSB justified	≥ 32fs	H/L	
1	0	1	20bit, MSB justified	20bit, LSB justified	≥ 40fs	H/L	
2	1	0	20bit, MSB justified	20bit, MSB justified	≥ 40fs	H/L	Default
3	1	1	IIS (I^2S)	IIS (I^2S)	32fs or ≥ 40fs	L/H	

Table 3. Audio Data Format

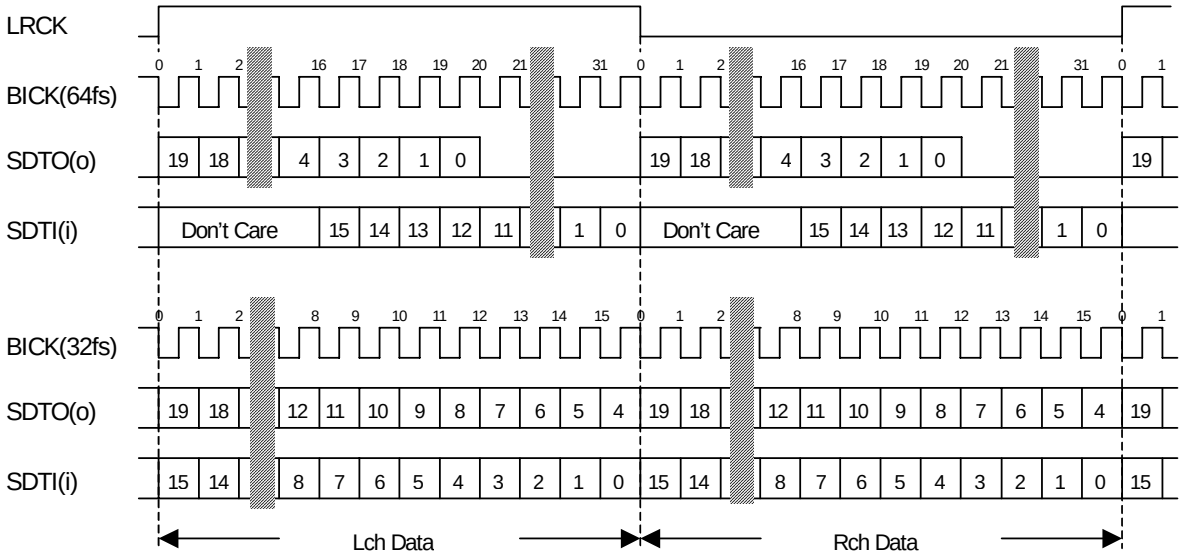


Figure 10. Mode 0 Timing

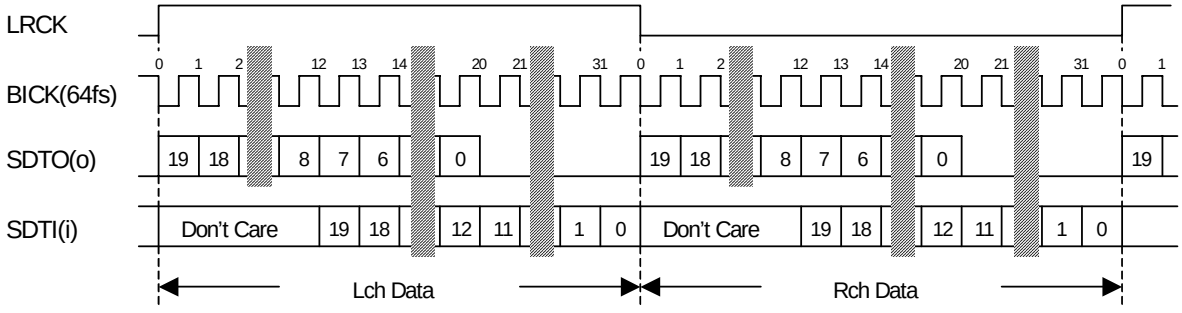


Figure 11. Mode 1 Timing

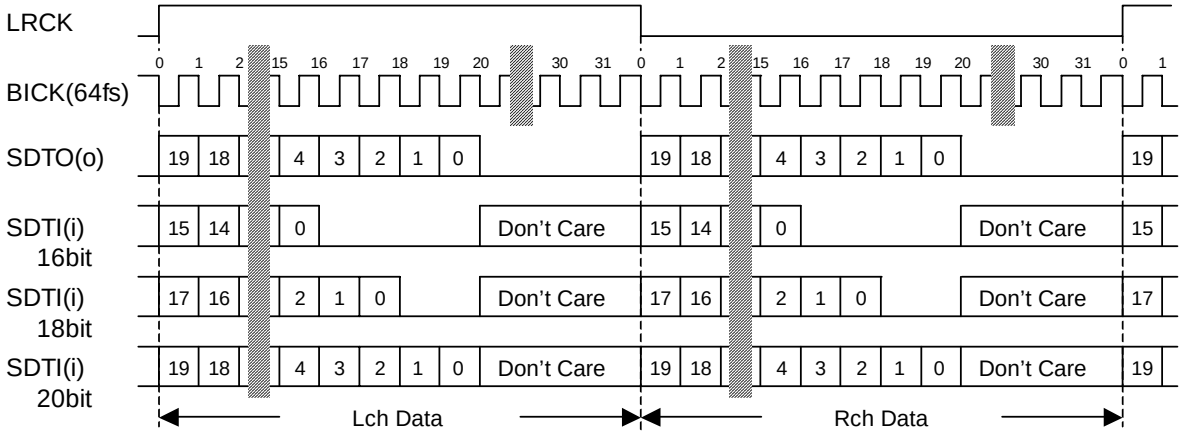


Figure 12. Mode 2 Timing

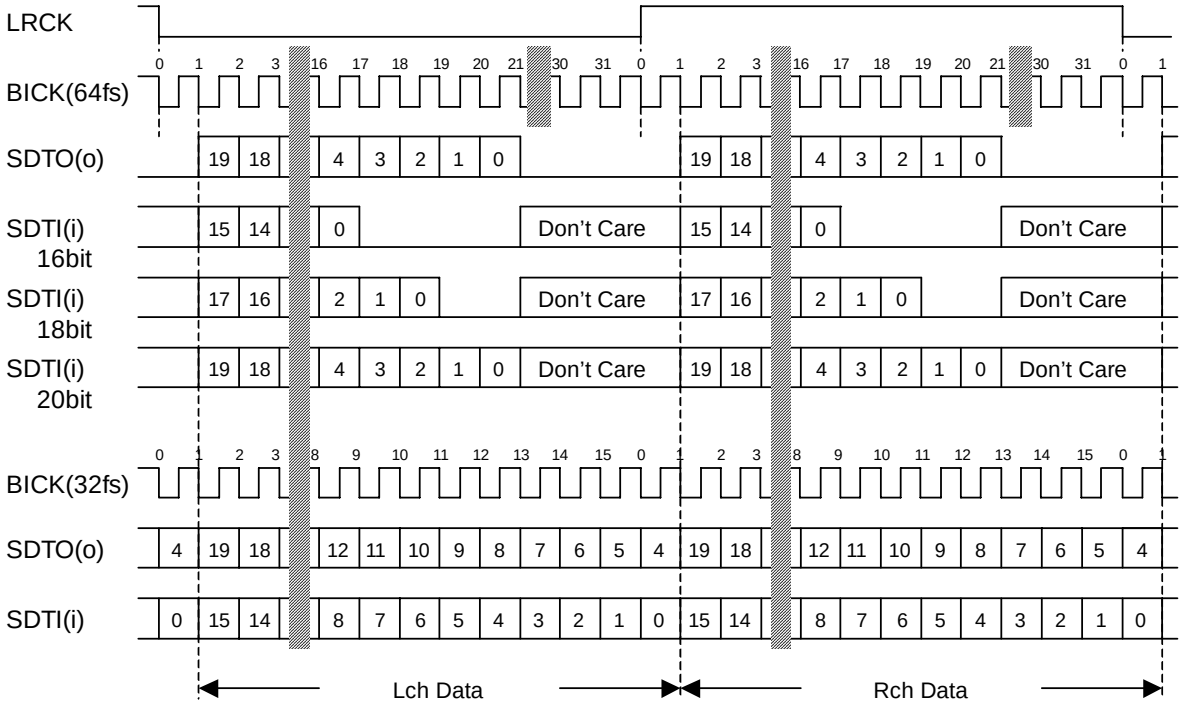


Figure 13. Mode 3 Timing

■ Digital High Pass Filter

The AK4569 has a Digital High Pass Filter (HPF) to cancel DC-offsets in the ADC and IPGA. The cut-off frequency of the HPF is 3.4Hz at fs=44.1kHz. This filter scales with the sampling frequency (fs).

■ ALC Operation

[1] ALC Limiter Operation

During the ALC limiter operation, when either Lch or Rch exceeds ALC limiter detection level (LMTH), IPGA value is attenuated by ALC limiter ATT step (LMAT1-0) automatically. The IPGA is then set to the same value for both channels.

When ZELMN = "1", the timeout period is set by LTM1-0 bits. The attenuation operation is done continuously until the input signal level becomes LMTH or less. After finishing the attenuation operation, if ALC bit does not change to "0", the operation repeats when the input signal level exceeds LMTH.

When ZELMN = "0", the ALC limiter operation is attenuated by the ZTM1-0 bits setting. The IPGA value is automatically attenuated using zero crossing detection.

The ALC operation of the AK4569 corresponds to the impulse noise. If the impulse noise is supplied at ZELMN = "0", the ALC limiter operation becomes faster period than a set of ZTM1-0 bits. In case of ZELMN = "1", it becomes the same period as LTM1-0 bits.

[2] ALC Recovery Operation

The ALC recovery operation waits for the WTM1-0 bits to be set after completing the ALC limiter. If the input signal does not exceed "ALC recovery waiting counter reset level (LMTH)", the ALC recovery operation is done. The IPGA value is automatically incremented by this operation up to the set reference level (REF6-0) with zero crossing detection which timeout period is set by ZTM1-0 bits. Then the IPGA value is set for both Lch and Rch. The ALC recovery operation is done at a period set by WTM1-0 bits. When zero cross is detected at the IPGA output during the wait period set by WTM1-0 bits, the ALC recovery operation waits until WTM1-0 period and the next recovery operation is done.

During the ALC recovery operation or the recovery waiting, when either input signal level of Lch or Rch in IPGA exceeds the ALC limiter detection level (LMTH), the ALC recovery operation changes into the ALC limiter operation immediately.

When
(ALC recovery waiting counter reset level: LMTH) ≤ (IPGA output level) < (ALC limiter detection level: LMTH)
during the ALC recovery operation, the ALC recovery operation wait timer is reset. Therefore, when
(ALC recovery waiting counter reset level: LMTH) > (IPGA output level),
the ALC recovery operation wait timer starts.

The ALC operation of the AK4569 corresponds to the impulse noise. If the impulse noise is supplied, the ALC recovery operation becomes faster period than a set of ZTM1-0 or WTM1-0 bits.

Others:

When either channel enters the limiter operation while waiting time for a zero crossing, the present ALC recovery operation stops, according as the small value of IPGA (a channel waiting zero crossing), the ALC limiter operation is done. When both channels are waiting for the next ALC recovery operation, the ALC limiter operation is done from the IPGA value of a point in time.

ZTM1-0 bits set zero crossing timeout and WTM1-0 bits set the ALC recovery operation period. When the ALC recovery waiting time (WTM1-0 bits) is shorter than zero crossing timeout period (ZTM1-0 bits), the ALC recovery is operated by the zero crossing timeout period. Therefore, in this case, the ALC recovery operation period is not constant.

[3] ALC Operation Example

The following registers should not be changed during the ALC operation:
LTM1-0, LMTH, LMAT1-0, WTM1-0, ZTM1-0, RATT, REF6-0, ZELMN.

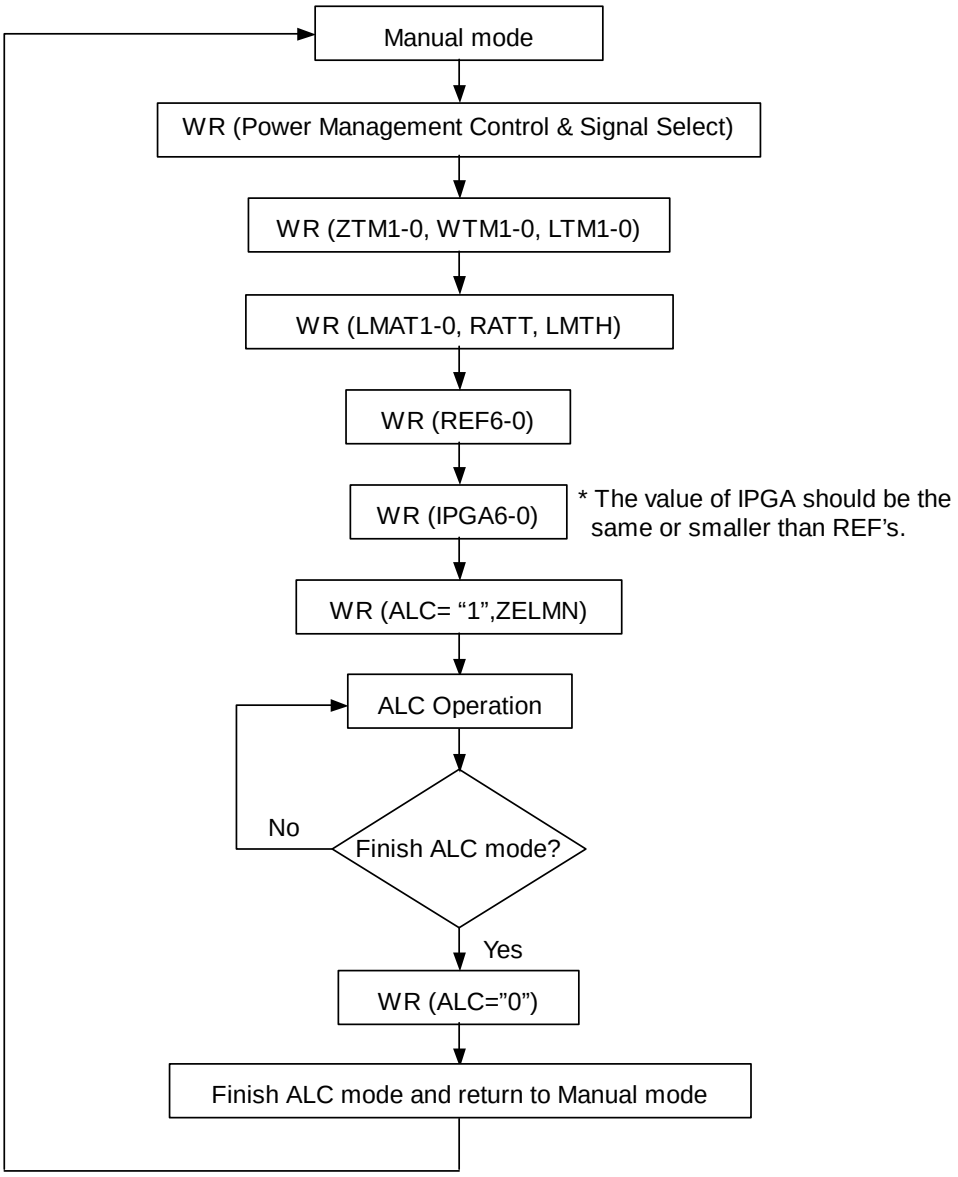


Figure 14. Registers set-up sequence at ALC operation (WR=Write)

■ IPGA Operation

[Write Operation at ALC Enabled]

The values of IPGA6-0 bits are ignored during ALC operation.

[Write Operation at ALC Disabled]

Channel independent zero crossing detection is used. If there are no zero crossings, then the level will change after a timeout. The ZTM1-0 bits set the zero crossing timeout. When a μP writes to the IPGA6-0 bits, the zero crossing counter is reset and starts. When the IPGA output signal detects zero crossing or a zero crossing timeout, the written value from the μP becomes valid.

When writing to the IPGA6-0 bits continually, the control register should be written by an interval more than zero crossing timeout. If not, there is a possibility that each IPGA of L/R channels has a different gain.

[IPGA Gain after completing ALC operation]

The IPGA6-0 bits are not updated by the actual gain of IPGA changed during ALC operation. In order to set the actual gain of IPGA with the IPGA6-0 bits, the IPGA6-0 bits should be written after zero crossing timeout period when completing ALC operation (ALC bit= “1” → “0”).

■ Digital Attenuator

The AK4569 has a channel-independent digital attenuator (256 levels, 0.5dB step). This digital attenuator is placed before the D/A converter. ATTL/R7-0 bits set the attenuation level (0dB to −127dB or MUTE) for each channel (Table 19). At DATTC= "1", ATTL7-0 bits control both Lch and Rch attenuation levels. At DATTC= "0", ATTL7-0 bits control the Lch level and ATTR7-0 bits control the Rch level.

The ATS bit sets the transition time between set values of ATT7-0 bits as either 1061/fs or 7424/fs (Table 15). When ATS= "0", a soft transition between the set values occurs(1062 levels). It takes 1061/fs (24ms@fs=44.1kHz) from FFH(0dB) to 00H(MUTE). The ATTs are 00H when the PMDAC bit is "0". When the PMDAC returns to "1", the ATTs fade to their current value. Digital attenuator is independent of the soft mute function.

■ Soft Mute

Soft mute operation is performed in the digital domain. When SMUTE bit goes to "1", the output signal is attenuated by −∞ ("0") via the cycle set by TM1-0 bit (Table 18). When SMUTE bit returns to "0", the mute is cancelled and the output attenuation gradually changes to 0dB via the cycle set by TM1-0 bits. If the soft mute is cancelled within the cycle set by TM1-0 bits after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.

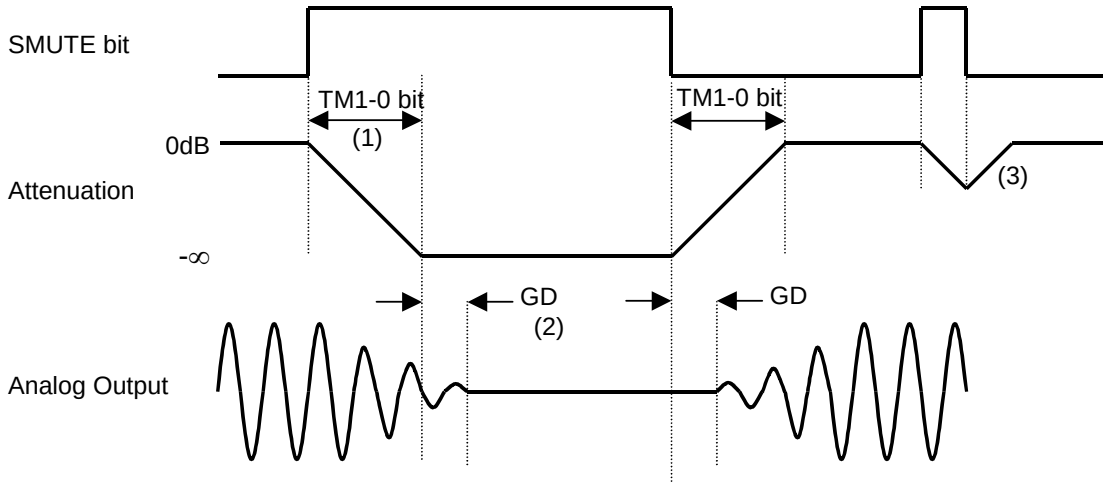


Figure 15. Soft Mute Function

NOTE:
(1) The output signal is attenuated until −∞ ("0") by the cycle set by TM1-0 bits.
(2) Analog output corresponding to digital input has the group delay (GD).
(3) If the soft mute is cancelled within the cycle set by TM1-0 bits, the attenuation is discontinued and returned to 0dB(the setting value).

■ De-emphasis Filter

The AK4569 includes a digital de-emphasis filter (tc = 50/15μs) by IIR filter corresponding to three sampling frequencies (32kHz, 44.1kHz and 48kHz). The de-emphasis filter is enabled by setting DEM1-0 bits (Table 16).

■ Bass Boost Function

By controlling BST1-0 bits, the low frequency boost signal can be output from DAC. The setting value is common in Lch and Rch (Table 17).

The cut-off frequency (fc) of HPF depends on the external resistor and capacitor values. Table 4 shows the relationship of external resistor, capacitor, fc and output power, where load resistance of headphone is 16Ω. Output level of headphone amp is 1.5Vpp (typ).

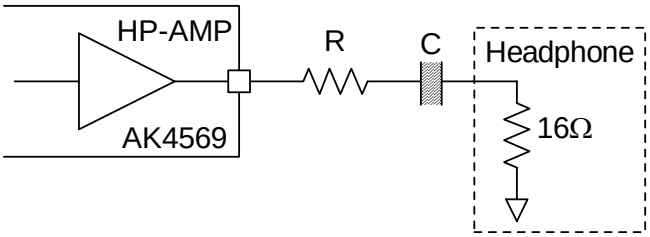


Figure 16. External Circuit Example of Headphone

R [Ω]	C [μF]	fc [Hz] BOOST=OFF	fc [Hz] BOOST=MID	Output Power [mW]
6.8	47	148.6	65	8.7
	100	69.8	27	
16	47	105.8	43	4.4
	100	49.7	20	

Table 4. Relationship of external circuit, output power and frequency response

Note: Cut-off frequency (fc) at BOOST=MID is approximate value.

■ System Reset

The AK4569 should be reset once by bringing PDN "L" upon power-up. After exiting reset, VCOM, IPGA, ADC, DAC, HPL, HPR and MOUT switch to the power-down state. The contents of the control register are maintained until the reset is done.

ADC exits reset and power down state by MCLK after PMADC bit is changed to "1", and then ADC is powered up and the internal timing starts clocking by LRCK "↑". ADC is in the power-down mode until MCLK and LRCK are input. DAC also exits reset and power down state when MCLK and LRCK are input after PMDAC= "1".

■ Power-Up/Down Sequence

1) ADC

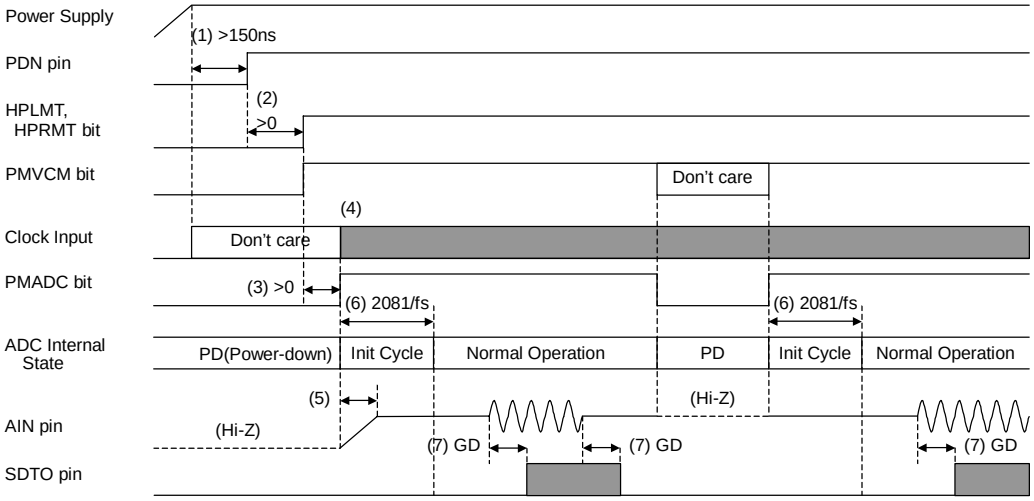


Figure 17. Power-up/down sequence of ADC

(1) PDN pin should be set to "H" at least 150ns after the power is supplied.
(2) HPLMT, HPRMT and PMVCM bits should be changed to "1" after PDN pin goes to "H".
(3) PMADC bit should be changed to "1" after HPLMT, HPRMT and PMVCM bits are changed to "1".
(4) External clocks (MCLK, BICK, LRCK) are needed to operate ADC.
(5) When PMADC bit is changed to "1", each AIN pin is biased to VCOM voltage. Rising time constant is determined by input capacitor for AC coupling and input resistance. In case of AINL2/AINR2 and 1µF input capacitor, time constant is

$$\tau = 1\mu F \times 12.5k\Omega = 12.5ms \text{ (typ)}$$

(6) The analog part of ADC is initialized during 2081/fs(=47ms@fs=44.1kHz) after exiting the power-down state. SDTO is "L" at that time.
(7) Digital output corresponding to analog input has the group delay (GD) of 17.0/fs(=385µs@fs=44.1kHz).

2) DAC → HP-amp

Power supply voltage for headphone amp is supplied from HVDD pin and centered on VCOM. Load resistance of headphone output is min.20Ω. When PMHPL and PMHPR bit are "0", headphone amplifiers are powered-down perfectly. Then HPL and HPR pins are fixed to "L" (HVSS) and a capacitor of MUTET pin works to avoid pop noise.

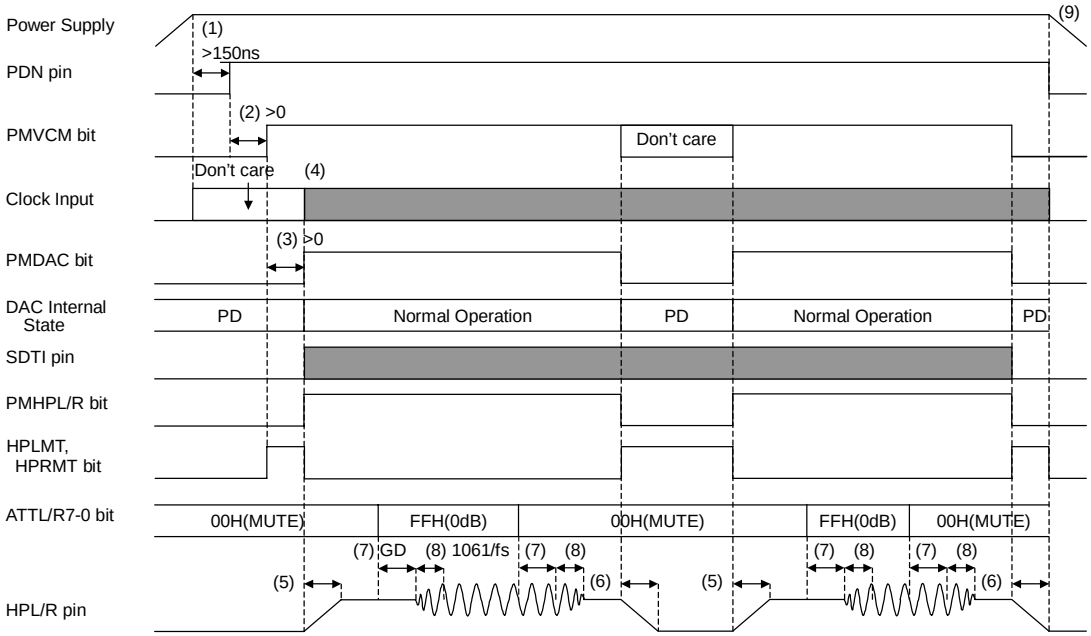


Figure 18. Power-up/down sequence of DAC and HP-amp

(1) PDN pin should be set to "H" at least 150ns after the power is supplied.
(2) HPLMT, HPRMT and PMVCM bits should be changed to "1" after PDN pin goes to "H".
(3) PMDAC, PMHPL, PMHPR bits should be changed to "1" and HPLMT, HPRMT bits should be changed to "0" after HPLMT, HPRMT, PMVCM bits are changed to "1". Once PMHPL and PMHPR bits are changed to "1", HPLMT and HPRMT bits should be inverted from PMHPL and PMHPR bits respectively.
(4) External clocks (MCLK, BICK, LRCK) are needed to operate DAC. When PMDAC bit = "0", these clocks can be stopped. Headphone amp can operate without these clocks.
(5) Rise time of headphone amp is determined by external capacitor of MUTET pin. When C=1μF,
Rise Time Constant of Headphone Amp: τ = 100ms
(6) Fall time of headphone amp is determined by output capacitor for AC coupling. When C=100μF,
Fall Time Constant of Headphone Amp: τ = 200ms
(7) Analog output corresponding to digital input has the group delay (GD) of 16.8/fs(=381μs@fs=44.1kHz).
(8) ATS bit sets transition time of digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).
(9) Power supply should be switched off after headphone amp is powered down (HPL/R pins become "L").

3) DAC → MOUT

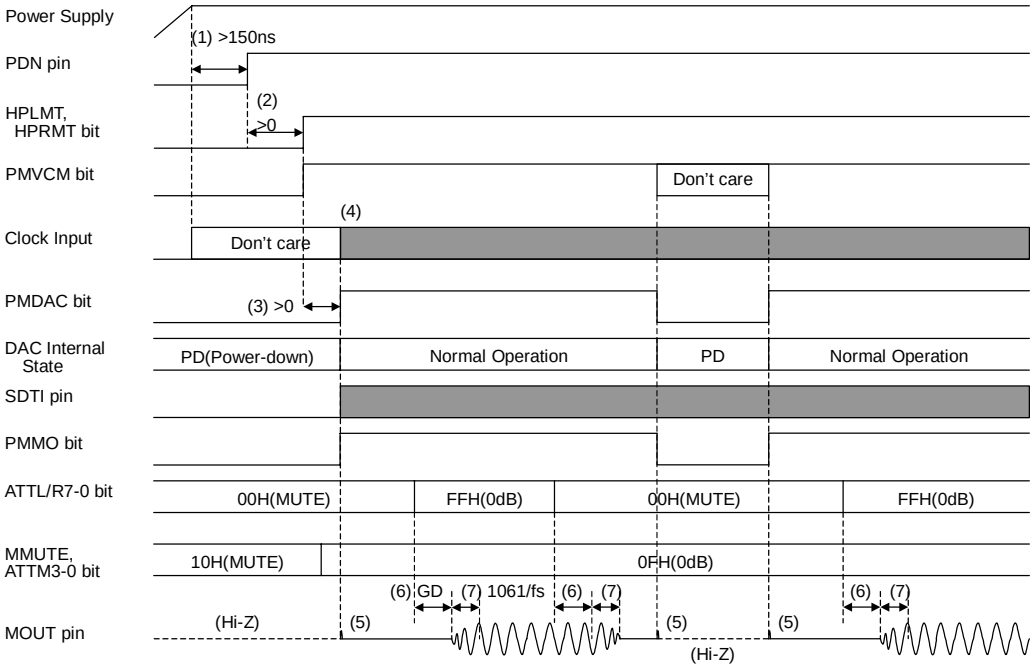


Figure 19. Power-up/down sequence of DAC and MOUT

(1) PDN pin should be set to "H" at least 150ns after the power is supplied.
(2) HPLMT, HPRMT and PMVCM bits should be changed to "1" after PDN pin goes to "H".
(3) PMDAC and PMMO bits should be changed to "1" after HPLMT, HPRMT and PMVCM bits are changed to "1".
(4) External clocks (MCLK, BICK, LRCK) are needed to operate DAC. When PMDAC= "0", these clocks can be stopped. MOUT buffer can operate without these clocks.
(5) When PMMO bit is changed to "1", pop noise is output from MOUT pin.
(6) Analog output corresponding to digital input has the group delay (GD) of 16.8/fs(=381μs@fs=44.1kHz).
(7) ATS bit sets transition time of digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).

4) LIN/RIN/MIN → HP-amp, MOUT

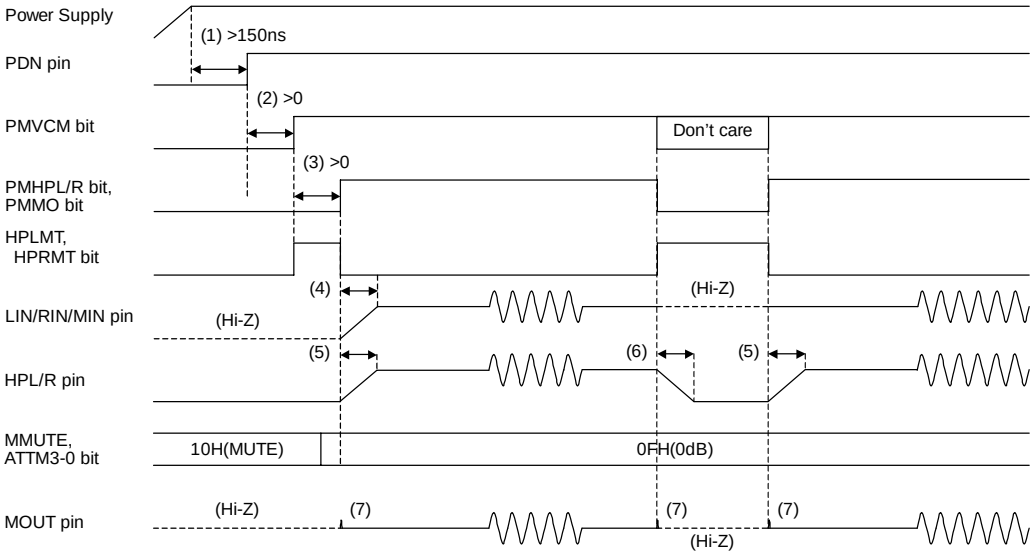


Figure 20. Power-up/down sequence of LIN/RIN/MIN, HP-amp and MOUT

(1) PDN pin should be set to "H" at least 150ns after the power is supplied.
(2) HPLMT, HPRMT and PMVCM bits should be changed to "1" after PDN pin goes to "H".
(3) PMHPL, PMHPR, PMMO bits should be changed to "1" and HPLMT, HPRMT bits should be changed to "0" after HPLMT, HPRMT, PMVCM bits are changed to "1". Once PMHPL and PMHPR bits are changed to "1", HPLMT and HPRMT bits should be inverted from PMHPL and PMHPR bits respectively.
(4) When PMHPL, PMHPR or PMMO bit is changed to "1", LIN, RIN and MIN are biased to VCOM voltage. Rising time constant is determined by input capacitor for AC coupling and input resistance 50kΩ (typ). In case of 0.1μF input capacitor, time constant is

$$\tau = 0.1\mu F \times 50k\Omega = 5ms \text{ (typ)}$$

(5) Rise time of headphone amp is determined by external capacitor of MUTET pin. When C=1μF,

Rise Time Constant of Headphone Amp: τ = 100ms

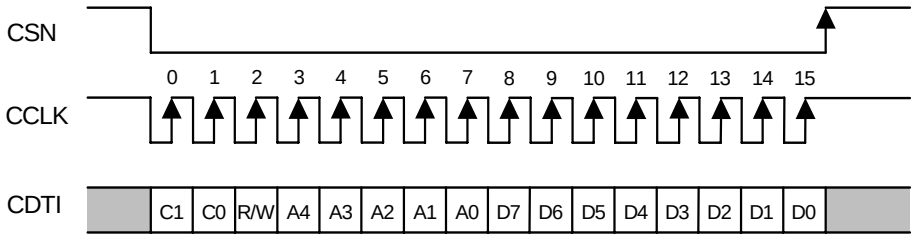
(6) Fall time of headphone amp is determined by output capacitor for AC coupling. When C=100μF,

Fall Time Constant of Headphone Amp: τ = 200ms

(7) When PMMO bit is changed to "1", pop noise is output from MOUT pin.

■ Serial Control Interface

Internal registers may be written via to the 3 wire µP interface pins (CSN, CCLK and CDTI). The data on this interface consists of Chip address (2bits, Fixed to “10”), Read/Write (1bit, Fixed to “1”, Write only), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK. For write operations, data is latched after a low-to-high transition of CSN. The clock speed of CCLK is 5MHz(max). The value of internal registers is initialized at PDN= “L”.



C1-C0: Chip Address (Fixed to “10”)
R/W: Read/Write (Fixed to “1” : Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 21. Control Interface

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	HPRMT	HPLMT	PMMO	PMHPR	PMHPL	PMDAC	PMADC	PMVCM
01H	Input Select	0	0	0	ADM	INR2	INR1	INL2	INL1
02H	Timer Select	0	0	ZTM1	ZTM0	WTM1	WTM0	LTM1	LTM0
03H	ALC Mode Control 1	0	0	ALC	ZELMN	LMAT1	LMAT0	RATT	LMTH
04H	ALC Mode Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0
05H	IPGA Control	0	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
06H	Mode Control	MCKAC	MCKPD	0	ATS	HPM	DIF1	DIF0	DFS
07H	DAC Control	TM1	TM0	SMUTE	DATTC	BST1	BST0	DEM1	DEM0
08H	Output Select 0	0	0	MINR	RINR	DACR	MINL	LINL	DACL
09H	Output Select 1	0	0	0	0	MINM	RINM	LINM	DACM
0AH	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
0BH	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
0CH	MOUT ATT	0	0	0	MMUTE	ATTM3	ATTM2	ATTM1	ATTM0

All registers inhibit writing at PDN pin = "L".

Note: Unused bits must contain a "0" value.
Note: For addresses from 0DH to 1FH, data must not be written.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	HPRMT	HPLMT	PMMO	PMHPR	PMHPL	PMDAC	PMADC	PMVCM
Default		0	0	0	0	0	0	0	0

PMVCM: Power Management for VCOM Block
0: Power OFF (Default)
1: Power ON

PMADC: Power Management for IPGA and ADC Blocks
0: Power OFF (Default)
1: Power ON
MCLK should be present when PMADC bit= "1".

PMDAC: Power Management for DAC Blocks
0: Power OFF (Default)
1: Power ON
When PMDAC bit is changed from "0" to "1", DAC is powered-up to the current register values (ATT value, sampling rate, etc).

PMHPL: Power Management for Lch of Headphone Amp
0: Power OFF (Default). HPL pin becomes HVSS(0V).
1: Power ON

PMHPR: Power Management for Rch of Headphone Amp
0: Power OFF (Default). HPR pin becomes HVSS(0V).
1: Power ON

PMMO: Power Management for Mono Output
0: Power OFF (Default) MOUT pin becomes Hi-Z.
1: Power ON

HPLMT: Mute for Lch of Headphone Amp
0: Normal operation (Default). MUTET pin is connected to VCOM pin internally.
1: Mute. MUTET pin is connected to HPL pin internally.

HPLMT: Mute for Rch of Headphone Amp
0: Normal operation (Default). MUTET pin is connected to VCOM pin internally.
1: Mute. MUTET pin is connected to HPR pin internally.

HPLMT	HPRMT	MUTET
0	0	Connected to VCOM
0	1	Connected to HPR
1	0	Connected to HPL
1	1	Connected to HPL,HPR

Table 5. MUTET internal connection

All blocks can be powered-down by setting the PDN pin to "L" regardless of register values setup. In this case, all control register values are initialized.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Input Select	0	0	0	ADM	INR2	INR1	INL2	INL1
Default		0	0	0	0	0	1	0	1

INL2-1: Select ON/OFF of IPGA Lch input.
0: OFF
1: ON
Default: INL2=0, INL1=1

INR2-1: Select ON/OFF of IPGA Rch input.
0: OFF
1: ON
Default: INR2=0, INR1=1

ADM: Mono Recording Mode
0: Stereo (Default)
1: MONO
When ADM= “1”, input signal to AINL1 or AINL2 pin is input to both Lch and Rch of ADC.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Timer Select	0	0	ZTM1	ZTM0	WTM1	WTM0	LTM1	LTM0
Default		0	0	0	0	0	0	0	0

LTM1-0: ALC limiter operation period (Table 6)

When zero crossing is disabled (ZELMN = "1"), the IPGA value is changed immediately by ALC limiter operation. When the IPGA value is changed continuously, the change is done by the period specified by LTM1-0 bits. Default: "00".

LTM1	LTM0		ALC Limiter Operation Period			
			8kHz	16kHz	44.1kHz	
0	0	0.5/fs	63μs	31μs	11μs	Default
0	1	1/fs	125μs	63μs	23μs	
1	0	2/fs	250μs	125μs	45μs	
1	1	4/fs	500μs	250μs	91μs	

Table 6. ALC Limiter Operation Period at zero crossing disable (ZELMN bit= "1")

WTM1-0: ALC Recovery Waiting Period (Table 7)

WTM1-0 bits set the recovery operation period when any limiter operation does not occur during an ALC operation. Default: "00".

WTM1	WTM0		ALC Recovery Operation Waiting Period			
			8kHz	16kHz	44.1kHz	
0	0	128/fs	16ms	8ms	2.9ms	Default
0	1	256/fs	32ms	16ms	5.8ms	
1	0	512/fs	64ms	32ms	11.6ms	
1	1	1024/fs	128ms	64ms	23.2ms	

Table 7. ALC Recovery Operation Waiting Period

ZTM1-0: ALC Zero Crossing Timeout Period (Table 8)

When IPGA output detects zero crossing or timeout, the IPGA value is changed by a μP WRITE operation, ALC recovery operation, or ALC limiter operation. Default: "00".

ZTM1	ZTM0		Zero Crossing Timeout Period			
			8kHz	16kHz	44.1kHz	
0	0	128/fs	16ms	8ms	2.9ms	Default
0	1	256/fs	32ms	16ms	5.8ms	
1	0	512/fs	64ms	32ms	11.6ms	
1	1	1024/fs	128ms	64ms	23.2ms	

Table 8. Zero Crossing Timeout Period

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	ALC Mode Control 1	0	0	ALC	ZELMN	LMAT1	LMAT0	RATT	LMTH
Default		0	0	0	0	0	0	0	0

LMTH: ALC Limiter Detection Level / Recovery Waiting Counter Reset Level (Table 9)

LMTH	ALC Limiter Detection Level	ALC Recovery Waiting Counter Reset Level	
0	ADC Input ≥ –6.0dBFS	–6.0dBFS > ADC Input ≥ –8.0dBFS	Default
1	ADC Input ≥ –4.0dBFS	–4.0dBFS > ADC Input ≥ –6.0dBFS	

Table 9. ALC1 Limiter Detection Level / Recovery Waiting Counter Reset Level

RATT: ALC Recovery GAIN Step (Table 10)

During the ALC recovery operation, the number of steps changed from the current IPGA value is set. For example, when the current IPGA value is 3FH, RATT = "1" is set, the IPGA changes to 41H due to the ALC recovery operation, the output signal level is gained by 1dB (=0.5dB x 2). When the IPGA value exceeds the reference level (REF6-0 bits), the IPGA value does not increase.

RATT	GAIN STEP	
0	1	Default
1	2	

Table 10. ALC Recovery Gain Step Setting

LMAT1-0: ALC Limiter ATT Step (Table 11)

During the ALC limiter operation, when either Lch or Rch exceeds the ALC limiter detection level set by LMTH bit, LMAT1-0 bits set the number of steps attenuated from the current IPGA value. For example, when the current IPGA value is 3FH when LMAT1-0 bit = "11", the IPGA value changes to 3BH by the ALC limiter operation, the input signal level is attenuated by 2dB (=0.5dB x 4). When the attenuation value exceeds IPGA = "00H" (Mute), it clips to "00H".

LMAT1	LMAT0	ATT STEP	
0	0	1	Default
0	1	2	
1	0	3	
1	1	4	

Table 11. ALC Limiter ATT Step Setting

ZELMN: Zero Crossing Detection Enable at ALC Limiter Operation

0: Enable (Default)

1: Disable

In case of ZELMN = "0", when IPGA output detects zero crossing or timeout, the IPGA value is changed by the ALC operation. Zero crossing timeout is the same as ALC recovery operation. In case of ZELMN = "1", the IPGA value is changed immediately.

ALC: ALC Enable Flag

0: ALC Disable (Default)

1: ALC Enable

ALC is enabled at ALC bit is "1". Default: "0" (Disable).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	ALC Mode Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0
Default		0	0	1	1	1	1	1	1

REF6-0: Reference Value at ALC Recovery Operation, 0.5dB step, 103 levels, Default: "3FH" (Table 12)

During the ALC recovery operation, if the IPGA value exceeds the set reference value by gain operation, IPGA does not become larger than the reference value. For example, when REF= "40H", RATT= "1" (2 step) and IPGA= "3FH", then IPGA is going to become 3FH + 2step = 41H, but IPGA becomes 40H in fact, since REF=40H.

DATA	GAIN		
	AINL1, AINR1 (LINE IN)	AINL2, AINR2 (MIC IN)	
67H	+20.0dB	+32.0dB	
66H	+19.5dB	+31.5dB	
65H	+19.0dB	+31.0dB	
:	:	:	
3FH	0dB	+12.0dB	Default
:	:	:	
27H	–12.0dB	0dB	
:	:	:	
02H	–30.5dB	–18.5dB	
01H	–31.0dB	–19.0dB	
00H	MUTE (–∞)	MUTE (–∞)	

Table 12. Reference Value Setting at ALC Recovery Operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	IPGA Control	0	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
Default		0	0	1	1	1	1	1	1

IPGA6-0: Input Analog PGA, 0.5dB step, 103 levels, Default: "3FH" (Table 13)

When IPGA gain is changed, IPGA6-0 bits should be written while PMADC bit is "1" and ALC bit is "0". IPGA gain is reset when PMADC bit is "0", and then IPGA operation starts from the default value when PMADC is changed to "1". When ALC bit is changed from "1" to "0", IPGA holds the last gain value set by ALC operation.

DATA	GAIN		
	AINL1, AINR1 (LINE IN)	AINL2, AINR2 (MIC IN)	
67H	+20.0dB	+32.0dB	
66H	+19.5dB	+31.5dB	
65H	+19.0dB	+31.0dB	
:	:	:	
3FH	0dB	+12.0dB	Default
:	:	:	
27H	–12.0dB	0dB	
:	:	:	
02H	–30.5dB	–18.5dB	
01H	–31.0dB	–19.0dB	
00H	MUTE (–∞)	MUTE (–∞)	

Table 13. Input Gain Setting

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Mode Control	MCKAC	MCKPD	0	ATS	HPM	DIF1	DIF0	DFS
Default		0	0	0	0	0	1	0	0

DFS: Sampling Speed Mode Select (Table 2)

DIF1-0: Audio Data Interface Format
Default: “10” (Mode 2)

HPM: Mono Output Select of Headphone
0: Normal Operation (Default)
1: Mono. (L+R)/2 signals from the DAC are output to both Lch and Rch of headphone.
Setting of HPM bit is enabled only at DACL=DACR= “1”.

DACL	HPM	HPL pin Output	
0	x	No output from DAC	Default
1	0	Output from Lch of DAC	
	1	Output (L+R)/2 from DAC	

Table 14. Mono Output Select of Headphone
(Note. Rch is same.)

ATS: Digital attenuator transition time setting (Table 15)

ATS	ATT speed		
	0dB to MUTE	1 step	
0	1061/fs	4/fs	Default
1	7424/fs	29/fs	

Table 15. Transition time between set values of ATT7-0 bits

MCKPD: MCLK Input Buffer Control
0: Enable (Default)
1: Disable
When MCLK input with AC coupling is stopped, MCKPD bit should be set to “1”.

MCKAC: MCLK Input Mode Select
0: CMOS input (Default)
1: AC coupling input

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	DAC Control	TM1	TM0	SMUTE	DATTC	BST1	BST0	DEM1	DEM0
Default		0	0	0	0	0	0	0	1

DEM1-0: De-emphasis Filter Frequency Select

DEM1	DEM0	De-emphasis	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 16. De-emphasis Filter Frequency Select

BST1-0: Low Frequency Boost Function Select

BST1	BST0	BOOST	
0	0	OFF	Default
0	1	MIN	
1	0	MID	
1	1	MAX	

Table 17. Low Frequency Boost Select

DATTC: DAC Digital Attenuator Control Mode Select

0: Independent (Default)

1: Dependent

At DATTC= “1”, ATTL7-0 bits control both Lch and Rch attenuation level, while register values of ATTL7-0 bits are not written to ATTR7-0 bits. At DATTC= “0”, ATTL7-0 bits control Lch level and ATTR7-0 bits control Rch level.

SMUTE: Soft Mute Control

0: Normal operation (Default)

1: DAC outputs soft-muted

TM1-0: Soft Mute Time Select

TM1	TM0	Cycle	
0	0	1024/fs	Default
0	1	512/fs	
1	0	256/fs	
1	1	128/fs	

Table 18. Soft Mute Time Setting

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Output Select 0	0	0	MINR	RINR	DACR	MINL	LINL	DACL
Default		0	0	0	0	0	0	0	0

DACL: DAC Lch output signal is added to Lch of headphone amp.
0: OFF (Default)
1: ON

LINL: Input signal to LIN pin is added to Lch of headphone amp.
0: OFF (Default)
1: ON

MINL: Input signal to MIN pin is added to Lch of headphone amp.
0: OFF (Default)
1: ON

DACR: DAC Rch output signal is added to Rch of headphone amp.
0: OFF (Default)
1: ON

RINR: Input signal to RIN pin is added to Rch of headphone amp.
0: OFF (Default)
1: ON

MINR: Input signal to MIN pin is added to Rch of headphone amp.
0: OFF (Default)
1: ON

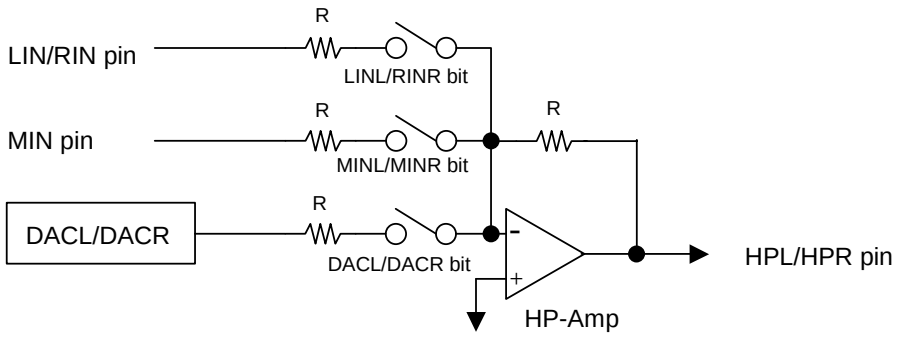


Figure 22. Summation circuit for headphone amp output

At HPM=0, gain of summation is 0dB for all input path.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Output Select 1	0	0	0	0	MINM	RINM	LINM	DACM
Default		0	0	0	0	0	0	0	0

DACM: DAC Lch and Rch outputs are added to MOUT buffer amp. Summation gain is –6dB for each channel.
0: OFF (Default)
1: ON

LINM: Input signal to LIN pin is added to MOUT buffer amp.
0: OFF (Default)
1: ON

RINM: Input signal to RIN pin is added to MOUT buffer amp.
0: OFF (Default)
1: ON

MINM: Input signal to MIN pin is added to MOUT buffer amp.
0: OFF (Default)
1: ON

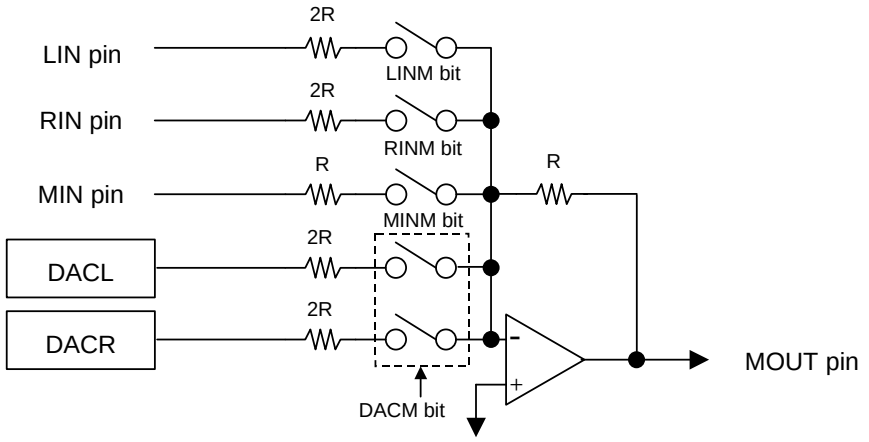


Figure 23. Summation circuit for MOUT

Gain of summation is 0dB for MIN and –6dB for LIN, RIN, DACL and DACR.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
0BH	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
Default		0	0	0	0	0	0	0	0

ATTL7-0: Setting of the attenuation value of output signal from DACL
ATTR7-0: Setting of the attenuation value of output signal from DACR

The AK4569 has channel-independent digital attenuator (256 levels, 0.5dB step). This digital attenuator is placed before D/A converter. ATTL/R7-0 bits set the attenuation level (0dB to –127dB or MUTE) of each channel. Digital attenuator is independent of soft mute function.

ATTL/R7-0	Attenuation	
FFH	0dB	
FEH	–0.5dB	
FDH	–1.0dB	
FCH	–1.5dB	
:	:	
:	:	
02H	–126.5dB	
01H	–127.0dB	
00H	MUTE (–∞)	Default

Table 19. Digital Volume ATT values

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	MOUT ATT	0	0	0	MMUTE	ATTM3	ATTM2	ATTM1	ATTM0
Default		0	0	0	1	0	0	0	0

ATTM3-0: Analog volume control for MOUT

MMUTE: Mute control for MOUT

0: Normal operation. ATTM3-0 bits control attenuation value.
1: Mute. ATTM3-0 bits are ignored. (Default)

MMUTE	ATTM3-0	Attenuation	
0	0FH	0dB	
	0EH	–2dB	
	0DH	–4dB	
	0CH	–6dB	
	:	:	
	:	:	
	01H	–28dB	
	00H	–30dB	
1	x	MUTE	Default

Table 20. MOUT Volume ATT values

SYSTEM DESIGN

Figure 24 shows the system connection diagram. An evaluation board [AKD4569] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

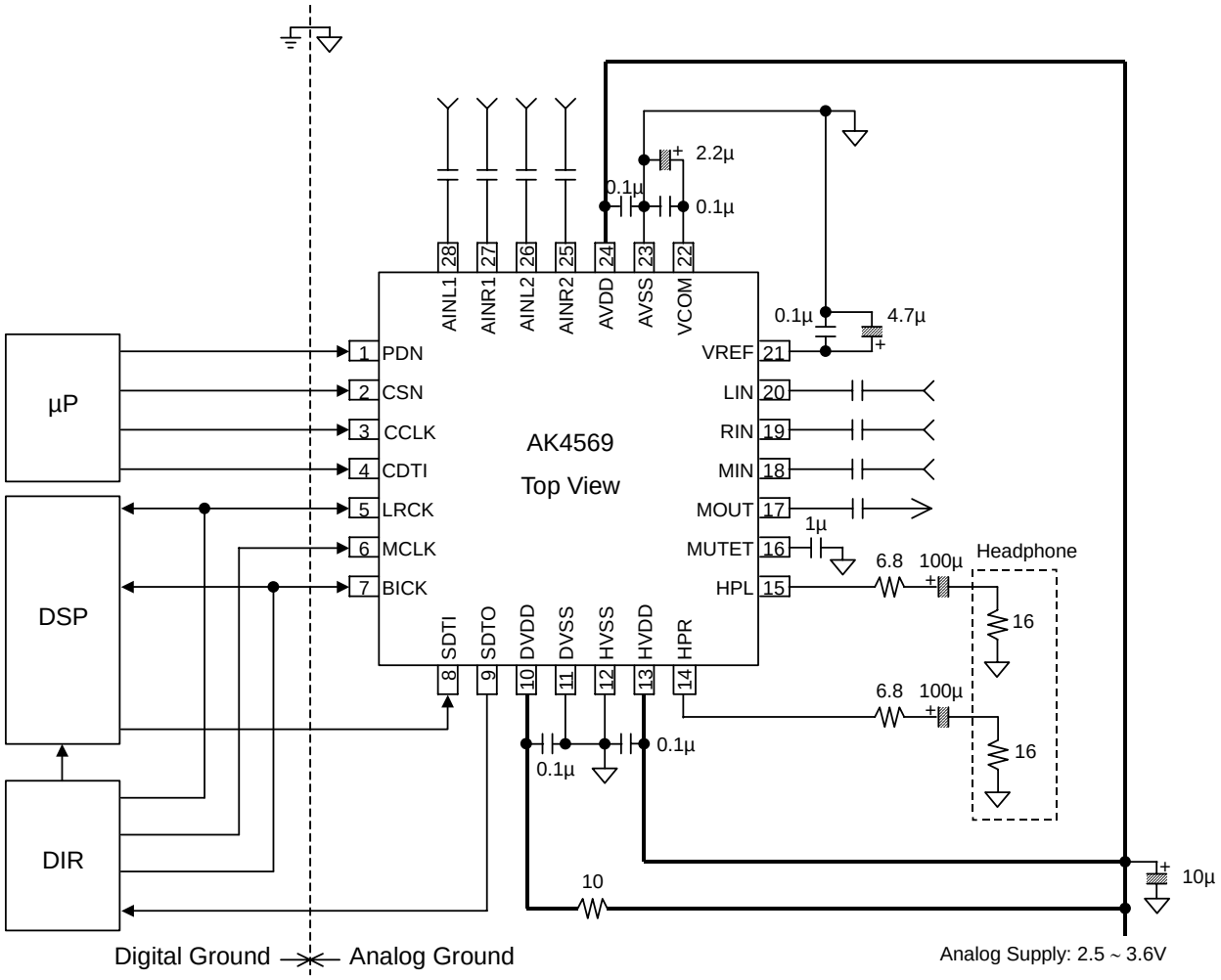


Figure 24. Typical Connection Diagram

1. Grounding and Power Supply Decoupling

The AK4569 requires careful attention to power supply and grounding arrangements. AVDD is usually supplied from the analog power supply in the system and DVDD is supplied from AVDD via a 10Ω resistor. Alternatively if AVDD, DVDD and HVDD are supplied separately, the power up sequence is not critical. AVSS, DVSS and HVSS must be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close to the AK4569 as possible, with the small value ceramic capacitors being the nearest.

2. Internal Voltage Reference

Internal voltage reference is output on the VREF pin (typ. 2.1V). An electrolytic capacitor 4.7μF in parallel with a 0.1μF ceramic capacitor is attached between VREF and AVSS to eliminate the effects of high frequency noise. VCOM is 1.25V(typ) and is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor should be connected between VCOM and AVSS to eliminate the effects of high frequency noise. A ceramic capacitor should be connected to VCOM pin and located as close as possible to the AK4569. No load current may be drawn from VREF and VCOM pins. All signals, especially clocks, should be kept away from the VCOM and VREF pins in order to avoid unwanted coupling into the AK4569.

3. Analog Inputs

The analog inputs are single-ended and the input resistance 50kΩ (typ) for AINL1/AINR1 pins and 12.5kΩ (typ) for AINL2/AINR2 pins. The input signal range is 1.5Vpp centered on VCOM voltage. Usually, the input signal cuts DC with a capacitor. The cut-off frequency is fc=(1/2πRC). The AK4569 can accept input voltages from AVSS to AVDD. The ADC output data format is 2's complement. The ADC's DC offset is removed by the internal HPF (fc=3.4Hz@fs=44.1kHz).

4. Analog Outputs

The analog outputs are single-ended outputs and 1.5Vpp(typ) centered on the VCOM voltage. The input data format is 2's compliment. The output voltage is a positive full scale for 7FFFFH(@20bit) and negative full scale for 80000H(@20bit). The ideal output is VCOM voltage for 00000H(@20bit). If the noise generated by the delta-sigma modulator beyond the audio band causes problems, attenuation by an external filter is required.

DC offsets on the analog outputs is eliminated by AC coupling since the analog outputs have a DC offset equal to VCOM plus a few mV.

■ Application Circuit Example

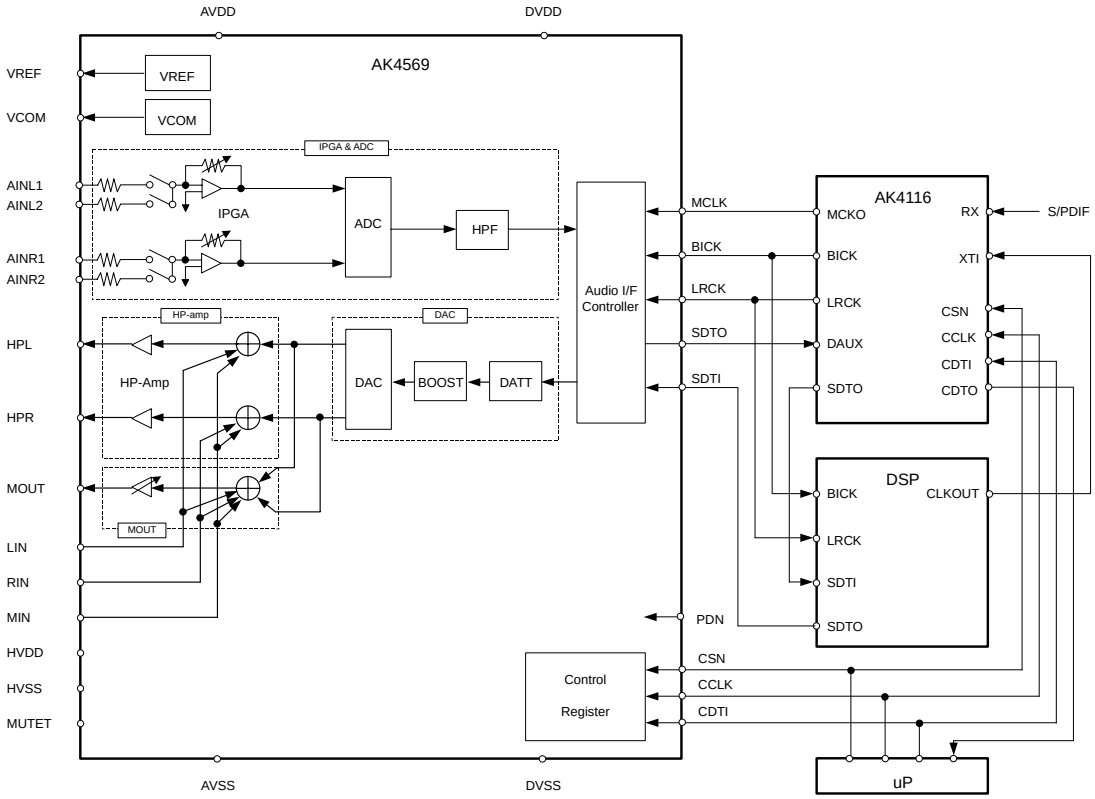


Figure 25. Application Circuit Example

<Clock and Data Flow>

1) Analog Recording

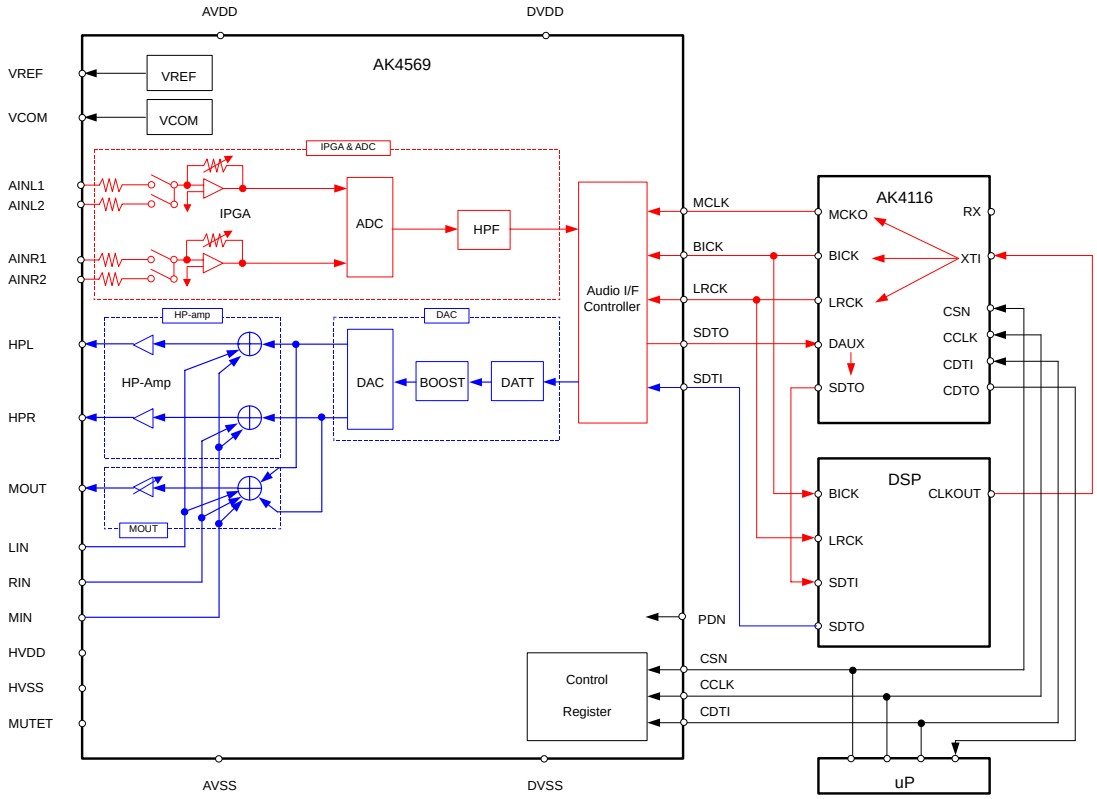


Figure 26. Clock and Data Flow during Analog Recording
(with DAC monitor)

2) Digital Recording

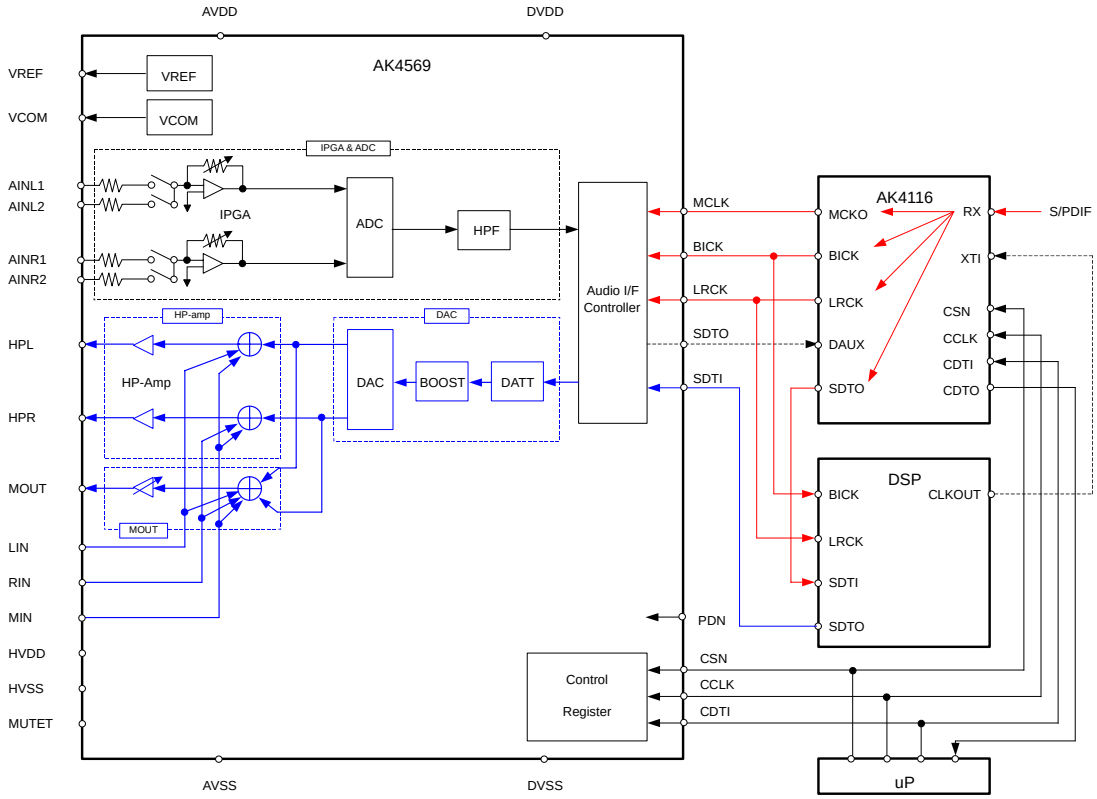


Figure 27. Clock and Data Flow during Digital Recording
(with DAC monitor)

3) Playback

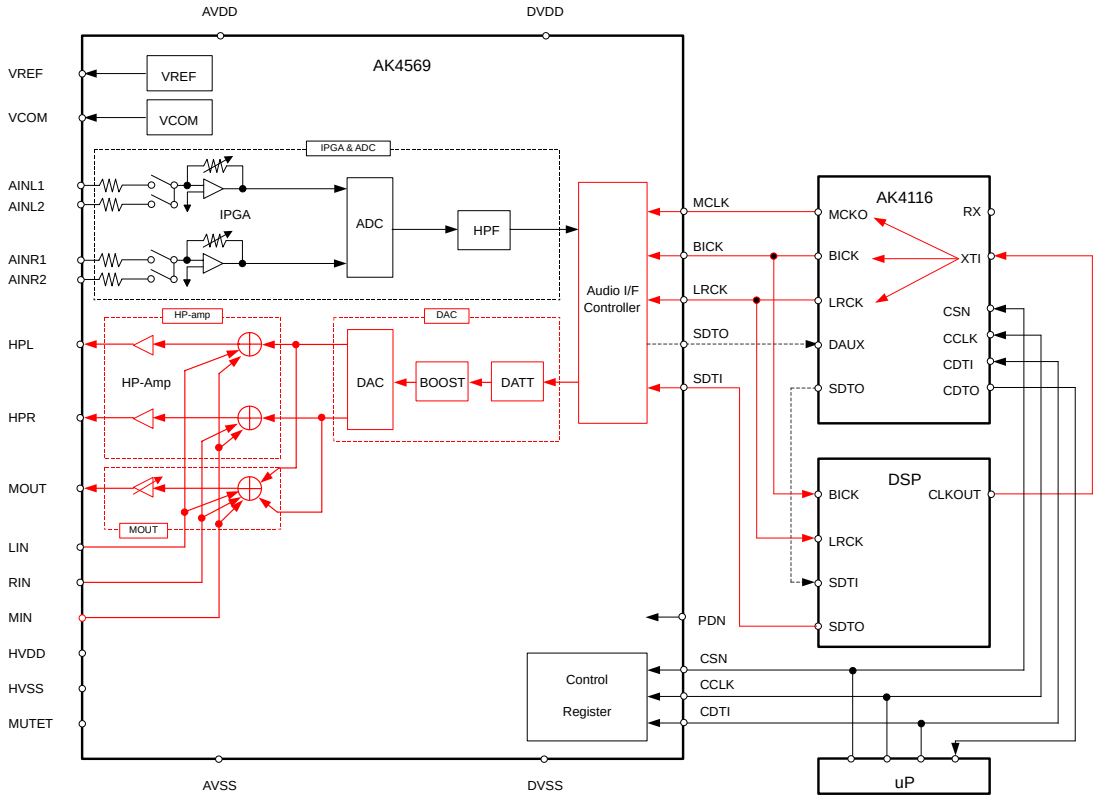
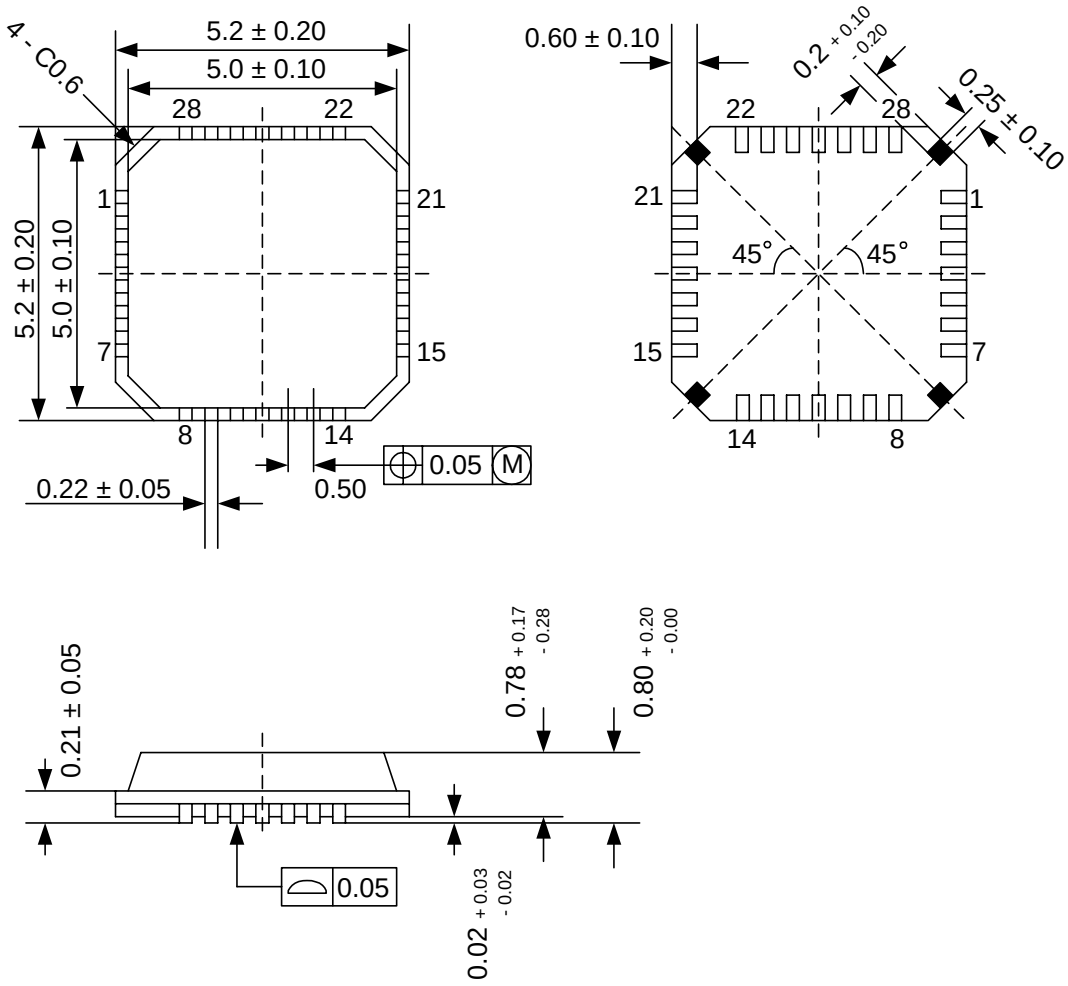


Figure 28. Clock and Data Flow during Playback

PACKAGE

● 28pin QFN (Unit: mm)

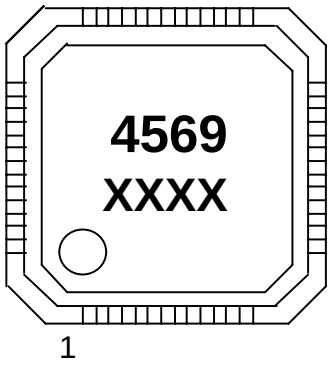


Note: The black parts of back package should be open.

■ Package & Lead frame material

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING



XXXX : Date code identifier (4 digits)

Revision History

Date (YY/MM/DD)	Revision	Reason	Page	Contents
04/02/20	00	First Edition		
05/07/19	01	Error correct	21	Bass Boost Function Figure 16: “AK4566” → “AK4569”
			38-43	System Design Figures 24 to 28: “AK4566” → “AK4569”
			45	Marking “4566” → “4569”

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