AK4563A
Low Power 16bit 4ch ADC & 2ch DAC with ALC

GENERAL DESCRIPTION

The AK4563A is low power operation, 16bit CODEC that include 4ch ADC and 2ch DAC. The AK4563A also includes ALC (Automatic Level Control) circuit, therefore is suitable for microphone application and etc. As the ALC circuit can be stopped by controlling μP, IPGA can also be used as the manual volume. Digital I/F can be input/output from 1.5V to 3.0V by external power supply. The AK4563A can be powered-down by each block, therefore the AK4563A is suitable to low power dissipation in system.

FEATURES

1. **Resolution : 16bits**
2. **Recording Functions**
   - **4ch Analog Input PGA (Programmable Gain Amplifier)**
   - **Digital ALC (Automatic Level Control) circuit**
   - **FADEIN / FADEOUT**
   - **Digital HPF for DC-offset cancellation (fc=3.7Hz@fs=48kHz)**
   - **Peak-Meter Output (2ch)**
3. **Playback Function**
   - **Digital De-emphasis Filter (tc = 50/15μs, fs=32k, 44.1k and 48kHz)**
4. **Power Management**
5. **CODEC (ADC: 4ch, DAC: 2ch)**
   - **Single-ended Inputs/Outputs**
   - **Input / Output Level: 1.5Vpp@VREF=2.5V (= 0.6 x VREF)**
   - **S/(N+D): 83dB(ADC), 86dB(DAC) @VREF=2.5V**
   - **DR, S/N: 87dB(ADC), 91dB(DAC) @VREF=2.5V**
6. **Master Clock: 256fs/384fs**
7. **Sampling Rate: 8kHz ~ 50kHz**
8. **Audio Data Interface Format: MSB-First, 2's compliment (AK4516A Compatible)**
   - **ADC: 16bit MSB justified, 16bit LSB justified, I^2S**
   - **DAC: 16bit MSB justified, 16bit LSB justified, I^2S**
9. **Power Supply**
   - **CODEC, PGA: 2.3 ~ 3.0V (typ.2.5V)**
   - **Digital I/F: 1.5 ~ 3.0V(typ.2.5V)**
10. **Power Supply Current**
    - **ALL Power ON: 18mA**
    - **(ALC + ADC) x 4ch: 13.5mA**
    - **DAC: 5.5mA**
11. **Ta = -20 ~ 85 °C**
12. **Package: 28pin VSOP**

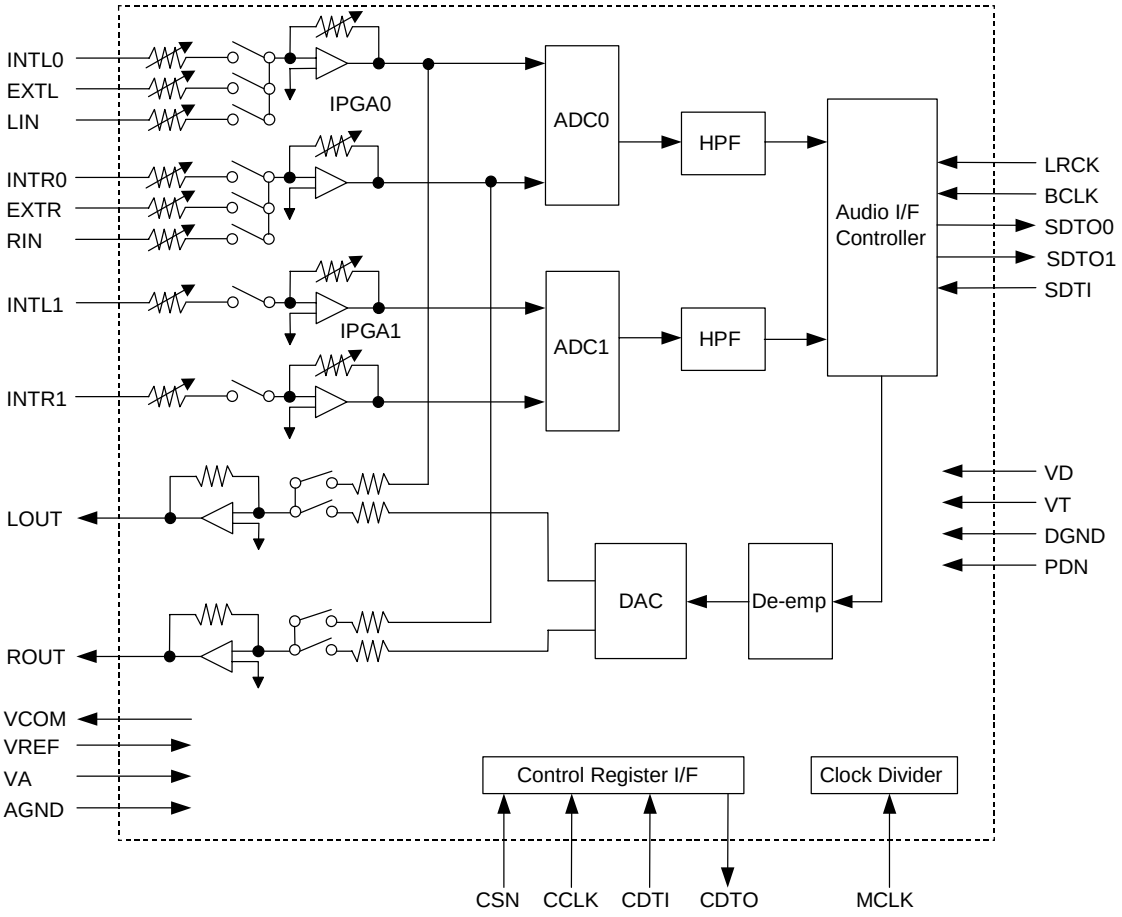
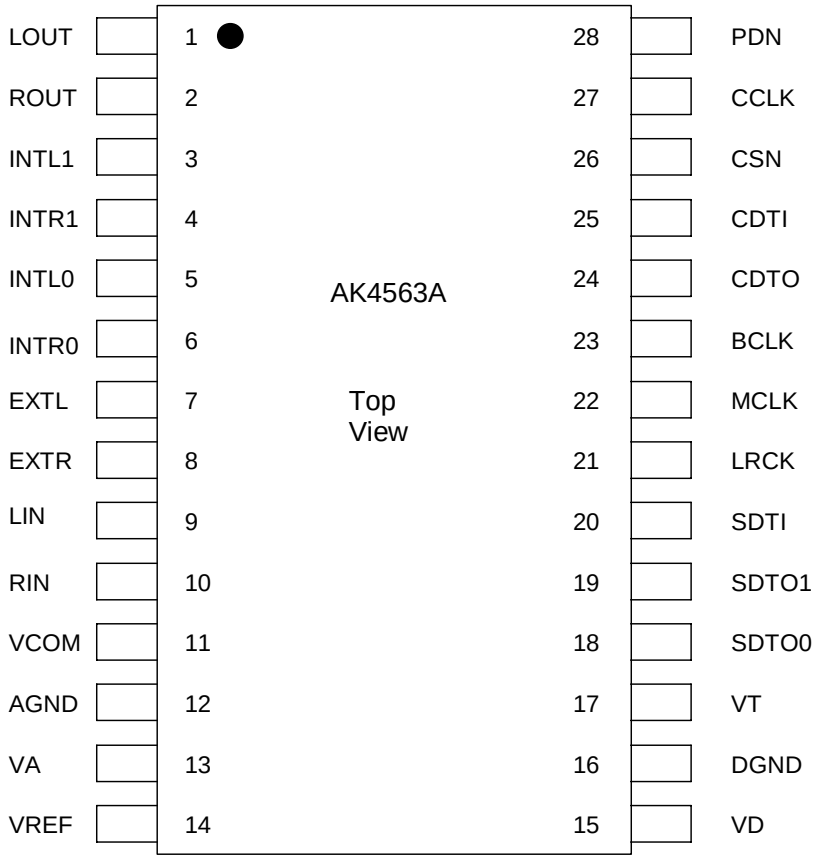


Figure 1. AK4563A Block Diagram

■ Ordering Guide

AK4563AVF	-20 ~ +85°C	28pin VSOP (0.65mm pitch)
AKD4563A	Evaluation board for AK4563A	

■ Pin Layout



PIN / FUNCTION

No.	Pin Name	I/O	Function
1	LOUT	O	Lch Analog Output Pin
2	ROUT	O	Rch Analog Output Pin
3	INTL1	I	Lch INT #1 Input Pin
4	INTR1	I	Rch INT #1 Input Pin
5	INTL0	I	Lch INT #0 Input Pin
6	INTR0	I	Rch INT #0 Input Pin
7	EXTL	I	Lch EXT Input Pin
8	EXTR	I	Rch EXT Input Pin
9	LIN	I	Lch Line Input Pin
10	RIN	I	Rch Line Input Pin
11	VCOM	O	Common Voltage Output Pin, 0.45 x VA Bias voltage of ADC inputs and DAC outputs
12	AGND	-	Analog Ground Pin
13	VA	-	Analog Power Supply Pin, +2.3 ~ 3.0V
14	VREF	I	ADC & DAC Voltage Reference Input Pin, VA Used as a voltage reference of ADC & DAC. VREF is connected externally to fltered VA.
15	VD	-	Digital Power Supply Pin, +2.3 ~ 3.0V
16	DGND	-	Digital Ground Pin
17	VT	-	Digital I/F Power Supply Pin, +1.5 ~ 3.0V
18	SDTO0	O	Audio Serial Data #0 Output Pin
19	SDTO1	O	Audio Serial Data #1 Output Pin
20	SDTI	I	Audio Serial Data Input Pin
21	LRCK	I	Input/Output Channel Clock Pin
22	MCLK	I	Master Clock Input Pin
23	BCLK	I	Audio Serial Data Clock Pin
24	CDTO	O	Control Data Output Pin
25	CDTI	I	Control Data Input Pin
26	CSN	I	Chip Select Pin
27	CCLK	I	Control Data Clock Pin
28	PDN	I	Power Down & Reset Pin, “L”: Power Down & Reset, “H”: Normal Operation

Note: All digital input pins should not be left floating.

ABSOLUATE MAXIMUM RATING

(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supply	Analog (VA pin)	VA	-0.3	4.6	V
	Digital 1 (VD pin)	VD	-0.3	4.6	V
	Digital 2 (VT pin)	VT	-0.3	4.6	V
	| DGND – AGND | (Note 2)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage INTL1-0, INTR1-0, EXTL, EXTR, LIN, RIN, VREF		VINA	-0.3	VA+0.3	V
Digital Input Voltage		VIND	-0.3	VT+0.3	V
Ambient Temperature		Ta	-20	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AGND and DGND should be the same voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supply	Analog (VA pin)	VA	2.3	2.5	3.0	V
	Digital 1 (VD pin) (Note 3)	VD	2.3 or VA-0.3	2.5	VA	V
	Digital 2 (VT pin)	VT	1.5	2.5	VD	V
Reference Voltage	Analog Reference Voltage (VREF pin) (Note 4)	VREF	-	-	VA	V

Note 1. All voltages with respect to ground.
Note 3. Minimum value is the high value either 2.3V or VA-0.3V.
Note 4. VREF and VA should be same voltage.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VA, VD, VT=2.5V; fs=48kHz; Signal Frequency =1kHz; Measurement frequency = 10Hz ~ 20kHz; S/(N+D), D-Range and S/N are value against Full-scale; Unless otherwise specified)

Parameter			min	typ	max	Units
Input PGA Characteristics (IPGA):						
Input Voltage (INTL1-0, INTR1-0, EXTL, EXTR, LIN, RIN pins) (Note 5)			1.35	1.5	1.65	Vpp
Input Resistance: MIC (INTL1-0,INTR1-0,EXTL,EXTR pins)			6.5	10	14.5	kΩ
LINE (LIN, RIN pins)			80	125	176	kΩ
Step Size (Note 6)	MIC	LINE				
	+28dB ~ -8dB	+6dB ~ -30dB	0.1	0.5	0.9	dB
	-8dB ~ -16dB	-30dB ~ -38dB	0.1	1	1.9	dB
	-16dB ~ -32dB	-38dB ~ -54dB	0.1	2	3.9	dB
	-32dB ~ -40dB	-54dB ~ -62dB	-	2	-	dB
	-40dB ~ -52dB	-62dB ~ -74dB	-	4	-	dB
ADC Analog Input Characteristics: (Note 7)						
Resolution					16	Bits
S/(N+D) (-2dBFS Input)			74	83		dB
D-Range (EIAJ)			81	87		dB
S/N (EIAJ)			81	87		dB
Interchannel Isolation			85	100		dB
Interchannel Gain Mismatch				0.2	0.5	dB
DAC Analog Output Characteristics: Measured by LOUT/ROUT						
Resolution					16	Bits
S/(N+D) (0dBFS Input)			77	86		dB
D-Range (EIAJ)			85	91		dB
S/N (EIAJ)			85	91		dB
Interchannel Isolation			85	100		dB
Interchannel Gain Mismatch				0.2	0.5	dB
Output Voltage (Note 8)			1.35	1.5	1.65	Vpp
Load Resistance			10			kΩ
Load Capacitance					20	pF
Power Supplies						
Power Supply Current: VA+VD+VT						
Normal Operation (PDN= "H")						
All Power ON (PM4-0= "1")				18	27	mA
IPGA0+ADC0+IPGA1+ADC1 (PM3-0= "1")			-	13.5	-	mA
DAC (PM4= "1")			-	5.5	-	mA
Power-down mode (PDN= "L") (Note 9)				10	100	μA

Note 5. Full-scale voltage of analog inputs when IPGA0 and IPGA1 bits are "0" and are set to 0dB. Its voltage is proportional to VREF. Vin = 0.6 x VREF.

Note 6. IPGA1 does not have a gain table of LINE side.

Note 7. ADC0 is input from INTL0/INTR0 or EXTL/EXTR or LIN/RIN and it measures included in IPGA0. The gain of IPGA0 is set 0dB. ADC1 is input from INTL1/INTR1 and it measures included in IPGA1. The gain of IPGA1 is set 0dB.
DC-offset in "IPGA0+ADC0" and "IPGA1+ADC1" are cancelled by internal HPF.

Note 8. Analog output voltage is proportional to VREF. Vout = 0.6 x VREF.

Note 9. All digital input pins except for PDN pin are held VT or DGND, and PDN pin is held DGND.

FILTER CHARCTERISTICS

(Ta=25°C; VA, VD=2.3 ~ 3.0V; VT=1.5~ 3.0V; fs=48kHz; De-emphasis = OFF)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 10)	±0.1dB	PB	0		18.9	kHz
	-1.0dB		-	21.8	-	kHz
	-3.0dB		-	23.0	-	kHz
Stopband (Note 10)		SB	29.4			kHz
Passband Ripple		PR			±0.1	dB
Stopband Attenuation		SA	65			dB
Group Delay (Note 11)		GD	-	17.0	-	1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 10)	-3.0dB	FR	-	3.7	-	Hz
	-0.56dB		-	10	-	Hz
	-0.15dB		-	20	-	Hz
DAC Digital Filter:						
Passband (Note 10)	±0.1dB	PB	0		21.7	kHz
	-6.0dB		-	24.0	-	kHz
Stopband (Note 10)		SB	26.2			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay (Note 11)		GD	-	14.8	-	1/fs
Group Delay Distortion		ΔGD		0		μs
DAC Digital Filter + Analog Filter:						
Frequency Response: 0 ~ 20.0kHz		FR		±0.5		dB

Note 10. The passband and stopband frequencies scale with fs. For example, ADC: PB=0.454 x fs(@-1.0dB), DAC: PB=0.454 x fs(@-0.1dB).

Note 11. The calculating delay time which occurred by digital filtering. The time is from the input of analog signal to setting the 16bit data of both channels to the output register for ADC.
For DAC, this time is from setting the 16bit data of both channels on input register to the output of analog signal.

DC CHARACTERISTICS

(Ta=25°C; VA, VD=2.3 ~ 3.0V, VT=1.5 ~ 3.0V)

Parameter	Symbol	min	typ	max	Units
Input High Level Voltage	VIH	80%VT	-	-	V
Input Low Level Voltage	VIL	-	-	20%VT	V
Output High Level Voltage: Iout=-400μA	VOH	VT-0.4	-	-	V
Output Low Level Voltage: Iout=400μA	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARASTERISTICS

(Ta=25°C; VA, VD=2.3 ~ 3.0V, VT=1.5 ~ 3.0V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Control Clock Frequency					
Master Clock(MCLK) 256fs: Frequency	fCLK	2.048	12.288	12.8	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
384fs: Frequency	fCLK	3.072	18.432	19.2	MHz
Pulse Width Low	tCLKL	23			ns
Pulse Width High	tCLKH	23			ns
Channel Selection Clock (LRCK) frequency	fs	8	48	50	kHz
Duty		45	50	55	%
Audio Interface Timing					
BCLK Period	tBLK	312.5			ns
BCLK Pulse Width Low	tBLKL	130			ns
Pulse Width High	tBLKH	130			ns
BCLK "↓" to LRCK	tBLR	-tBLKH+50		tBLKL-50	ns
LRCK to SDTO(MSB) (Except IIS mode)	tDLR			80	ns
BCLK "↓" to SDTO	tDSS			80	ns
SDTI Hold Time	tSDH	50			ns
SDTI Setup Time	tSDS	50			ns
Control Interface Timing					
CCLK Period	tCCK	200(Note 12)			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High 1	tCCKH	80			ns
Pulse Width High 2	tCKH2	80			ns
CDTI Setup Time	tCDS	50			ns
CDTI Hold Time	tCDH	50			ns
CSN "H" Time	tCSW	150(Note 12)			ns
CSN "↓" to CCLK "↑"	tCSS	50(Note 12)			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
CDTO Output Delay Time	tDCD			70	ns
CSN "↑" to CDTO(Hi-Z)(Note 13)	tCCZ			70	ns
Reset/Calibration Timing					
PDN Pulse Width	tPDW	150			ns
PDN "↑" to SDTO0/SDTO1 valid	tPDV		4128		1/fs

Note 12. fs ≥ 22.4kHz.

In the case of fs < 22.4kHz, these three parameters must meet a relationship of (tCSW + tCSS + 6 × tCCK) > 1/(32 × fs) in addition to these specifications. For example, when tCCK=200ns and tCSS=50ns at fs=8kHz, tCSW(min) is 2657ns. When tCSW=150ns and tCSS=50ns fs=8kHz, tCCK(min) is 618ns.

When 08H or 09H address is read and fs < 39.1kHz, tCCK must meet a relationship tCCK > 1/(128 × fs) in addition to these specifications. For example, when fs=8kHz, tCCK(min) is 977ns.

Note 13. R_L=1kΩ/10% Change (Pulled-up operates for VT.)

■ Timing Diagram

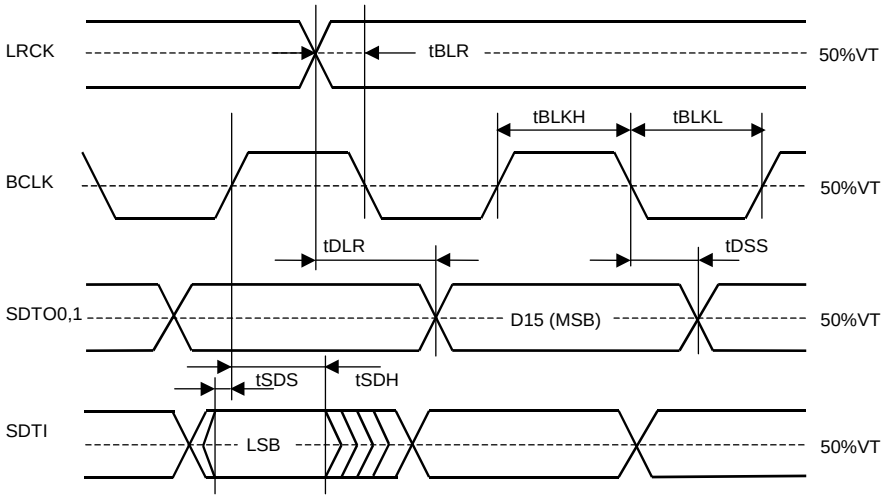


Figure 2. Audio Data Input/Output Timing (Audio I/F Format: No.0)

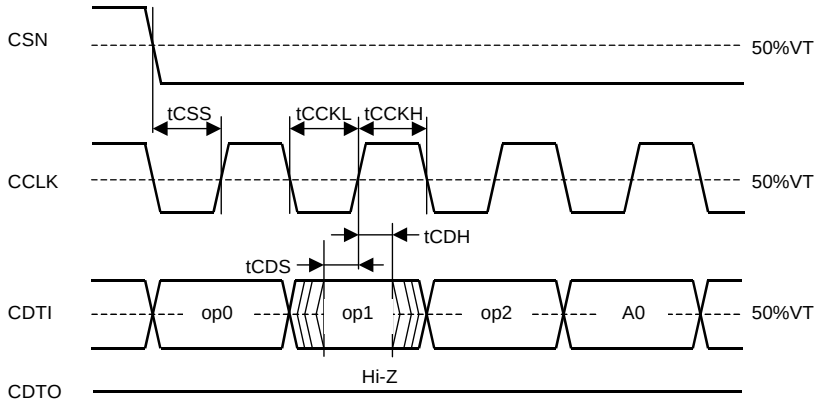


Figure 3. WRITE/READ Command Input Timing

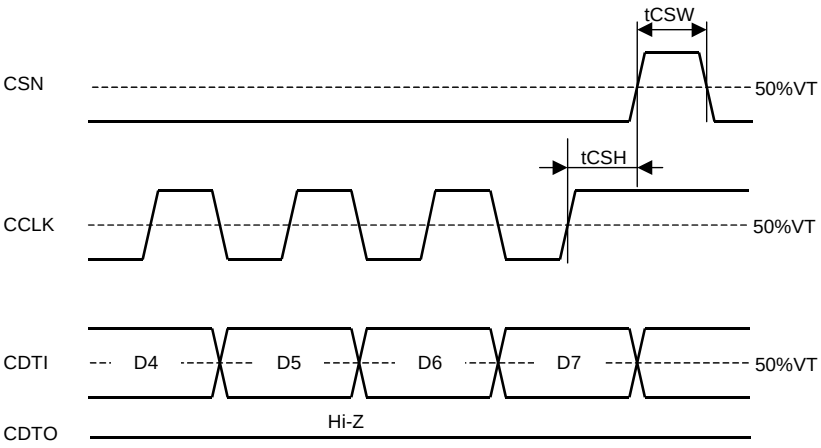


Figure 4. WRITE Data Input Timing

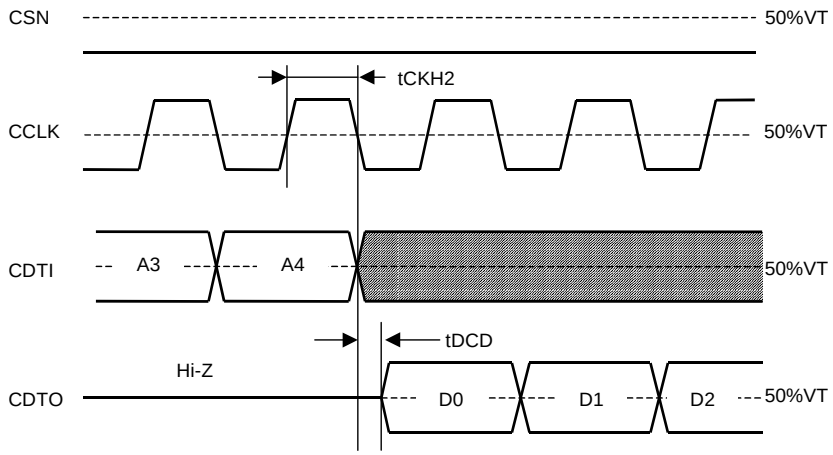


Figure 5. READ Data Output Timing 1

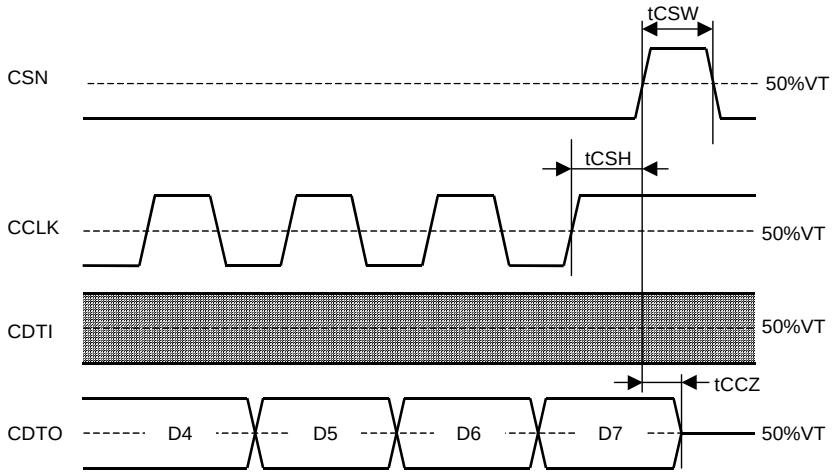


Figure 6. READ Data Input Timing 2

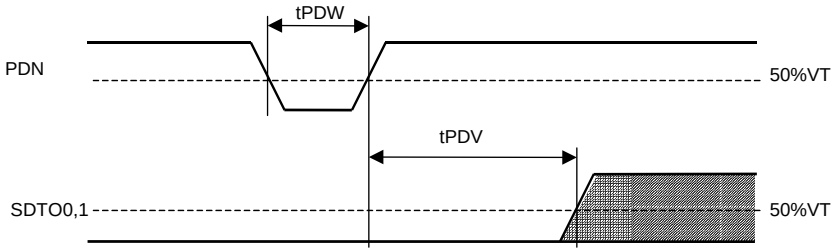


Figure 7. Reset Timing

OPERATION OVERVIEW

■ System Clock Input

The clocks which are required to operate are MCLK (256fs/384fs), LRCK (fs) and BCLK (32fs~). The master clock (MCLK) should be synchronized with LRCK but the phase is free of care.
The MCLK can be input 256fs or 384fs. When 384fs is input, the internal master clock is divided into 2/3 automatically.
*fs is sampling frequency.

All external clocks (MCLK, BCLK and LRCK) should always be present whenever ADC or DAC is in operation. If these clocks are not provided, the AK4563A may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4563A should be in the power-down mode.

■ System Reset

AK4563A should be reset once by bringing PDN pin “L” upon power-up. After the system reset operation, the all internal AK4563A registers are initial value.

The initial cycle is 4128/fs=86ms@fs=48kHz. During offset calibration, the ADC digital data outputs of both channels are forced to a 2’s compliment “0”. Output data of settles data equivalent for analog input signal after offset calibration. This cycle is not for DAC.

As a normal offset calibration may not be executed, nothing write at address 01H during offset calibration.

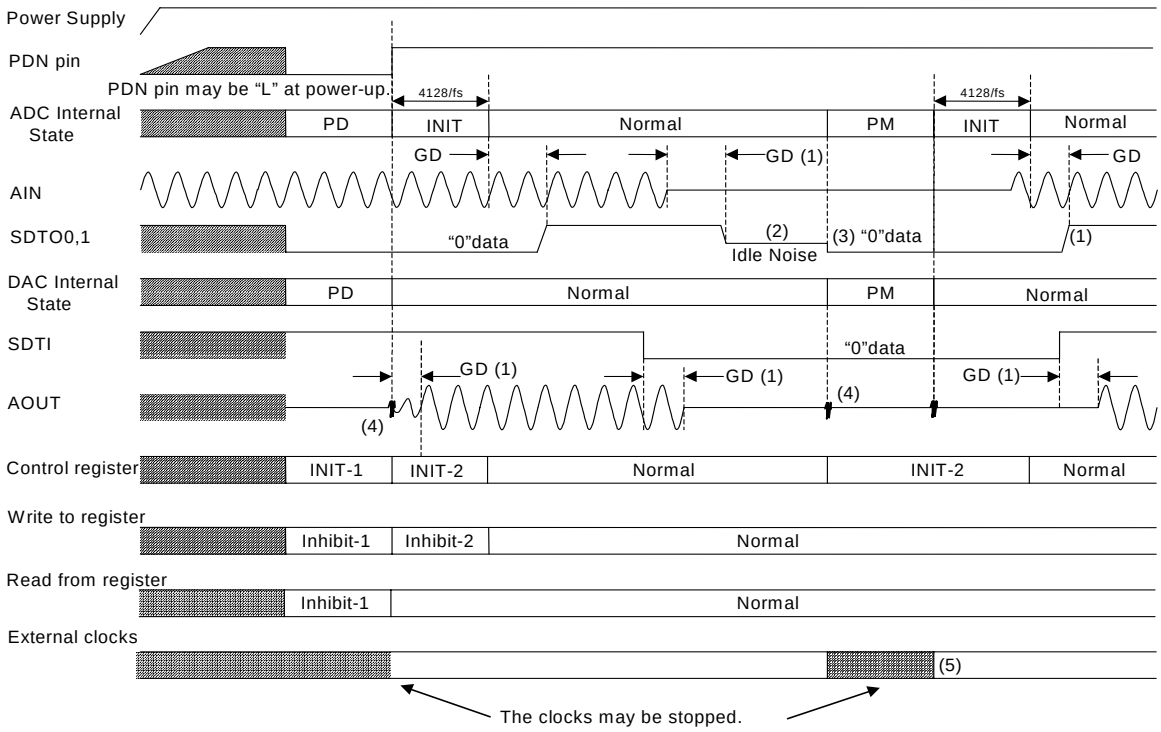


Figure 8. Power-up/Power-down Timing Example

- INIT: Initializing. At this time, STAT bit is "0". When this flag becomes "1", INIT process has completed. IPGA0 and IPGA1 are MUTE state.
- PD: Power-down state. ADC is output "0", analog output of DAC goes floating.
- PM: Power-down state by operating Power Management bit
- INIT-1: Initializing all registers.
- INIT-2: Initializing read only registers in control registers.
- Inhibit-1: Inhibits writing and reading to all control registers.
- Inhibit-2: Inhibits writing to all control registers.

Note: Please refer to "explanation of register" about the condition of each register.

(1) Digital output corresponding to analog input and analog output corresponding to digital input have the group delay (GD).
(2) If the analog signal does not be input, the digital outputs have the op-amp of input and some noise in ADC.
(3) ADC data is "0" data at power-down.
(4) A few noise occurs at the "↓ ↑" of PDN signal. Please mute the analog output externally if the noise influences the system application.
(5) When the external clocks are stopped, the AK4563A should be in the power-down mode (PDN pin = "L" or PM5-0 bit = "0") .

■ Digital High Pass Filter (HPF)

The ADC has HPF for the DC offset cancel. The cut-off frequency of HPF is 3.7Hz (@fs=48kHz) and it is -0.15dB at 20Hz. It also scales with the sampling frequency (fs).

■ Audio Serial Interface Format

Data is shifted in/out the SDTI/SDTO0, 1 pins using BCLK and LRCK inputs. Four serial data are selected by the DIF0 and DIF1 pins as shown in Table 1. In all modes, the serial data is MSB-first, 2's compliment format and it is latched by "↑" of BCLK.
When DIF1= "0" and DIF0="1", only BCLK=64fs is acceptable.

No.	DIF1 bit	DIF0 bit	SDTO0/SDTO1(ADC)	SDTI(DAC)	BCLK	Figure	
0	0	0	MSB justified	LSB justified	≥ 32fs	Figure 9	RESET
1	0	1	LSB justified	LSB justified	= 64fs	Figure 10	
2	1	0	MSB justified	MSB justified	≥ 32fs	Figure 11	
3	1	1	I^2S compatible	I^2S compatible	≥ 32fs	Figure 12	

Table 1. Audio Data Format

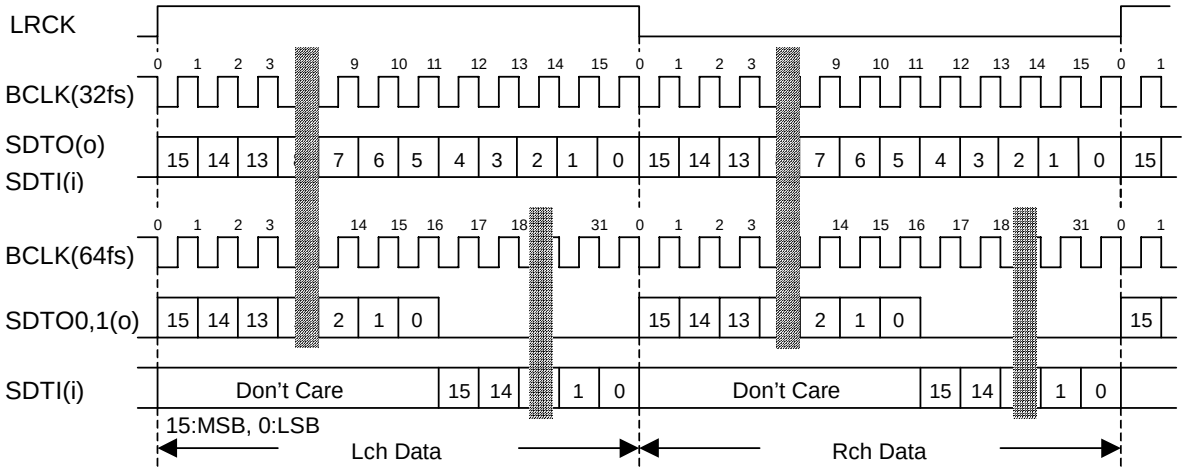


Figure 9. Audio Data Timing (No.0)

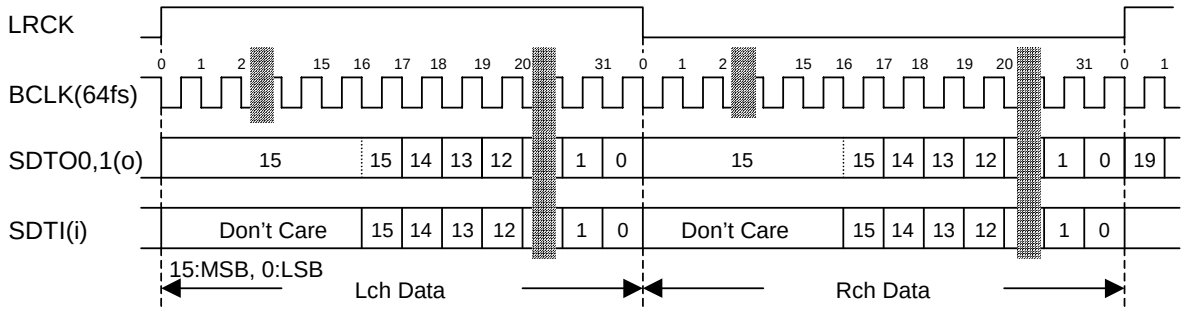


Figure 10. Audio Data Timing (No.1)

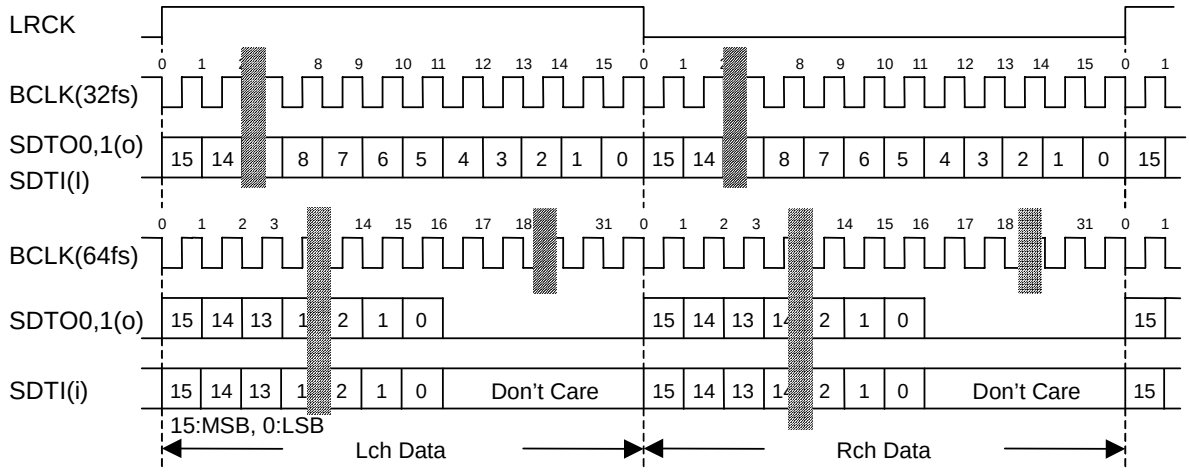


Figure 11. Audio Data Timing (No.2)

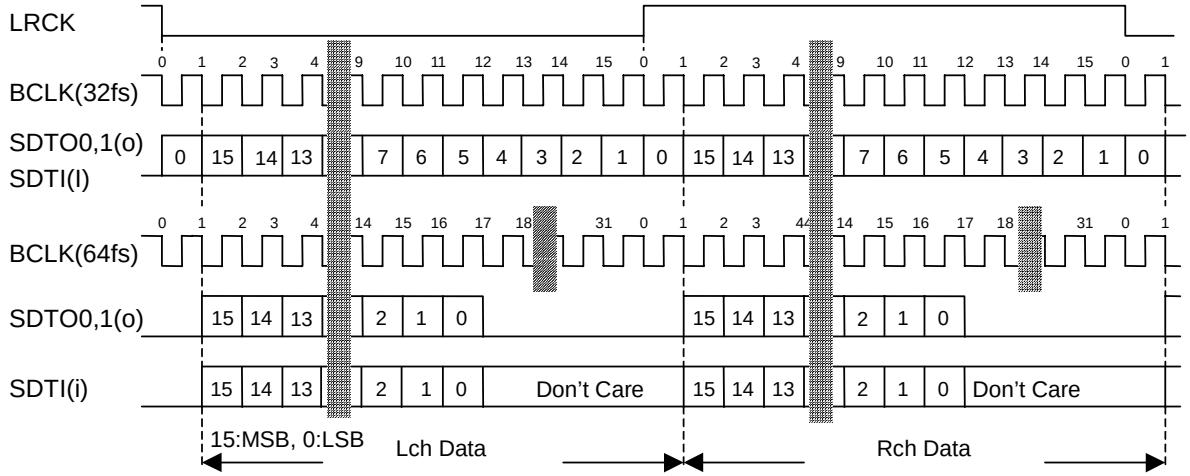
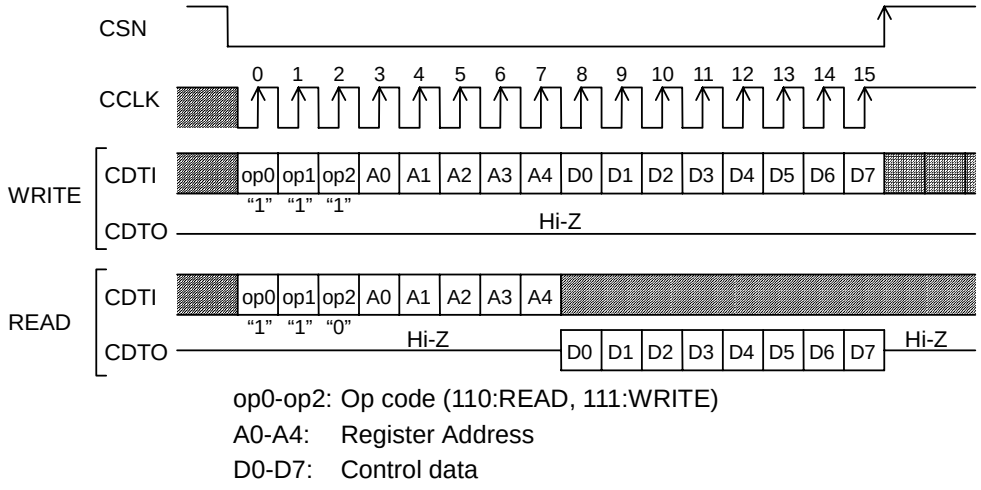


Figure 12. Audio Data Timing (No.3)

■ Control Register R/W Timing

The data on the 4 wires serial interface consists of op-code (3bit), address (LSB-first, 5bit) and control data (LSB-first, 8bit). The transmitting data is output to each bit by "↓" of CCLK, the receiving data is latched by "↑" of CCLK. Writing data becomes effective by "↑" of CSN. Reading data becomes Hi-z (Floating) by "↑" of CSN. CSN should be held to "H" at no access. In case of connecting between CDTI and CDTO, the I/F can be also contolled by 3-wires.

CCLK always needs 16 edges of "↑" during CSN = "L". Reading/Writing of the address except 00H ~ 09H are inhibited. Reading/Writing of the control registers by except op0 = op1 = "1" are invalid.



op0-op2: Op code (110:READ, 111:WRITE)
A0-A4: Register Address
D0-D7: Control data

Figure 13. Control Data Timing

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Input Select	0	0	0	0	LINE	EXT	INT1	INT0
01H	Power Management	0	0	PM5	PM4	PM3	PM2	PM1	PM0
02H	Mode Control	0	0	0	FS	DIF1	DIF0	DEM1	DEM0
03H	Timer Select	FDTM1	FDTM0	ZTM1	ZTM0	WTM1	WTM0	LTM1	LTM0
04H	ALC Mode Control 1	0	0	LMAT1	LMAT0	FDATT	RATT1	RATT0	LMTH
05H	ALC Mode Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0
06H	Operation Mode	0	0	ZELMN	FR	STAT	FDIN	FDOUT	ALC
07H	Input PGA Control	0	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
08H	Peak Hold Lch	PHL7	PHL6	PHL5	PHL4	PHL3	PHL2	PHL1	PHL0
09H	Peak Hold Rch	PHR7	PHR6	PHR5	PHR4	PHR3	PHR2	PHR1	PHR0

■ Register Definitions

The following condition can not read and write all registers.
*** PDN pin = "L"**

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Input Select	0	0	0	0	LINE	EXT	INT1	INT0
R/W		R/W							
RESET		0	0	0	0	0	0	1	1

INT0: Select ON/OFF of INTL0 and INTR0 (0: OFF, 1: ON)
INT1: Select ON/OFF of INTL1 and INTR1 (0: OFF, 1: ON)
EXT: Select ON/OFF of EXTL and EXTR (0: OFF, 1: ON)
LINE: Select ON/OFF of LIN and RIN (0:OFF, 1:ON)

When LINE bit is "1", INT0, INT1 and EXT bits are ignored.
Gain tables of IPGA0 and IPGA1 are changed by LINE bit.
When LINE bit is "1", gain table of IPGA becomes LINE side. But IPGA1 becomes mute state because it does not have a LINE table.

When INT0 and EXT bits change into "1" at the same time, input signals are mixed by Gain 0dB.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management	0	0	PM5	PM4	PM3	PM2	PM1	PM0
R/W		R/W							
RESET		0	0	0	1	1	1	1	1

PM5-0: Power Management (0: Power down, 1: Power up)

PM1-0: IPGA and ALC circuit power control.
After exiting PM1-0 = "00", IPGA goes reset value. (refer to "Operation of IPGA" description)

PM1	PM0	IPGA1	IPGA0	
0	0	OFF	OFF	
0	1	OFF	ON	
1	0	Lch ON	ON	
1	1	ON	ON	RESET

Table 2. IPGA and ALC circuit power control

PM3-2: Power control of ADC

PM3	PM2	ADC1	ADC0	
0	0	OFF	OFF	
0	1	OFF	ON	
1	0	Lch ON	ON	
1	1	ON	ON	RESET

Table 3. ADC power control

When the number of ADC channels is changed, PM3-2 bits should be via "00" (ADC0 and ADC1 are powerd-down.).
For example, in case of changing from 2ch mode (PM3-2 bits = "01") to 4ch mode (PM3-2 bit = "11"), PM3-2 bit should change into "11" via "00".

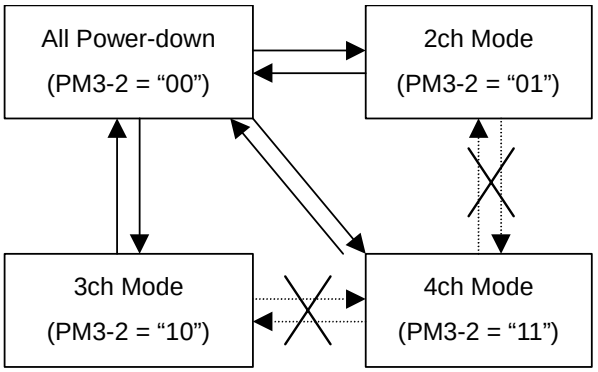


Figure 14. ADC Power-up/down Sequence by Power Management bit

In case of exiting all power-down mode (PM3-2 = "00"), the initializing cycle (4128/fs) is started. Then all outputs of ADC become "0".

In case of 3ch mode (PM1-0 = "10", PM3-2 = "10"), right channel of IPGA1 and ADC1 is powered-down. Then right channel of ADC1 is output "0".

PM4: Power control of DAC
PM5: Used both as power control of analog loopback circuit and as selection of MUX. (0: DAC, 1: Analog loopback)

When PM5 goes “1”, input for output-AMP is selected to analog loopback circuit from DAC output. Output MUX and AMP are powered-down when PDN = “L” or PM4 = PM5 = “0”.

The loopback output and the MUX selecting DAC output is a MIXER with the switch in practice. Therefore, when both PM4 and PM5 select ON, the analog loopback signal and DAC output are mixed by Gain 1.

PM5-0 bits can be partially powered-down by ON/OFF (“1”/ “0”) of PM5-0 bits. When PDN pin goes “L”, all the circuit in AK4563A can be powered-down regardless of PM5-0 bits.
When the AK4563A is powered-down by PM5-0 bits, contents of registers are kept.
However IPGA gain is reset when PM1-0 bits are “00”. (refer to “Operation of IPGA” description)

VCOM circuit is powered-down when PM bit is all “0”.

MCLK, BCLK and LRCK should not stopped except the case of PM0 = PM1 = PM2 = PM3 = PM4 = PM5 = “0” or PDN= “L”.

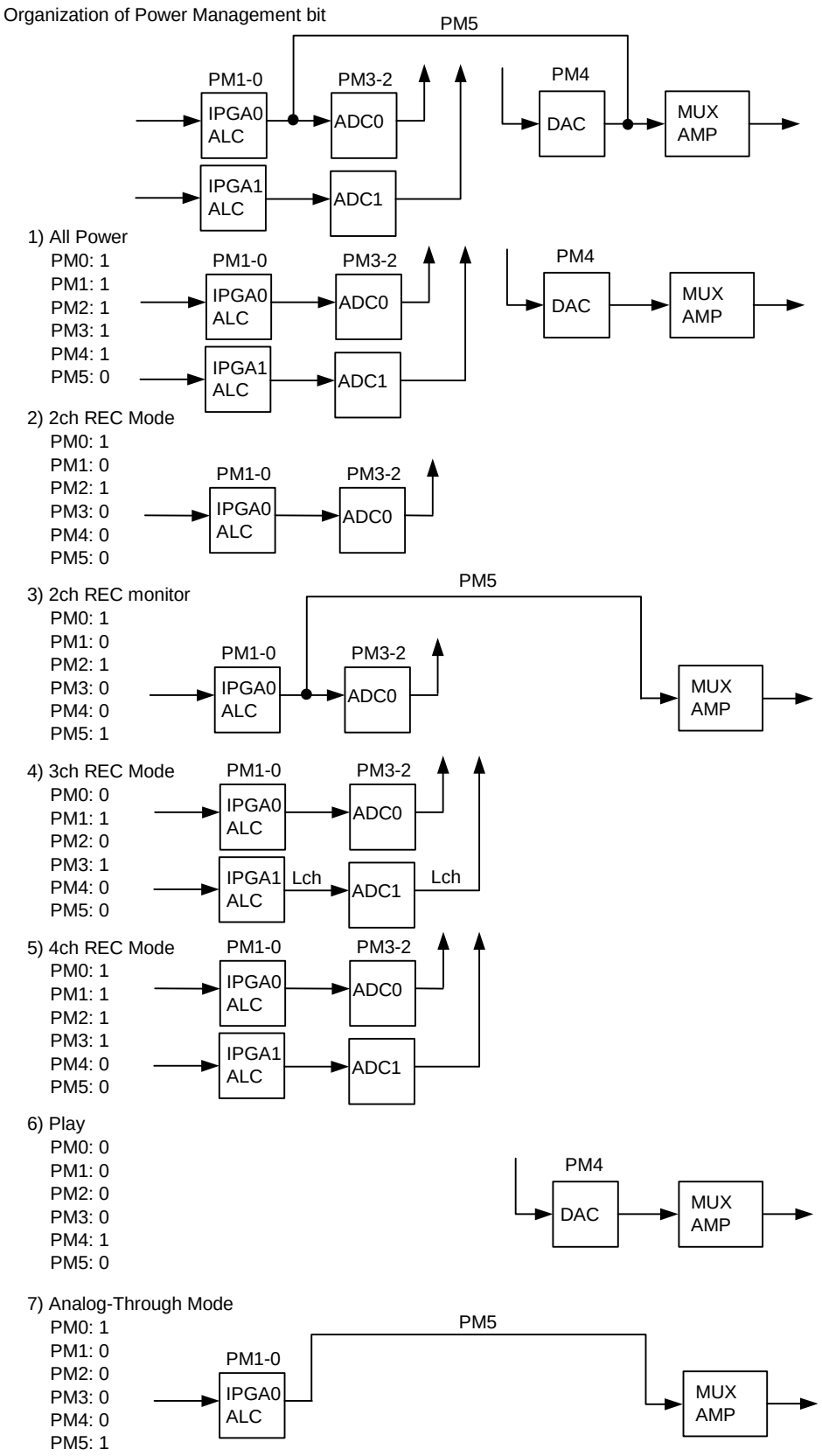


Figure 15. Power Management

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Mode Control	0	0	0	FS	DIF1	DIF0	DEM1	DEM0
R/W		R/W							
RESET		0	0	0	1	0	0	0	1

DEM1-0: Select De-emphasis frequency

The AK4563A includes the digital de-emphasis filter (tc = 50/15μs) by IIR filter. The filter corresponds to three sampling frequencies (32kHz, 44,1kHz and 48kHz). The de-emphasis filter selected by DEM0 and DEM0 bits are enabled for input audio data.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	RESET
1	0	48kHz	
1	1	32kHz	

Table 4. Select De-emphasis frequency

DIF1-0: Select Audio Serial Interface Format (AK4516A compatible)

No.	DIF1	DIF0	SDTO0/SDTO1(ADC)	SDTI(DAC)	BCLK	Figure	
0	0	0	MSB justified	LSB justified	≥ 32fs	Figure 9	RESET
1	0	1	LSB justified	LSB justified	=64fs	Figure 10	
2	1	0	MSB justified	MSB justified	≥ 32fs	Figure 11	
3	1	1	I^2S compatible	I^2S compatible	≥ 32fs	Figure 12	

Table 5. Select Audio Serial Interface Format

FS: Select Sampling Frequency

0:fs=32kHz

1:fs=48kHz (RESET)

FS bit can set limiter period (LTM1-0 bit), recovery period (WTM1-0 bit), zero crossing timeout (ZTM1-0 bit) and FADEIN/FADEOUT period (FDTM1-0 bit) the same period at fs=32kHz and 48kHz.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Timer Select	FDTM1	FDTM0	ZTM1	ZTM0	WTM1	WTM0	LTM1	LTM0
R/W		R/W							
RESET		0	0	0	0	0	0	0	1

LTM1-0: ALC Limiter Period

The IPGA value is changed immediately. When the IPGA value is changed continuously, the change is done by the period specified by LTM1-0 bit.

These periods are value at fs=32kHz (FS bit = "0") or fs=48kHz (FS bit = "1").

LTM1	LTM0	Period	
0	0	63μs	
0	1	125μs	RESET
1	0	250μs	
1	1	500μs	

Table 6. ALC Limiter Operation Period

WTM1-0: ALC Recovery Waiting Period

A period of recovery operation when any limiter operation does not during ALC operation.

Recovery operation is done at period set by WTM1-0 bits.

When the input signal level exceeds auto recovery waiting counter reset level set by LMTH bit, the auto recovery waiting counter is reset.

The waiting timer starts when the input signal level becomes below the auto recovery waiting counter reset level.

These periods are value at fs=32kHz (FS bit = "0") or fs=48kHz (FS bit = "1").

WTM1	WTM0	Period	
0	0	8ms	RESET
0	1	16ms	
1	0	64ms	
1	1	512ms	

Table 7. ALC Recovery Operation Waiting Period

ZTM1-0: Zero crossing timeout at writing operation by μP and ALC recovery operation

When IPGA of each L/R channels do zero crossing or timeout independently, the IPGA value is changed by μP WRITE operation or ALC recovery operation.

These periods are value at fs=32kHz (FS bit = "0") or fs=48kHz (FS bit = "1").

ZTM1	ZTM0	Period	
0	0	8ms	RESET
0	1	16ms	
1	0	64ms	
1	1	512ms	

Table 8. Zero Crossing Timeout

FDTM1-0: FADEIN/OUT Period Setting

The FADEIN/OUT operation is done by a period set by FDTM1-0 bits when FDIN or FDOUT bits are set "1". When IPGA of each L/R channel do zero crossing or timeout independently, the IPGA value is changed.

These period are value at fs=32kHz (FS bit = "0") or fs=48kHz (FS bit = "1").

FDTM1	FDTM0	Period	
0	0	24ms	RESET
0	1	32ms	
1	0	48ms	
1	1	64ms	

Table 9. FADEIN/OUT Period

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	ALC Mode Control 1	0	0	LMAT1	LMAT0	FDATT	RATT1	RATT0	LMTH
R/W		R/W							
RESET		0	0	0	0	0	0	0	0

LMTH: Auto Limiter Detection Level / Auto Recovery Waiting Counter Reset Level

LMTH	ALC Limiter Detection Level	ALC Recovery Waiting Counter Reset Level
0	ADC Input ≥ –4.0dB	-4.0dB > ADC Input ≥ -6.0dB
1	ADC Input ≥ –2.0dB	-2.0dB > ADC Input ≥ -4.0dB

RESET

Table 10. Auto Limiter Detection Level / Auto Recovery Waiting Counter Reset Level

RATT1-0: ALC Recovery GAIN Step

During the ALC recovery operation, the number of steps changed from current IPGA value is set. For example, when the current IPGA value is 30H, RATT1= “0”, RATT0= “1” are set, IPGA changes to 32H by the auto limiter operation, the input signal level is gained by 1dB (=0.5dB x 2).

When the IPGA value exceeds the reference level (REF6-0), the IPGA value does not increase.

RATT1	RATT0	GAIN Step
0	0	1
0	1	2
1	0	3
1	1	4

RESET

Table 11. ALC Recovery GAIN Step

FDATT: FADEIN/OUT ATT Step

During the FADEIN/OUT operation, the number of steps changed from current IPGA value is set. For example, when the current IPGA value is 30H, FDATT = “1” are set, IPGA changes to 32H (FADEIN) or 2EH (FADEOUT) by the FADEIN/OUT operation, the input signal level is gained by 1dB(=0.5dB x 2).

When the IPGA value exceeds the reference level (REF6-0) or 00H, the IPGA value does not increase.

FDATT	ATT Step
0	1
1	2

RESET

Table 12. FADEIN/OUT ATT Step

LMAT1-0: ALC Limiter ATT Step

During the ALC limiter operation, when input signal exceeds the ALC limiter detection level set by LMTH, the number of steps attenuated from current IPGA value is set. For example, when the current IPGA value is 68H in the state of LMAT1-0 = “11”, it becomes IPGA=64H by the ALC limiter operation, the input signal level is attenuated by 2dB (=0.5dB x 4).

The ALC limiter period is set by LTM1-0 bits at ZELMN = “1” and ZTM1-0 bits at ZELMN = “0”.

When the attenuation value exceeds IPGA = “00H” (MUTE), it clips to “00”.

LMAT1	LMAT0	ATT Step
0	0	1
0	1	2
1	0	3
1	1	4

RESET

Table 13. ALC Limiter ATT Step

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	ALC Mode Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0
R/W		R/W							
RESET		0	28H						

REF6-0: Set the Reference value at ALC Recovery Operation

During the ALC recovery operation, when IPGA value becomes the reference value set by REF6-0, the gain of the ALC recovery operation exceeds the reference value. The reference value is set commonly as for Lch and Rch of IPGA0 and IPGA1.

During the ALC recovery operation, if IPGA value exceeds the setting reference value by GAIN operation, IPGA does not become the larger than the reference value.

For example, when REF6-0 = 30H, RATT = 2 step and IPGA = 2FH, IPGA will become 2FH + 2 step = 31H by the ALC recovery operation, but IPGA value becomes 30H as REF value is 30H.

IPGA should be certainly set to the same value or smaller than REF value before entering ALC mode (including the FADEIN/OUT operation).

DATA	GAIN(dB)		Step	Level
	MIC	LINE		
60H	+28.0	+6.0	0.5dB	73
5FH	+27.5	+5.5		
5EH	+27.0	+5.0		
•	•	•		
28H	+0.0	-22.0		
27H	-0.5	-22.5		
•	•	•		
19H	-7.5	-29.5		
18H	-8.0	-30.0		
17H	-9.0	-31.0	1dB	8
16H	-10.0	-32.0		
•	•	•		
11H	-15.0	-37.0		
10H	-16.0	-38.0		
0FH	-18.0	-40.0	2dB	12
0EH	-20.0	-42.0		
•	•	•		
05H	-38.0	-60.0		
04H	-40.0	-62.0		
03H	-44.0	-66.0	4dB	3
02H	-48.0	-70.0		
01H	-52.0	-74.0		
00H	MUTE	MUTE		1

Table 14. Setting Reference Value at ALC Recovery Operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Operation Mode	0	0	ZELMN	FR	STAT	FDIN	FDOUT	ALC
R/W		R/W				RD	R/W		
RESET		0	0	0	0	0	0	0	0

ALC: ALC Enable Flag
0: ALC Disable (RESET)
1: ALC Enable

FDOUT: FADEOUT Enable Flag
0: FADEOUT Disable (RESET)
1: FADEOUT Enable

FDIN: FADEIN Enable Flag
0: FADEIN Disable (RESET)
1: FADEIN Enable

STAT: Status Flag
0: ALC (including FADEIN and FADEOUT) operation or initializing operation (RESET)
1: Manual Mode

STAT bit is “0” during initializing operation after exiting power-down by PDN pin. After the finish of the initializing operation, STAT bit becomes “1”.

During the ALC operation, STAT bit becomes “1” after the max “1” ATT/GAIN operation is completed by internal state.

FR: Select ALC operation Mode
0: The ALC operation corresponds to impulse noise. (RESET)
1: The ALC operation is the same as AK4516A

ZELMN: Enable zero crossing detection at ALC Limiter operation
0: Enable (RESET)
1: Disable
In case of ZELMN = “0”, IPGA of each L/R channel do zero crossing or timeout independently, the IPGA value is changed by the ALC operation. Zero crossing timeout is the same as the ALC recovery operation. In case of ZELMN = “1”, the IPGA value is changed immediately.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Input PGA Control	0	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
R/W		R/W							
RESET		0	28H						

IPGA6-0: Input Analog PGA; 97 levels; Commonly Lch and Rch of IPGA0 and IPGA1.

The IPGA value should be the same or smaller than REF value before the ALC1 operation including the FADEIN/FADEOUT operation.

When IPGA gain is changed, IPGA6-0 bits should be written while PM1-0 bits are not "00" and ALC bit is "0". (refer to "Operation of IPGA" description)

DATA	GAIN(dB)		Step	Level
	MIC	LINE		
60H	+28.0	+6.0	0.5dB	73
5FH	+27.5	+5.5		
5EH	+27.0	+5.0		
•	•	•		
28H	+0.0	-22.0		
27H	-0.5	-22.5		
•	•	•		
19H	-7.5	-29.5		
18H	-8.0	-30.0		
17H	-9.0	-31.0	1dB	8
16H	-10.0	-32.0		
•	•	•		
11H	-15.0	-37.0		
10H	-16.0	-38.0		
0FH	-18.0	-40.0	2dB	12
0EH	-20.0	-42.0		
•	•	•		
05H	-38.0	-60.0		
04H	-40.0	-62.0		
03H	-44.0	-66.0	4dB	3
02H	-48.0	-70.0		
01H	-52.0	-74.0		
00H	MUTE	MUTE		1

Table 15. Input Gain Setting

There is not LINE table in IPGA1

IPGA value is reset at PM1-0 = "00".

■ Operation of IPGA

[Reading operation]

When the IPGA value is read by μP, the IPGA value is the written value finally. Therefore, the actual value may differ to the IPGA value which is read by μP.

[Writing operation at ALC Enable]

During the ALC operation including the FADEIN/OUT operation, if the IPGA value is written by uP, the IPGA value does not reflect the present value.

[Writing operation at ALC Disable]

The zero crossing detection of IPGA is done to L/R channels independently. Zero crossing timeout is set by ZTM1-0 bits.
When the control register is written from μP, the zero crossing counter for L/R channels commonly is reset and its counter starts. When the signal detects zero crossing or zero crossing timeout, the written value from μP becomes a valid for the first time.
In case of writing to the control register continually, the control register should be written by an interval more than zero crossing timeout. If an appointed interval is written, there is possible to the different value the IPGA value of L/R channels. For example, when the present IPGA value is updated by zero crossing detection in a channel of one side and other channel is not updated, if the new data is written in IPGA, the updated channel is keeping the last IPGA value and other channel is updated to a new IPGA value by the last zero crossing counter. Therefore, zero crossing counter does not reset when the zero crossing detection is waiting.

[IPGA Gain after completing ALC operation]

The IPGA gain changed by ALC operation is not reflected to the IPGA register. Therefore, when completing ALC operation (ALC bit; "1" → "0"), the IPGA register is different from the actual gain of IPGA. The value should be re-written to the IPGA register in order to set the actual gain of IPGA with a register value.

[Operation of IPGA at power-down by the control register]

Gain of IPGA0 and IPGA1 is reset when PM1-0 bits are "00", and then IPGA operation starts from the default value after exiting PM1-0 bits = "00". When IPGA6-0 bits are read, the register values written by the last write operation are read out regardless the actual gain.

[Operation of IPGA when the number of IPGA channels is changed]

When the number of IPGA channels is changed, PM1-0 bits should be done via "00". If PM1-0 bits are not done via "00", there is a possibility that gain between IPGA0 and IPGA1 is different. However, powered-up all channels become the same gain when IPGA value is written at ALC disabled state (ALC bit = "0") or the ALC Limiter/Recovery operation is done.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Lch Peak Hold	PHL7	PHL6	PHL5	PHL4	PHL3	PHL2	PHL1	PHL0
09H	Rch Peak Hold	PHR7	PHR6	PHR5	PHR4	PHR3	PHR2	PHR1	PHR0
R/W		RD							
RESET		00H							

PHL7-0: Lch Peak Hold (Absolute Value)
PHR7-0: Rch Peak Hold (Absolute Value)

The peak data is output from **ADC0,** it is held L/R independently.
These registers are reset by reading from μP.

$20 \times \log_{10} [(Data) / 256)] < Peak\ Level\ [dB] \leq 20 \times \log_{10} [(Data+1) / 256)]$

Data	Peak Level
FFH	0.0dB ~ -0.034 dB
FEH	-0.034dB ~ -0.068dB
FDH	-0.068dB ~ -0.102dB
•	•
02H	-38.62dB ~ -42.14dB
01H	-42.14dB ~ -48.16dB
00H	-48.16dB ~ -∞(infinity)

Table 16. Peak Level

These registers are reset on the following any conditions.
- PDN pin = “L”
- PM2 = PM3 = “0”

FUNCTION DETAIL

■ ALC Operation

1. ALC Limiter Operation

During the ALC limiter operation, when either Lch or Rch in IPGA0 and IPGA1 exceed ALC limiter detection level (LMTH), IPGA value is attenuated by ALC limiter ATT step (LMAT1-0) automatically. Then the IPGA value is changed commonly for L/R channels in IPGA0 and IPGA1. Timeout period is set by LTM1-0 bits. The operation for attenuation is done continuously until the input signal level becomes LMTH or less. After finishing the operation for attenuation, if ALC bit does not change into "0", the operation of attenuation repeats when the input signal level exceed LMTH.

When FR bit is "0", the ALC operation corresponds to the impulse noise in additional to the ALC operation of AK4516A. Then if the impulse noise is supplied at ZELMN = "0", the ALC recovery operation becomes the faster period than a set of ZTM1-0 bits. In case of ZELMN = "1", it becomes the same period as LTM1-0 bits.
When FR bit is "1", the ALC operation in AK4563A is the same as AK4516A's.

[Explanation for ALC operation]

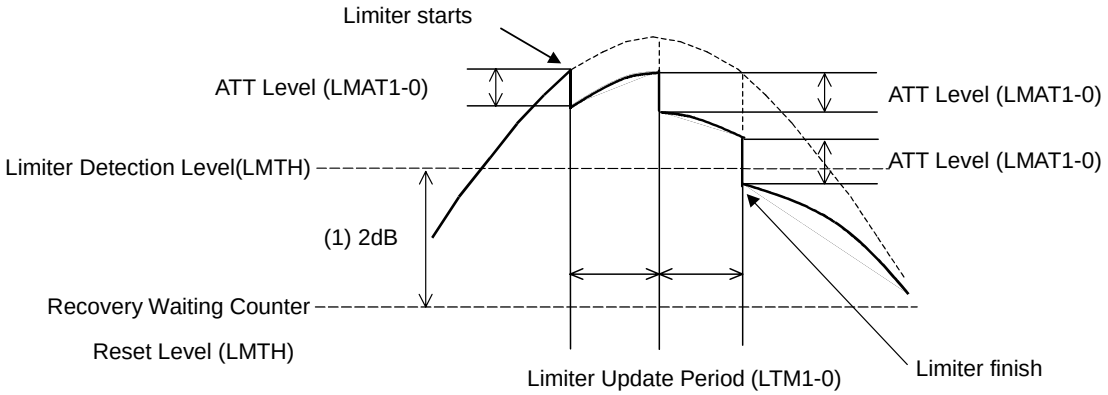


Figure 16. Disable ALC zero crossing detection (ZELMN = "1")

(1) When the signal is input between 2dB, the AK4563A does not operate the ALC limiter and recovery.

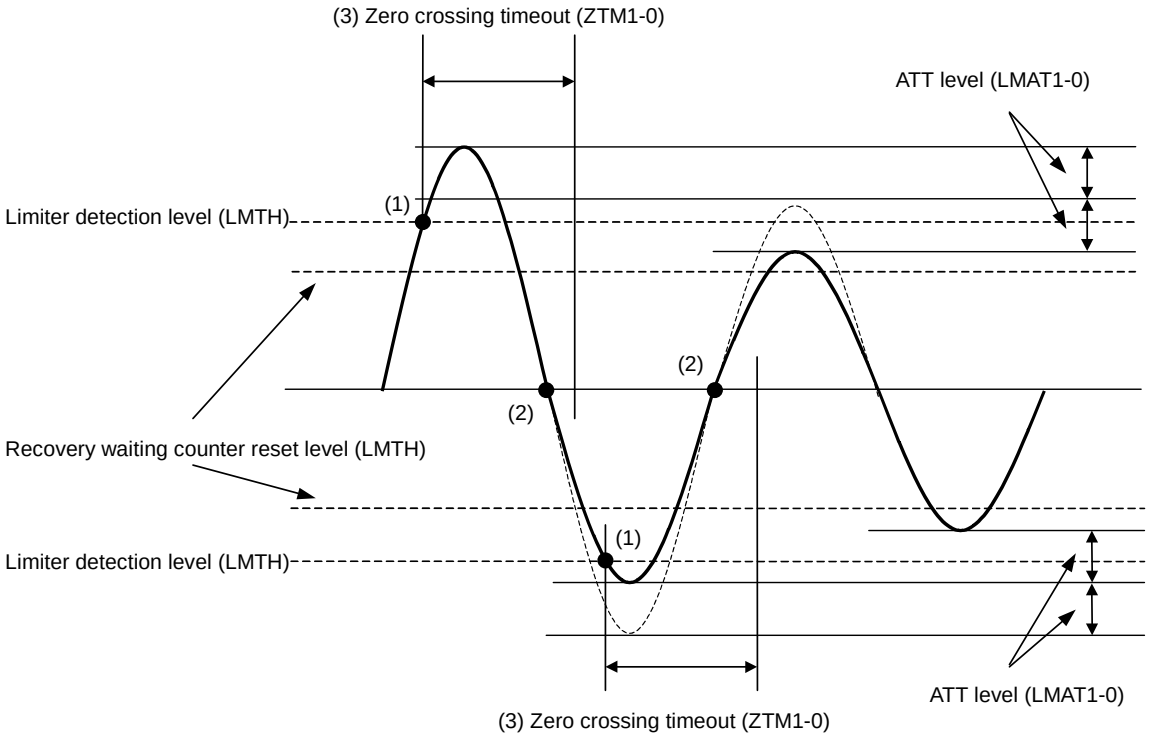


Figure 17. In case of continuing the limiter operation (ZELMN = "0")

(1) When the input level exceeds the ALC limiter detection level, the ALC limiter operation starts. Zero crossing counter starts at the same time.
(2) Zero crossing detection. When the input signal is detected, the IPGA value is attenuated until the value set by LMAT1-0 and the ALC limiter operation is finished.
(3) Zero crossing timeout is set by ZTM1-0 bits. But the first zero crossing timeout cycle after starting the limiter operation may be the short cycle by the state of the last zero crossing counter. (For example, in case of doing the limiter operation during the recovery operation)

2. ALC Recovery Operation

The ALC recovery operation waits until a time of setting WTM1-0 bits after completing the ALC limiter. If the input signal does not exceed “ALC recovery waiting counter reset level (LMTH)”, the ALC recovery operation is done. The IPGA value increases automatically by this operation up to the set reference level (REF6-0 bits). Then the IPGA value is set for L/R commonly. The ALC recovery operation is done at a period set by WTM1-0 bits.
When L/R channels in IPGA0 and IPGA1 are detected by zero crossing operation during WTM1-0, the ALC recovery operation waits until WTM1-0 period and the next recovery operation is done.

During the ALC recovery operation or the recovery waiting, when either input signal level of L/R channels in IPGA0 and IPGA1 exceed the ALC limiter detection level (LNTH), the ALC recovery operation changes into the ALC limiter operation immediately
In case of “ALC recovery waiting counter reset level (LMTH) ≤ Input Signal < ALC limiter detection level (LMTH)” during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. Therefore, in case of “ALC recovery waiting counter reset level (LMTH) > Input Signal”, the waiting timer of ALC recovery operation starts.

If the impulse noise is supplied at FR = “0”, the ALC recovery operation becomes the faster period than a set of ZTM1-0 and WTM1-0 bits. When FR bit is “1”, the ALC operation in AK4561 is the same as AK4516A’s.

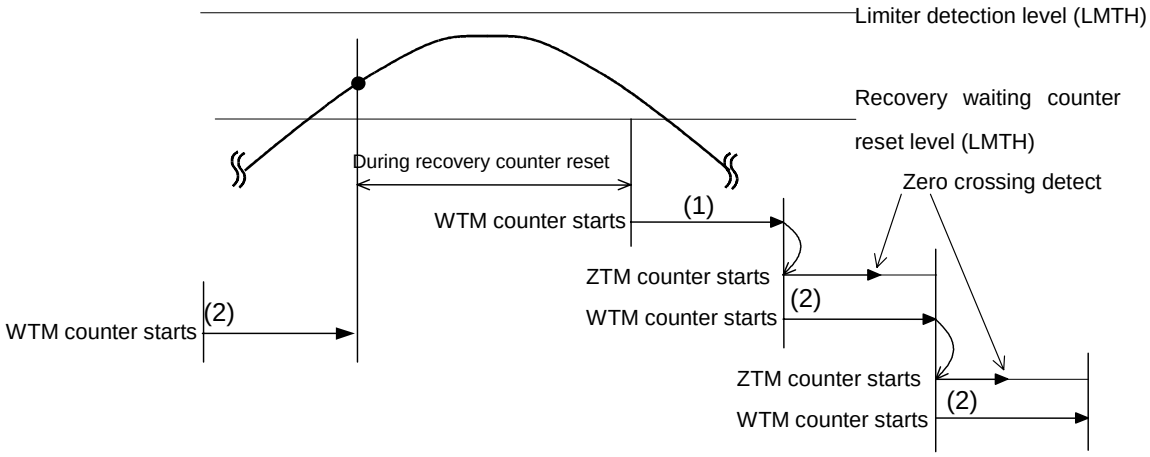


Figure 18. The transition from the limiter operation to the recovery operation

(1). When the input signal is below the ALC recovery waiting counter reset level, the ALC recovery operation waits the time set by WTM1-0 bits. If the input signal does not exceed the ALC limiter detection level or the ALC recovery waiting counter reset level, the ALC recovery operation is done only once.
(2). The IPGA value is changed by the zero crossing operation in ALC recovery operation, but the next counter of the ALC recovery waiting timer is also starting.

Other:

When a channel of one side enters the limiter operation during the waiting zero crossing, the present ALC recovery operation stops, according as the small value of IPGA (a channel of waiting zero crossing), the ALC limiter operation is done.
When both channels are waiting for the next ALC recovery operation, the ALC limiter operation is done from the IPGA value of a point in time.

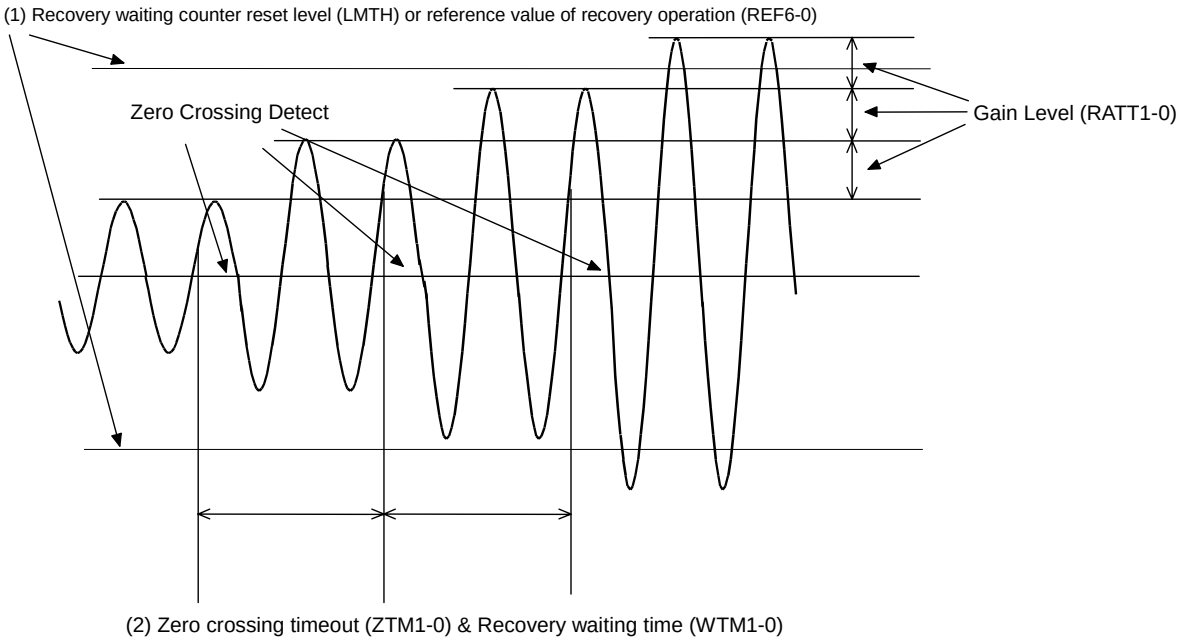


Figure 19. The ALC Recovery Operation

(1) When the input signal exceeds the ALC recovery waiting counter reset level, the ALC recovery operation stops, the ALC recovery operation is repeated when input signal level is below “ALC recovery waiting counter reset level (LMTH)” again. When the IPGA value by repeating the ALC recovery operation reaches the reference level (REF6-0 bits), the ALC recovery operation stops also.
(2) ZTM1-0 bits set zero crossing timeout and WTM1-0 bits sets the ALC recovery operation period. When the ALC recovery waiting time (WTM1-0 bits) is shorter than zero crossing timeout period of ZTM1-0 bit, the ALC recovery is operated by the zero crossing timeout period of ZTM1-0 bit. Therefore, in this case the auto recovery operation period is not constant.

Does not change the following registers during the ALC operation.
• LTM1-0, LMTH, LMAT1-0, WTM1-0, ZTM1-0, RATT, REF6-0, ZELMN

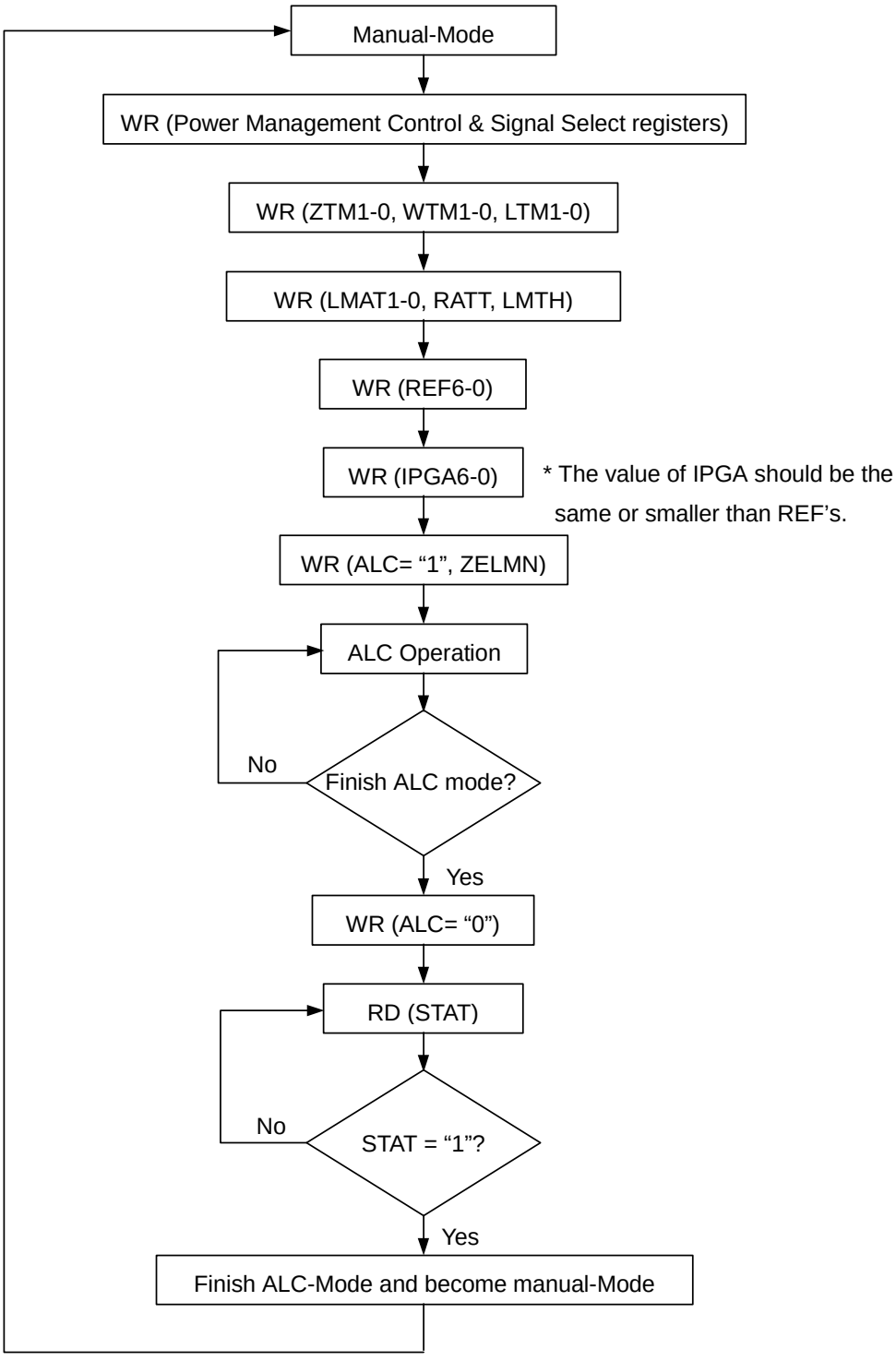


Figure 20. Registers set-up sequence at ALC operation

■ FADEIN Mode

In FADEIN Mode, the IPGA value is increased at the value set by FDATT when FDIN bit changes from “0” to “1”. The update period can be set by FDTM1-0 bits. The FADEIN Mode is always detected by the zero crossing operation. This operation is kept over the REF value or until the limiter operation at once. If the limiter operation is done during FADAIN cycle, the FADEIN operation becomes the ALC operation.

NOTE: When FDIN and FDOUT bits are “1”, FDOUT operation is enabled.

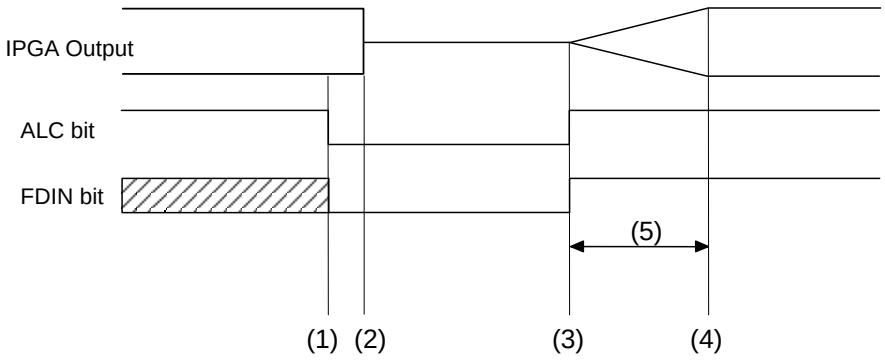


Figure 21. Example for controlling sequence in FADEIN operation

(1) WR (ALC = FDIN = “0”): The ALC operation is disabled. To start the FADEIN operation, FDIN bit is written in “0”.
(2) WR (IPGA = “MUTE”): The IPGA output is muted.
(3) WR (ALC = FDIN = “1”): The FADEIN operation starts. The IPGA changes from the MUTE state to the FADEIN operation.
(4) The FADEIN operation is done until the limiter detection level (LMTH) or the reference level (REF6-0). After completing the FADEIN operation, the AK4563A becomes the ALC operation.
(5) FADEIN time can be set by FDTM1-0 and FDATT bits
E.g. FDTM1-0 = 32ms, FDATT = 1step
(96 x FDTM1-0) / FDATT = 96 x 32ms / 1 = 3.07s

■ FADEOUT Mode

In FADEOUT mode, the present IPGA value is decreased until the MUTE state when FDOUT bit changes from "0" to "1". This operation is always detected by the zero crossing operation.
If the large signal is input to the ALC circuit during the FADEOUT operation, the ALC limiter operation is done. However a total time of the FADEOUT operation is the same time, even if the limiter operation is done. The period of FADEOUT is set by FDTM1-0 bits, a number of step can be set by FDATT bit.
When FDOUT bit changes into "0" during the FADEOUT operation, the ALC operation start from the preset IPGA value.
When FDOUT and ALC bits change into "0" at the same time, the FADEOUT operation stops and the IPGA becomes the value at that time.

NOTE: When FDIN and FDOUT bits are "1", FDOUT operation is enabled.

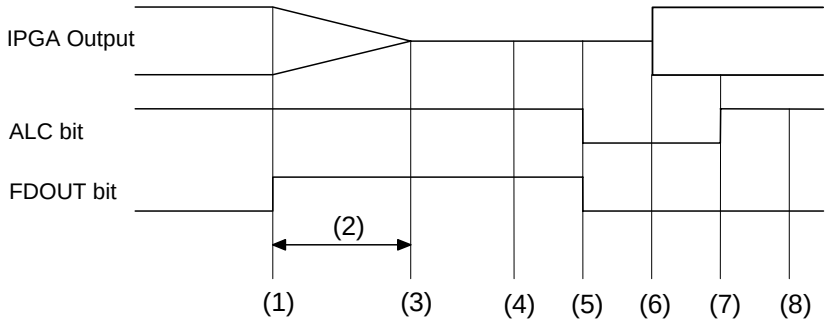


Figure 22. Example for controlling sequence in FADEOUT operation

(1) WR (FDOUT = "1"): The FADEOUT operation starts. Then ALC bit should be always "1".
(2) FADEOUT time can be set by FDTM1-0 and FDATT bits.
During the FADEIN operation, the zero crossing timeout period is ignored and becomes the same as the FADEIN period.
E.g. FDTM1-0 = 32ms, FDATT = 1step
(96 x FDTM1-0) / FDATT = 96 x 32ms / 1 = 3.07s
(3) The FADEOUT operation is completed. The IPGA value is the MUTE state. If FDOUT bit is keeping "1", the IPGA value is keeping the MUTE state.
(4) Analog and digital outputs mutes externally. Then the IPGA value is the MUTE state.
(5) WR (ALC = FDOUT = "0"): Exit the ALC and FADEOUT operations
(6) WR (IPGA): The IPGA value changes the initial value (exiting MUTE state).
(7) WR (ALC = "1", FDOUT = "0"): The ALC operation restarts. But the ALC bit should not write until completing zero crossing operation of IPGA.
(8) Release a mute function of analog and digital outputs externally.

SYSTEM DESIGN

Figure 23 shows the system connection diagram. An evaluation board (AKD4563A) is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

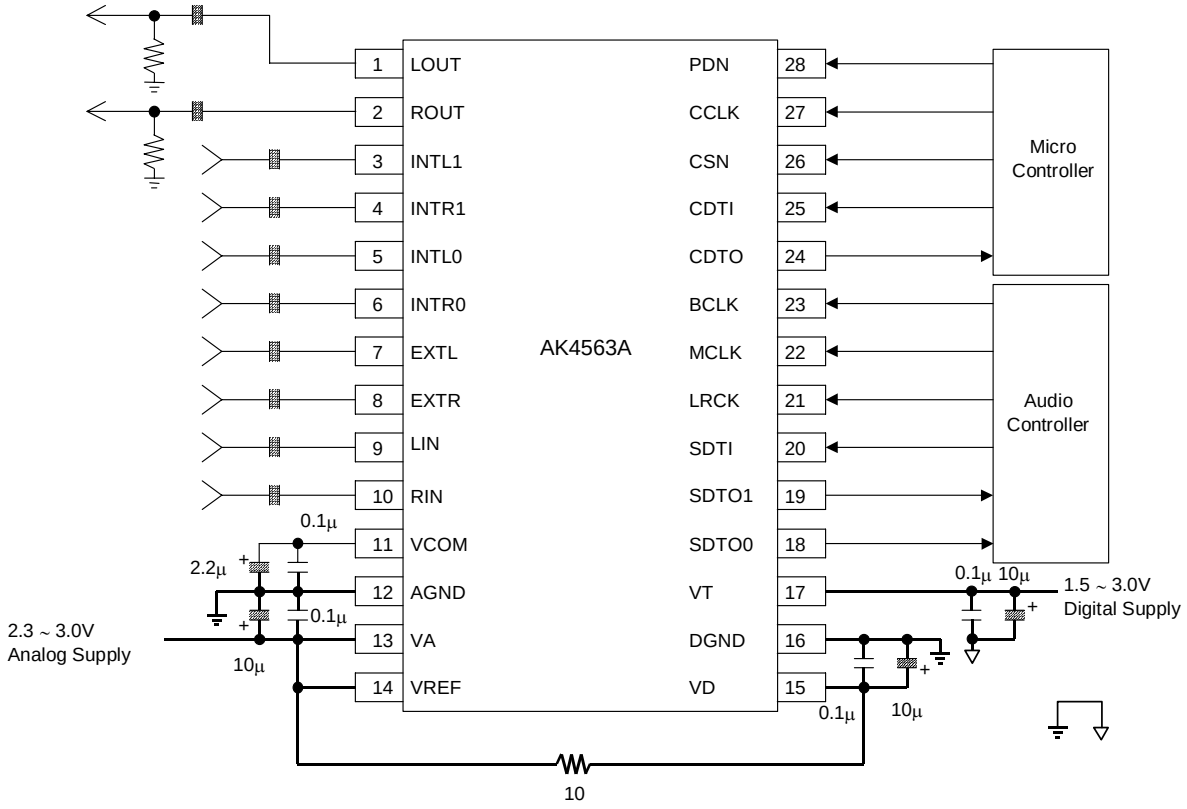


Figure 23. System Connection Diagram

Note:

- AGND and DGND of AK4563A should be distributed separately from the ground of external controller etc.
- When LOUT/ROUT drives some capacitive load, some resistor should be added in series between LOUT/ROUT and capacitive load.

1. Grounding and Power Supply Decoupling

The AK4563A requires careful attention to power supply and grounding arrangements. VA is usually supplied from analog supply in system and VD is supplied from analog supply in system via a resistor of 10 ohms. Alternatively if VA and VD are supplied separately, the power up sequence is not taken care. VT is a power supply pin to interface with the external ICs and is supplied from digital supply in system. AGND and DGND of the AK4563A should be connected to analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4563A as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

The differential voltage between VREF and AGND sets the analog input/output range. VREF pin is normally connected to VA with a 0.1μF ceramic capacitor. VCOM is output to 0.45 x VA(typ.) and is a signal ground of this chip. An electrolytic capacitor 2.2μF parallel with a 0.1μF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the AK4563A.

3. Analog Inputs

The analog inputs are single-ended and the input resistance is 10kΩ (typ) at MIC gain table and 125kΩ (typ) at LINE gain table. The input signal range scales with the VREF voltage and nominally 0.6 x VREF Vpp centered in the internal common voltage. Usually the input signal is AC coupled with capacitor. The cut-off frequency is fc = (1/2πRC). The AK4563A can accept input voltages to (VA-0.1) Vpp. The ADC output data format is 2's complement. The output code is 7FFFH(@16bit) for input above a positive full scale and 8000H(@16bit) for input below a negative fill scale. The ideal code is 0000H(@16bit) with no input signal. The DC offset including ADC own DC offset removed by the internal HPF (fc=3.7Hz@fs=48kHz).

The AK4563A samples the analog inputs at 64fs. The digital filter rejects noise above the stopband except for multiples of 64fs. The AK4563A includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

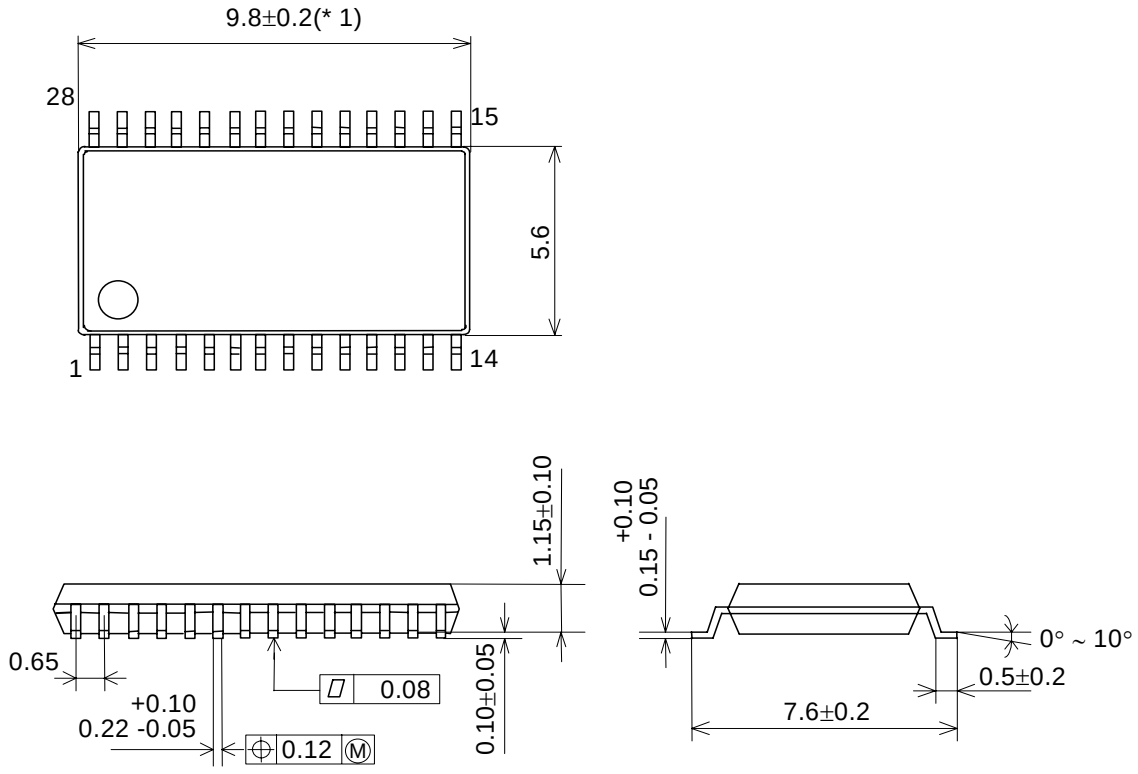
4. Analog Outputs

The analog outputs are single-ended and nominally 0.6 x VREF Vpp centered in the internal common voltage. The input data format is 2's complement. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The ideal output is the VCOM voltage for 0000H(@16bit). If the noise generated by the delta-sigma modulator beyond the audio band would be the problem, the attenuation by external circuit is required.

DC offsets on analog outputs are eliminated by AC coupling since analog outputs have DC offsets of a few mV + VCOM volrage.

PACKAGE

28pin VSOP (Unit: mm)

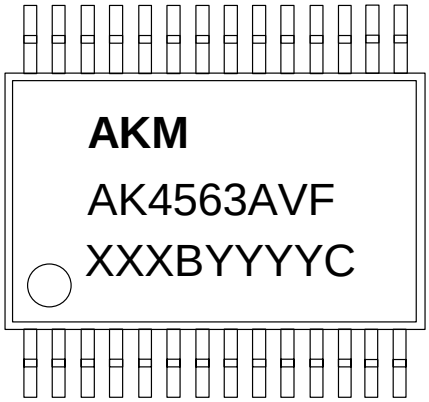


*1: Dimension does not include mold flash.

■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate (Pb free)

MARKING



XXXBYYYYC data code identifier

XXXB : Lot number (X : Digit number, B : Alpha character)
YYYYC : Assembly date (Y : Digit number, C Alpha character)

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