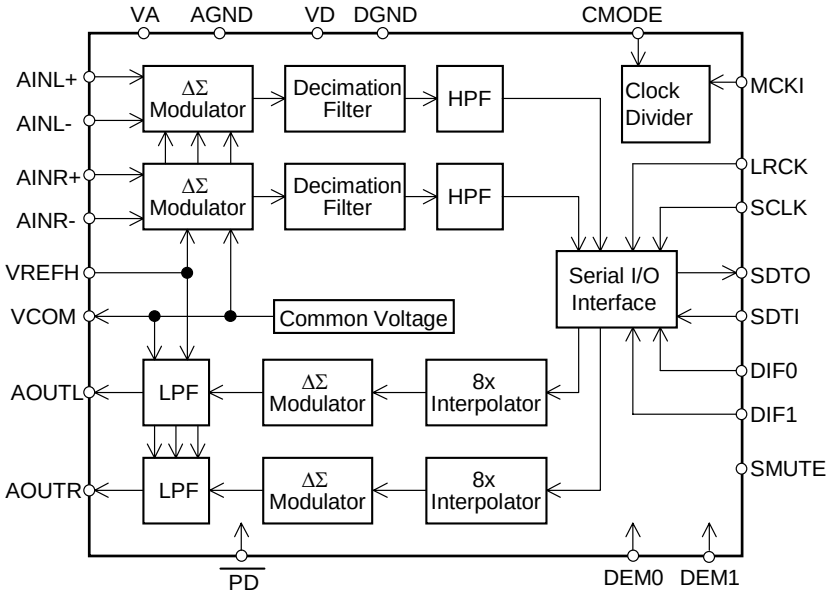
AK4523
20Bit Stereo ΔΣ ADC & DAC

GENERAL DESCRIPTION

The AK4523 has a dynamic range of 100dB and is well-suited middle-range MD, surround system, musical instruments and car audio. Signal inputs and outputs are single-ended. The DAC outputs are analog filtered to remove out of band noise. External components are minimized.

FEATURES

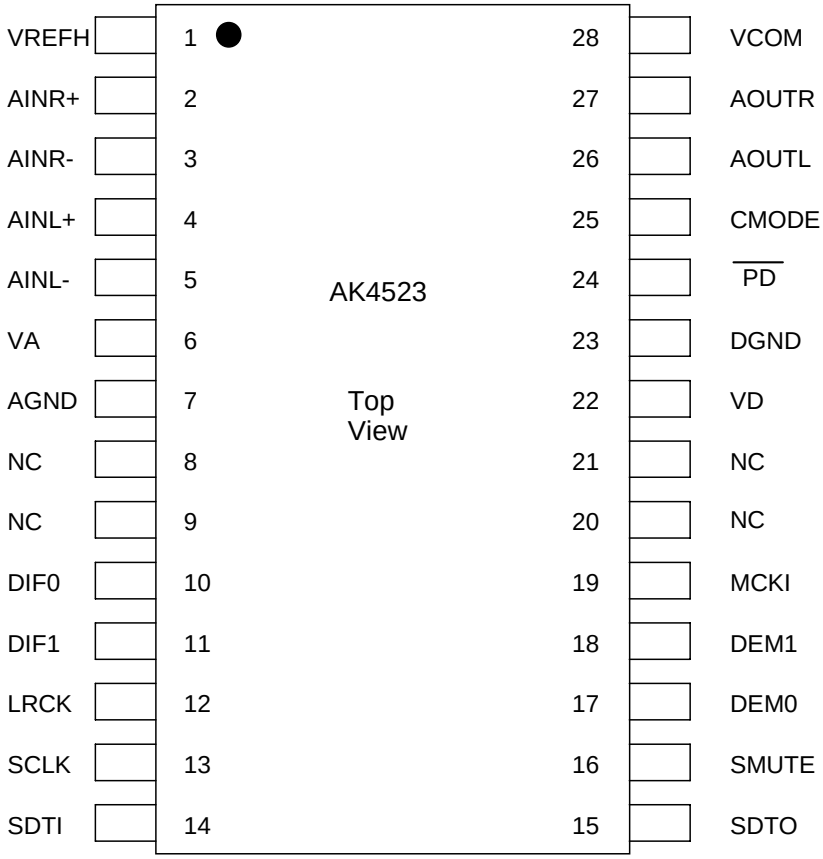
- ☐ **ΔΣ Stereo ADC**
  - **- 64x Oversampling**
  - **- Sample Rate Ranging from 16kHz to 48kHz**
  - **- S/(N+D): 92dB**
  - **- Dynamic range, S/N: 100dB**
  - **- Digital HPF for offset cancellation**
- ☐ **ΔΣ Stereo DAC**
  - **- 128x Oversampling**
  - **- Sampling Rate Ranging from 16kHz to 48kHz**
  - **- 2nd order SCF + 2nd order CTF**
  - **- Digital de-emphasis for 32kHz, 44.1kHz, 48kHz sampling**
  - **- S/(N+D): 90dB**
  - **- Dynamic Range, S/N: 100dB**
  - **- Soft Mute**
- ☐ **High Jitter Tolerance**
- ☐ **Master Clock: 256fs, 384fs, 512fs**
- ☐ **Analog Power Supply: 4.5 to 5.5V, Digital Power Supply: 3.0 to 5.5V**



■ Ordering Guide

AK4523VF	-40 ~ +85°C	28pin VSOP (0.65mm pitch)
AKD4523	Evaluation Board for AK4523	

■ Pin Layout



■ Difference between AK4523 and AK4522

	AK4523	AK4522
Digital Power Supply	3.0~5.5V	2.7~5.5V
Ambient Operating	-40~85°C	-10~70°C
Package	28pin VSOP	24pin VSOP

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VREFH	I	Positive Voltage Reference Input Pin, VA Used as a positive voltage reference by ADC & DAC. VREFH should be connected externally to filtered VA.
2	AINR+	I	Rch Analog Positive Input Pin
3	AINR-	I	Rch Analog Negative Input Pin
4	AINL+	I	Lch Analog Positive Input Pin
5	AINL-	I	Lch Analog Negative Input Pin
6	VA	-	Analog Power Supply Pin
7	AGND	-	Analog Ground Pin
8	NC	-	No connect No internal bonding.
9	NC	-	No connect No internal bonding.
10	DIF0	I	Audio Data Interface Format 0 Pin
11	DIF1	I	Audio Data Interface Format 1 Pin
12	LRCK	I	Input Channel Clock Pin
13	SCLK	I	Audio Serial Data Clock Pin
14	SDTI	I	Audio Serial Data Input Pin
15	SDTO	O	Audio Serial Data Output Pin
16	SMUTE	I	Soft Mute Pin When this pin goes “H”, soft mute cycle is initiated. When returning “L”, the output mute releases.
17	DEM0	I	De-emphasis Frequency Select 0 Pin
18	DEM1	I	De-emphasis Frequency Select 1 Pin
19	MCKI	I	Master Clock Input Pin
20	NC	-	No connect No internal bonding.
21	NC	-	No connect No internal bonding.
22	VD	-	Digital Power Supply Pin
23	DGND	-	Digital Ground Pin
24	$\overline{\text{PD}}$	I	Power-Down Mode Pin
25	CMODE	I	Master Clock Select Pin (Internal biased pin) “H”: 384fs, “L”: 256fs, “NC”: 512fs
26	AOUTL	O	Lch Analog Output Pin
27	AOUTR	O	Rch Analog Output Pin
28	VCOM	O	Common Voltage Output Pin, VA/2

Note: All input pins except for CMODE pin should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog	VA	-0.3	6.0	V
	Digital	VD	-0.3	6.0	V
	|AGND-DGND| (Note 2)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	VA+0.3	V
Digital Input Voltage		VIND	-0.3	VD+0.3	V
Ambient Temperature (power applied)		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note:1. All voltages with respect to ground.
2. AGND and DGND must be same voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	VA	4.5	5.0	5.5	V
(Note 3)	Digital	VD	3.0	5.0	VA	V
Voltage Reference		VREFH	90%VA		VA	V

Note:1. All voltages with respect to ground.
3. The power up sequence between VA and VD is not critical.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VA, VD=5V; AGND=DGND=0V; VREFH=VA; fs=44.1kHz; SCLK=64fs;
Signal Frequency =1kHz; 20bit Data; Measurement Frequency=10Hz ~ 20kHz; unless otherwise specified)

Parameter			min	typ	max	Units
ADC Analog Input Characteristics: Differential Inputs; Analog Source Impedance=470Ω						
Resolution					20	Bits
S/(N+D)	(-0.5dB Input)	(Note 4)	84	92		dB
DR	(-60dB Input, A-Weighted)	(Note 5)	94	100		dB
S/N	(A-Weighted)	(Note 5, 6)	94	100		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0.1	0.3	dB
Gain Drift				20		ppm/°C
Input Voltage	(AIN=0.6 x VREFH)	(Note 7)	2.85	3.0	3.15	Vpp
Input Resistance			15	25		kΩ
Power Supply Rejection		(Note 8)		50		dB
DAC Analog Output Characteristics:						
Resolution					20	Bits
S/(N+D)			80	90		dB
DR	(-60dB Output, A-Weighted)	(Note 5)	94	100		dB
S/N	(A-Weighted)	(Note 6, 9)	94	100		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0.2	0.5	dB
Gain Drift				20		ppm/°C
Output Voltage	(AOUT=0.58 x VREFH)		2.65	2.9	3.15	Vpp
Load Resistance			5			kΩ
Load Capacitance					25	pF
Power Supply Rejection		(Note 8)		50		dB
Power Supplies						
Power Supply Current (VA=VD=5V)						
Analog, VA	$\overline{PD}$ = "H"			42	55	mA
Digital, VD	$\overline{PD}$ = "H"			10	20	mA
Power Down	$\overline{PD}$ = "L"	(Note 10)		0.4	2	mA

Note: 4. In case of single ended input, S/(N+D)=80dB(typ, @VA=5V).
5. In case of 16bit, DR and S/N of ADC are 98dB. DR of DAC is 98dB.
6. S/N measured by CCIR-ARM is 96dB at each converter and 94dB at ADC to DAC loopback.
7. Full scale input for each AIN+/- pin is 1.5Vpp in differential mode.
8. PSR is applied to VA, VD with 1kHz, 50mVpp. VREFH pin is held a constant voltage.
9. As the input data is "0", S/N is 100dB regardless of resolution.
10. All digital input pins are held VD or DGND.

FILTER CHARACTERISTICS

(Ta=25°C; VA=4.5 ~ 5.5V, VD=3.0 ~ 5.5V; DEM0="1", DEM1="0")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 11)	-0.005dB	PB	0		19.76	kHz
	-0.02dB		0		20.02	kHz
	-0.06dB		0		20.20	kHz
	-6.0dB		0		22.05	kHz
Stopband		SB	24.34			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 12)		GD		29.3		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 5)	-3dB	FR		0.9		Hz
	-0.5dB			2.7		Hz
	-0.1dB			6.0		Hz
DAC Digital Filter:						
Passband (Note 11)	-0.06dB	PB	0		20.0	kHz
	-6.0dB		0		22.05	kHz
Stopband		SB	24.1			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay (Note 12)		GD		14.7		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±0.2	-	dB

Note: 11. The passband and stopband frequencies scale with fs.
For example, 20.02kHz at -0.02dB is 0.454 x fs. The reference frequency of these responses is 1kHz.

12. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 20bit data of both channels to the output register for ADC.
For DAC, this time is from setting the 20bit data of both channels on input register to the output of analog signal.

DIGITAL CHARACTERISTICS

(Ta=25°C; VA=4.5 ~ 5.5V, VD=3.0 ~ 5.5V)

Parameter	Symbol	min	typ	Max	Units
High-Level Input Voltage (Except CMODE pin)	VIH	70%VD	-	-	V
Low-Level Input Voltage (Except CMODE pin)	VIL	-	-	30%VD	V
High-Level Input Voltage (CMODE pin)	VIH	95%VD	-	-	V
Low-Level Input Voltage (CMODE pin)	VIL	-	-	10%VD	V
Hight-Level Output Voltage (Iout=-80µA)	VOH	VD-0.4	-	-	V
Low-Level Output Voltage (Iout=80µA)	VOL	-	-	0.4	V
Input Leakage Current (Note 13)	Iin	-	-	±10	µA

Note: 13. CMODE pin has internal pull-up and pull-down devices, nominally 50kohm.

SWITCHING CHARACTERISTICS

(Ta=25°C; VA=4.5 ~ 5.5V; VD=3.0 ~ 5.5V; C_L=20pF)

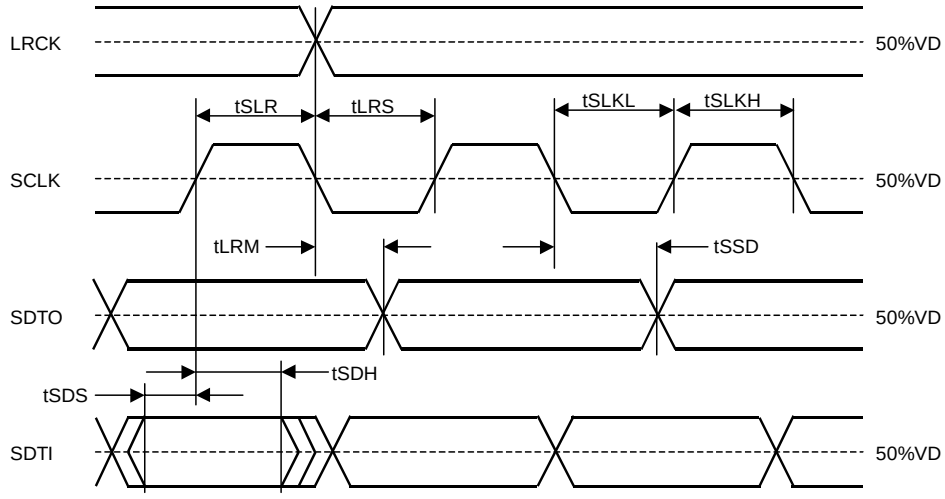
Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
256fs:		fCLK	4.096		12.288	MHz
Pulse Width Low		tCLKL	27			ns
Pulse Width High		tCLKH	27			ns
384fs:		fCLK	6.144		18.432	MHz
Pulse Width Low		tCLKL	20			ns
Pulse Width High		tCLKH	20			ns
512fs:		fCLK	8.192		24.576	MHz
Pulse Width Low		tCLKL	15			ns
Pulse Width High		tCLKH	15			ns
LRCK Timing						
Frequency		fs	16		48	kHz
Duty Cycle		dfs	45		55	%
Serial Interface Timing						
SCLK Period		tSCK	320			ns
SCLK Pulse Width Low		tSCKL	65			ns
Pulse Width High		tSCKH	65			ns
LRCK Edge to SCLK "↑"	(Note 14)	tLRS	45			ns
SCLK "↑" to LRCK Edge	(Note 14)	tSLR	45			ns
LRCK to SDTO (MSB)		tLRM			40	ns
SCLK "↓" to SDTO		tSSD			70	ns
SDTI Hold Time		tSDH	40			ns
SDTI Setup Time		tSDS	25			ns
Reset Timing						
$\overline{PD}$ Pulse Width	(Note 15)	tPD	150			ns
$\overline{PD}$ "↑" to SDTO valid	(Note 16)	tPDV		516		1/fs

Note 14. SCLK rising edge must not occur at the same time as LRCK edge.

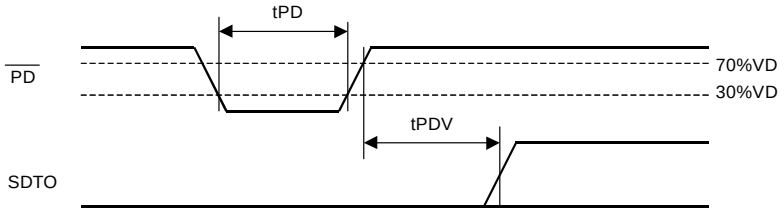
15. The AK4523 can be reset by bringing $\overline{PD}$ "L".
    When the state of CMODE change during operation, the AK4523 should be reset by $\overline{PD}$.

16. These cycles are the number of LRCK rising from $\overline{PD}$ rising.

■ Timing Diagram



Serial Interface Timing



Reset & Initialize Timing

OPERATION OVERVIEW

■ System Clock

The master clock (MCLK) can be external clock input to the MCKI pin. CMODE is used to select either MCLK=256fs, 384fs or 512fs. The relationship between the MCLK and the desired sample rate is defined in Table 1. The LRCK clock input must be synchronized with MCLK, however the phase is not critical. Internal timing is synchronized to LRCK upon power-up. All external clocks must be present unless $\overline{PD}$ = "L", otherwise excessive current may result from abnormal operation of internal dynamic logic.

fs	MCLK			SCLK
	256fs CMODE = "L"	384fs CMODE = "H"	512fs CMODE = "NC"	64fs
32.0kHz	8.1920MHz	12.2880MHz	16.384MHz	2.048MHz
44.1kHz	11.2896MHz	16.9344MHz	22.579MHz	2.822MHz
48.0kHz	12.2880MHz	18.4320MHz	24.576MHz	3.072MHz

Table 1. System Clock Example

When the state of CMODE change under operation, the AK4523 should be reset by $\overline{PD}$. At that case, the analog outputs should be muted externally because some click noise may occur.

■ Audio Serial Interface Format

Data is shifted in/out the SDTI/SDTO pins using SCLK and LRCK inputs. Four serial data modes selected by the DIF0 and DIF1 pins are supported as shown in Table 2. In all modes the serial data has MSB first, 2's compliment format. The data is clocked out on the falling edge of SCLK and latched on the rising edge. For mode 3, if SCLK is 32fs, then the least significant bits will be truncated.

Mode	DIF1	DIF0	SDTO (ADC)	SDTI (DAC)	L/R	SCLK (Slave)
0	0	0	20bit, MSB justified	16bit, LSB justified	H/L	≥ 32fs
1	0	1	20bit, MSB justified	20bit, LSB justified	H/L	≥ 40fs
2	1	0	20bit, MSB justified	20bit, MSB justified	H/L	≥ 40fs
3	1	1	IIS (I2S)	IIS (I2S)	L/H	32fs or ≥ 40fs

Table 2. Serial Data Modes

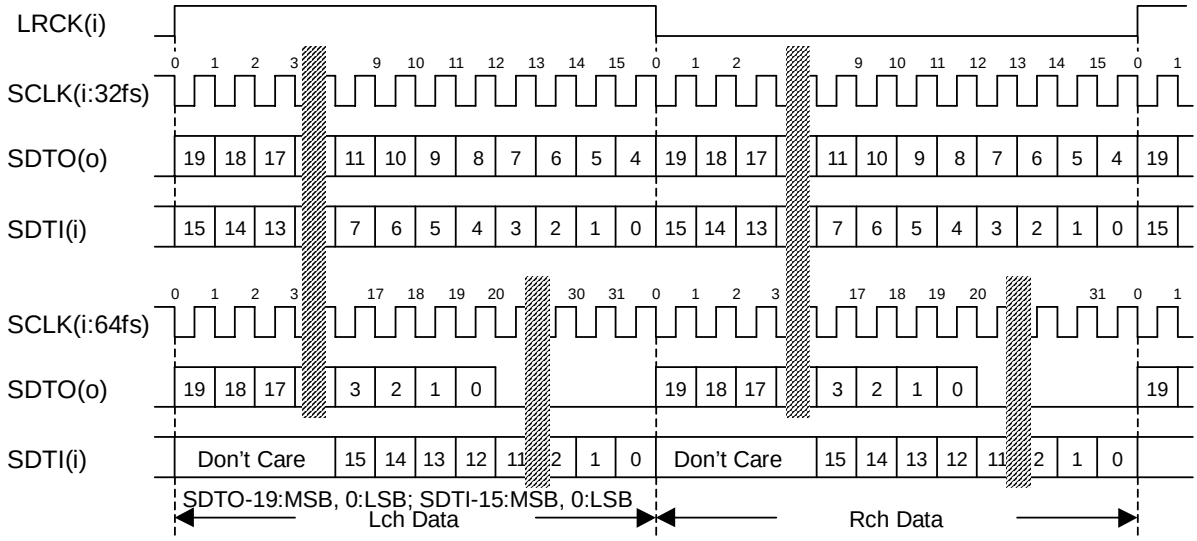


Figure 1. Mode 0 Timing

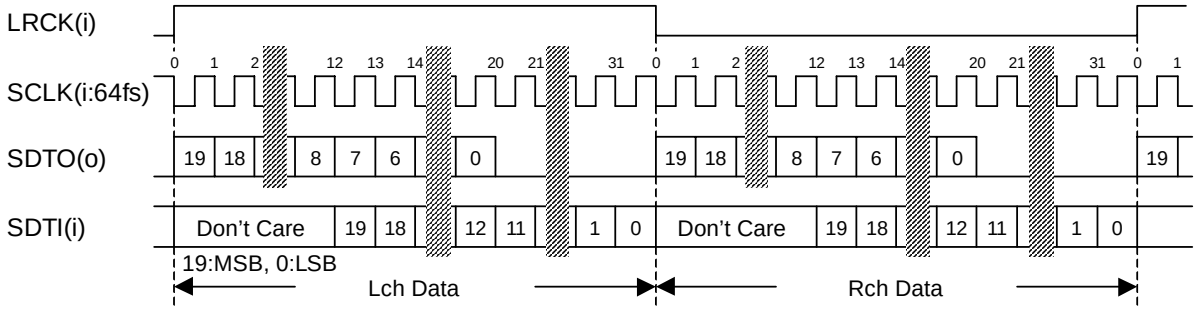


Figure 2. Mode 1 Timing

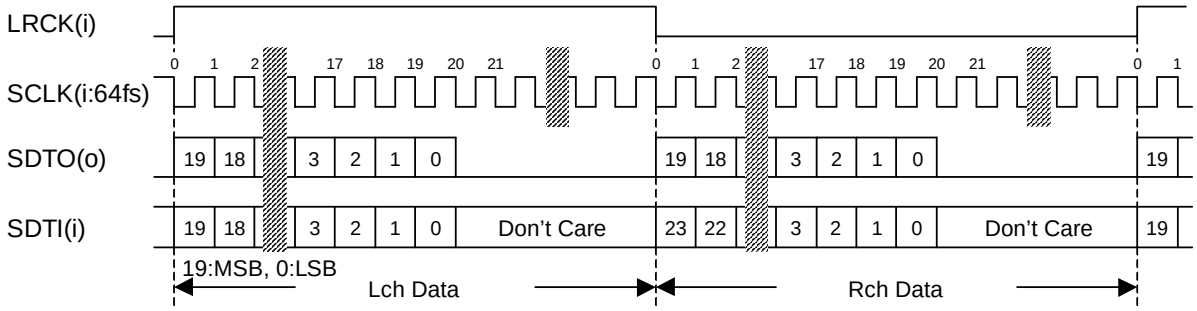


Figure 3. Mode 2 Timing

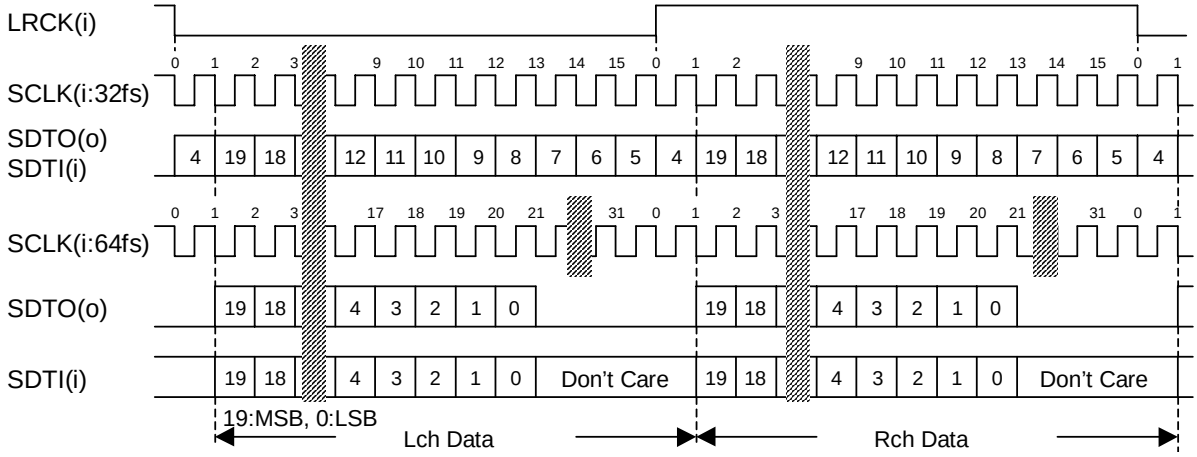


Figure 4. Mode 3 Timing

■ Digital High Pass Filter

The ADC of AK4523 has a digital high pass filter for DC offset cancel. The cut-off frequency of the HPF is 0.9Hz at fs=44.1kHz and also scales with sampling rate (fs).

■ De-emphasis Filter

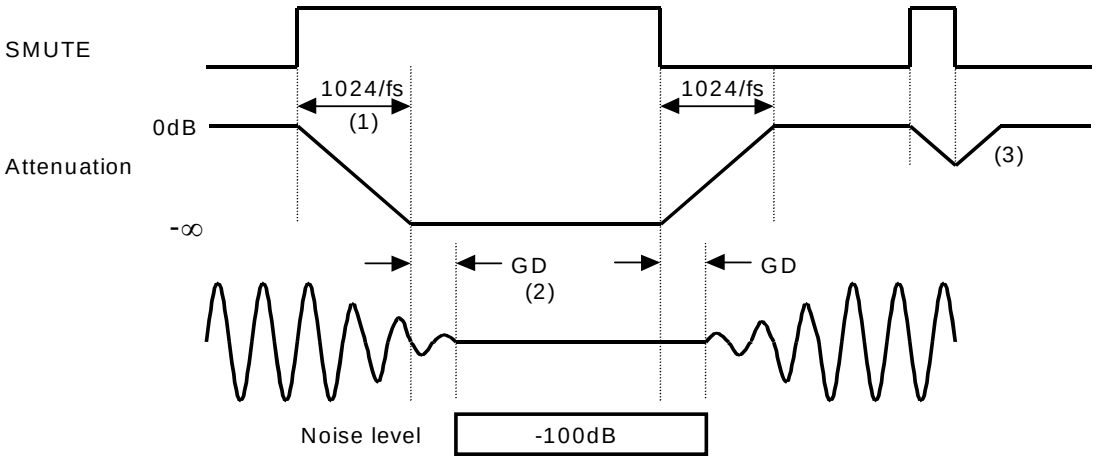
The DAC of AK4523 includes the digital de-emphasis filter (tc=50/15μs) by IIR filter. This filter corresponds to three frequencies (32kHz, 44.1kHz and 48kHz). The de-emphasis filter selected by DEM0 and DEM1 is enabled for input audio data. The de-emphasis is also disabled at DEM0="1" and DEM1="0".

DEM1	DEM0	Mode
0	0	44.1kHz
0	1	OFF
1	0	48kHz
1	1	32kHz

Table 3. De-emphasis filter control

■ Soft Mute Operation

Soft mute operation is performed at digital domain. When SMUTE goes to "H", the output signal is attenuated by -∞ during 1024 LRCK cycles. When SMUTE is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.



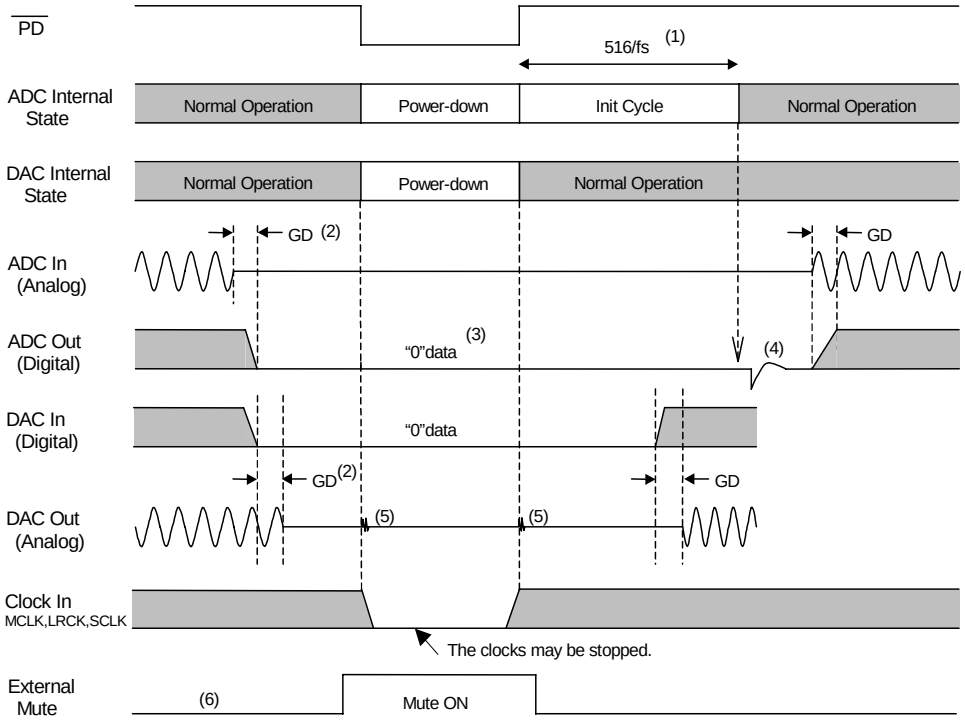
Notes:

(1) The output signal is attenuated by -∞ during 1024 LRCK cycles (1024/fs).
(2) Analog output corresponding to digital input has the group delay (GD).
(3) If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.

Figure 5. Soft Mute Operation

■ Power-Down & Reset

The ADC and DAC of AK4523 are placed in the power-down mode by bringing a power down pin, $\overline{PD}$ "L" and each digital filter is also reset at the same time.This reset should always be done after power-up. In case of the ADC, an analog initialization cycle starts after exiting the power-down mode. Therefore, the output data, SDTO becomes available after 516 cycles of LRCK clock. This initialization cycle does not affect the DAC operation. Figure 6 shows the power-up sequence.



(1) The analog part of ADC is initialized after exiting the power-down state.
(2) Digital output corresponding to analog input and analog output corresponding to digital input have the group delay (GD).
(3) ADC output is "0" data at the power-down state.
(4) Small click noise occurs at the end of initialization of the analog part. Please mute the digital output externally if the click noise influences system application.
(5) Click noise occurs at the edge of $\overline{PD}$.
(6) Please mute the analog output externally if the click noise (5) influences system application.

Figure 6. Power-up sequence

SYSTEM DESIGN

Figure 7 shows the system connection diagrams. This is an example which analog signal is input by single ended circuit. In case of differential input, please refer to Figure 10. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

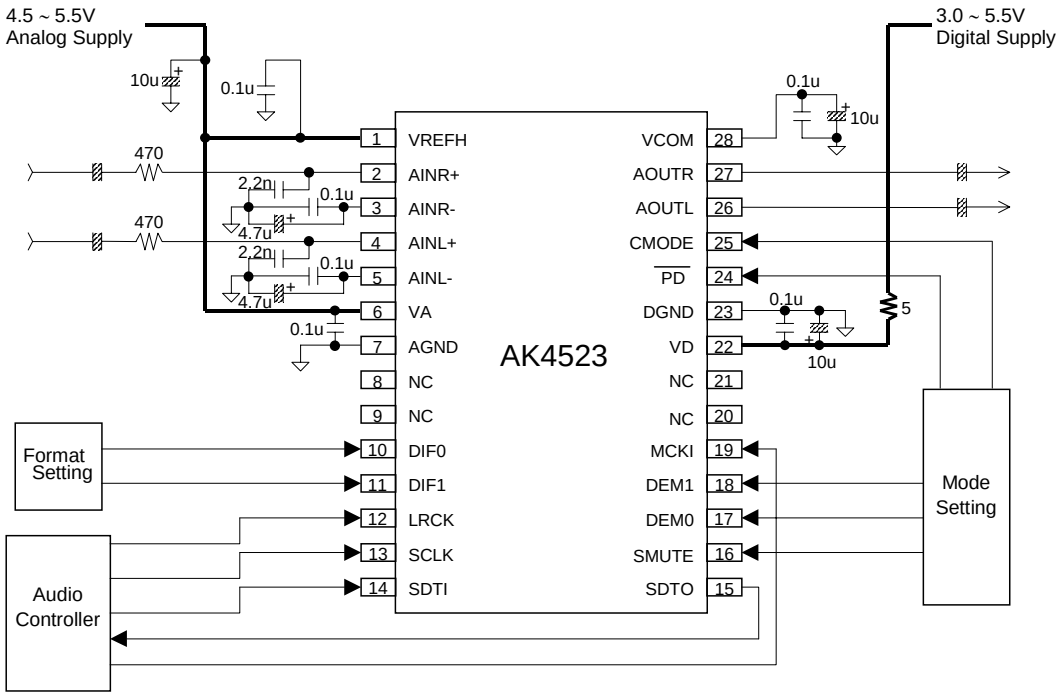


Figure 7. Typical Connection Diagram

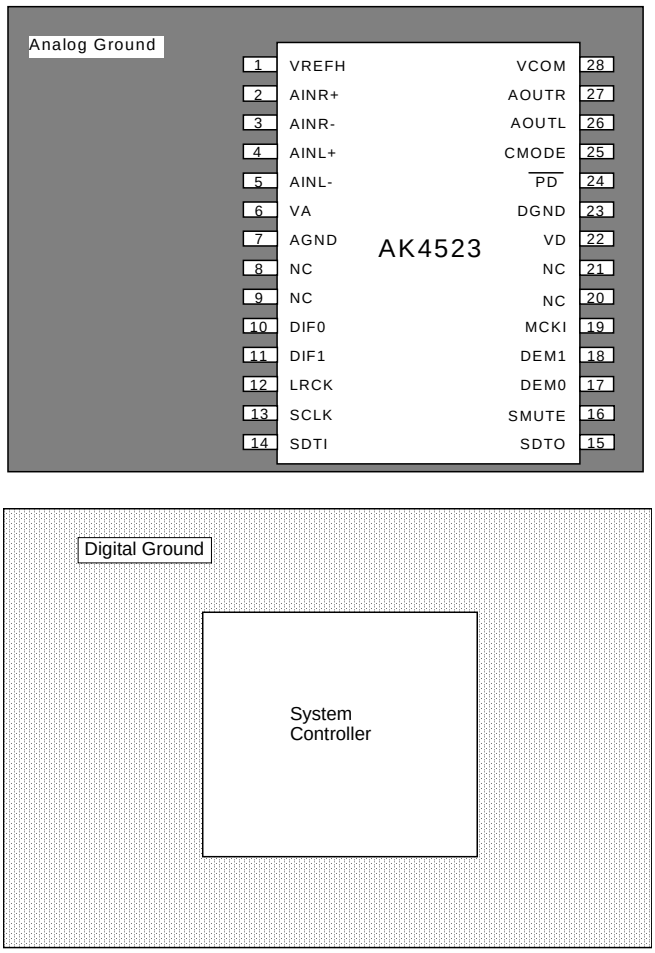


Figure 8. Ground Layout

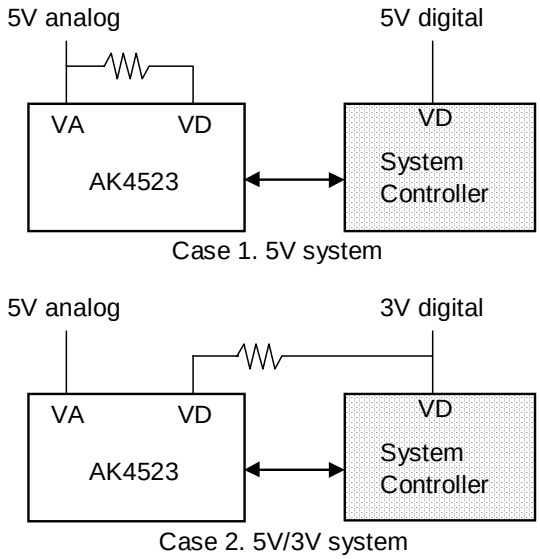


Figure 9. Power Supply Arrangement

1. Grounding and Power Supply Decoupling

The AK4523 requires careful attention to power supply and grounding arrangements. VA and VD are usually supplied from analog supply in system. Alternatively if VA and VD are supplied separately, the power up sequence is not critical. AGND and DGND of the AK4523 should be connected to analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4523 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

The differential voltage between VREFH and AGND sets the analog input/output range. VREFH pin is normally connected to VA with a 0.1µF ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor 10µF parallel with a 0.1µF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREFH and VCOM pins in order to avoid unwanted coupling into the AK4523.

3. Analog Inputs

The ADC inputs are differential and internally biased to the common voltage (VA/2) with 25kΩ (typ) resistance. Figure 7 is a circuit example which analog signal is input by single end. The signal can be input from either positive or negative input and the input signal range scales with the supply voltage and nominally 0.6 x VREFH Vpp. In case of single ended input, the distortion around full scale degrades compared with differential input. Figure 10 is a circuit example which analog signal is input to both positive and negative input and the input signal range scales with the supply voltage and nominally 0.3 x VREFH Vpp. The AK4523 can accept input voltages from AGND to VA. The ADC output data format is 2's complement. The output code is 7FFFFH(@20bit) for input above a positive full scale and 80000H(@20bit) for input below a negative fill scale. The ideal code is 00000H(@20bit) with no input signal. The DC offset is removed by the internal HPF.

The AK4523 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. A simple RC filter (fc=150kHz) may be used to attenuate any noise around 64fs and most audio signals do not have significant energy at 64fs.

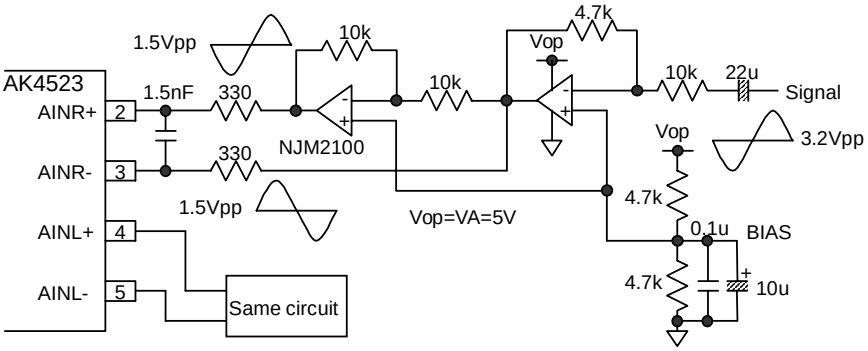


Figure 10. Differential Input Buffer Example

4. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The input signal range scales with the supply voltage and nominally 0.58 x VREFH Vpp. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFH(@20bit) and a negative full scale for 80000H(@20bit). The ideal output is VCOM voltage for 00000H(@20bit). The internal switched-capacitor filter and continuous-time filter remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband.

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV. Figure 11 shows the example of external op-amp circuit with 6dB gain. The output signal is inverted by using the circuit in this case.

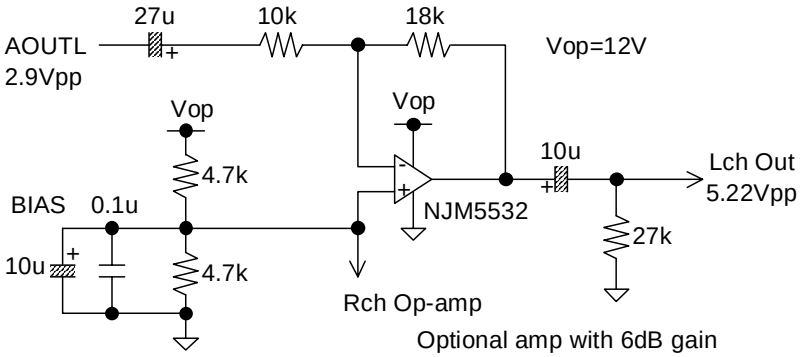
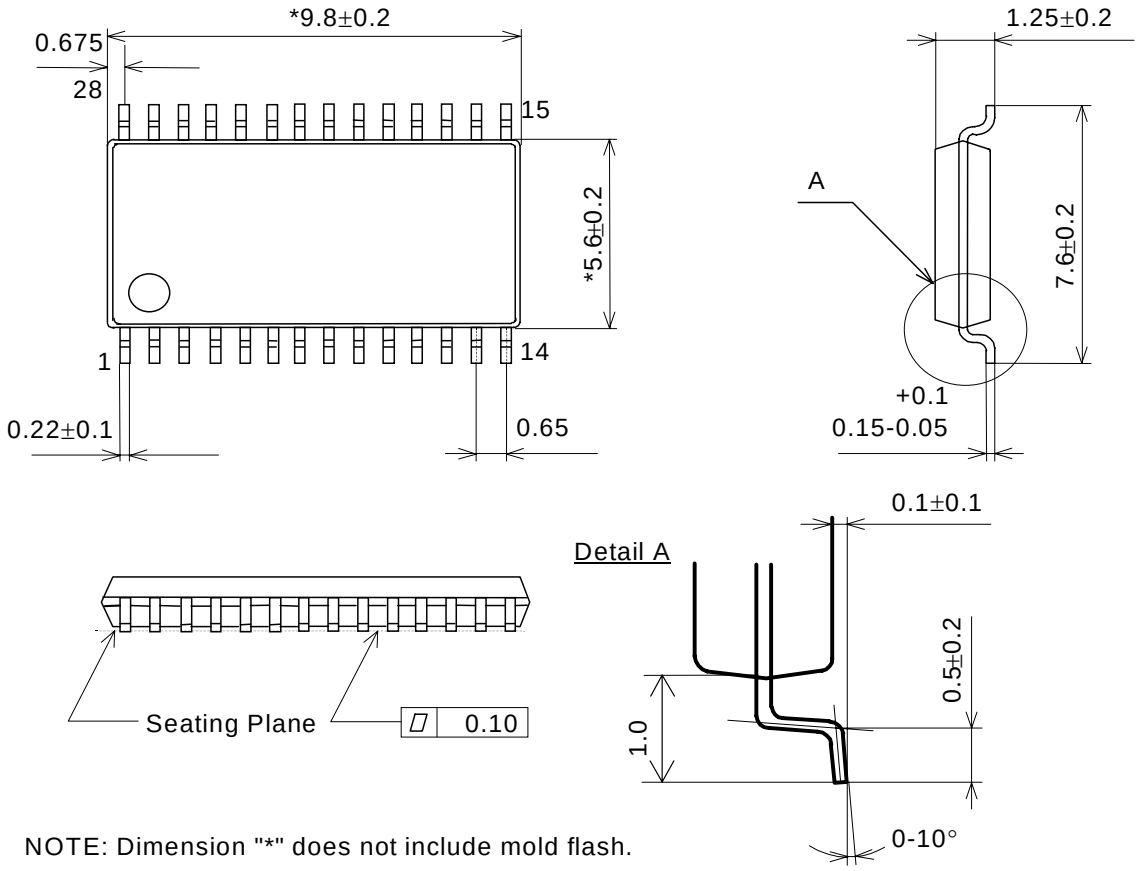


Figure 11. External analog circuit example (gain=6dB)

PACKAGE

28pin VSOP (Unit: mm)

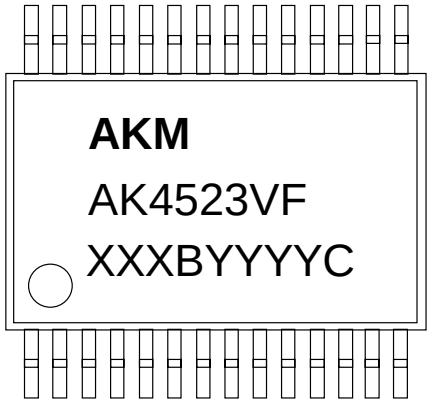


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



XXXBYYYYC: data code identifier

XXXB: Lot number (X: Digit number, B: Alpha character)
YYYYC: Assembly data (Y: Digit number, C: Alpha character)

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