Ordering number : ENA1337

SANYO Semiconductors
DATA SHEET

LC01700PW — CMOS LSI FM tuner IC for VICS

Overview

LC01700PW is an FM tuner IC for vehicle-mounted VICS incorporating FM FE, IF, OP AMP, PLL.
VICS tuner can be developed by one chip.
This IC can make up a small FM tuner module mounted for navigation.

Features

- Dedicated FM tuner IC for VICS in Japan and RDS in Europe.
- Variable gain LNA incorporated.
- A pulse counter detection method employed in the FM detection circuit. No adjustment necessary.
- Less number of external parts.
- BUS control tuner IC enabling control with I^2C BUS.
- OP AMP provided to adjust the composite frequency level appropriate to VICS and RDS.
- 6Bit-ADC incorporated to enable digital output of S meter.

Functions

- FM-FE+IF+OP AMP+PLL

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		6	V
Maximum input voltage	V_{DD} H		6	V
Maximum output voltage	V_{DD} L		6	V
Allowable power dissipation	Pd max	Ta ≤ 85°C	400	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-50 to +150	°C

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Operating supply voltage range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{DD}	Not to exceed the absolute maximum rating	4.5 to 5.5	V
Supply voltage range	V_{DD}		5.0	V

Serial interface voltage level

V_{DD} : Communications bus voltage

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High level input voltage	V_{IH}		2.4		V_{DD}	V
Low level input voltage	V_{IL}		0.0		0.7	V
High level output voltage (open·drain)	V_{OH}				V_{DD}*	V
Low level output voltage (open·drain)	V_{OL}		0.0		$0.2V_{DD}$	V

* High level output voltage causes the open drain to become the high-impedance state.
Since the drain is pulled up to V_{DD}, the voltage is equal to V_{DD}.

Electrical Characteristics at Ta = 25°C, unless otherwise specified. fc = 83MHz, Vin = 60dBμVEMF, fm = 1kHz,
Audio filter : HPF =100Hz, LPF = 15kHz
Sample application circuit (Sample application circuit) look-up
Register map <writing> look-up

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
S/N 30dB sensitivity	SN30	22.5kHz dev, fm = 1kHz, S/N = 30dB input level		15	20	dBμVEMF
S/N 10dB sensitivity *1	SN10	7.5kHz dev, fm = 76kHz, S/N = 10dB input level *2		25		dBμVEMF
Seek sensitivity (LO)	Seek	22.5kHz dev, Vin = 40dBμVEMF Vsm = 2.0V adjustment Pin 18 (STDO) Lo → Hi input level	15	22	29	dBμVEMF
S/N ratio 1	SN_1	22.5kHz dev, fm = 1kHz	50	60		dB
S/N ratio 2	SN_2	7.5kHz dev, fm = 76kHz *2		35		dB
Total harmonic distortion 1	THD_1	22.5kHz dev, fm = 1kHz		0.1	1	%
Total harmonic distortion 2	THD_2	75.0kHz dev, fm = 1kHz		0.2	1	%
Total harmonic distortion 3	THD_3	22.5kHz dev, fm = 1kHz, Vin = 120dBμVEMF		0.1	1	%
Image removal ratio	Image	22.5kHz dev, fm = 1kHz	40	50		dB
AM suppression ratio	AMR	AM 30% mod	45	55		dB
Audio output level 1	Vo_1	75.0kHz dev, fm = 1kHz	170	270	430	mVrms
Audio output level 2	Vo_2	7.5kHz dev, fm = 76kHz *2	16	25	40	mVrms
Current drain	I_{DD}	Input at no signal		30	45	mA

*1 S/N = 10dB at BER = 1%
*2 Audio filter : HPF = 100Hz, LPF = OFF

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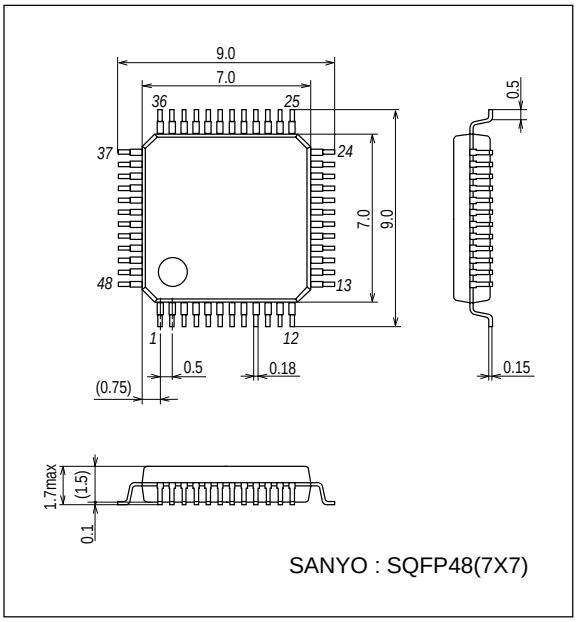
Package Dimensions

unit : mm (typ)

3163B



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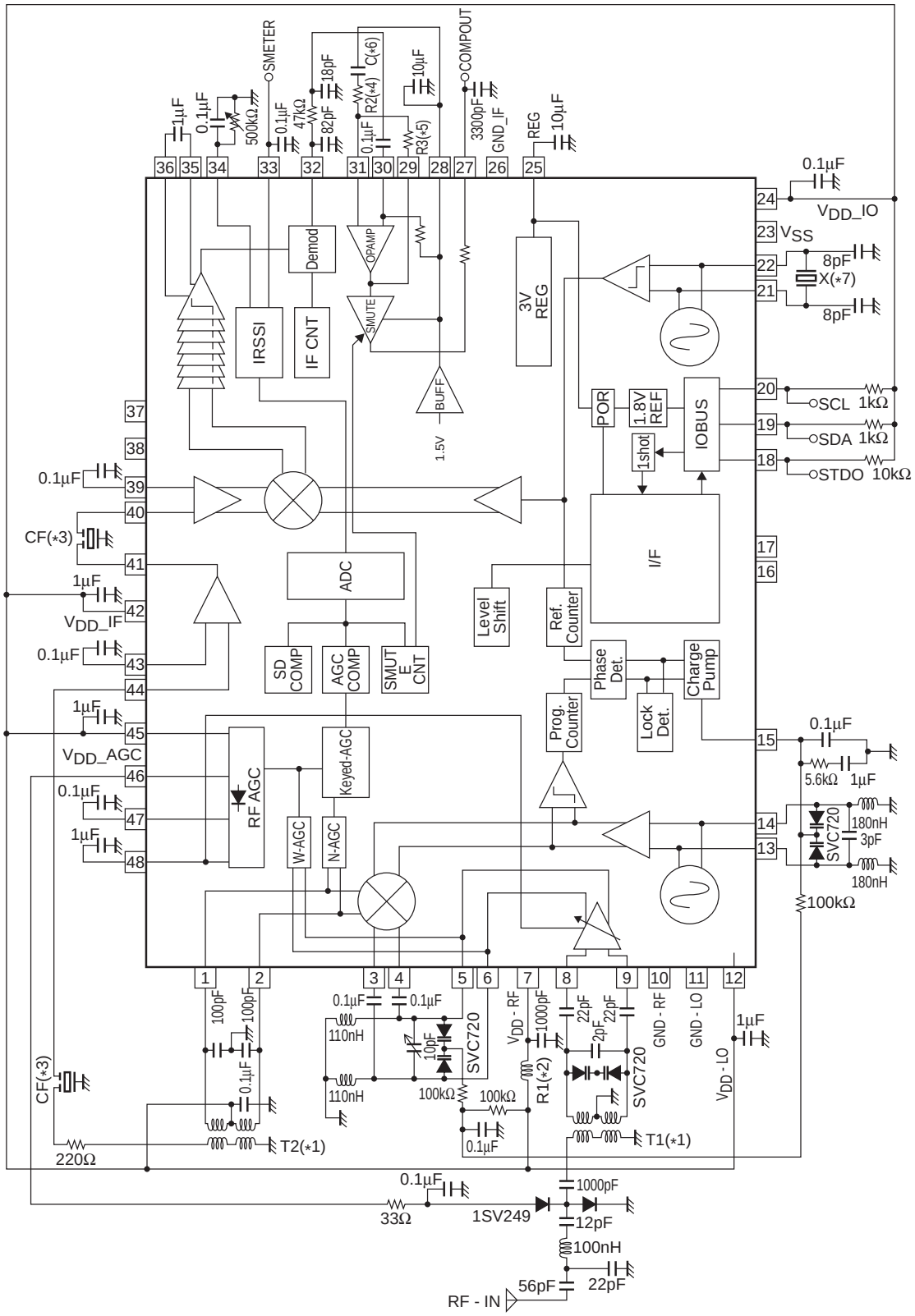
Sample Application Circuit (Block Diagram)



(*1) T1 -TOKO : 5CCE #A638AN -1840YFZ
T2 -TOKO : 5CCL ##613BG -0581WN

(*2) R1 -TAIYO YUDEN: BK1608HS102 -T

(*3) CF -MURATA : SFELL15M0GQQTS01 -B0 3dB Bandwidth 230 50kHz

(*4) R2 -fm = 1kHz : NM fm = 76kHz : 6.8kΩ

(*5) R3 -fm = 1kHz : 0Ω m = 76kHz : 6.8kΩ

(*6) C -fm = 1kHz : NM fm = 76kHz : 680pF

(*7) X -NIHON DENPA KOGYO CO.,LTD : AT41 14.55MHz

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Pin Description

Pin No.	Pin Name	Type	Description
1	MIX_ON	OUT	1stMIX signal output (-)
2	MIX_OP	OUT	1stMIX signal output (+)
3	MIX_IP	IN	1stMIX signal input (+)
4	MIX_IN	IN	1stMIX signal input (-)
5	LNA_ON	OUT	LNA signal output (-)
6	LNA_OP	OUT	LNA signal output (+)
7	V_{DD}_RF	POWER	RF block power
8	FM_IP	IN	FM signal input (+)
9	FM_IN	IN	FM signal input (-)
10	GND_RF	GND	RF block GND
11	GND_LO	GND	LO block GND
12	V_{DD}_LO	POWER	LO block power
13	LOSC2	IN/OUT	VCO resonant load pin 2
14	LOSC1	IN/OUT	VCO resonant load pin 1
15	VT	OUT	Charge pump output
16	NC1	NC	NC
17	NC2	NC	NC
18	STDO	OUT	Monitor output/reset detection output
19	SDA	IN/OUT	Serial data I/O (I^2C)
20	SCL	IN	Serial clock input (I^2C)
21	XOSC2	IN/OUT	Crystal oscillator pin 2
22	XOSC1	IN/OUT	Crystal oscillator pin 1
23	V_{SS}	GND	Digital block GND
24	V_{DD}_IO	POWER	5V power for interface
25	V_{DD}	OUT	Digital block power (built-in regulator output)
26	GND_IF	GND	IF block GND
27	COMPOUT	OUT	Composite signal output
28	DETREF	IN/OUT	FM detection signal amplifier reference voltage
29	DETADJ	OUT	FM detection signal amplitude adjustment
30	DETINP	IN	FM detection signal amplifier input (+)
31	DETINN	IN	FM detection signal amplifier input (-)
32	FDO	OUT	FM detection circuit output
33	SMETER	IN/OUT	S meter output
34	CRSSI	IN/OUT	Connection of smoothing capacitor for S-meter/S-meter output voltage adjustment
35	LIM2	IN/OUT	Limiter offset canceling capacitor connection 2
36	LIM1	IN/OUT	Limiter offset canceling capacitor connection 1
37	NC3	NC	NC
38	NC4	NC	NC
39	IF2nd_IN	IN	2ndMIX signal input (-)
40	IF2nd_IP	IN	2ndMIX signal input (+)
41	IF1stOUT	OUT	1st IF amplifier signal output
42	V_{DD}_IF	POWER	IF block power
43	IF1st_IN	IN	1st IF amplifier signal input (-)
44	IF1st_IP	IN	1st IF amplifier signal input (+)
45	V_{DD}_AGC	POWER	Pin diode AGC circuit power
46	FMAGC	OUT	FM pin diode driver output
47	CAGC	IN/OUT	AGC circuit smoothing capacitor connection 2
48	LNAAGC	IN/OUT	AGC circuit smoothing capacitor connection 1

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Communications Specifications

Communications specifications are shown below :

Serial Interface(I^2C-bus) ; Serial interface (I^2C-bus)

Send/receive is made via I^2C-bus that consists of two bus lines, each being a serial • data • line (SDA) and serial • clock • line (SCL). This bus enables 8-bit bi-directional serial data transmission at maximum 400kbit/s (fast mode). This is not compatible with the Hs mode.

1. Terms used in I^2C

The following terms are used in I^2C.

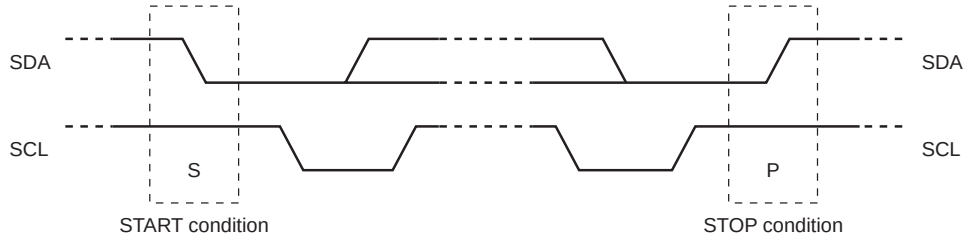
Terms	Description
Transmitter	Device to send data to the bus
Receiver	Device to receive data from the bus
Master	Device to start data transmission, to generate the clock signal, and to end data transmission
Slave	Device whose address is designated by the master

2. "Start" and "Stop" conditions

"Start" condition must be satisfied at start of data communications and "Stop" condition must be satisfied at end of communications.

The condition in which the SDA line changes from "H" to "L" with SCL at "H" is called the "Start" line.

The condition in which the SDA line changes from "L" to "H" with SCL at "H" is called the "Stop" condition.



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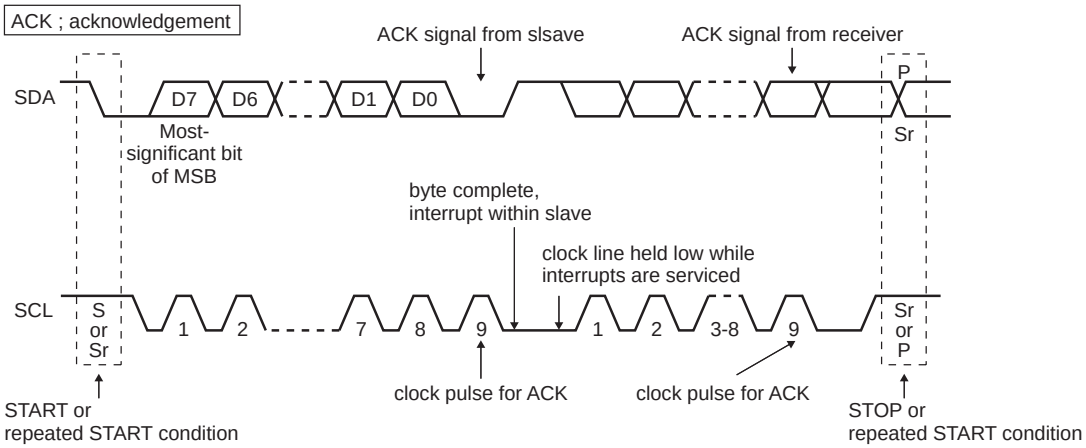
3. Data transmission

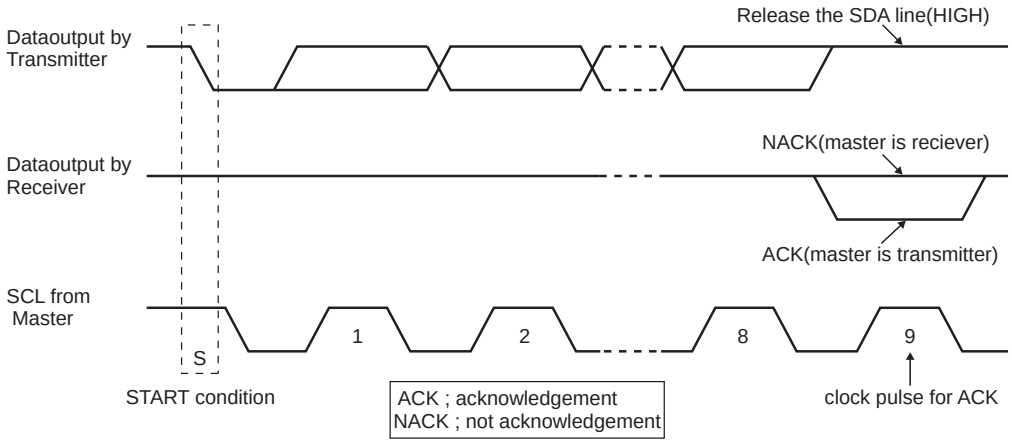
The length of each byte output to the SDA line is always 8 bits. An acknowledge bit is always necessary after each byte, Data is transmitted sequentially from the most significant bit (MSB).

During data transfer, the slave address is transmitted after the "Start" condition (S). Data transfer is always ended by the "Stop" condition (P) generated by the master.



4. Acknowledge (Confirmation of reception)

When the master generates the acknowledge clock pulse, the transmitter opens the SDA line (SDA line entering the "H" state). When the acknowledge clock pulse is in the "H" state, the receiver sets the SDA line to "L" each time it receives one byte (eight bits) of data. When the master functions as receiver, the master informs the end of data to the slave by omitting acknowledgement at the end of data sent from the slave.



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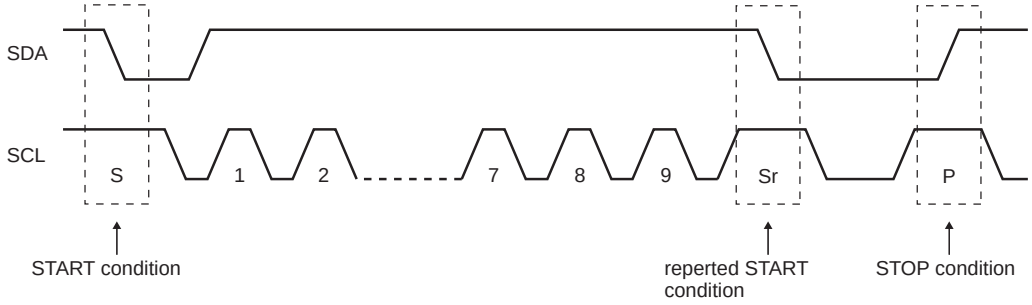
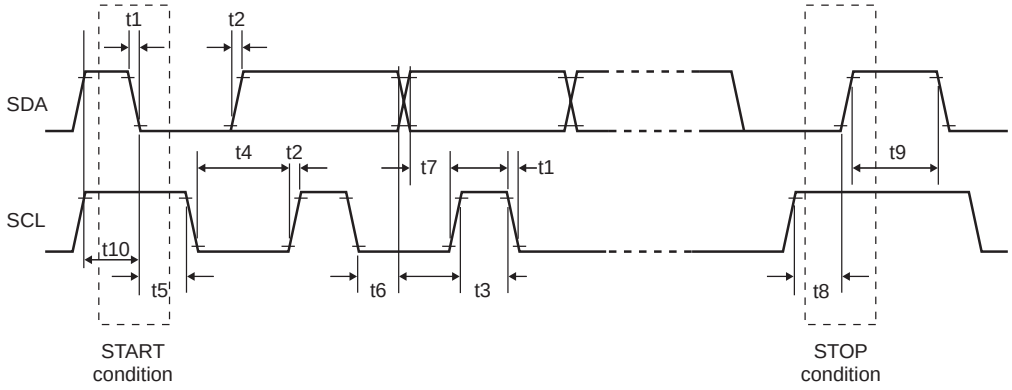
5. Software reset

After power ON, enter the signal as follows to avoid malfunction. If the communication is interrupted (microcomputer reset, etc.), entry of the following signal enables normal operation.



6. Electrical Specification and Timing for I/O Stages



Bus line characteristics

Parameter	Symbol	FAST-MODE		unit	For SCL = 100kHz (Example)
		min	max		
SCL clock frequency	fSCL	-	400	kHz	100
SDA, SCL fall time	t1	20+0.1Cb	300	ns	-
SDA, SCL rise time	t2	20+0.1Cb	300	ns	-
SCL "H" time	t3	0.6	-	µs	3
SCL "L" time	t4	1.3	-	µs	7
"Start" condition hold time	t5	0.6	-	µs	10
Data hold time For I^2C bus device	t6	0.3	-	µs	-
Data setup time	t7	0.1	-	µs	3
"Stop" condition setup time	t8	0.6	-	µs	10
"Stop"-"Start" bus free time	t9	1.3	-	µs	20
"Start" condition setup time	t10	0.6	-	µs	-
Bus line capacitive load	Cb	-	400	pF	-

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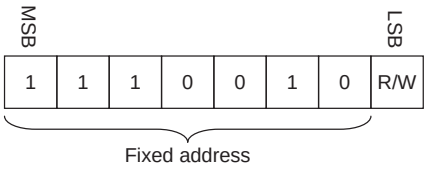
7. Definition of each bit in one byte

7-1. Slave address

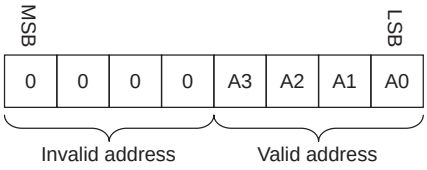
The slave address consists of a fixed seven-bit address "1110010" uniqueto the chip and the eighth bit or a data direction bit (R/W) : Send (Write) when this bit is "0" and Receive (Read) when this bit is "1".



R/W	BIT
READ	1
WRITE	0

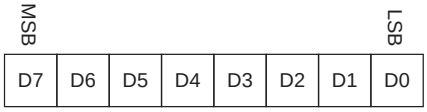
7-2. Register address

Since the total number of internal registers is 16, 4-bit data set on the MSB side becomes invalid.



7-3. Register data

Each register data consists of eight bits.



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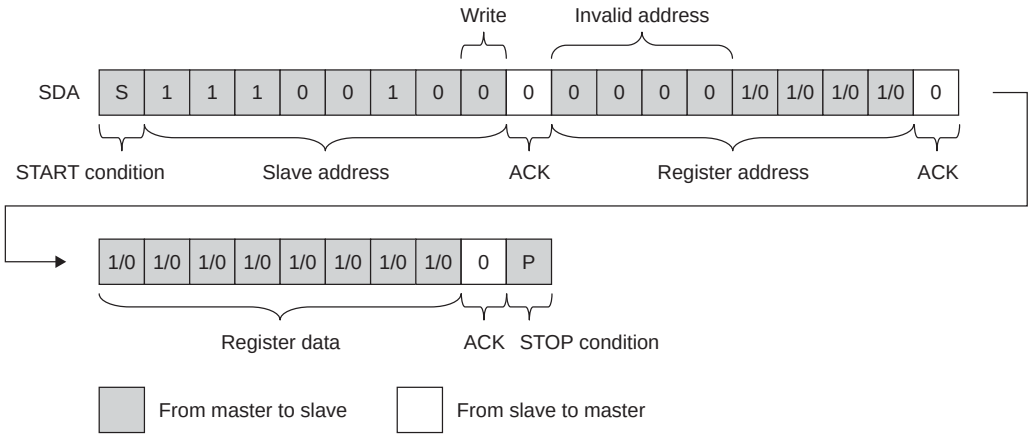
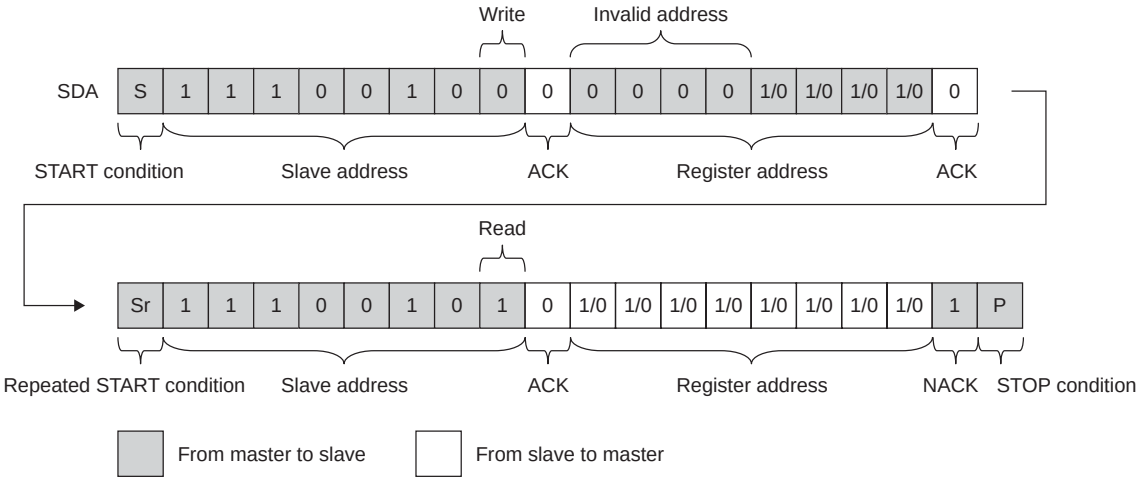
8. Command Format

8-1. Individual register • data writing



8-2. Individual register • data reading



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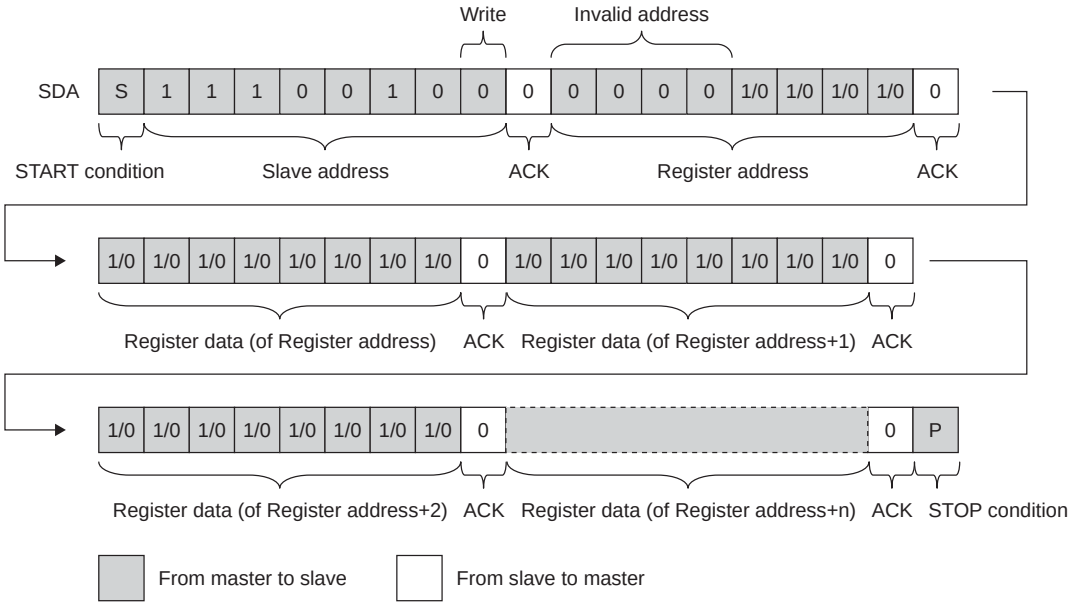
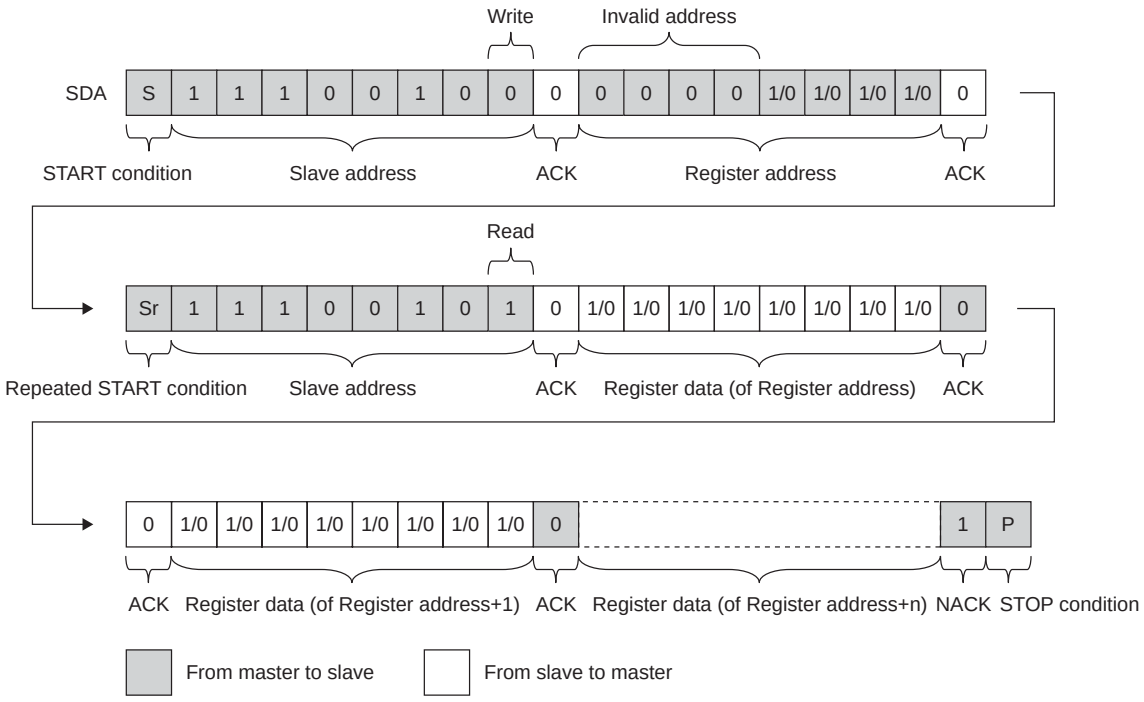
8-3. Consecutive register • data writing



Continuous data transmission after transmission of initially-set address data of register • data writing sequence enables writing of data in the consecutive register • data area. In this case, the register • address increases by one address from the initially-set address of the sequence and continues increasing till the "Stop" condition (P) is generated.

8-4. Consecutive register • data reading



When the master returns ACK (0 data) after reading of the initial register • address • data of read sequence, the register • address increases by one address, enabling consecutive reading of data corresponding to each register address. If the master does not return ACK (0 data), the register address does not increase.

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Register Map <writing>

* Register value : Decimal notation

Register address	Bit	Name	Functions	Bit operation	Default value
0	7	PE	Power enable (all blocks)	0:OFF 1:ON	1
	6	SWSTD	Selection of digital signal monitor pin output /reset detection output	0:RSTDET 1:SD 2:LDO 3:KAGC 4:IFCNT_CLK 5:RSSI_CLK 6:PROCNTR 7:REFCNTR	1
	5				
	4				
	3	LOBIAS	Oscillation level adjustment	0:Oscillation level small	0
	2				
	1				
	0			15:Oscillation level large	
1	7	SDREG	LO/DX changeover (seek determination level adjustment)	15:10dBμV	25
	6				
	5			*1dB STEP	
	4				
	3			55:50dBμV	
	2			(As for value reference value)	
	1	CTE	2ndIF count measurement start control	0:OFF 1:ON (automatically OFF)	0
	0	RSTDET	Initial register writing for reset detection	0:Reset 1:Normal	1
2	7	PCNT	PLL synthesizer program data	0:LSB	
	6				
	5				
	4				
	3				
	2				
	1				
	0				
3	7				
	6				
	5				
	4				
	3				
	2				
	1				
	0				
4	7	GT	2ndIF count time selection	0:4ms 1:8ms 2:32ms 3:64ms	0
	6				
	5	CSEL	PLL master clock signal selection	0:10.95MHz 1:11.25MHz 2:14.55MHz 3:14.75MHz 4:21.15MHz 5:21.45MHz	2
	4				
	3				
	2	FSEL	PLL comparative frequency setting	0:50kHz	0
	1				
	0				
5	7	RSEL	PLL REF reference frequency selection	0:50kHz	0
	6	ADCLK	RSSIADC clock frequency changeover	0:800kHz	0
	5	DZSEL	Dead zone adjustment	0:0ns 1:2ns 2:10ns 3:20ns	0
	4				
	3	CI	ChargePump output current setting	0:0μA	1
	2			*10μA STEP	
	1				
	0			15:150μA	

$$\mathrm{PCNT} = \frac{\text{Receiver frequency} + 1\text{stl frequency}}{50\mathrm{kHz}} (\text{upperlocal setting})$$

$$\mathrm{PCNT} = \frac{\text{Receiver frequency} + 1\text{stl frequency}}{50\mathrm{kHz}} (\text{lowerlocal setting})$$

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* Register value : Decimal notation

Register address	Bit	Name	Functions	Bit operation	Default value
6	7			0:Fixing	0
	6	PEVCO	Power enable (VCO)	0:OFF 1:ON	1
	5	BGRTEST	BGR (RFAGC circuit) inspection mode changeover	0:OFF 1:ON	0
	4			0:Fixing	0
	3	SMTREG	Softmute start point adjustment	0:Softmute function OFF	10
	2			1:-4dBμV *2dB STEP	
	1			15:24dBμV	
	0			(As for value reference value)	
7	7	RSSIGAIN	RSSI detection sensitivity adjustment	0:31mV/dB *1mV/dB STEP	4
	6		*RSSI output gradient	7:38mV/dB	
	5			(As for value reference value)	
	4	RSSITMP	RSSI detection temperature characteristics adjustment	0:4dB *0.5dB STEP	3
	3		*Front-end circuit temperature characteristics compensation	7:7.5dB	
	2			(As for value reference value)	
	1			0:Fixing	0
	0				
8	7	WAGC	W_AGC sensitivity adjustment	0:Sensitivity low *1.1dB STEP	15
	6				
	5				
	4			15:Sensitivity high	
	3	NAGC	N_AGC sensitivity adjustment	0:Sensitivity low *1.1dB STEP	6
	2				
	1				
	0			15:Sensitivity high	
9	7	KAGC	Keyed-AGC judgment level adjustment	0:-3dBμV	6
	6			*2dB STEP	
	5			15:27dBμV	
	4			(As for value reference value)	
	3	WAGCSW	W_AGC_ON/OFF	0:OFF 1:ON	1
	2	NAGCSW	N_AGC_ON/OFF	0:OFF 1:ON	1
	1	ATTAGCSW	ATT_AGC_ON/OFF	0:OFF 1:ON	1
	0	LNAAGCSW	LNA_AGC_ON/OFF	0:OFF 1:ON	1
10	7	KAGCSW	Keyed-AGC_ON/OFF	0:OFF 1:ON	0
	6	WKAGCSW	Keyed-W_AGC sensitivity changeover	0:No sensitivity change 1:-10dB sensitivity change	0
	5	LNAG	LNA gain adjustment	0:17dB 1:19dB	3
	4			2:21dB 3:23dB	
	3	MIXG	1stMIX gain adjustment	0:-0.2dB 1:2.8dB	3
	2			2:4.5dB 3:5.4dB	
	1	IFAG	1stIFA gain adjustment	0:7dB 1:10dB	3
	0			2:13dB 3:16dB	
11	7			0:Fixing	0
	6				
	5				
	4	XOSCADJ	Crystal oscillation level adjustment	0:oscillation allowance, small	0
	3				
	2			7:oscillation allowance, large	
	1			0:Fixing	0
	0			0:Fixing	0

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* Register value : Decimal notation

Register address	Bit	Name	Functions	Bit operation	Default value
12	7	RMXG	Composite output level adjustment	0:3.1dB 1:3.7dB 2:4.4dB 3:5.2dB	0
	6				
	5			4:6.0dB 5:6.9dB 6:8.0dB 9:9.1dB	
	4	DEMODR	Detection output level adjustment	0:106mVrm 1:119mVrms 2:151mVrms 3:167mVrms	7
	3			4:212mVrm 5:230mVrms 6:276mVrms 7:297mVrms	
	2			(As for value reference value)	
	1	PERF	Power enable (RF block)	0:OFF 1:ON	1
	0	PEIF	Power enable (IF block)	0:OFF 1:ON	1
13	7	PEDEM	Power enable (LIM/DEMOD)	0:OFF 1:ON	1
	6	PEAMP	Power enable (audio amplifier)	0:OFF 1:ON	1
	5	PEXOSC	Power enable (XOSC)	0:OFF 1:ON	1
	4	PELNA	Power enable (LNA)	0:OFF 1:ON	1
	3	PELO1	Power enable (LO block_VCOetc)	0:OFF 1:ON	1
	2	PELO2	Power enable (LO block_LOBUFetc)	0:OFF 1:ON	1
	1	PEREFCNT	Power enable (REF counter)	0:OFF 1:ON	1
	0	PERFAGC	Power enable (RFAGC block)	0:OFF 1:ON	1
14	7				
	6				
	5				
	4				
	3				
	2				
	1				
	0				
15	7				
	6				
	5				
	4				
	3				
	2				
	1				
	0				

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Register Map <reading>

* Register value : Decimal notation

Register address	Bit	Name	Functions	Bit operation	Default value
0	7	PE	Power enable (all blocks)	0:OFF 1:ON	1
	6	SWSTD	Selection of digital signal monitor pin output /reset detection output	0:RSTDET 1:SD 2:LDO 3:KAGC 4:IFCNT_CLK 5:RSSI_CLK 6:PROCNTR 7:REFCNTR	1
	5				
	4				
	3	LOBIAS	GM adjustment of the oscillation circuit core block	0:Oscillation level small 15:Oscillation level large	0
	2				
	1				
	0				
1	7	SDREG	LO/DX changeover (seek determination level adjustment)	15:10dBμV *1dB STEP 55:50dBμV (As for value reference value)	25
	6				
	5				
	4				
	3				
	2				
	1	CTE	2ndIF count measurement start control	0:OFF 1:ON (automatically OFF)	0
	0	RSTDET	Initial register writing for reset detection	0:Reset 1:Normal	1
2	7	IFCOUT	2ndIF count value output	0:LSB $2\text{ndIF frequency} = \frac{\text{IFCOUT value}(2\text{ndIF count value})}{\text{GT}}$	
	6				
	5				
	4				
	3				
	2				
	1				
	0				
3	7				
	6				
	5				
	4				
	3				
	2				
	1				
	0				
4	7	GT	2ndIF count time selection	0:4ms 1:8ms 2:32ms 3:64ms	0
	6				
	5	CSEL	PLL master clock signal selection	0:10.95MHz 1:11.25MHz 2:14.55MHz 3:14.75MHz 4:21.15MHz 5:21.45MHz	2
	4				
	3				
	2	FSEL	PLL comparative frequency setting	0:50kHz	0
	1				
	0				
5	7	RSEL	PLL REF reference frequency selection	0:50kHz	0
	6	ADCLK	RSSIADC clock frequency changeover	0:800kHz	0
	5	DZSEL	Dead zone adjustment	0:0ns 1:2ns 2:10ns 3:20ns	0
	4				
	3	CI	ChargePump output current setting	0:0μA *10μA STEP 15:150μA	1
	2				
	1				
	0				

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* Register value : Decimal notation

Register address	Bit	Name	Functions	Bit operation	Default value
6	7			0:Fixing	0
	6	PEVCO	Power enable (VCO)	0:OFF 1:ON	1
	5	BGRTEST	BGR(RFAGC circuit) inspection mode changeover	0:OFF 1:ON	0
	4			0:Fixing	0
	3	SMTREG	Softmute start point adjustment	0:Softmute function OFF	10
	2			1:-4dBμV *2dB STEP	
	1			15:24dBμV	
	0			(As for value reference value)	
7	7	RSSIGAIN	RSSI detection sensitivity adjustment	0:31mV/dB *1mV/dB STEP	4
	6		*RSSI output gradient	7:38mV/dB	
	5			(As for value reference value)	
	4	RSSITMP	RSSI detection temperature characteristics adjustment	0:4dB *0.5dB STEP	3
	3		*Front-end circuit temperature characteristics compensation	7:7.5dB	
	2			(As for value reference value)	
	1			0:Fixing	0
	0				
8	7	WAGC	W_AGC sensitivity adjustment	0:Sensitivity low *1.1dB STEP	15
	6				
	5				
	4			15:Sensitivity high	
	3	NAGC	N_AGC sensitivity adjustment	0:Sensitivity low *1.1dB STEP	6
	2				
	1				
	0			15:Sensitivity high	
9	7	KAGC	Keyed-AGC judgment level adjustment	0:-3dBμV	6
	6			*2dB STEP	
	5			15:27dBμV	
	4			(As for value reference value)	
	3	WAGCSW	W_AGC_ON/OFF	0:OFF 1:ON	1
	2	NAGCSW	N_AGC_ON/OFF	0:OFF 1:ON	1
	1	ATTAGCSW	ATT_AGC_ON/OFF	0:OFF 1:ON	1
	0	LNAAGCSW	LNA_AGC_ON/OFF	0:OFF 1:ON	1
10	7	KAGCSW	Keyed-AGC_ON/OFF	0:OFF 1:ON	0
	6	WKAGCSW	Keyed-W_AGC sensitivity changeover	0:No sensitivity change 1:-10dB sensitivity change	0
	5	LNAG	LNA gain adjustment	0:17dB 1:19dB	3
	4			2:21dB 3:23dB	
	3	MIXG	1stMIX gain adjustment	0:0dB 1:2dB	3
	2			2:4dB 3:6dB	
	1	IFAG	1stIFA gain adjustment	0:7dB 1:10dB	3
	0			2:13dB 3:16dB	
11	7			0:Fixing	0
	6				
	5				
	4	XOSCADJ	Crystal oscillation level adjustment	0:oscillation allowance, small	0
	3				
	2			7:Oscillation allowance, larg	
	1			0:Fixing	0
	0			0:Fixing	0

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* Register value : Decimal notation

Register address	Bit	Name	Functions	Bit operation	Default value
12	7	RMXG	Composite output level adjustment	0:3.1dB 1:3.7dB 2:4.4dB 3:5.2dB	0
	6				
	5			4:6.0dB 5:6.9dB 6:8.0dB 9:9.1dB	
	4	DEMODR	Detection output level adjustment	0:106mVrm 1:119mVrms 2:151mVrms 3:167mVrms	7
	3			4:212mVrm 5:230mVrms 6:276mVrms 7:297mVrms	
	2			(As for value reference value)	
	1	PERF	Power enable (RF block)	0:OFF 1:ON	1
	0	PEIF	Power enable (IF block)	0:OFF 1:ON	1
13	7	PEDEM	Power enable (LIM/DEMOD)	0:OFF 1:ON	1
	6	PEAMP	Power enable (audio amplifier)	0:OFF 1:ON	1
	5	PEXOSC	Power enable (XOSC)	0:OFF 1:ON	1
	4	PELNA	Power enable (LNA)	0:OFF 1:ON	1
	3	PELO1	Power enable (LO block_VCOetc)	0:OFF 1:ON	1
	2	PELO2	Power enable (LO block_LOBUFetc)	0:OFF 1:ON	1
	1	PEREFCNT	Power enable (REF counter)	0:OFF 1:ON	1
	0	PERFAGC	Power enable (RFAGC block)	0:OFF 1:ON	1
14	7	WAGCOUT	W_AGC output	0:LSB	
	6				
	5				
	4				
	3	SMTSWOUT	Soft mute changeover control signal output	0:LSB	
	2				
	1				
	0				
15	7	RSSIOUT	RSSI digital output	0:LSB	
	6				
	5				
	4				
	3				
	2				
	1				
	0				

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