Innovasic®
Semiconductor
Extended Life Semiconductor Solutions

IA186XL/IA188XL
16-Bit Microcontroller
Data Sheet

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1. Introduction

The Innovasic Semiconductor IA186XL and IA188XL microcontrollers are form, fit, and function replacements for the original Intel 80C186XL and 80C188XL 16-bit high-integration embedded processors.

These devices are produced using Innovasic's Managed IC Lifetime Extension System (MILES™). This cloning technology, which produces replacement ICs beyond simple emulations, ensures complete compatibility with the original device, including any "undocumented features." Additionally, the MILES™ process captures the clone design in such a way that production of the clone can continue even as silicon technology advances.

The IA186XL and IA188XL microcontrollers replace the obsolete Intel 80C186XL and 80C188XL devices, allowing users to retain existing board designs, software compilers/assemblers, and emulation tools, thereby avoiding expensive redesign efforts.

1.1 General Description

The Innovasic Semiconductor IA186XL and IA188XL microcontrollers are an upgrade for the 80C186XL/80C188XL microcontroller designs, with integrated peripherals to provide increased functionality and reduce system costs. The IA186XL and IA188XL devices are designed to satisfy requirements of embedded products.

The IA186XL and IA188XL microcontrollers have a set of base peripherals beneficial to many embedded applications and include a standard numeric interface, an interrupt control unit, a chip-select unit/Ready Generation Logic, a DRAM refresh control unit, a Power-Save Control unit, and three 16-bit timer/counters.

The IA186XL and IA188XL microcontrollers operate at 5.0 volts ± 10%.

The following functional description describes the base architecture of the 80C186XL. The 80C186XL is a very high integration 16-bit microprocessor. It combines some of the most common microprocessor system components onto one chip. The 80C186XL is object-code compatible with the 8086/8088 microprocessors and adds ten new instruction types to the 8086/8088 instruction set.

The 80C186XL has two major modes of operation, Compatible and Enhanced. In Compatible Mode, the 80C186XL is completely compatible with the 80186, with the exception of 8087 support. The Enhanced mode adds three new features to the system design. These are Power-Save control, Dynamic RAM refresh, and an asynchronous Numerics Coprocessor interface (80C186XL only).

1.2 Features

The primary features of the IA186XL and IA188XL microcontrollers are as follows:

- Form, fit, and function compatible version of the low power Intel 80C186XL/80C188XL
- Operation modes:
  - Enhanced mode
    - DRAM refresh control unit
    - Power-save mode
    - Direct interface to 80C187 (IA186XL only)
  - Compatible mode
    - Pin-for-pin replacement for NMOS 80186/80188 non-numeric applications
- Integrated feature set
  - Static, modular CPU
  - Clock generator
  - Two independent DMA channels
  - Programmable interrupt controller
  - Three programmable 16-bit timers
  - Dynamic RAM refresh control unit
  - Programmable memory and peripheral chip select logic
  - Programmable wait state generator
  - Local bus controller
  - Power-save mode
  - System-level testing support (high impedance test mode)
- Completely object-code compatible with existing 8086/8088 software and has ten additional instructions over 8086/8088
- Crystal supports internal 20–33 MHz operation
- Direct addressing capability to 1 MByte memory and 64 Kbyte I/O
- Available in 68-Lead:
  - Plastic Leaded Chip Carrier (PLCC)
- Available in 80-Lead:
  - Plastic Quad Flat Pack (PQFP)
  - Low Profile Quad Flat Pack (LQFP)
- Extended Temperature Range (-40°C to +85°C)

Chapter 4, Functional Description, provides details of the IA186XL and IA188XL microcontrollers, including the features listed above.

2. Packaging, Pin Descriptions, and Physical Dimensions

Information on the packages and pin descriptions for the IA186XL and the IA188XL is provided separately. Refer to sections, figures, and tables for information on the device of interest.

2.1 Packages and Pinouts

The Innovasic Semiconductor IA186XL and IA188XL microcontroller is available in the following packages:

- 68-Lead Plastic Leaded Chip Carrier (PLCC), equivalent to original PLCC package
- 80-Lead Plastic Quad Flat Pack (PQFP), equivalent to original PQFP package
- 80-Lead Low Profile Quad Flat Pack (LQFP), equivalent to original SQFP package

2.1.1 IA186XL 68 PLCC Package

The pinout for the IA186XL 68 PLCC package is as shown in Figure 1. The corresponding pinout is provided in Table 1.

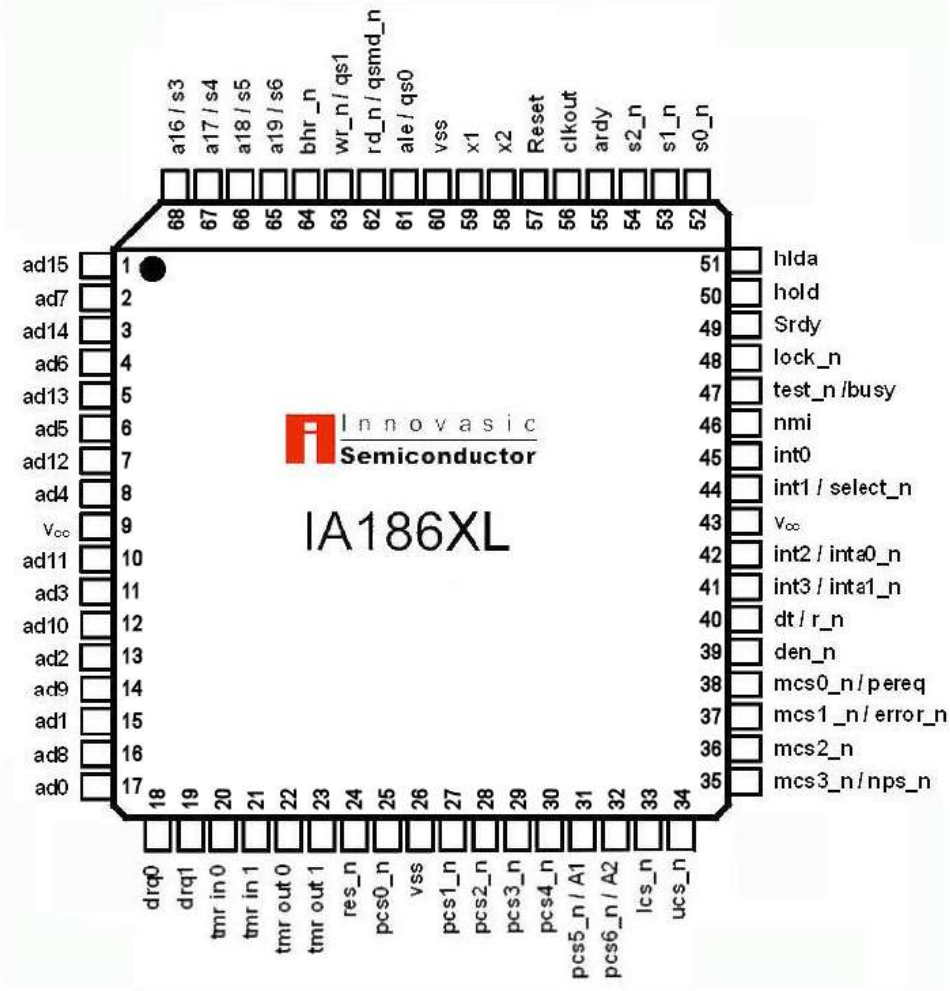


Figure 1. IA186XL 68-Lead PLCC Package Diagram

Table 1. IA186XL 68-Lead PLCC Pin Listing

Pin	Name
1	ad15
2	ad7
3	ad14
4	ad6
5	ad13
6	ad5
7	ad12
8	ad4
9	v_{cc}
10	ad11
11	ad3
12	ad10
13	ad2
14	ad9
15	ad1
16	ad8
17	ad0

Pin	Name
18	drq0
19	drq1
20	tmr in 0
21	tmr in 1
22	tmr out 0
23	tmr out 1
24	res_n
25	pcs0_n
26	v_{ss}
27	pcs1_n
28	pcs2_n
29	pcs3_n
30	pcs4_n
31	pcs5_n/a1
32	pcs6_n/a2
33	lcs_n
34	ucs_n

Pin	Name
35	mcs3_n/nps_n
36	mcs2_n
37	mcs1 _n/error_n
38	mcs0_n/pereq
39	den_n
40	dt/r_n
41	int3/inta1_n
42	int2/inta0_n
43	v_{cc}
44	int1/select_n
45	int0
46	nmi
47	test_n /busy
48	lock_n
49	srdy
50	hold
51	hlda

Pin	Name
52	s0_n
53	s1_n
54	s2_n
55	ardy
56	clkout
57	reset
58	x2
59	x1
60	v_{ss}
61	ale/qs0
62	rd_n/qsmd_n
63	wr_n/qs1
64	bhe_n
65	a19/s6
66	a18/s5
67	a17/s4
68	a16/s3

2.1.2 IA188XL 68 PLCC Package

The pinout for the IA188XL 68 PLCC package is as shown in Figure 2. The corresponding pinout is provided in Table 2.

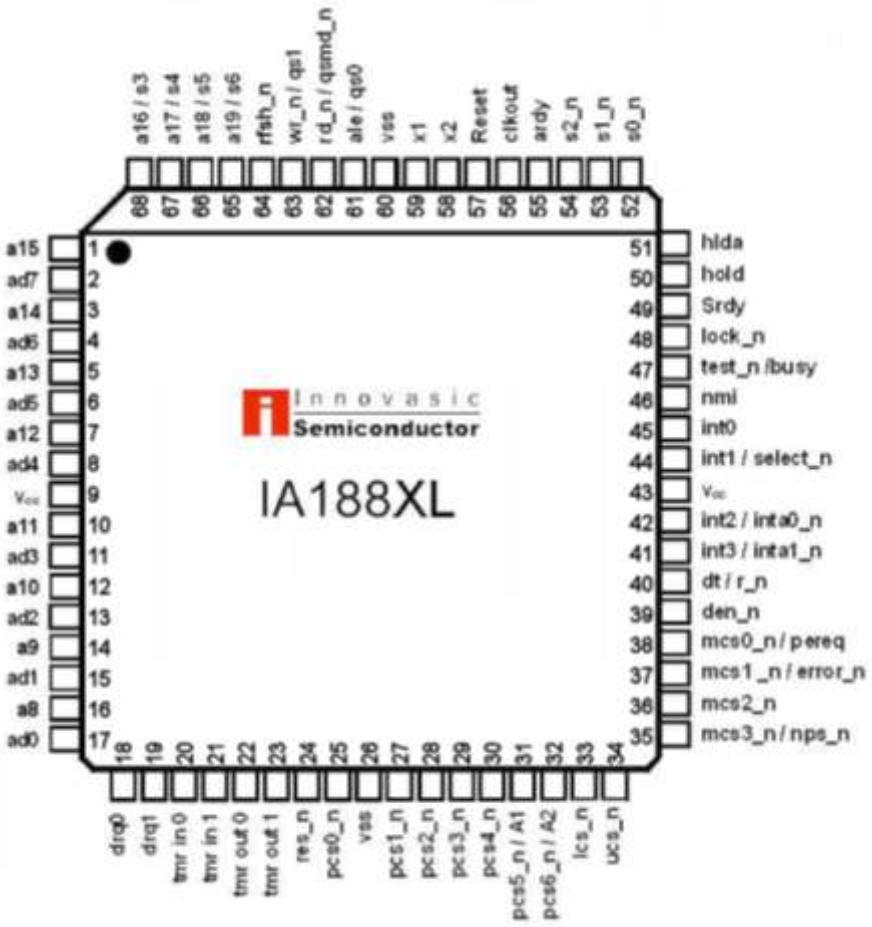


Figure 2. IA188XL 68-Lead PLCC Package Diagram

Table 2. IA188XL 68-Lead PLCC Pin Listing

Pin	Name
1	a15
2	ad7
3	a14
4	ad6
5	a13
6	ad5
7	a12
8	ad4
9	v_{cc}
10	a11
11	ad3
12	a10
13	ad2
14	a9
15	ad1
16	a8
17	ad0

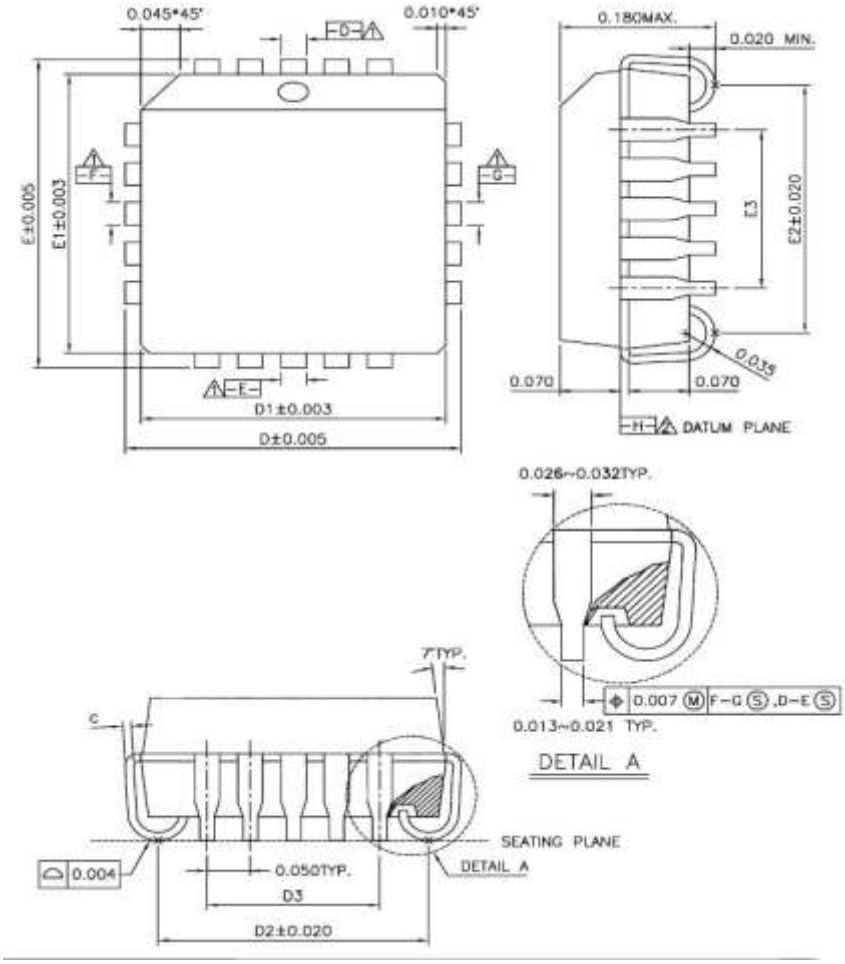
Pin	Name
18	drq0
19	drq1
20	tmr in 0
21	tmr in 1
22	tmr out 0
23	tmr out 1
24	res_n
25	pcs0_n
26	v_{ss}
27	pcs1_n
28	pcs2_n
29	pcs3_n
30	pcs4_n
31	pcs5_n/a1
32	pcs6 _n/a2
33	lcs_n
34	ucs_n

Pin	Name
35	mcs3_n/nps_n
36	mcs2_n
37	mcs1 _n/error_n
38	mcs0 _n/pereq
39	den_n
40	dt/r_n
41	int3/inta1_n
42	int2/inta0_n
43	v_{cc}
44	int1/select_n
45	int0
46	nmi
47	test_n /busy
48	lock_n
49	srdy
50	hold
51	hlda

Pin	Name
52	s0_n
53	s1_n
54	s2_n
55	ardy
56	clkout
57	reset
58	x2
59	x1
60	v_{ss}
61	ale/qs0
62	rd _n/qsmd_n
63	wr _n/qs1
64	rfsh_n
65	a19/s6
66	a18/s5
67	a17/s4
68	a16/s3

2.1.3 PLCC Physical Dimensions

The physical dimensions for the 68 PLCC are as shown in Figure 3.



Legend:

Symbol	Min	Nom	Max
c	–	0.008	–
D	–	1.190”	–
D1	–	1.154”	–
D2	–	0.910	
D3	–	0.800	–
E	–	1.190”	–
E1	–	1.154”	–
E2	–	0.910	–
E3	–	0.800	–
F	–	1.110”	–

1. Datums D–E and F–G to be determined where center leads exit plastic body at Datum Plane –H–.

2. Datum Plane –H– located at top of mold parting line and coincident with top of lead. Where lead exits plastic body.

Note: Controlling dimension in inches.

Figure 3. PLCC Physical Package Dimensions

2.1.4 IA186XL 80 PQFP Package

The pinout for the IA186XL 80 PQFP package is as shown in Figure 4. The corresponding pinout is provided in Table 3.

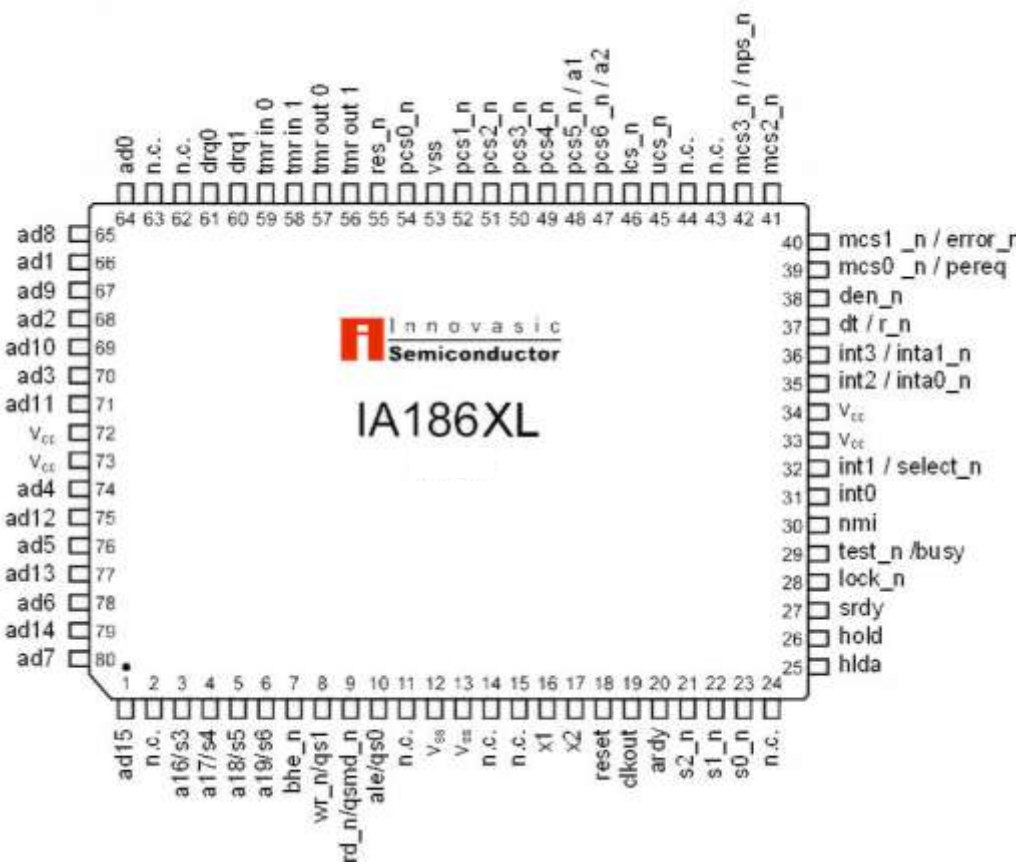


Figure 4. IA186XL 80-Lead PQFP Package Diagram

Table 3. IA186XL 80-Lead PQFP Pin Listing

Pin	Name
1	ad15
2	n.c.
3	a16/s3
4	a17/s4
5	a18/s5
6	a19/s6
7	bhe_n
8	wr_n/qs1
9	rd_n/qsmd_n
10	ale/qs0
11	n.c.
12	V_{SS}
13	V_{SS}
14	n.c.
15	n.c.
16	x1
17	x2
18	reset
19	clkout
20	ardy

Pin	Name
21	s2_n
22	s1_n
23	s0_n
24	n.c.
25	hlda
26	hold
27	srdy
28	lock_n
29	test_n /busy
30	nmi
31	int0
32	int1/select_n
33	V_{CC}
34	V_{CC}
35	int2/inta0_n
36	int3/inta1_n
37	dt/r_n
38	den_n
39	mcs0 _n/pereq
40	mcs1 _n/error_n

Pin	Name
41	mcs2_n
42	mcs3_n/nps_n
43	n.c.
44	n.c.
45	ucs_n
46	lcs_n
47	pcs6 _n/a2
48	pcs5_n/a1
49	pcs4_n
50	pcs3_n
51	pcs2_n
52	pcs1_n
53	V_{SS}
54	pcs0_n
55	res_n
56	tmr out 1
57	tmr out 0
58	tmr in 1
59	tmr in 0
60	drq1

Pin	Name
61	drq0
62	n.c.
63	n.c.
64	ad0
65	ad8
66	ad1
67	ad9
68	ad2
69	ad10
70	ad3
71	ad11
72	V_{CC}
73	V_{CC}
74	ad4
75	ad12
76	ad5
77	ad13
78	ad6
79	ad14
80	ad7

2.1.5 IA188XL 80 PQFP Package

The pinout for the IA186XL 80 PQFP package is as shown in Figure 5. The corresponding pinout is provided in Table 4.

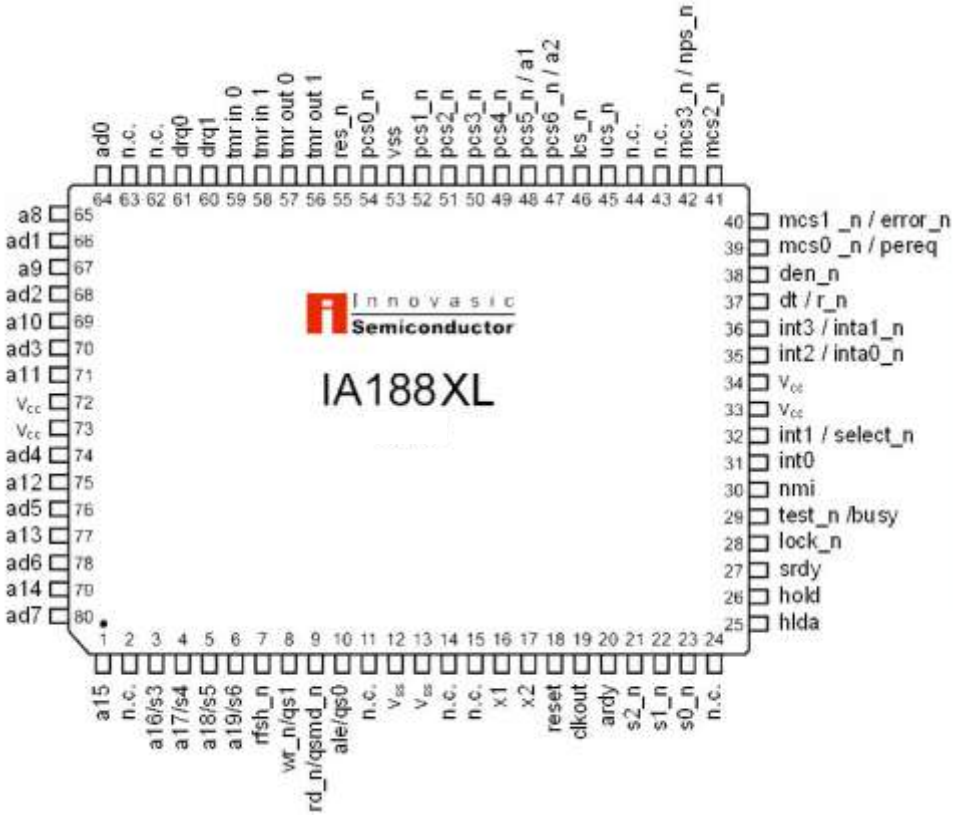


Figure 5. IA188XL 80-Lead PQFP Package Diagram

Table 4. IA188XL 80-Lead PQFP Pin Listing

Pin	Name
1	a15
2	n.c.
3	a16/s3
4	a17/s4
5	a18/s5
6	a19/s6
7	rfsh_n
8	wr_n/qs1
9	rd_n/qsmd_n
10	ale/qs0
11	n.c.
12	V_{SS}
13	V_{SS}
14	n.c.
15	n.c.
16	x1
17	x2
18	reset
19	clkout
20	ardy

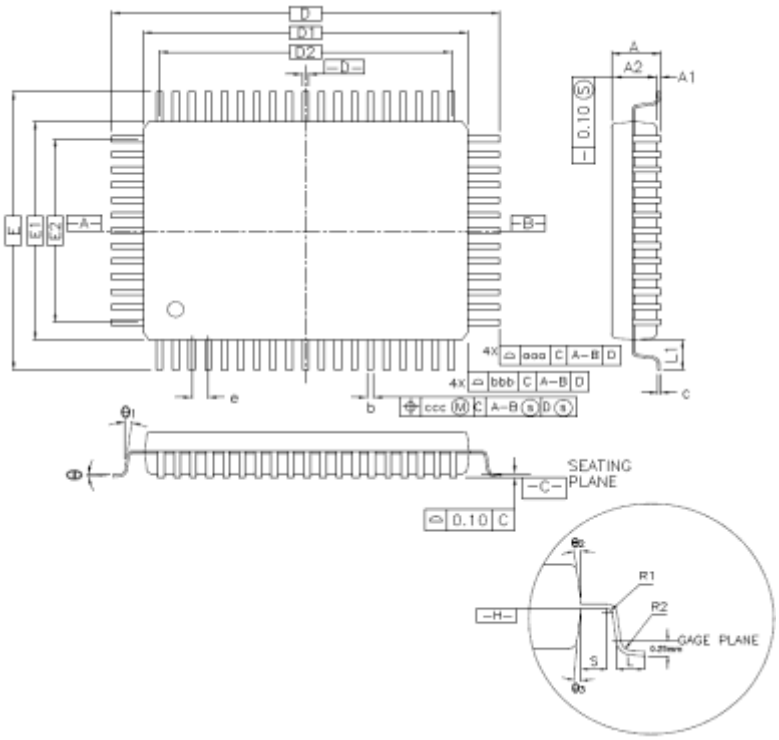
Pin	Name
21	s2_n
22	s1_n
23	s0_n
24	n.c.
25	hlda
26	hold
27	srdy
28	lock_n
29	test_n /busy
30	nmi
31	int0
32	int1/select_n
33	V_{CC}
34	V_{CC}
35	int2/inta0_n
36	int3/inta1_n
37	dt/r_n
38	den_n
39	mcs0 _n/pereq
40	mcs1 _n/error_n

Pin	Name
41	mcs2_n
42	mcs3_n/nps_n
43	n.c.
44	n.c.
45	ucs_n
46	lcs_n
47	pcs6 _n/a2
48	pcs5_n/a1
49	pcs4_n
50	pcs3_n
51	pcs2_n
52	pcs1_n
53	V_{SS}
54	pcs0_n
55	res_n
56	tmr out 1
57	tmr out 0
58	tmr in 1
59	tmr in 0
60	drq1

Pin	Name
61	drq0
62	n.c.
63	n.c.
64	ad0
65	a8
66	ad1
67	a9
68	ad2
69	a10
70	ad3
71	a11
72	V_{CC}
73	V_{CC}
74	ad4
75	a12
76	ad5
77	a13
78	ad6
79	a14
80	ad7

2.1.6 PQFP Physical Dimensions

The physical dimensions for the 80 PQFP are as shown in Figure 6.



Notes:
1. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimension D1 and E1 do not include mold mismatch and are determined a datum plane –H–.
2. Dimension b does not include dambar protrusion. Allowable dambar protrusion will not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located on the lower radius of the lead foot.

Legend:

	Millimeter			Inch		
Symbol	Min	Nom	Max	Min	Nom	Max
A	–	–	3.40	–	–	0.134
A1	0.25	–	–	0.010	–	–
A2	2.55	2.72	3.05	0.100	0.107	0.120
D	23.90 Basic			0.941 Basic		
D1	20.00 Basic			0.787 Basic		
E	17.90 Basic			0.705 Basic		
E1	14.00 Basic			0.551 Basic		
R2	0.013	–	0.30	0.005	–	0.012
R1	0.013	–	–	0.005	–	–
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	–	–	0°	–	–
θ2, θ3[a]	7° REF			7° REF		
θ2, θ3[b]	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.95 REF			0.077 REF		
S	0.40	–	–	0.016	–	–
b	0.30	0.35	0.45	0.012	0.014	0.018
e	0.80 BSC			0.031 BSC		
D2	18.40 REF			0.724		
E2	12.00 REF			0.472		
Tolerances of Form and Position						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.20			0.008		

[a]Alloy 42 L/F.
[b]Copper L/F.

Figure 6. PQFP Physical Package Dimensions

2.1.7 IA186XL 80 LQFP Package

The pinout for the IA186XL 80 LQFP package is as shown in Figure 7. The corresponding pinout is provided in Table 5.

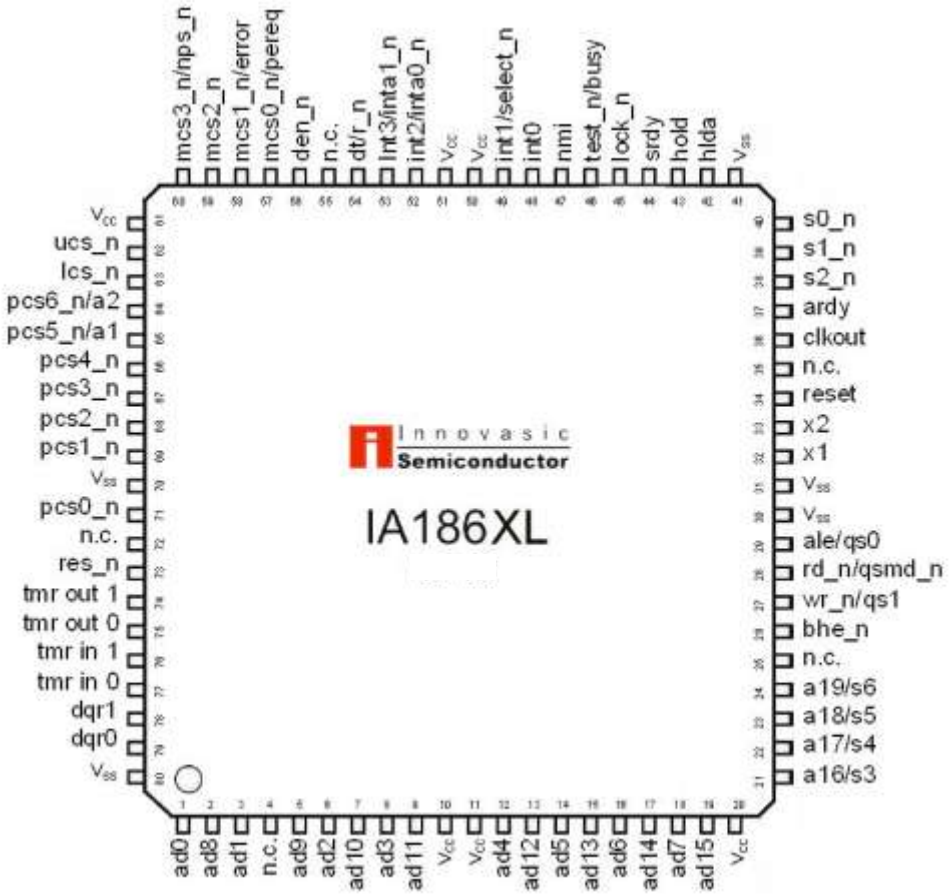


Figure 7. IA186XL 80-Lead LQFP Package Diagram

Table 5. IA186XL 80-Lead LQFP Pin Listing

Pin	Name
1	ad0
2	ad8
3	ad1
4	n.c.
5	ad9
6	ad2
7	ad10
8	ad3
9	ad11
10	v_{cc}
11	v_{cc}
12	ad4
13	ad12
14	ad5
15	ad13
16	ad6
17	ad14
18	ad7
19	ad15
20	v_{cc}

Pin	Name
21	a16/s3
22	a17/s4
23	a18/s5
24	a19/s6
25	n.c.
26	bhe_n
27	wr_n/qs1
28	rd_n/qsmd_n
29	ale/qs0
30	v_{ss}
31	v_{ss}
32	x1
33	x2
34	reset
35	n.c.
36	clkout
37	ardy
38	s2_n
39	s1_n
40	s0_n

Pin	Name
41	v_{ss}
42	hlda
43	hold
44	srdy
45	lock_n
46	test_n/busy
47	nmi
48	int0
49	int1/select_n
50	v_{cc}
51	v_{cc}
52	int2/inta0_n
53	int3/inta1_n
54	dt/r_n
55	n.c.
56	den_n
57	mcs0_n/pereq
58	mcs1_n/error
59	mcs2_n
60	mcs3_n/nps_n

Pin	Name
61	v_{cc}
62	ucs_n
63	lcs_n
64	pcs6_n/a2
65	pcs5_n/a1
66	pcs4_n
67	pcs3_n
68	pcs2_n
69	pcs1_n
70	v_{ss}
71	pcs0_n
72	n.c.
73	res_n
74	tmr out 1
75	tmr out 0
76	tmr in 1
77	tmr in 0
78	dqr1
79	dqr0
80	v_{ss}

2.1.8 IA188XL 80 LQFP Package

The pinout for the IA188XL 80 LQFP package is as shown in Figure 8. The corresponding pinout is provided in Table 6.

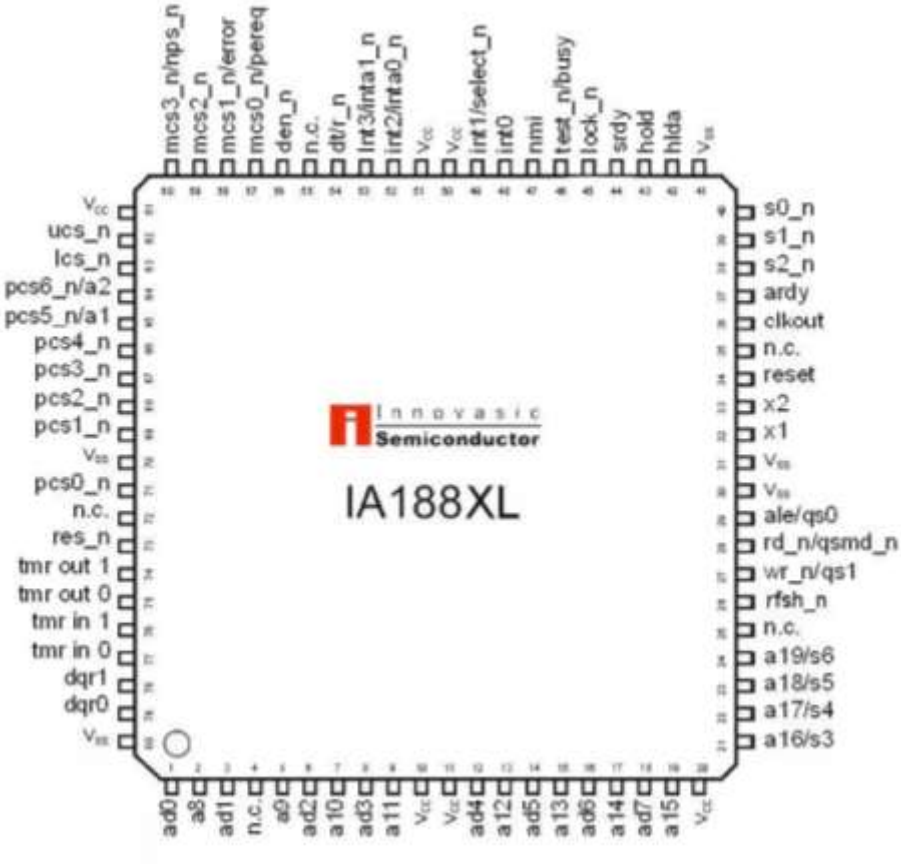


Figure 8. IA188XL 80-Lead LQFP Package Diagram

Table 6. IA188XL 80-Lead LQFP Pin Listing

Pin	Name
1	ad0
2	a8
3	ad1
4	n.c.
5	a9
6	ad2
7	a10
8	ad3
9	a11
10	v_{cc}
11	v_{cc}
12	ad4
13	a12
14	ad5
15	a13
16	ad6
17	a14
18	ad7
19	a15
20	v_{cc}

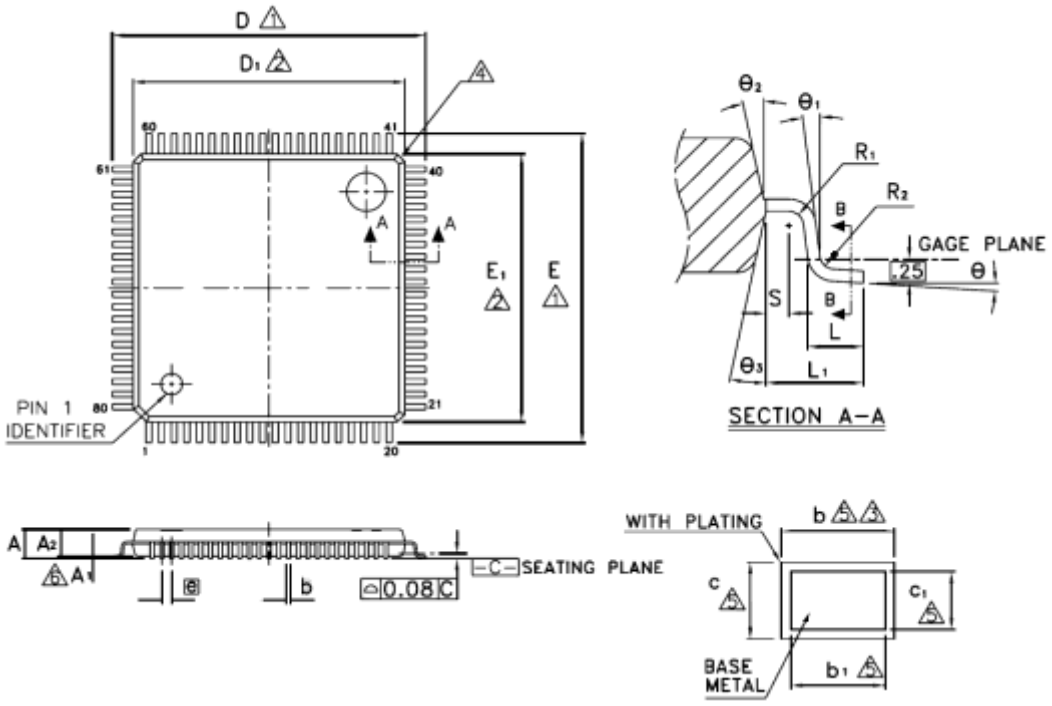
Pin	Name
21	a16/s3
22	a17/s4
23	a18/s5
24	a19/s6
25	n.c.
26	rfsh_n
27	wr_n/qs1
28	rd_n/qsmd_n
29	ale/qs0
30	v_{ss}
31	v_{ss}
32	x1
33	x2
34	reset
35	n.c.
36	clkout
37	ardy
38	s2_n
39	s1_n
40	s0_n

Pin	Name
41	v_{ss}
42	hlda
43	hold
44	srdy
45	lock_n
46	test_n/busy
47	nmi
48	int0
49	int1/select_n
50	v_{cc}
51	v_{cc}
52	int2/inta0_n
53	Int3/inta1_n
54	dt/r_n
55	n.c.
56	den_n
57	mcs0_n/pereq
58	mcs1_n/error
59	mcs2_n
60	mcs3_n/nps_n

Pin	Name
61	v_{cc}
62	ucs_n
63	lcs_n
64	pcs6_n/a2
65	pcs5_n/a1
66	pcs4_n
67	pcs3_n
68	pcs2_n
69	pcs1_n
70	v_{ss}
71	pcs0_n
72	n.c.
73	res_n
74	tmr out 1
75	tmr out 0
76	tmr in 1
77	tmr in 0
78	dqr1
79	dqr0
80	v_{ss}

2.1.9 LQFP Physical Dimensions

The physical dimensions for the 80 LQFP are as shown in Figure 9.



Legend:

Symbol	Dimension in mm Min	Nom	Max	Dimension in Inch Min	Nom	Max
A	–	–	1.60	–	–	0.063
A_1	0.05	–	0.15	0.002	–	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	–	0.20	0.004	–	0.008
c_1	0.09	–	0.16	0.004	–	0.006
D	14.00 BSC			0.551 BSC		
D_1	12.00 BSC			0.472 BSC		
E	14.00 BSC			0.551 BSC		
E_1	12.00 BSC			0.472 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	–	–	0.003	–	–
R_2	0.08	–	0.20	0.003	–	0.008
S	0.20	–	–	0.008	–	–
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°

1. To be determined at seating plane C.
2. Dimensions D1 and E1 do not include mold protrusion. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Dimension b does not include dambar protrusion. Dambar cannot be located on the lower radius of the foot.
4. Exact shape of each corner is optional.
5. These dimensions apply to the flat section of the lead between 0.10 and 0.25mm from the lead tip.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.

Notes:
1. Exact shape of each corner is optional.
2. Controlling dimension: mm.

Figure 9. LQFP Physical Package Dimensions

2.2 IA186XL Pin/Signal Descriptions

Descriptions of the pin and signal functions for the IA186XL microcontroller are provided in Table 7.

Several of the IA186XL pins have different functions depending on the operating mode of the device. Each of the different signals supported by a pin is listed and defined in Table 7, indexed alphabetically in the first column of the table. Additionally, the name of the pin associated with the signal as well as the pin numbers for the PLCC, PQFP, and LQFP packages are provided in the "Pin" column. If the signal and pin names are the same, no entry is provided in the "Pin-Name" column. Signals not used in a specific package type are designated "NA."

Table 7. IA186XL Pin/Signal Descriptions

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
a1	pcs5_n/a1	31	48	65	Latched address bit a1
a2	pcs6_n/a2	32	47	64	Latched address bit a2
a16	a16/s3	68	3	21	**a**ddress bits **16**–**19**. Input/Output. These pins provide the four most-significant bits of the Address Bus. • T_1 signals are active High • T_2, T_3, T_w and T_4: Low S6 = CPU-initiated bus or High = DMA-initiated bus or refresh bus cycle. • s3, s4, s5 Low during same T states
a17	a17/s4	67	4	22	
a18	a18/s5	66	5	23	
a19	a19/s6	65	6	24	
ad0	ad0	17	64	1	**a**ddress/**d**ata bits **0**–**15**. Input/Output. These pins provide the multiplexed Address Bus and Data Bus. During the address portion of the IA186XL bus cycle, Address Bits [0–15] are presented on the bus and can be latched using the ale signal (see next table entry). During the data portion of the IA186XL bus cycle, 8- or 16-bit data are present on these lines.
ad1	ad1	15	66	3	
ad2	ad2	13	68	6	
ad3	ad3	11	70	8	
ad4	ad4	8	74	12	
ad5	ad5	6	76	14	
ad6	ad6	4	78	16	
ad7	ad7	2	80	18	
ad8	ad8	16	65	2	
ad9	ad9	14	67	5	
ad10	ad10	12	69	7	
ad11	ad11	10	71	9	
ad12	ad12	7	75	13	
ad13	ad13	5	77	15	
ad14	ad14	3	79	17	
ad15	ad15	1	1	19	

Table 7. IA186XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
ale	ale/qs0	61	10	29	**a**ddress **l**atch **e**nable. Output. Active High. This signal is used to latch the address information during the address portion of a bus cycle.
ardy	ardy	55	20	37	**a**synchronous **r**ea**dy** tells the processor the addressed memory space or i/o device will complete the transfer.
bhe_n	bhe_n	64	7	26	**b**yte **h**igh **e**nable. Output. Active Low. When **bhe_n** is asserted (low), it indicates that the bus cycle in progress is transferring data over the upper half of the data bus. Additionally, **bhe_n** and **ad0** encode the following bus information: ad0 bhe_n Bus Status 0 0 Word Transfer 0 1 Even Byte Transfer 1 0 Odd Byte Transfer 1 1 Refresh Operation Note: **bhe_n** is multiplexed with **refresh_n**.
busy	test_n/busy	47	29	46	**busy**. Input. Active High. When the **busy** input is asserted, it causes the IA186XL to suspend operation during the execution of the Intel 80C187 Numerics Coprocessor instructions. Operation resumes when the pin is sampled low.
clkout	clkout	56	19	36	**cl**oc**k ou**tput. Output. The **clkout** pin provides a timing reference for inputs and outputs of the IA186XL. This clock output is one-half the input clock (**clkin**) frequency. The **clkout** signal has a 50% duty cycle, transitioning every falling edge of **clkin**.
den_n	den_n	39	38	56	**d**ata **en**able. Output. Active Low. This signal is used to enable of bidirectional transceivers in a buffered system. The **den_n** signal is asserted (low) only when data are to be transferred on the bus.
drq0	drq0	18	61	79	**d**ma **r**e**q**uest**0** or **1** is asserted high by an external device when ready for DMA Channel 0 or 1 to perform a transfer. These signals are level-triggered and internally synchronized
drq1	drq1	19	60	78	

Table 7. IA186XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
dt/r_n	dt/r_n	40	37	54	**d**ata **t**ransmit**/r**eceive. Output. This signal is used to control the direction of data flow for bidirectional buffers in a buffered system. When **dt/r_n** is high, the direction indicated is transmit; when **dt/r_n** is low, the direction indicated is receive.
error_n	mcs1_n/error_n	37	40	58	**error**. Input. Active Low. When this signal is asserted (low), it indicates that the last numerics coprocessor operation resulted in an exception condition
hlda	hlda	51	25	42	**h**o**ld a**cknowledge. Output. Active High. When **hlda** is asserted (high), it indicates that the IA186XL has relinquished control of the local bus to another bus master in response to a HOLD request (see next table entry). When **hlda** is asserted, the IA186XL data bus and control signals are floated allowing another bus master to drive the signals directly.
hold	hold	50	26	43	**hold**. Input. Active High. This signal is a request indicating that an external bus master wishes to gain control of the local bus. The IA186XL will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.
int0	int0	45	31	48	**int**errupt N (N = **0**–**4**). Input/Output. Active High. These maskable inputs interrupt program flow and cause execution to continue at an interrupt vector of a specific interrupt type as follows: • **int0**: Type 12 • **int1**: Type 13 • **int2**: Type 14 • **int3**: Type 15 To allow interrupt expansion, **int0** and **int1** can be used with the interrupt acknowledge signals **inta0_n** and **inta1_n** (see next table entries) to serve as external interrupt inputs or interrupt acknowledge outputs.
int1	int1	44	32	49	
int2	int2/inta0_n	42	35	52	
int3	int3/inta1_n	41	36	53	

Table 7. IA186XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
lcs_n	lcs_n	33	46	63	**l**ower **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.
lock_n	lock_n	48	28	45	**lock**. Output. Active Low. When asserted (low), this signal indicates that the bus cycle in progress is cannot be interrupted. While **lock_n** is active, the IA186XL will not service bus requests such as HOLD. When **resin_n** is active, this pin is weakly held high and must not be driven low.
mcs0_n	mcs0_n/pereq	38	39	57	**m**id-range memory **c**hip **s**elect.
mcs1_n	mcs1_n/error_n	37	40	58	
mcs2_n	mcs2_n	36	41	59	
mcs3_n	mcs3_n/nps_n	35	42	60	
n.c.	n.c.	NA	2, 11, 14, 15, 24, 43, 44, 62, 63	4, 25, 35, 55, 72	**n**ot **c**onnected.
nmi	nmi	46	30	47	**n**on-**m**askable **i**nterrupt. Input. Active High. When the **nmi** signal is asserted (high) it causes a Type 2 interrupt.
nps_n	mcs3_n/nps_n	35	42	60	**n**umeric **p**rocessor **s**elect
pcs0_n	pcs0_n	25	54	71	**p**eripheral **c**hip **s**elect signals **0**–**6**.
pcs1_n	pcs1_n	27	52	69	
pcs2_n	pcs2_n	28	51	68	
pcs3_n	pcs3_n	29	50	67	
pcs4_n	pcs4_n	30	49	66	
pcs5_n	pcs5_n/a1	31	48	65	
pcs6_n	pcs6_n/a2	32	47	64	
pereq	mcs0_n/pereq	38	39	57	numerics co**p**rocessor **e**xternal **req**uest. Input. Active High. When asserted (high), this signal indicates that a data transfer between an Intel 80C187 Numerics Coprocessor and memory is pending.
qs0	ale/qs0	61	10	29	**q**ueue **s**tatus **0**, **q**ueue **s**tatus **1**
qs1	wr_n/qs1	63	8	27	
qsmd_n	rd_n/qsmd_n	62	9	28	**q**ueue **s**tatus **mod**e

Table 7. IA186XL Pin/Signal Descriptions *(Continued)*

Signal	Pin Name	Pin PLCC	Pin PQFP	Pin LQFP	Description
rd_n	rd_n/qsmd_n	62	9	28	**rea**d. output. Active Low. When asserted (low), **rd_n** indicates that the accessed memory or I/O device must drive data from the location being accessed onto the data bus.
res_n	res_n	24	55	73	**res_n** causes the processor to immediately terminate its present activity, clear the internal logic, and enter a dormant state.
reset	reset	57	18	34	**reset** is an output signal indicating the CPU is being reset and can be used as a system rest.
s0_n	s0_n	52	23	40	**s**tatus [**2**:**0**]_**n** are outputs. During a bus cycle, the status (i.e., type) of cycle is encoded on these lines as follows: **s2_n** **s1_n** **s0_n** Bus Cycle Status 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Processor HALT 1 0 0 Queue Instruction Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 No Bus Activity
s1_n	s1_n	53	22	39	
s2_n	s2_n	54	21	38	
s3	a16/s3	68	3	21	**s**tatus [**6**:**3]** are Inputs/Outputs. Bus Cycle A19/s6 A18/s5 A17/s4 A16/s3 T_1 A19 A18 A17 A16 T_2 N 0 0 0 T_3 N 0 0 0 T_w N 0 0 0 T_4 N 0 0 0 N = 0 for CPU bus cycle. N = 1 for DMA or refresh cycle.
s4	a17/s4	67	4	22	
s5	a18/s5	66	5	23	
s6	a19/s6	65	6	24	
srdy	srdy	49	27	44	**s**ynchronous **rea**d**y**
test_n	test_n/busy	47	29	46	**test**. Input. Active Low. When the **test_n** input is high (i.e., not asserted), it causes the IA186XL to suspend operation during the execution of the WAIT instruction. Operation resumes when the pin is sampled low (asserted).
tmr in 0	tmr in 0	20	59	77	**tim**e**r 0 in**put. Input. Depending on the Timer Mode programmed for Timer 0, this input is used either as clock input or a control signal.

Table 7. IA186XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
tmr in 1	tmr in 1	21	58	76	**t**imer **1 in**put. Input. Depending on the Timer Mode programmed for Timer 1, this input is used either as clock input or a control signal.
tmr out 0	tmr out 0	22	57	75	**tim**e**r 0 out**put. Output. Depending on the Timer Mode programmed for Timer 0, this output can provide a single clock or a continuous waveform.
tmr out 1	tmr out 1	23	56	74	**t**imer **1 out**put. Output. Depending on the Timer Mode programmed for Timer 1, this output can provide a single clock or a continuous waveform.
ucs_n	ucs_n	34	45	62	**u**pper **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.
v_{cc}	v_{cc}	9, 43	33, 34, 72, 73	10, 11, 20, 50, 51, 61	Power (**V_{CC}**). This pin provides power for the IA186XL device. It must be connected to a +5V DC power source.
v_{ss}	v_{ss}	26, 60	12, 13, 53	30, 31, 41, 70, 80	Ground (**V_{SS}**). This pin provides the digital ground (0V) for the IA186XL. It must be connected to a V_{SS} board plane.
wr_n	wr_n/qs1	63	8	27	**wr**ite. Output. Active Low. When asserted (low), **wr_n** indicates that data available on the data bus are to be latched into the accessed memory or I/O device.
x1	x1	59	16	32	**x1** and **x2** are inputs for the crystal
x2	x2	58	17	33	

2.3 IA188XL Pin/Signal Descriptions

Descriptions of the pin and signal functions for the IA188XL microcontroller are provided in Table 8.

Several of the IA188XL pins have different functions depending on the operating mode of the device. Each of the different signals supported by a pin is listed and defined in Table 8, indexed alphabetically in the first column of the table. Additionally, the name of the pin associated with the signal as well as the pin numbers for the PLCC, QFP, and LQFP packages are provided in the "Pin" column. If the signal and pin names are the same, no entry is provided in the "Pin-Name" column.

Table 8. IA188XL Pin/Signal Descriptions

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
a1	pcs5_n/a1	31	48	65	Latched address bit **a1**
a2	pcs6_n/a2	32	47	64	Latched address bit **a2**
a16	a16/s3	68	3	21	**a**ddress bits **16**–**19**. Input/Output. These pins provide the four most-significant bits of the Address Bus. • T_1 signals are active High • T_2, T_3, T_w and T_4: Low S6 = CPU-initiated bus or High = DMA- initiated bus or refresh bus cycle. • s3, s4, s5 Low during same T states
a17	a17/s4	67	4	22	
a18	a18/s5	66	5	23	
a19	a19/s6	65	6	24	
ad0	ad0	17	64	1	**a**ddress/**d**ata bits **015**. Input/Output. These pins provide the multiplexed Address Bus and Data Bus. During the address portion of the IA186XL bus cycle, address bits 0 through 15 are presented on the bus and can be latched using the ale signal (see next table entry). During the data portion of the IA186XL bus cycle, 8- or 16-bit data are present on these lines.
ad1	ad1	15	66	3	
ad2	ad2	13	68	6	
ad3	ad3	11	70	8	
ad4	ad4	8	74	12	
ad5	ad5	6	76	14	
ad6	ad6	4	78	16	
ad7	ad7	2	80	18	
a8	a8	16	65	2	valid address information is provided for the entire bus cycle
a9	a9	14	67	5	
a10	a10	12	69	7	
a11	a11	10	71	9	
a12	a12	7	75	13	
a13	a13	5	77	15	
a14	a14	3	79	17	
a15	a15	1	1	19	

Table 8. IA188XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
ale	ale/qs0	61	10	29	**a**ddress **l**atch **e**nable. Output. Active High. This signal is used to latch the address information during the address portion of a bus cycle.
ardy	ardy	55	20	37	**a**synchronous **r**ea**dy** tells the processor the addressed memory space or i/o device will complete the transfer.
rfsh_n	rfsh_n	64	7	26	**rfsh_n** is asserted low to indicate a refresh bus cycle
busy	test_n/busy	47	29	46	**busy**. Input. Active High. When the **busy** input is asserted, it causes the IA186XL to suspend operation during the execution of the Intel 80C187 Numerics Coprocessor instructions. Operation resumes when the pin is sampled low.
clkout	clkout	56	19	36	**cl**oc**k ou**tput. Output. The **clkout** pin provides a timing reference for inputs and outputs of the IA186XL. This clock output is one-half the input clock (**clkin**) frequency. The **clkout** signal has a 50% duty cycle, transitioning every falling edge of **clkin**.
den_n	den_n	39	38	56	**d**ata **en**able. Output. Active Low. This signal is used to enable of bidirectional transceivers in a buffered system. The **den_n** signal is asserted (low) only when data are to be transferred on the bus.
drq0	drq0	18	61	79	**d**ma **r**e**q**uest**0** or **1** is asserted high by an external device when ready for DMA Channel 0 or 1 to perform a transfer. These signals are level-triggered and internally synchronized
drq1	drq1	19	60	78	
dt/r_n	dt/r_n	40	37	54	**d**ata **t**ransmit**/r**eceive. Output. This signal is used to control the direction of data flow for bidirectional buffers in a buffered system. When **dt/r_n** is high, the direction indicated is transmit; when **dt/r_n** is low, the direction indicated is receive.
error_n	mcs1_n/error_n	37	40	58	**error**. Input. Active Low. When this signal is asserted (low), it indicates that the last numerics coprocessor operation resulted in an exception condition

Table 8. IA188XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
hlda	hlda	51	25	42	**h**o**ld a**cknowledge. Output. Active High. When **hlda** is asserted (high), it indicates that the IA186XL has relinquished control of the local bus to another bus master in response to a HOLD request (see next table entry). When **hlda** is asserted, the IA186XL data bus and control signals are floated allowing another bus master to drive the signals directly.
hold	hold	50	26	43	**hold**. Input. Active High. This signal is a request indicating that an external bus master wishes to gain control of the local bus. The IA186XL will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.
int0	int0	45	31	48	**int**errupt N (N = **04**). Input/Output. Active High. These maskable inputs interrupt program flow and cause execution to continue at an interrupt vector of a specific interrupt type as follows: • **int0**: Type 12 • **int1**: Type 13 • **int2**: Type 14 • **int3**: Type 15 To allow interrupt expansion, **int0** and **int1** can be used with the interrupt acknowledge signals **inta0_n** and **inta1_n** (see next table entries) to serve as external interrupt inputs or interrupt acknowledge outputs.
int1	int1	44	32	49	
int2	int2/inta0_n	42	35	52	
int3	int3/inta1_n	41	36	53	
lcs_n	lcs_n	33	46	63	**l**ower **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.

Table 8. IA188XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
lock_n	lock_n	48	28	45	**lock**. Output. Active Low. When asserted (low), this signal indicates that the bus cycle in progress is cannot be interrupted. While **lock_n** is active, the IA186XL will not service bus requests such as HOLD. When **resin_n** is active, this pin is weakly held high and must not be driven low.
mcs0_n	mcs0_n/pereq	38	39	57	**m**id-range memory **c**hip **s**elect
mcs1_n	mcs1_n/error_n	37	40	58	
mcs2_n	mcs2_n	36	41	59	
mcs3_n	mcs3_n/nps_n	35	42	60	
n.c.	n.c.	NA	2, 11, 14, 15, 24, 43, 44, 62, 63	4, 25, 35, 55, 72	**n**ot **c**onnected
nmi	nmi	46	30	47	**n**on-**m**askable **i**nterrupt. Input. Active High. When the **nmi** signal is asserted (high) it causes a Type 2 interrupt .
nps_n	mcs3_n/nps_n	35	42	60	**n**umeric **p**rocessor **s**elect
pcs0_n	pcs0_n	25	54	71	**p**eripheral **c**hip **s**elect signals **0**–**6**
pcs1_n	pcs1_n	27	52	69	
pcs2_n	pcs2_n	28	51	68	
pcs3_n	pcs3_n	29	50	67	
pcs4_n	pcs4_n	30	49	66	
pcs5_n	pcs5_n/a1	31	48	65	
pcs6_n	pcs6_n/a2	32	47	64	
pereq	mcs0_n/pereq	38	39	57	numerics co**p**rocessor **e**xternal **req**uest. Input. Active High. When asserted (high), this signal indicates that a data transfer between an Intel 80C187 Numerics Coprocessor.and memory is pending.
qs0	ale/qs0	61	10	29	**q**ueue **s**tatus **0**, **q**ueue **s**tatus **1**
qs1	wr_n/qs1	63	8	27	
qsmd_n	rd_n/qsmd_n	62	9	28	**q**ueue **s**tatus **mo**d**e**
rd_n	rd_n/qsmd_n	62	9	28	**r**ea**d**. output. Active Low. When asserted (low), **rd_n** indicates that the accessed memory or I/O device must drive data from the location being accessed onto the data bus.
res_n	res_n	24	55	73	**res_n** causes the processor to immediately terminate its present activity, clear the internal logic, and enter a dormant state.

Table 8. IA188XL Pin/Signal Descriptions *(Continued)*

Signal	Pin Name	PLCC	PQFP	LQFP	Description
reset	reset	57	18	34	**reset** is an output signal indicating the CPU is being reset and can be used as a system rest
s0_n	s0_n	52	23	40	**s**tatus [**2**:**0**]_**n** are outputs. During a bus cycle the status (i.e., type) of cycle is encoded on these lines as follows: **s2_n s1_n s0_n** Bus Cycle Status 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Processor HALT 1 0 0 Queue Instruction Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 No Bus Activity
s1_n	s1_n	53	22	39	
s2_n	s2_n	54	21	38	
s3	a16/s3	68	3	21	**s**tatus [**6**:**3**] are inputs/outputs. Bus Cycle A19/s6 A18/s5 A17/s4 A16/s3 T_1 A19 A18 A17 A16 T_2 N 0 0 0 T_3 N 0 0 0 T_w N 0 0 0 T_4 N 0 0 0 N = 0 for CPU bus cycle. N = 1 for DMA or refresh cycle.
s4	a17/s4	67	4	22	
s5	a18/s5	66	5	23	
s6	a19/s6	65	6	24	
srdy	srdy	49	27	44	**s**ynchronous **rea**d**y**
test_n	test_n/busy	47	29	46	**test**. Input. Active Low. When the **test_n** input is high (i.e., not asserted), it causes the IA186XL to suspend operation during the execution of the WAIT instruction. Operation resumes when the pin is sampled low (asserted).
tmr in 0	tmr in 0	20	59	77	**timer 0 in**put. Input. Depending on the Timer Mode programmed for Timer 0, this input is used either as clock input or a control signal.
tmr in 1	tmr in 1	21	58	76	**timer 1 in**put. Input. Depending on the Timer Mode programmed for Timer 1, this input is used either as clock input or a control signal.
tmr out 0	tmr out 0	22	57	75	**timer 0 out**put. Output. Depending on the Timer Mode programmed for Timer 0, this output can provide a single clock or a continuous waveform.

Table 8. IA188XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
tmr out 1	tmr out 1	23	56	74	**tim**e**r 1 out**put. Output. Depending on the Timer Mode programmed for Timer 1, this output can provide a single clock or a continuous waveform.
ucs_n	ucs_n	34	45	62	**u**pper **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.
v_{cc}	v_{cc}	9, 43	33, 34, 72, 73	10, 11, 20, 50, 51, 61	Power ($\mathbf{V_{CC}}$). This pin provides power for the IA186XL device. It must be connected to a +5V DC power source.
v_{ss}	v_{ss}	26, 60	12, 13, 53	30, 31, 41, 70, 80	Ground ($\mathbf{V_{SS}}$). This pin provides the digital ground (0V) for the IA186XL. It must be connected to a V_{SS} board plane.
wr_n	wr_n/qs1	63	8	27	**wr**ite. Output. Active Low. When asserted (low), **wr_n** indicates that data available on the data bus are to be latched into the accessed memory or I/O device.
x1	x1	59	16	32	**x1** and **x2** are inputs for the crystal
x2	x2	58	17	33	

3. Maximum Ratings, Thermal Characteristics, and DC Parameters

For the Innovasic Semiconductor IA186XL and IA188XL microcontrollers, the absolute maximum ratings, thermal characteristics, and DC parameters are provided in Tables 9 through 11, respectively.

Table 9. IA186XL and IA188XL Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65°C to +150°C
Case Temperature under Bias	−65°C to +120°C
Supply Voltage with Respect to v_{ss}	−0.5V to +6.5V
Voltage on Pins other than Supply with Respect to v_{ss}	−0.5V to +(Vcc + 0.5)V

Table 10. IA186XL and IA188XL Thermal Characteristics

Symbol	Characteristic	Value	Units
T_A	Ambient Temperature	-40°C to 85°C	°C
P_D	Power Dissipation	MHz × ICC × V/1000	W
Θ_{Ja}	68-Lead PLCC Package	32	°C/W
	80-Lead PQFP Package	46	
	80-Lead LQFP Package	52	
T_J	Average Junction Temperature	$T_A + (P_D \times \Theta_{Ja})$	°C

Table 11. IA186XL and IA188XL DC Parameters

Symbol	Parameter	Min	Max	Units	Notes
5.0 Volt Operation V_{CC}	Supply Voltage	4.5	5.5	V	–
V_{IL}	Input Low Voltage	−0.5	0.8	V	Does not include x1 or res_n
V_{IL1}	Clock input low voltage (x1 + res_n)	−0.5	0.6	V	–
V_{IH}	Input High Voltage (x1 + res_n)	2.0	V_{CC} + 0.5	V	Does not include x1 or res_n
V_{IH1}	Input High Voltage	3.9	V_{CC} + 0.5	V	–
V_{OL}	Output Low Voltage	–	0.45	V	I_{OL} = 2.5 mA (SO, 1, 2) I_{OL} = 2.0 mA (others)
V_{OH}	Output High Voltage	2.4	V_{CC}	V	I_{OH} = −2.4 mA @ 2.4V[a]
		V_{CC} −0.5	V_{CC}	V	I_{OH} = 200 µA @ V_{CC} −0.5[a]
I_{LI}	Input Leakage Current	–	± 10	µA	@ 0.5 MHz, 0.45V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Input Leakage Current for Pins	–	± 10	µA	@ 0.5 MHz, 0.45V ≤ V_{OUT} ≤ V_{CC} floating at Hold or by invoking ONCE mode
I_{CC}	Power Supply Current	–	5	mA/MHz	V_{CC} = 5.5V[b]
		–	100	µA	@ DC, 0°C V_{CC} = 5.5V
C_{IN}	Input Pin Capacitance	0	10	pF	T_F = 1 MHz[c]
C_{OUT}	Output Pin Capacitance	0	20	pF	T_F = 1 MHz[c]
V_{CHO}	Clock Output High	V_{CC} −0.5	–	V	I_{CHO} = −500 µA
Operating temperature is −40°C to 85°C, V_{CC} = 5V ± 10%.					

[a]The following pins: lcs_n, mcs0_n/pereq, mcs1_n/error_n, rd_n/qsmd_n, test_n/busy, and ucs_n have internal pullup devices. Loading pins above I_{OH} = −200 µA can result in unpredictable operation. See Chapter 6, Reset Operation, and Chapter 7, Bus Timing.

[b]Power supply current is determined with the device in reset with pins x1 and x2 driven and other non-power pins open.

[c]Characterization conditions are (1) frequency = 1 MHz, (2) unmeasured pins at GND, and (3) V_{IN} at + 5.0V or 0.45V. This parameter is not tested.

4. Functional Description

4.1 Device Architecture

Architecturally, the IA186XL and IA188XL microcontrollers include the following functional modules:

- Bus Interface Unit
- Clock Generator
- Interrupt Control Unit
- Timer/Counter Unit
- Chip-Select Unit
- Refresh Control Unit
- Power-Save Control
- DMA Unit

A functional block diagram of the IA186XL/IA188XL is shown in Figure 10. Descriptions of the functional modules are provided in the following subsections.

4.1.1 Bus Interface Unit

A local bus controller generates the local bus control signals. It also employs a hold/hlda protocol for relinquishing the local bus to other bus masters. Its outputs can be used to enable external buffers and to direct the flow of data on and off the local bus. The bus controller is responsible for generating 20 bits of address, read and write strobes, bus-cycle status information and data. This controller is also responsible for reading data from the local bus during a read operation. Synchronous and asynchronous ready input pins are provided to extend a bus cycle beyond the minimum four clocks. The bus controller also generates two control signals (den_n and dt/r_n) when interfacing to external transceiver chips. This capability allows the addition of transceivers for simple buffering of the multiplexed address/data bus. During reset, the local bus controller performs the following actions:

1. Drives den_n, rd_n, and wr_n HIGH for one clock cycle, then floats them
2. Drives s0_n ±s2_n to the inactive state (all HIGH) and then floats
3. Drives lock_n HIGH and then floats
4. Floats ad0–15 (ad0–8), a16–19 (a9–a19), bhe_n (rfsh_n), dt/r_n
5. Drives ale LOW
6. Drives hlda LOW

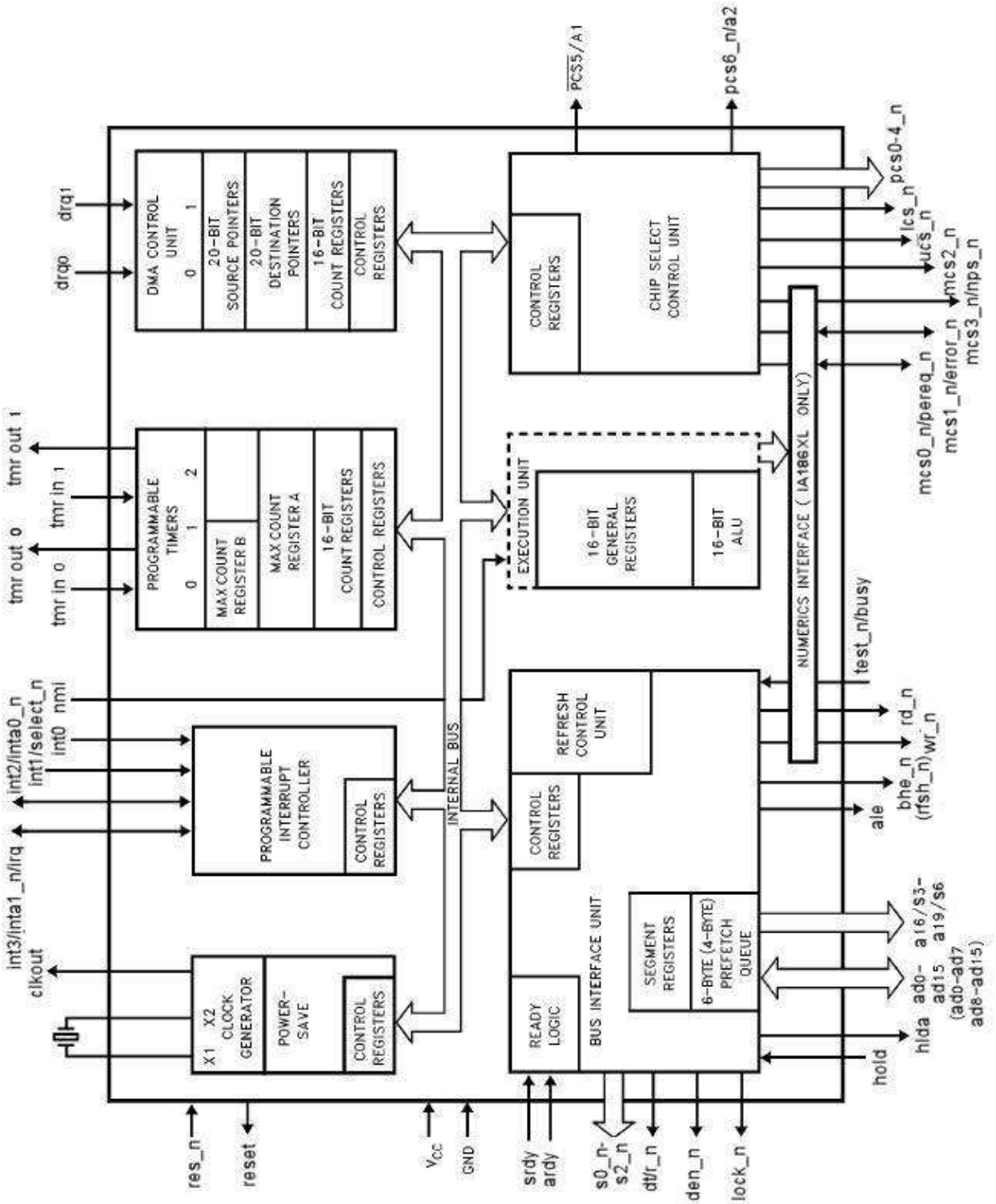


Figure 10. IA186XL/IA188XL Functional Block Diagram

The rd_n/qsmd_n, ucs_n, lcs_n, mcs0_n/pereq, mcs1_n/error_n, and test_n/busy pins include internal pull-up devices that are active while res_n is applied. Excessive loading or grounding of these pins causes the IA186XL to enter an alternative mode of operation resulting in the following:

1. rd_n/qsmd_n low results in Queue Status Mode
2. ucs_n and lcs_n low results in ONCE Mode
3. test_n/busy low (and high later) results in Enhanced Mode.

4.1.2 Clock Generator

The IA186XL/IA188XL uses an on-chip clock generator to supply internal and external clocks. The clock generator makes use of a crystal oscillator and includes a divide-by-two counter.

Figure 11 shows the various operating modes of the clock circuit. The clock circuit can use either a parallel resonant fundamental mode crystal network (A) or a third-overtone mode crystal network (B), or it can be driven by an external clock source (C).

The following parameters are recommended when choosing a crystal:
Temperature Range:

- Application Specific
- ESR (Equivalent Series Resistance): 60Ω max
- C0 (Shunt Capacitance of Crystal): 7.0 pF max
- CL (Load Capacitance): 20 pF ± 2 pF
- Drive Level: 2 mW max

4.1.3 Interrupt Control Unit

The IA186XL receives interrupts from a number of sources, both internal and external. It has 5 external and 2 internal interrupt sources (Timer/Counters and DMA). The internal interrupt controller merges these requests on a priority basis for individual service by the CPU.

4.1.4 Timer/Counter Unit

The IA186XL/IA188XL Timer/Counter Unit (TCU) provides three 16-bit programmable timers.wo of these are highly flexible and are connected to external pins for control or clocking. A third timer is not connected to any external pins and can only be clocked internally. However, it can be used to clock the other two timer channels. The TCU can be used to count external events, time external events, generate non-repetitive waveforms, generate timed interrupts, etc.

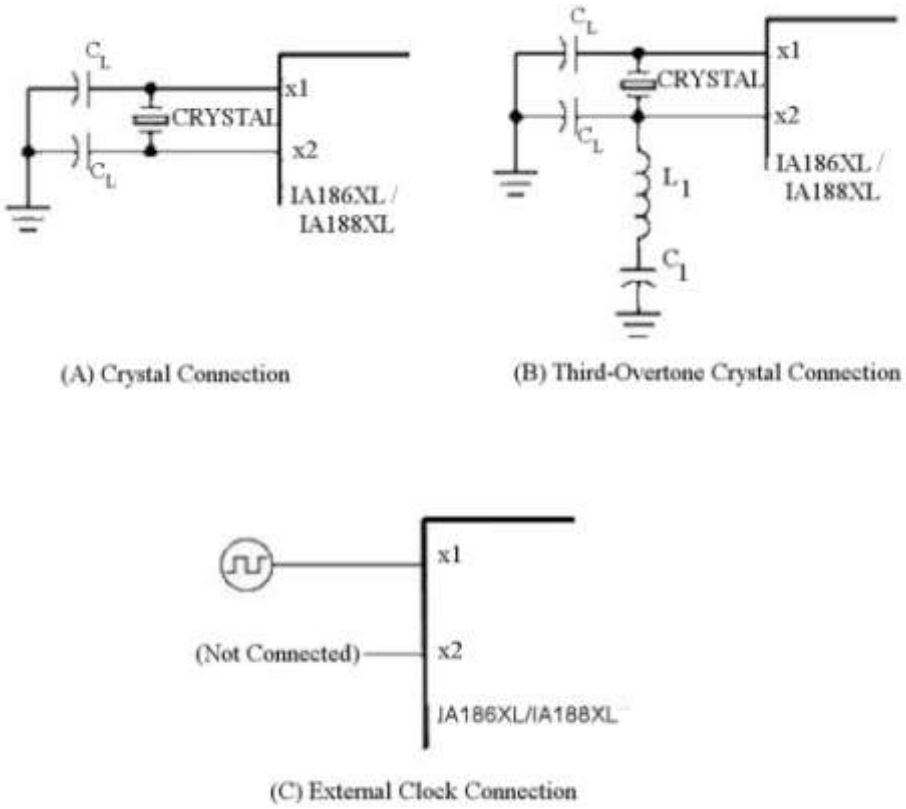


Figure 11. Clock Circuit Connection Options

4.1.5 Chip-Select/Ready Generation Logic

The IA186XL provides programmable chip-select generation for both memories and peripherals. The chip can be programmed to provide READY or WAIT state generation. It can also provide latched address bits A1 and A2. The select lines are active for all memory and I/O cycles in their programmed areas whether signals are generated by the CPU or by the DMA unit. The IA186XL provides six memory chip select outputs for three address areas; upper memory, lower memory, and midrange memory. One signal is provided for upper memory, one for lower memory and four for midrange memory (see Figure 12).

The IA186XL provides a chip select, called UCS, for upper memory. Upper memory is usually used for system memory because the IA186XL begins executing at memory location FFFF0H after reset. The IA186XL provides a chip select for low memory called LCS. Low memory contains the interrupt vector table starting at location 00000H. For midrange memory, the IA186XL provides four MCS lines that are active within a user-locatable memory block. This block can be located within 1 Mbyte of memory address space exclusive of the areas defined by UCS and LCS. Both the base address and size of this memory block are programmable.

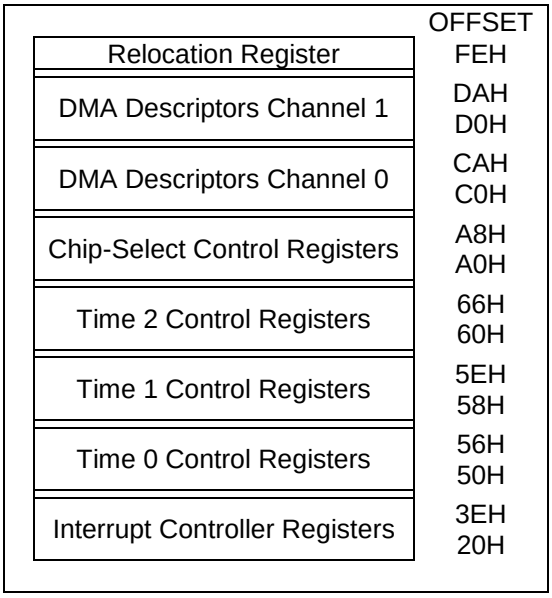


Figure 12. Internal Register Map

The IA186XL can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. The base address may be located in either memory or I/O space. The IA186XL can generate a READY signal internally for each of the memory or peripheral CS lines. The number of WAIT states to be inserted for each peripheral or memory is programmable to provide 0±3 wait states for all accesses to the area for which the chip select is active. In addition, the IA186XL may be programmed to ignore either external READY for each chip-select range individually or to factor external READY with the integrated ready generator. At reset, the Chip-Select/Ready Logic will perform the following actions:

1. All chip-select outputs will be driven HIGH
2. Upon leaving RESET, the UCS line will be programmed to provide chip selects to a 1-Kbyte block with the accompanying READY control bits set at 011 to insert 3 wait states in conjunction with external READY (i.e., UMCS resets to FFFBH)
3. No other chip select or READY control registers have any predefined values after RESET. They will not become active until the CPU accesses their control registers.

4.1.6 DRAM Refresh Control Unit

The Refresh Control Unit (RCU) automatically generates DRAM refresh bus cycles. The RCU operates only in Enhanced Mode. After a programmable period of time, the RCU generates a memory read request to the BIU. If the address generated during a refresh bus cycle is within the

range of a properly programmed chip select, that chip select will be activated when the BIU executes the refresh bus cycle.

4.1.7 Power-Save Control

When operating in Enhanced Mode, the IA186XL can enter a power-saving state by internally dividing the processor clock frequency by a programmable factor. This divided frequency is also available at the CLKOUT pin. All internal logic have their clocks slowed down by the division factor including the Refresh Control Unit and the timers. To maintain a real time count or a fixed DRAM refresh rate, these peripherals must be re-programmed when entering and leaving the power-save mode.

4.2 Peripheral Architecture

All IA186XL integrated peripherals are controlled by 16-bit registers contained within an internal control block of 256 bytes. The control block may be mapped into either memory or I/O space. Internal logic will recognize control block addresses and respond to bus cycles. An offset map of the 256-byte control register block is shown in Table 12, Internal Register Map.

4.3 Reference Documents

Additional information on the operation and programming of the 80C186XL/80C188XL can be found in the following Intel publications:

- 80C186XL/80C188XL and 80L186XL/80L188XL 16-Bit High-Integration Embedded Processors (272433-006)
- 80C186XL/80C188XL Microprocessor User's Manual (270830-00n)

Table 12. Internal Register Map

PCB Offset	Function	PCB Offset	Function	PCB Offset	Function	PCB Offset	Function
00H	Reserved	40H	Reserved	80H	Reserved	C0H	D0SRCL
02H	Reserved	42H	Reserved	82H	Reserved	C2H	D0SRCH
04H	Reserved	44H	Reserved	84H	Reserved	C4H	D0DSTL
06H	Reserved	46H	Reserved	86H	Reserved	C6H	D0DSTH
08H	Reserved	48H	Reserved	88H	Reserved	C8H	D0TC
0AH	Reserved	4AH	Reserved	8AH	Reserved	CAH	D0CON
0CH	Reserved	4CH	Reserved	8CH	Reserved	CCH	Reserved
0EH	Reserved	4EH	Reserved	8EH	Reserved	CEH	Reserved
10H	Reserved	50H	T0CNT	90H	Reserved	D0H	D1SRCL
12H	Reserved	52H	T0CMPA	92H	Reserved	D2H	D1SRCH
14H	Reserved	54H	T0CMPB	94H	Reserved	D4H	D1DSTL
16H	Reserved	56H	T0CON	96H	Reserved	D6H	D1DSTH
18H	Reserved	58H	T1CNT	98H	Reserved	D8H	D1TC
1AH	Reserved	5AH	T1CMPA	9AH	Reserved	DAH	D1CON
1CH	Reserved	5CH	T1CMPB	9CH	Reserved	DCH	Reserved
1EH	Reserved	5EH	T1CON	9EH	Reserved	DEH	Reserved
20H	Reserved	60H	T2CNT	A0H	UMCS	E0H	RFBASE
22H	EOI	62H	T2CMPA	A2H	LMCS	E2H	RFTIME
24H	POLL	64H	Reserved	A4H	PACS	E4H	RFCON
26H	POLLSTS	66H	T2CON	A6H	MMCS	E6H	Reserved
28H	IMASK	68H	Reserved	A8H	MPCS	E8H	Reserved
2AH	PRIMSK	6AH	Reserved	AAH	Reserved	EAH	Reserved
2CH	INSERV	6CH	Reserved	ACH	Reserved	ECH	Reserved
2EH	REQST	6EH	Reserved	AEH	Reserved	EEH	Reserved
30H	INSTS	70H	Reserved	B0H	Reserved	F0H	PWRSAV
32H	TCUCON	72H	Reserved	B2H	Reserved	F2H	PWRCON
34H	DMA0CON	74H	Reserved	B4H	Reserved	F4H	Reserved
36H	DMA1CON	76H	Reserved	B6H	Reserved	F6H	STEPID
38H	I0CON	78H	Reserved	B8H	Reserved	F8H	Reserved
3AH	I1CON	7AH	Reserved	BAH	Reserved	FAH	Reserved
3CH	I2CON	7CH	Reserved	BCH	Reserved	FCH	Reserved
3EH	I3CON	7EH	Reserved	BEH	Reserved	FEH	RELREG

5. AC Specifications

This chapter defines the AC specifications of the IA186XL/IA188XL. Input characteristics are provided in Figure 13 and Table 13. Output characteristics are provided in Figure 14 and Table 14. Relative timing characteristics are provided in Figure 15 and Table 15. Clock input and clock output timing characteristics are provided in Figure 19 and Table 16. Additional timing information is provided in Chapter 7, Bus Timing, and Chapter 8, Instruction Execution Times.

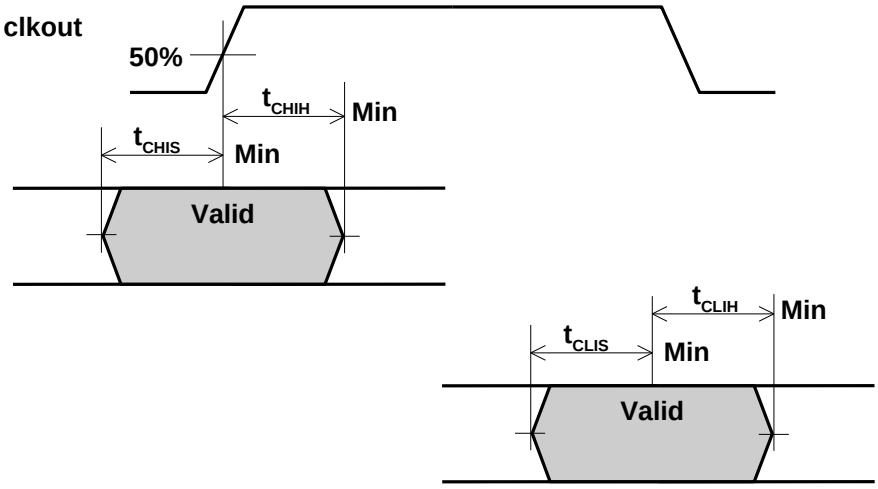


Figure 13. AC Input Characteristics

For specific 5.0-volt characteristics, refer to Table 13.

Table 13. AC Input Characteristics for 5.0-Volt Operation

Symbol	Pins	Min	Max	Units
t_{CHIS}	test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n, p2.6, p2.7	10	–	ns
t_{CHIH}	test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n	3	–	ns
t_{CLIS}	ad15–ad0, ad7–ad0 (IA188XL), ready	10	–	ns
t_{CLIS}	hold, pereq, error_n	10	–	ns
t_{CLIH}	ad15–ad0, ad7–ad0 (IA188XL), ready	3	–	ns
t_{CLIH}	hold, pereq, error_n	3	–	ns

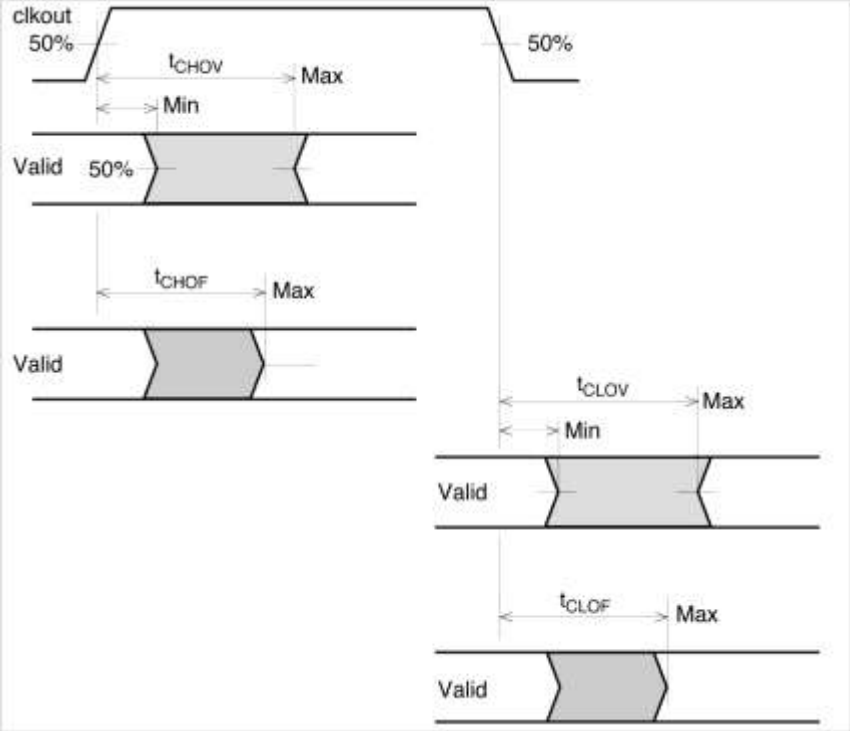


Figure 14. AC Output Characteristics

For specific 5.0-volt characteristics, refer to Table 14.

Table 14. AC Output Characteristics for 5.0-Volt Operation

Symbol	Parameter	Min	Max	Units
t_{CHOV}	ale, s2–s0_n, den_n, dt/r_n, bhe_n, rfsh_n (IA188XL), lock_n, a19–a16	3	17	ns
	pcs6_n–pcs0_n, mcs3_n–mcs0_n, lcs_n, ucs_n, ncs_n, rd_n, wr_n	3	20	ns
t_{CLOV}	bhe_n, rfsh_n (IA188XL), den_n, lock_n, resout, hlda, t0out, t1out, a19–a16	3	17	ns
	rd_n , wr_n, pcs6_n–pcs0_n, mcs3_n–mcs0_n, lcs_n, ucs_n, ad15–ad0, ad7–ad0 (IA188XL), a15–a8 (IA188XL), ncs_n, inta1_n–inta0_n, s2_n–s0_n	3	20	ns
t_{CHOF}	re_n, wr_n, bhe_n, rfsh_n (IA188XL), dt/r_n, lock_n, s2_n–s0_n, a19–a16	0	20	ns
t_{CLOF}	den_n, ad15–ad0, ad7–ad0 (IA188XL), a15–a8 (IA188XL)	0	20	ns

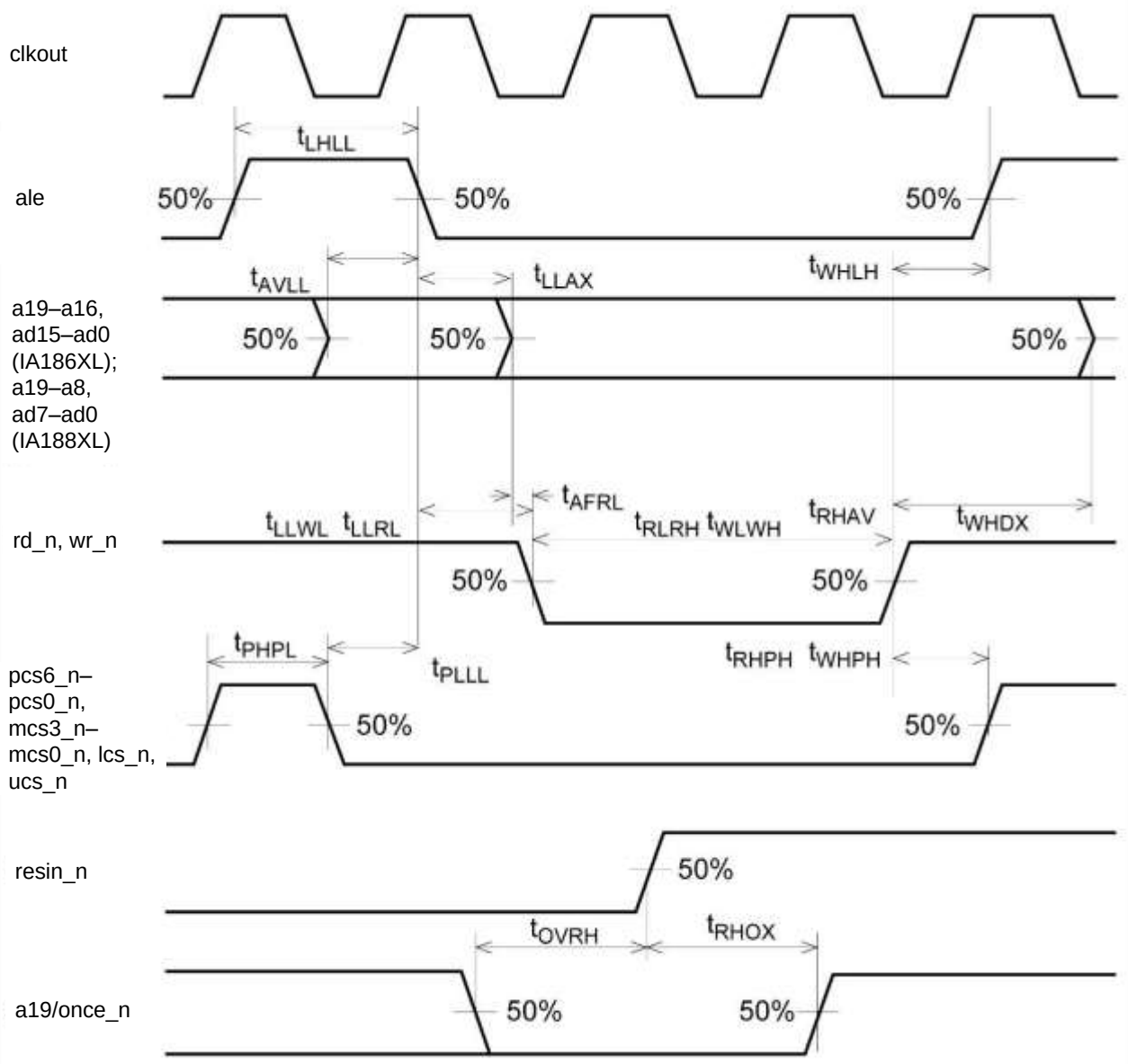


Figure 15. Relative Timing Characteristics

For specific relative timing characteristics, refer to Table 15.

Table 15. Relative Timing Characteristics

Symbol	Parameter	Min	Max	Units
t_{LHLL}	ale Rising to ale Falling	t – 15	–	ns
t_{AVLL}	Address Valid to ale Falling	½t –10	–	ns
t_{PLLL}	Chip Selects Valid to ale Falling	½t –10	–	ns
t_{LLAX}	Address Hold from ale Falling	½t –10	–	ns
t_{LLWL}	ale Falling to wr_n Falling	½t –15	–	ns
t_{LLRL}	ale Falling to rd_n Falling	½t –15	–	ns
t_{WHLH}	wr_n Rising to ale Rising	½t –10	–	ns
t_{AFRL}	Address Float to rd_n Falling	0	–	ns
t_{RLRH}	rd_n Falling to rd_n Rising	(2t) – 5	–	ns
t_{WLWH}	wr_n Falling to wr_n Rising	(2t) – 5	–	ns
t_{RHAV}	rd_n Rising to Address Active	t – 15	–	ns
t_{WHDX}	Output Data Hold after wr_n Rising	t – 15	–	ns
t_{WHPH}	wr_n Rising to Chip Select Rising	½t –10	–	ns
t_{RHPH}	rd_n Rising to Chip Select Rising	½t –10	–	ns
t_{PHPL}	cs_n inactive to cs_n active	½t –10	–	ns
t_{OVRH}	once_n Active to resin_n Rising	t	–	ns
t_{RHOX}	once_n Hold to resin_n Rising	t	–	Ns

5.1 AC Test Conditions

The AC specifications are tested with the 50-pF load shown in Figure 16. Specifications are measured at the $V_{CC}/2$ crossing point unless otherwise specified. The derating curves of Figures 17 and 18 show how timings vary with load capacitance.

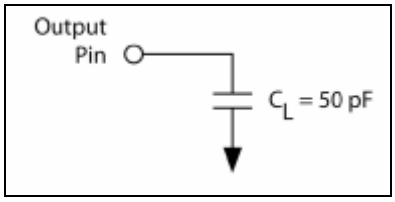


Figure 16. AC Test Load

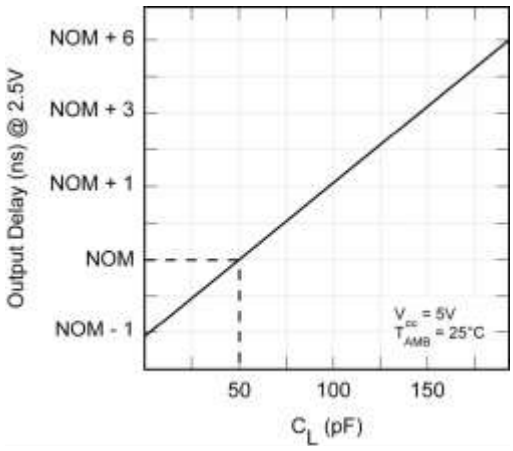


Figure 17. Typical Output Delay Variations Versus Load Capacitance

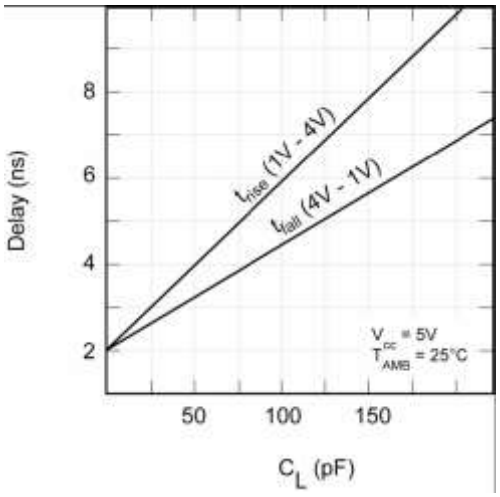


Figure 18. Typical Rise and Fall Variations Versus Load Capacitance

5.2 Clock Input and Clock Output Timing Characteristics

For clock input and clock output timing characteristics for 5.0-volt operation, see Table 16.

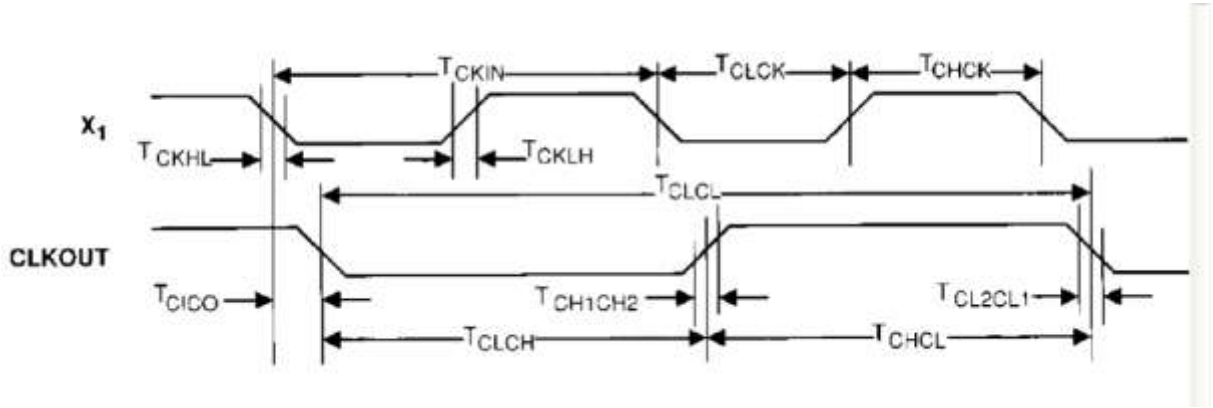


Figure 19. Clock Input and Clock Output Timing Characteristics

Table 16. Clock Input and Clock Output Timing Characteristics for 5.0-Volt Operation

Item	Symbol	Parameter	Min	Max	Units	Notes
–	XTF	clkin Frequency	0	66.67	MHZ	–
1	TCKIN	clkin Period	15	∞	ns	–
2	TCHCK	clkin High Time	6.5	∞	ns	Measure for VIH for high time, NIL for low time.
3	TCLCK	clkin Low Time	6.5	∞	ns	Measure for VIH for high time, NIL for low time.
4	TCKLH	clkin Rise Time	1	5	ns	Only required to guarantee ICC. Maximum limits are bounded for TC, TCH, and TCL.
5	TCKHL	clkin Fall Time	1	5	ns	Only required to guarantee ICC. Maximum limits are bounded for TC, TCH, and TCL.
6	TCICO	clkin to clkout Delay	0	11.5	ns	Specified for a 50-pF load. See Figure 17 for capacitive derating information.
7	TCLCL	clkout Period	–	2TCKIN	ns	–
8	TCHCL	clkout High Time	(TCLCL/2) – 5	(TCLCL/2) + 5	ns	Measure for VIH for high time, NIL for low time.
9	TCCCH	clkout Low Time	(TCLCL/2) – 5	(TCLCL/2) + 5	ns	Measure for VIH for high time, NIL for low time.
10	TCH1CH2	clkout Rise Time	1	6	ns	Specified for a 50-pF load. See Figure 17 for rise and fall times outside 50 pF.
11	TCL2CL1	clkout Fall Time	1	6	ns	Specified for a 50-pF load. See Figure 17 for rise and fall times outside 50 pF.

5.3 Serial Port Mode 0 Timing Characteristics

Serial Port Mode 0 timing characteristics are illustrated in Figure 20 and collected in Table 17.

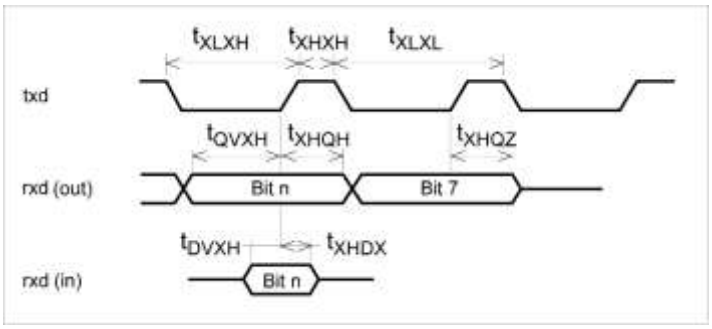


Figure 20. Serial Port Mode 0 Timing Characteristics

Table 17. Serial Port Mode 0 Timing Characteristics

Symbol	Parameter	Minimum	Maximum	Units
t_{XLXL}	txd Clock Period	t (n +1)	–	ns
t_{XLXH}	txd Clock Low to Clock High (n > 1)	2t – 35	2t + 35	ns
t_{XLXH}	txd Clock Low to Clock High (n = 1)	t – 35	t + 35	ns
t_{XHXL}	txd Clock High to Clock Low (n > 1)	(n – 1) t – 35	(n – 1) t + 35	ns
t_{XHXL}	txd Clock High to Clock Low (n = 1)	t – 35	t + 35	ns
t_{QVXH}	rxd Output Data Setup to txd Clock High (n > 1)	(n – 1) t – 35	–	ns
t_{QVXH}	rxd Output Data Setup to txd Clock High (n = 1)	t – 35	–	ns
t_{XHQX}	rxd Output Data Hold after txd Clock High (n > 1)	2t – 35	–	ns
t_{XHQX}	rxd Output Data Hold after txd Clock High (n = 1)	t – 35	–	ns
t_{XHQZ}	rxd Output Data Float after Last txd Clock High	–	t + 20	ns
t_{DVXH}	rxd Input Data Setup to txd Clock High	t + 20	–	ns
t_{XHDX}	rxd Input Data Hold after txd Clock High	0	–	ns

6. Reset Operation

The IA186XL/IA188XL will perform a reset operation any time the resin_n pin is active. Figure 21 shows the reset sequence when power is applied to the IA186XL/IA188XL. An external clock connected to clkin must not exceed the V_{CC} threshold being applied to the processor. This is normally not a problem if the clock driver is supplied with the same V_{CC} that supplies the processor. When attaching a crystal to the device, resin_n must remain active until both V_{CC} and clkout are stable (the length of time is application-specific and depends on the startup characteristics of the crystal circuit). The resin_n pin is designed to operate correctly using an RC reset circuit, but the designer must ensure that the ramp time for V_{CC} is not so long that resin_n is never really sampled at a logic low level when V_{CC} reaches minimum operating conditions.

> *Note: Failure to assert resin_n while the device is powering up will result in unpredictable operation.*

Figure 22, Warm Reset Timing, shows the timing sequence when resin_n is applied after V_{cc} is stable and the device has been operating. Any bus operation that is in progress at the time resin_n is asserted will terminate immediately.

While resin_n is active, bus signals lock_n, a19/once_n, and a18–a16 are configured as inputs and weakly held high by internal pull-up transistors. Only a19/ once_n can be overdriven to a low-to-enable ONCE Mode.

7. Bus Timing

Figures 21 through 27 present the various bus cycles that are generated by the processor. The figures show the relationship of the various bus signals to clkout. Together with the information present in AC Characteristics, the figures allow the user to determine all the critical timing analysis needed for a given application.

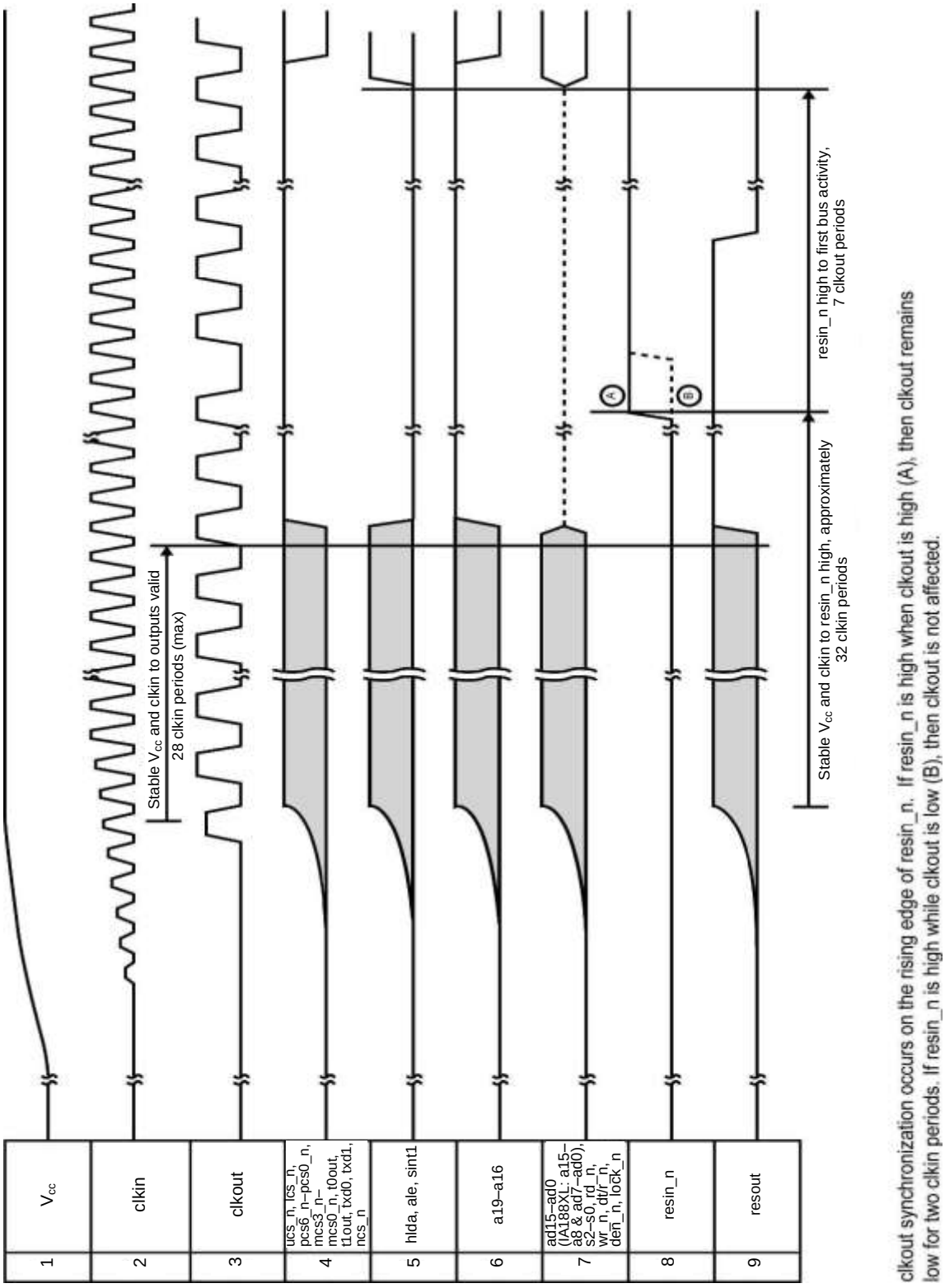


Figure 21. Cold Reset Timing

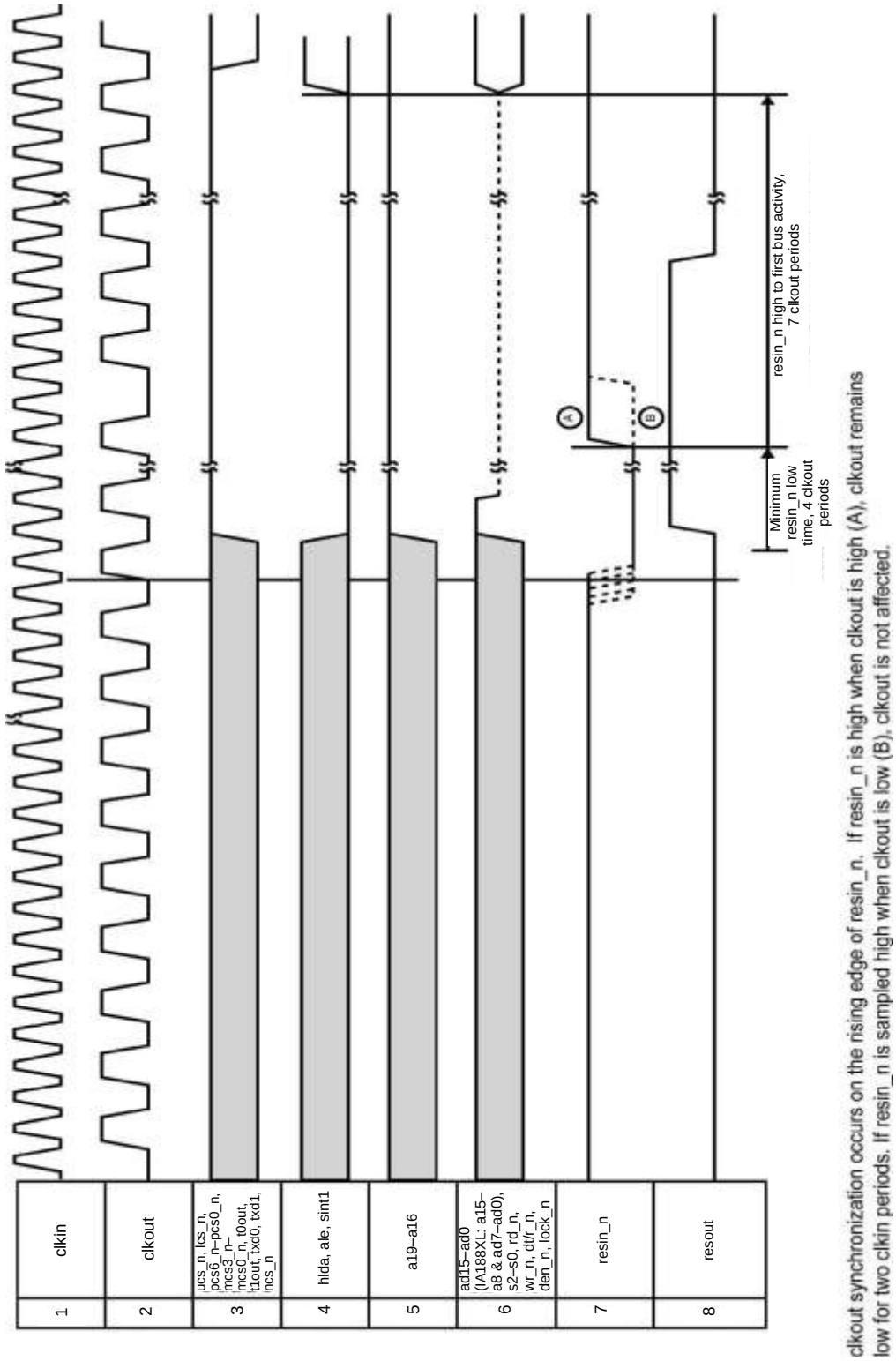


Figure 22. Warm Reset Timing

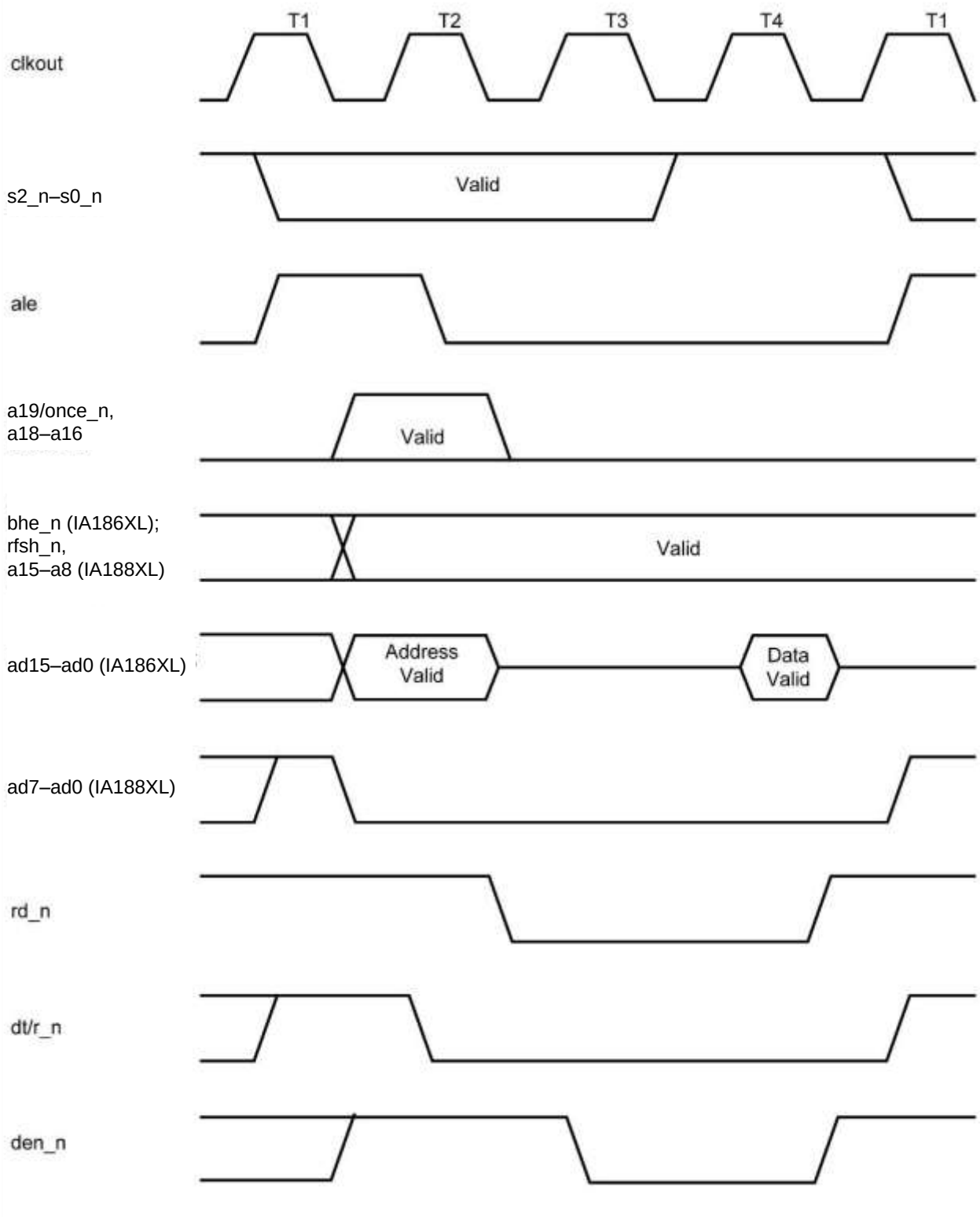


Figure 23. Read, Fetch, and Refresh Cycle Timing

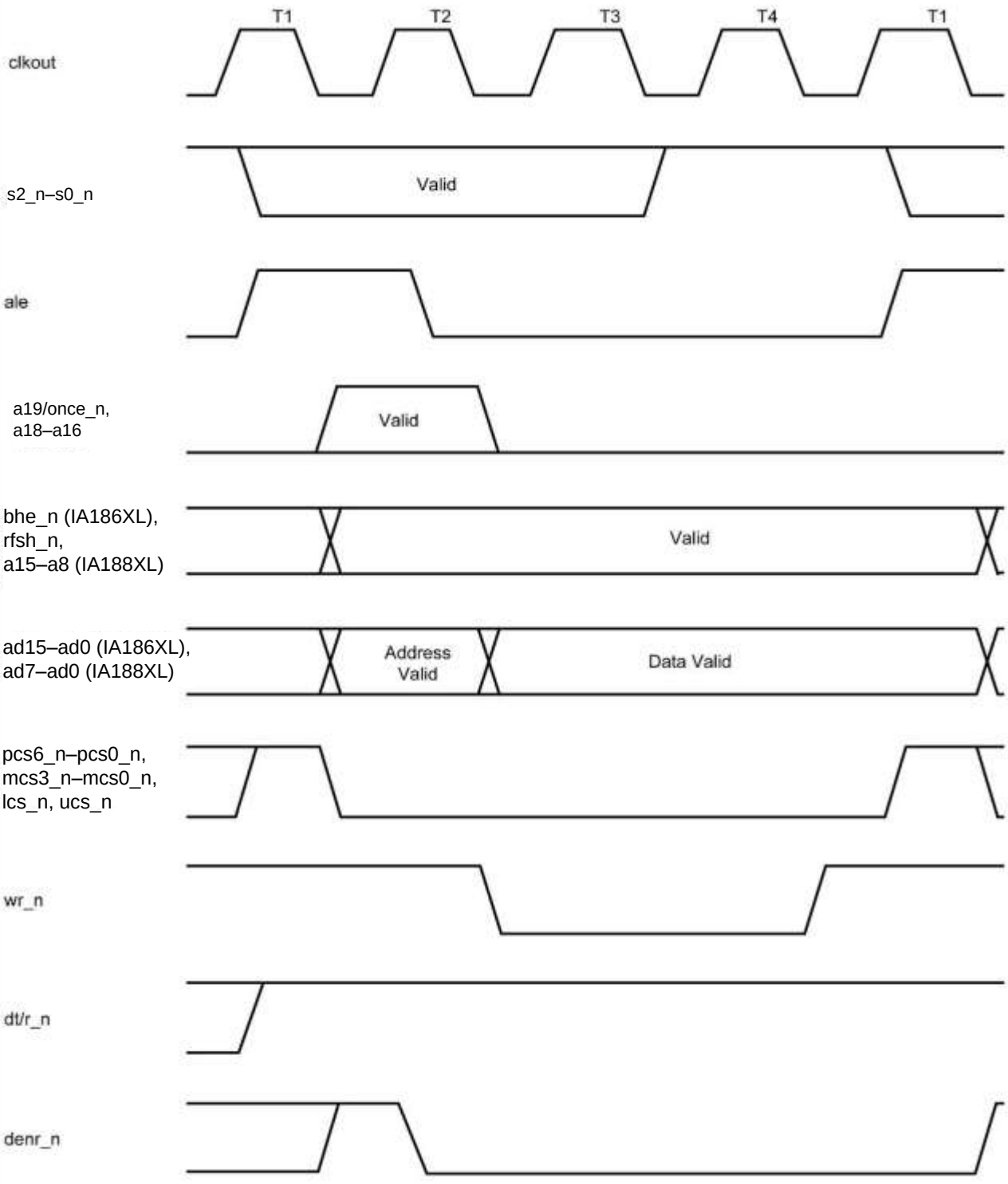


Figure 24. Write Cycle Timing

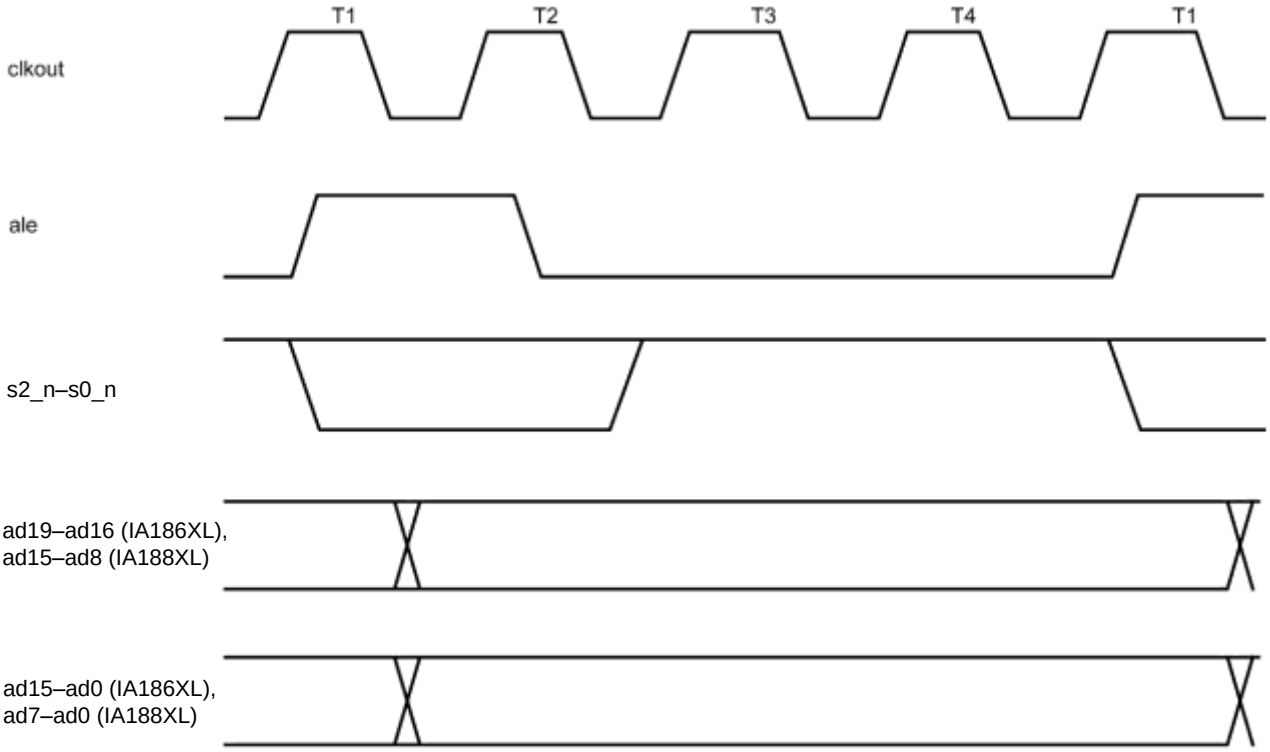


Figure 25. Halt Cycle Timing

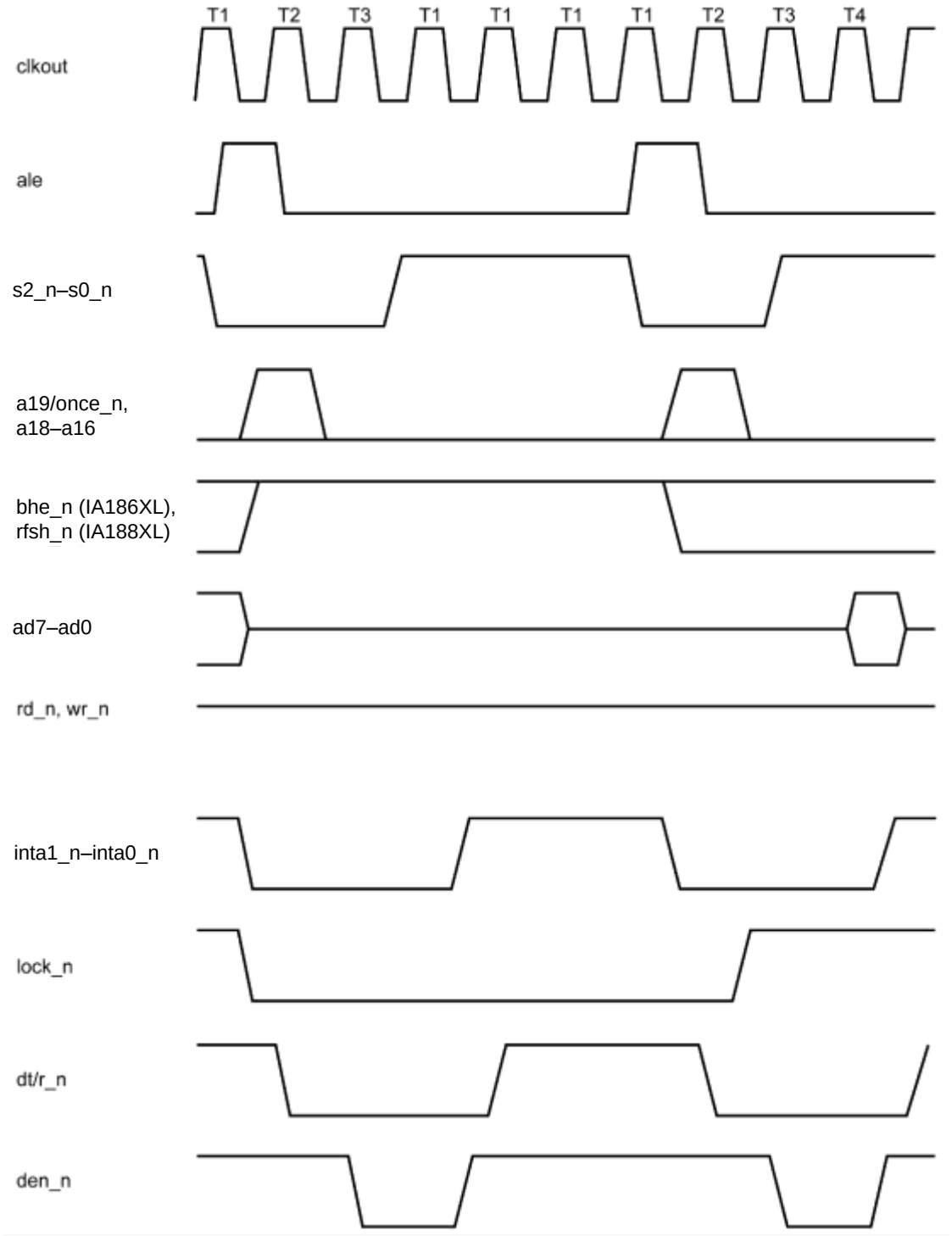


Figure 26. Interrupt Acknowledge (inta1_n, inta0_n) Cycle Timing

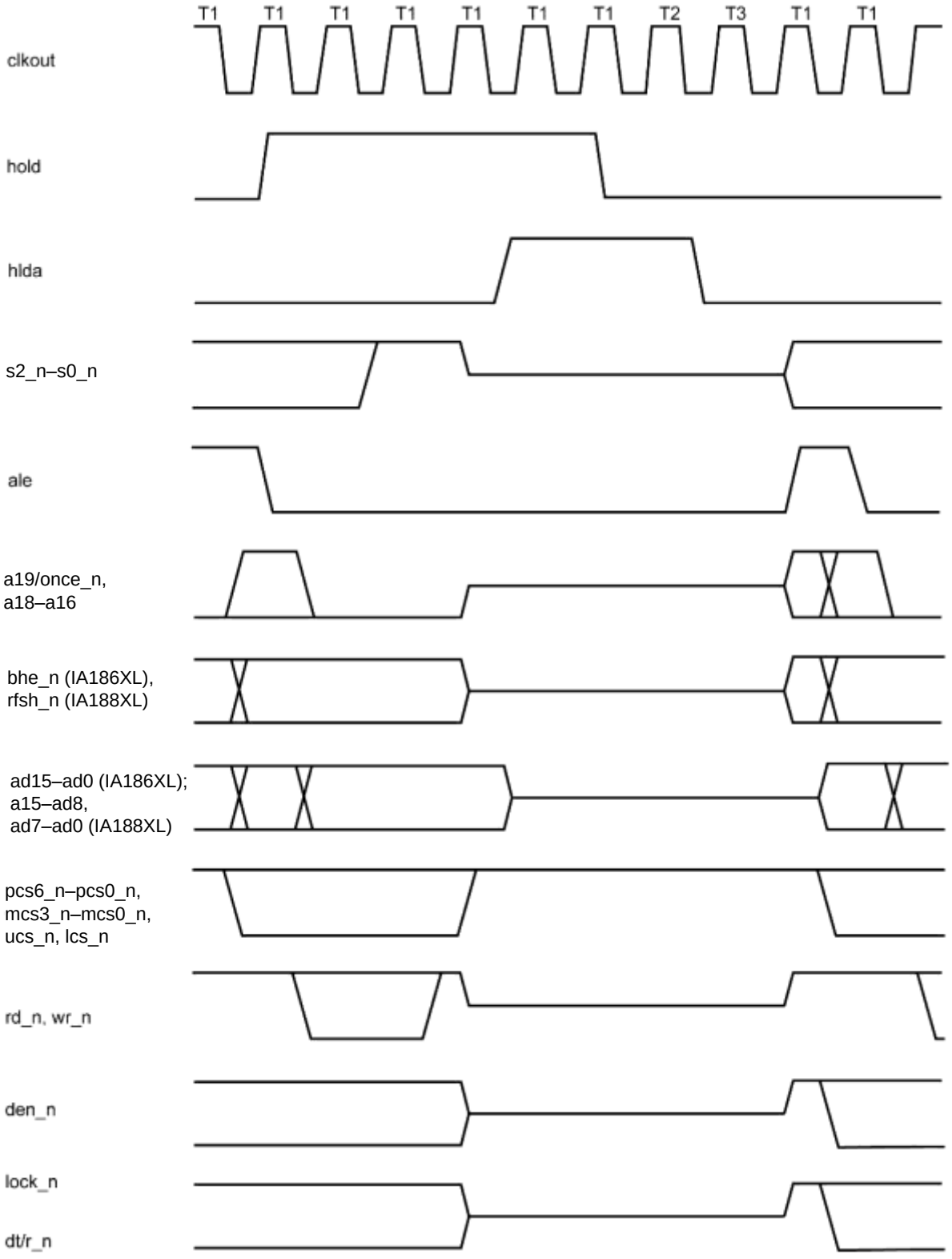


Figure 27. hold/hlda Timing

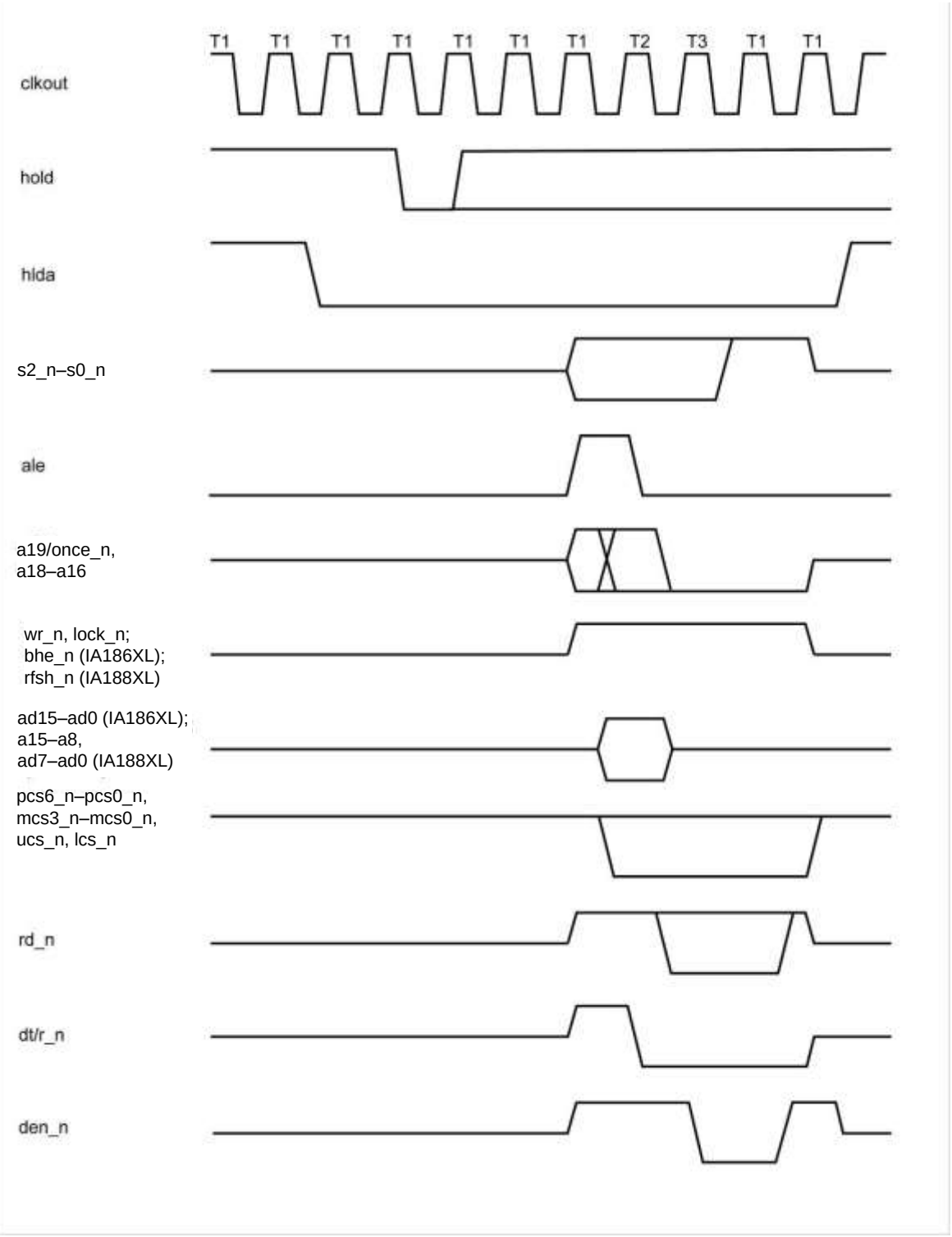


Figure 28. Refresh During Hold Acknowledge Timing

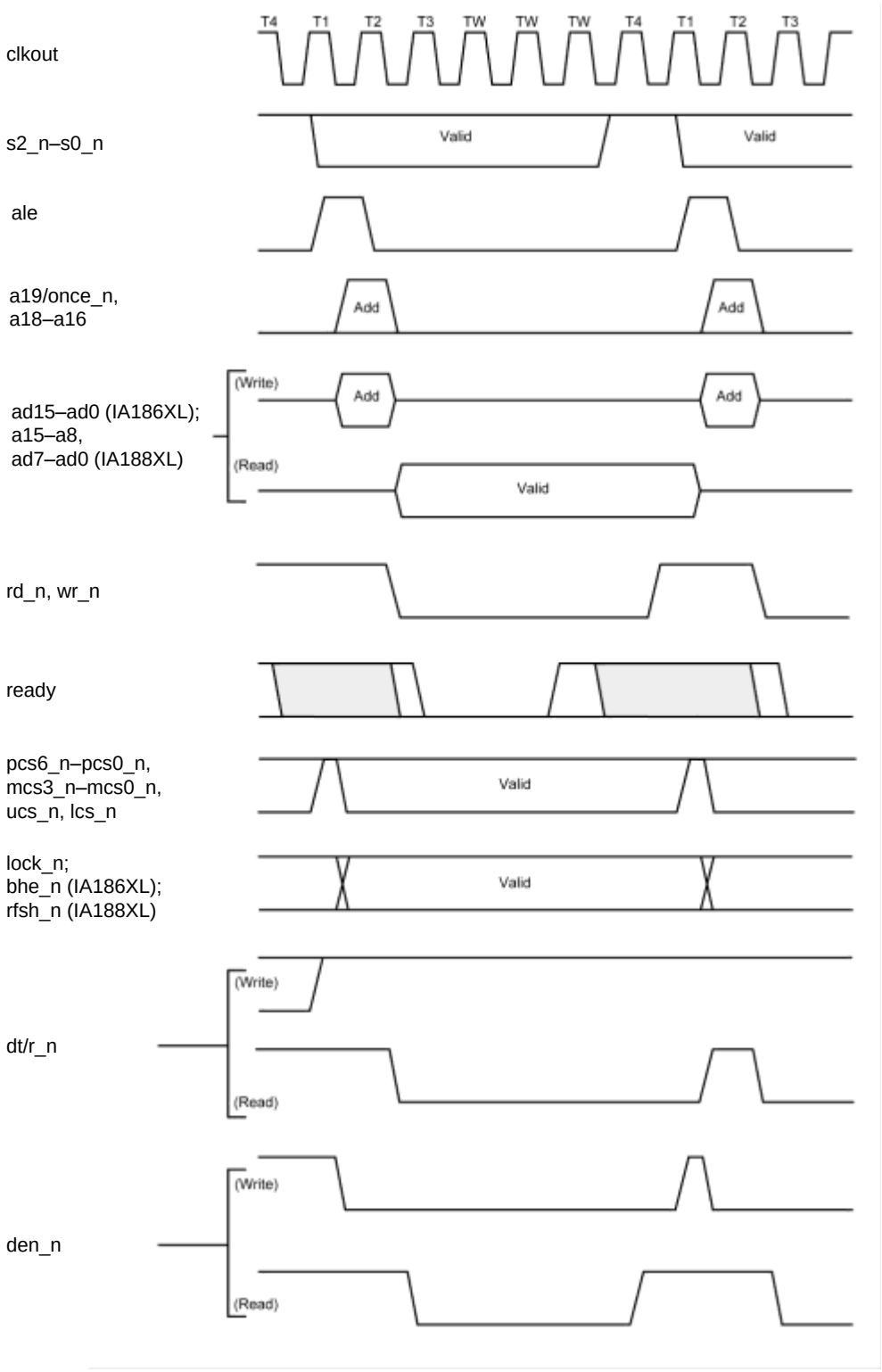


Figure 29. Ready Timing

8. Instruction Execution Times

Table 18 provides IA186XL and IA188XL execution times, mnemonic instruction, and additional information on execution, if required.

Table 18. Instruction Set Timing

Instruction	Clock Cycles		Comments
	IA186XL	IA188XL	
AAA	8	8	–
AAD	15	15	–
AAM	19	19	–
AAS	7	7	–
ADC Immediate to accumulator	3/4	3/4	8-bit/16-bit
ADC Immediate to register/memory	4/16	4/16[a]	register/memory
ADC Register/memory with register to either	3/10	3/10[a]	
ADD Immediate to accumulator	3/4	3/4	8-bit/16-bit
ADD Immediate to register/memory	4/16	4/16[a]	register/memory
ADD Register/memory with register either	3/10	3/10[a]	
AND Immediate to accumulator	3/4	3/4[a]	8-bit/16-bit
AND Immediate to register/memory	4/16	4/16[a]	register/memory
AND Register/memory and register to either	3/10	3/10[a]	
BOUND	33–35	33–35	–
CALL Direct intersegment	23	31	–
CALL Direct within segment	15	19	–
CALL Indirect intersegment	38	54	–
CALL Register/memory indirect with segment	13/19	17/27	register/memory
CBW	2	2	–
CLC	2	2	–
CLD	2	2	–
CLI	2	2	–
CMC	2	2	–
CMP Immediate with accumulator	3/4	3/4	8-bit/16-bit
CMP Immediate with register/memory	3/10	3/10[a]	register/memory
CMP Register with register/memory	3/10	3/10[a]	
CMP Register/memory with register	3/10	3/10[a]	

[a]Number of clock cycles for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

Table 18. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186XL	IA188XL	
CMPS	22	22[a]	–
CMPS (repeated *n* times)	5+22*n*	5+22*n*[a]	–
CS	2	2	–
CWD	4	4	–
DAA	4	4	–
DAS	4	4	–
DEC Register	3	3	–
DEC Register/memory	3/14	3/15[a]	register/memory
DIV Memory-Byte	35	35	–
DIV Memory-Word	44	44[a]	–
DIV Register-Byte	29	29	–
DIV Register-Word	38	38	–
DS	2	2	–
ENTER L − 0	15	19	–
ENTER L − 1	25	29	–
ENTER L > 1	22+16(*n*−1)	22+16(*n*−1)	–
ES	2	2	–
HLT	2	2	–
IDIV Memory-Byte	50–58	50–58	–
IDIV Memory-Word	59–67	59–67[a]	–
IDIV Register-Byte	44–52	44–52	–
IDIV Register-Word	53–61	53–61	–
IMUL Immediate (signed)	22–25/29–32	22–25/29–32	register/memory
IMUL Memory-Byte	31–34	31–34	–
IMUL Memory-Word	40–43	40–43[a]	–
IMUL Register-Byte	25–28	25–28	–
IMUL Register-Word	34–37	34–37	–
IN Fixed port	10	10[a]	–
IN Variable port	8	8[a]	–
INC Register	3	3	–
INC Register/memory	3/15	3/15[a]	register/memory
INS	14	14	–
INS (repeated *n* times)	8+8*n*	8+8*n*[a]	–
INT Type specified	47	47	–
INT Type 3	45	45	–
INTO	48/4	48/4	INTO taken/INTO not taken
IRET	28	28	–

[a]Number of clock cycles for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

Table 18. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186XL	IA188XL	
JA	4/13	4/13	Jump not taken/Jump taken
JAE	4/13	4/13	
JB	4/13	4/13	
JBE	4/13	4/13	
JCXZ	5/15	5/15	
JE	4/13	4/13	
JG	4/13	4/13	
JGE	4/13	4/13	
JL	4/13	4/13	
JLE	4/13	4/13	Jump not taken/Jump taken
JMP Register/memory indirect within segment	11/17	11/21	
JMP Direct intersegment	14	14	–
JMP Direct within segment	14	14	–
JMP Indirect inter-segment	26	34	–
JMP Short/long	14	14	–
JNA	4/13	4/13	Jump not taken/Jump taken
JNAE	4/13	4/13	
JNB	4/13	4/13	
JNBE	4/13	4/13	
JNE	4/13	4/13	
JNG	4/13	4/13	
JNGE	4/13	4/13	
JNL	4/13	4/13	
JNLE	4/13	4/13	
JNO	4/13	4/13	
JNP	4/13	4/13	
JNS	4/13	4/13	
JNZ	4/13	4/13	
JO	4/13	4/13	
JP	4/13	4/13	
JPE	4/13	4/13	
JPO	4/13	4/13	
JS	4/13	4/13	
JZ	4/13	4/13	
LAHF	2	2	–
LDS	18	26	–
LEA	6	6	–
LEAVE	8	8	–
LES	18	26	–

[a]Number of clock cycles for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

Table 18. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186XL	IA188XL	
LOCK	2	2	–
LODS	12	12[a]	–
LODS (repeated *n* times)	6+11*n*	6+11*n*[a]	–
LOOP	6/16	6/16	–
LOOPE	6/16	6/16	Loop not taken/Loop taken
LOOPNE	6/16	6/16	
LOOPNZ	6/16	6/16	
LOOPZ	6/16	6/16	Loop not taken/Loop taken
MOV Accumulator to memory	9	9[a]	–
MOV Immediate to register	3/4	3/4	8-bit/16-bit
MOV Immediate to register/memory	12/13	12/13	register/memory
MOV Memory to accumulator	8	8[a]	–
MOV Register to Register/Memory	2/12	2/12[a]	register/memory
MOV Register/memory to register	2/9	2/9[a]	
MOV Register/memory to segment register	2/9	2/13	
MOV Segment register to register/memory	2/11	2/15	
MOVS	14	14[a]	–
MOVS (repeated *n* times)	8+8*n*	8+8*n*[a]	–
MUL Memory-Byte	32–34	32–34	–
MUL Memory-Word	41–43	41–43[a]	–
MUL Register-Byte	26–28	26–28	–
MUL Register-Word	35–37	35–37	–
NEG	3/10	3/10[a]	register/memory
NOP	3	3	–
NOT	3/10	3/10[a]	register/memory
OR Immediate to accumulator	3/4	3/4[a]	8-bit/16-bit
OR Immediate to register/memory	4/16	4/16[a]	register/memory
OR Register/memory and register to either	3/10	3/10[a]	
OUT Fixed port	9	9[a]	–
OUT Variable port	7	7[a]	–
OUTS	14	14	–
OUTS (repeated *n* times)	8+8*n*	8+8*n*[a]	–
POP Memory	20	24	–
POP Register	10	14	–
POP Segment register	8	12	–
POPA	51	83	–
POPF	8	12	–
PUSH Immediate	10	14	–

[a]Number of clock cycles for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

Table 18. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186XL	IA188XL	
PUSH Memory	16	20	–
PUSH Register	10	14	–
PUSH Segment register	9	13	–
PUSHA	36	68	–
PUSHF	9	13	–
RET Inter-segment	22	30	–
RET Inter-segment adding immediate to SP	25	33	–
RET Within segment	16	20	–
RET Within segment adding immediate to SP	18	22	–
ROL Register/Memory by 1	2/15	2/15	register/memory
ROL Register/Memory by CL	5+n/17+n	5+n/17+n	
ROL Register/Memory by Count	5+n/17+n	5+n/17+n	register/memory
ROR Register/Memory by 1	2/15	2/15	
ROR Register/Memory by CL	5+n/17+n	5+n/17+n	
ROR Register/Memory by Count	5+n/17+n	5+n/17+n	
SAHF	3	3	–
SBB Immediate from accumulator	3/4	3/4[a]	8-bit/16-bit
SBB Immediate from register/memory	4/16	4/16[a]	register/memory
SBB Register/memory and register to either	3/10	3/10[a]	
SCAS	15	15[a]	–
SCAS (repeated *n* times)	5+15*n*	5+15*n*[a]	–
SHL Register/Memory by 1	2/15	2/15	–
SHL Register/Memory by CL	5+n/17+*n*	5+n/17+*n*	register/memory
SHL Register/Memory by Count	5+n/17+*n*	5+n/17+*n*	
SHR Register/Memory by 1	2/15	2/15	
SHR Register/Memory by CL	5+n/17+*n*	5+n/17+*n*	
SHR Register/Memory by Count	5+n/17+*n*	5+n/17+*n*	
SS	2	2	–
STC	2	2	–
SUB Immediate from accumulator	3/4	3/4	8-bit/16-bit
SUB Immediate from register/memory	4/16	4/16[a]	register/memory
SUB Register/memory and register to either	3/10	3/10[a]	
STD	2	2	–
STI	2	2	–

[a]Number of clock cycles for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

Table 18. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186XL	IA188XL	
STOS	10	10[a]	–
STOS (repeated n times)	6+9n	6+9n	–
TEST Immediate data and accumulator	3/4	3/4	8-bit/16-bit
TEST Immediate data and register/memory	4/10	4/10[a]	register/memory
TEST Register/memory and register	3/10	3/10[a]	
WAIT	6	6	test_n = 0
XCHG Register with accumulator	3	3	
XCHG Register/memory with register	4/17	4/17[a]	register/memory
XLAT	11	15	–
XOR Immediate to accumulator	3/4	3/4	8-bit/16-bit
XOR Immediate to register/memory	4/16	4/16[a]	register/memory
XOR Register/memory and register to either	3/10	3/10[a]	–

[a]Number of clock cycles for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

9. Innovasic Part Number Cross-Reference

Tables 19 through 21 cross-reference the Innovasic part number with the corresponding Intel part number.

Table 19. Innovasic Part Number Cross-Reference for the PLCC

Innovasic Part Number	Intel Part Number	Package Type	Temperature Grades
IA186XL-PLC68I-R-00 (lead free–RoHS)	N80C186XL25 N80C186XL20 N80C186XL12 TN80C186XL25 TN80C186XL20 TN80C186XL12 EE80C186XL25 EE80C186XL20 EE80C186XL12 EN80C186XL20 EN80C186XL12	68-Lead PLCC	Commercial and industrial
IA188XL-PLC68I-R-00 (lead free–RoHS)	N80C188XL25 N80C188XL20 N80C188XL12 TN80C188XL25 TN80C188XL20 TN80C188XL12 EE80C188XL25 EE80C188XL20 EE80C188XL12 EN80C188XL20 EN80C188XL12	68-Lead PLCC	Commercial and industrial

Table 20. Innovasic Part Number Cross-Reference for the PQFP

Innovasic Part Number	Intel Part Number	Package Type	Temperature Grades
IA186XL-PQF80I-R-00 (lead free–RoHS)	S80C186XL25 S80C186XL20 S80C186XL12 TS80C186XL25 TS80C186XL20 TS80C186XL12 EG80C186XL25 EG80C186XL20 ES80C186XL20	80-Lead PQFP	Commercial and industrial
IA188XL-PQF80I-R-00 (lead free–RoHS)	S80C188XL25 S80C188XL20 S80C188XL12 TS80C188XL25 TS80C188XL20 TS80C188XL12 EG80C188XL25 EG80C188XL20 ES80C188XL20	80-Lead PQFP	Commercial and industrial

Table 21. Innovasic Part Number Cross-Reference for the LQFP

Innovasic Part Number	Intel Part Number	Package Type	Temperature Grades
IA186XL-PLQ80I-R-00 (lead free–RoHS)	SB80C186XL25 SB80C186XL20 SB80C186XL12 YW80C186XL25 YW80C186XL20	80-Lead LQFP	Commercial and industrial
IA188XL-PLQ80I-R-00 (lead free–RoHS)	SB80C188XL25 SB80C188XL20 SB80C188XL12 YW80C188XL25 YW80C188XL20	80-Lead LQFP	Commercial and industrial

10. For Additional Information

The Innovasic Semiconductor IA186XL and IA188XL microcontrollers are form, fit, and function replacements for the original Intel 80C186XL and 80C188XL 16-bit high-integration embedded processors.

The Innovasic Support Team wants our information to be complete, accurate, useful, and easy to understand. Please feel free to contact our experts at Innovasic at any time with suggestions, comments, or questions.

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