Innovasic®
Semiconductor
Extended Life Semiconductor Solutions

IA186EB/IA188EB
8-Bit/16-Bit Microcontrollers

Data Sheet

Published by Innovasic Semiconductor, Inc.
3737 Princeton Drive NE, Suite 130, Albuquerque, NM 87107

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. Introduction

The Innovasic Semiconductor IA186EB and IA188EB microcontrollers are form, fit, and function replacements for the original Intel® 80C186EB, 80C188EB, 80L186EB, and 80L188EB 16-bit high-integration embedded processors.

These devices are produced using Innovasic's Managed IC Lifetime Extension System (MILES™). This cloning technology, which produces replacement ICs beyond simple emulations, ensures complete compatibility with the original device, including any "undocumented features." Additionally, the MILES process captures the clone design in such a way that production of the clone can continue even as silicon technology advances.

The IA186EB and IA188EB microcontrollers replace the obsolete Intel 80C186EB and 80C188EB devices, allowing users to retain existing board designs, software compilers/assemblers, and emulation tools, thereby avoiding expensive redesign efforts.

1.1 General Description

The Innovasic Semiconductor IA186EB and IA188EB microcontrollers are an upgrade for the 80C186EB/80C188EB microcontroller designs with integrated peripherals to provide increased functionality and reduce system costs. The IA186EB and IA188EB devices are designed to satisfy requirements of embedded products designed for telecommunications, office automation and storage, and industrial controls.

The IA186EB and IA188EB microcontrollers have a set of base peripherals beneficial to many embedded applications and include a standard numeric interface, an interrupt control unit, a chip-select unit, a DRAM refresh control unit, a power management unit, and three 16-bit timer/counters.

The IA186EB and IA188EB microcontrollers are capable of operating at 5.0 or 3.3 volts. This datasheet discusses both modes of operation. Where applicable, characteristics specific to either 3.3 or 5.0 volt operation are identified separately throughout this datasheet.

Additionally, the IA186EB and IA188EB include two integrated serial ports that support both synchronous and asynchronous communications, simplifying inter-processor and display communications. The IA186EB and IA188EB also have an enhanced chip-select unit and two multiplexed I/O ports. The enhanced chip-select unit offers 10 general chip selects, each with the ability to address up to 1 Mbyte. This enhanced unit enables memory-bank switching to expand the IA186EB/IA188EB 1-Mbyte address space. The I/O ports allow for basic functions such as scanning keypads for input. The ports can also be used to control system power consumption, disabling unneeded components.

The serial ports, I/O capabilities, and enhanced chip selects make the IA186EB/IA188EB an excellent processor for portable data acquisition or communication applications.

1.2 Features

The primary features of the IA186EB and IA188EB microcontrollers are as follows:

- Low-Power Operating Modes
  - Idle (freezes CPU clocks; peripherals are kept active)
  - Power-Down (freezes all internal clocks)

- Low-Power CPU Core (static)

- Direct Addressing Capability
  - Memory: 1 Mbyte
  - I/O: 64 Kbyte

- I/O Ports
  - 2 each, 8-Bit
  - Multiplexed

- Clock Generator

- Chip Selects
  - 10 each, Programmable
  - Integral Wait-State Generator

- Memory Refresh Control Unit

- Interrupt Controller, Programmable

- Counter/Timers
  - 3 each, 16-Bit
  - Programmable

- Serial Channels
  - 2 each, UARTs
  - Integral Baud Rate Generator

- Operating Frequency (system clock input)
  - 66.7 MHz @ 5V
  - 55.5 MHz @ 3.3V

Chapter 4, Functional Description, provides details of the IA186EB and IA188EB microcontrollers, including the features listed above.

2. Packaging, Pin Descriptions, and Physical Dimensions

Information on the packages and pin descriptions for the IA186EB and the IA188EB is provided separately. Refer to sections, figures, and tables for information on the device of interest.

2.1 Packages and Pinouts

The Innovasic Semiconductor IA186EB and IA188EB microcontroller is available in the following packages:

- 84-Pin Plastic Leaded Chip Carrier (PLCC), equivalent to original PLCC package
- 80-Pin Plastic Quad Flat Pack (PQFP), equivalent to original PQFP package
- 80-Pin Low-Profile Quad Flat Pack (LQFP), equivalent to original SQFP package

2.1.1 IA186EB 84 PLCC Package

The pinout for the IA186EB 84 PLCC Package is as shown in Figure 1. The corresponding pinout is provided in Table 1.

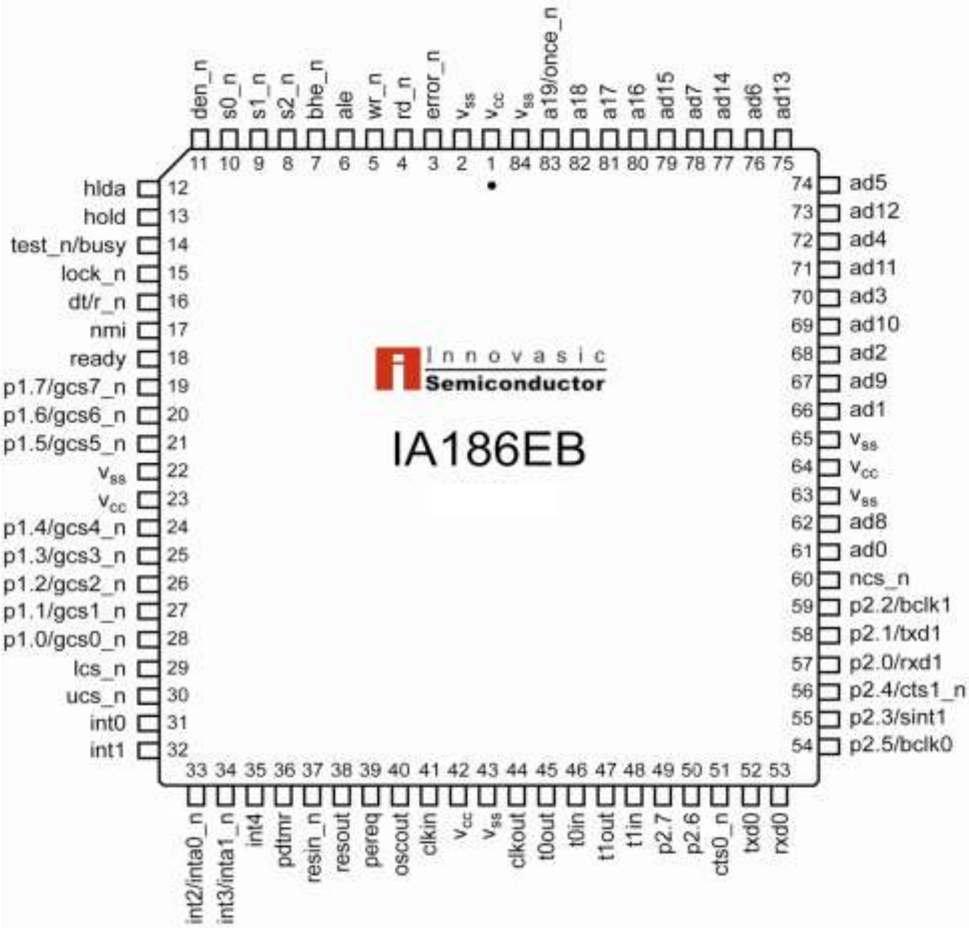


Figure 1. IA186EB 84-Pin PLCC Package Diagram

Table 1. IA186EB 84-Pin PLCC Pin Listing

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{cc}	22	V_{ss}	43	V_{ss}	64	V_{cc}
2	V_{ss}	23	V_{cc}	44	clkout	65	V_{ss}
3	error_n	24	p1.4/gcs4_n	45	t0out	66	ad1
4	rd_n	25	p1.3/gcs3_n	46	t0in	67	ad9
5	wr_n	26	p1.2/gcs2_n	47	t1out	68	ad2
6	ale	27	p1.1/gcs1_n	48	t1in	69	ad10
7	bhe_n	28	p1.0/gcs0_n	49	p2.7	70	ad3
8	s2_n	29	lcs_n	50	p2.6	71	ad11
9	s1_n	30	ucs_n	51	cts0_n	72	ad4
10	s0_n	31	int0	52	txd0	73	ad12
11	den_n	32	int1	53	rxd0	74	ad5
12	hlda	33	int2/inta0_n	54	p2.5/bclk0	75	ad13
13	hold	34	int3/inta1_n	55	p2.3/sint1	76	ad6
14	test_n/busy	35	int4	56	p2.4/cts1_n	77	ad14
15	lock_n	36	pdtmr	57	p2.0/rxd1	78	ad7
16	dt/r_n	37	resin_n	58	p2.1/txd1	79	ad15
17	nmi	38	resout	59	p2.2/bclk1	80	a16
18	ready	39	pereq	60	ncs_n	81	a17
19	p1.7/gcs7_n	40	oscout	61	ad0	82	a18
20	p1.6/gcs6_n	41	clkin	62	ad8	83	a19/once_n
21	p1.5/gcs5_n	42	V_{cc}	63	V_{ss}	84	V_{ss}

2.1.2 IA188EB 84 PLCC Package

The pinout for the IA188EB 84 PLCC Package is as shown in Figure 2. The corresponding pinout is provided in Table 2.

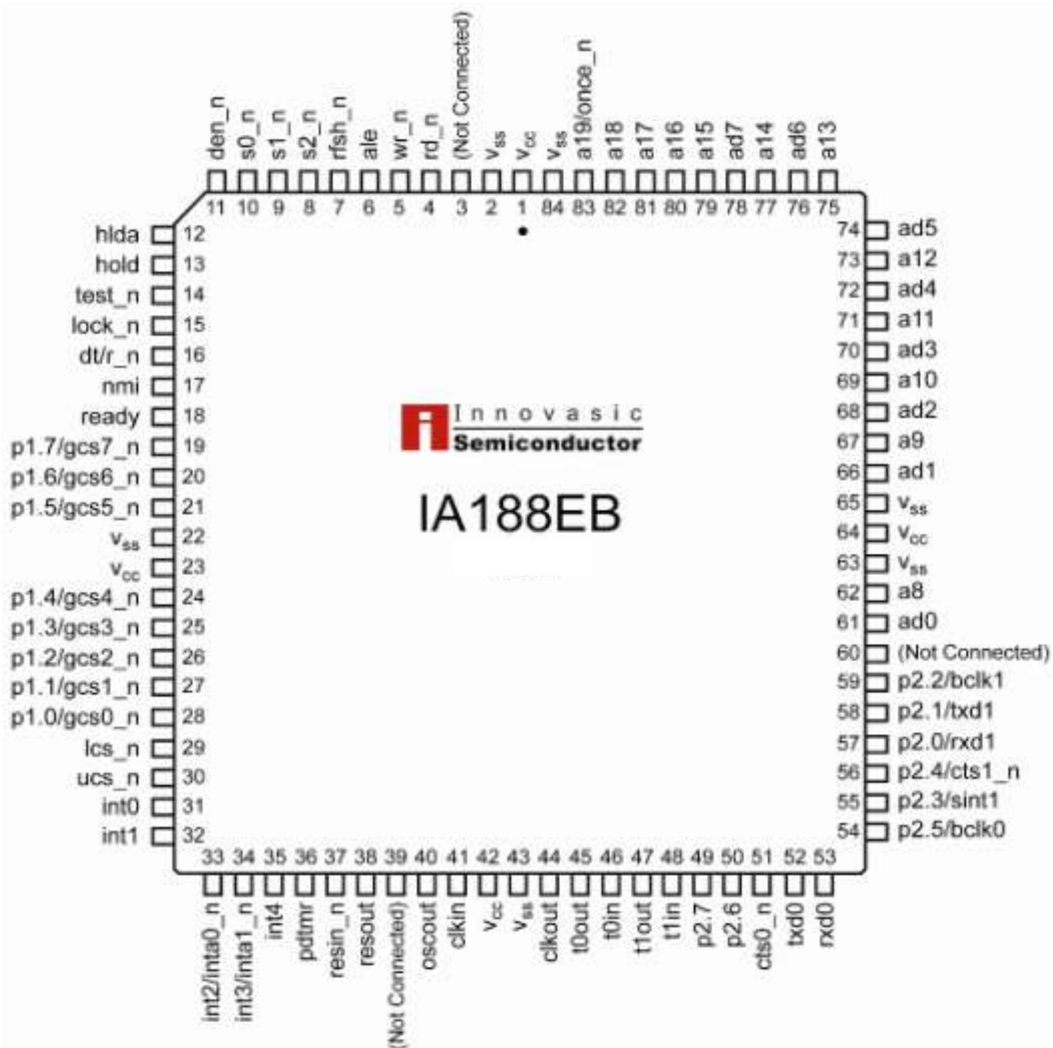


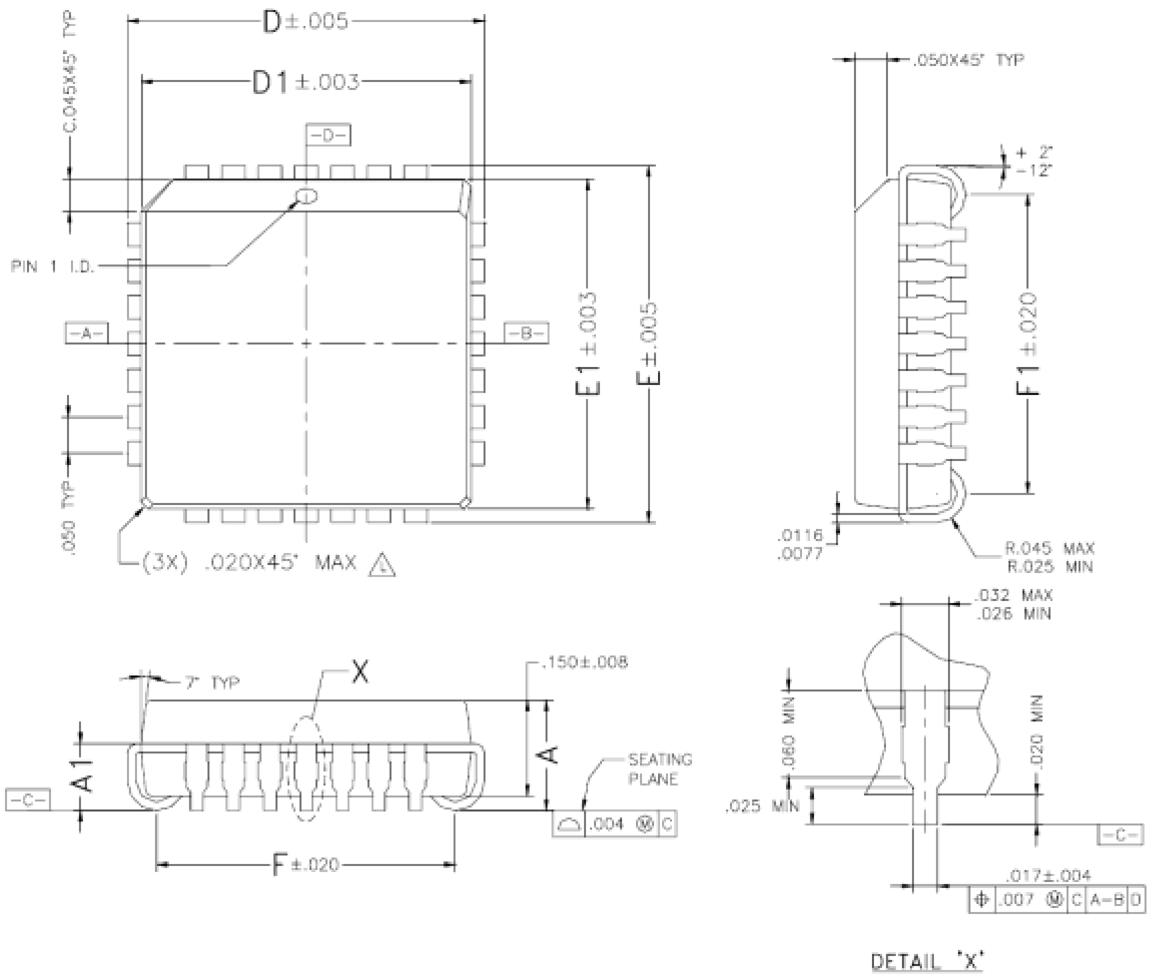
Figure 2. IA188EB 84-Pin PLCC Package Diagram

Table 2. IA188EB 84-Pin PLCC Pin Listing

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{cc}	22	V_{ss}	43	V_{ss}	64	V_{cc}
2	V_{ss}	23	V_{cc}	44	clkout	65	V_{ss}
3	Not Connected	24	p1.4/gcs4_n	45	t0out	66	ad1
4	rd_n	25	p1.3/gcs3_n	46	t0in	67	a9
5	wr_n	26	p1.2/gcs2_n	47	t1out	68	ad2
6	ale	27	p1.1/gcs1_n	48	t1in	69	a10
7	rfsh_n	28	p1.0/gcs0_n	49	p2.7	70	ad3
8	s2_n	29	lcs_n	50	p2.6	71	a11
9	s1_n	30	ucs_n	51	cts0_n	72	ad4
10	s0_n	31	int0	52	txd0	73	a12
11	den_n	32	int1	53	rxd0	74	ad5
12	hlda	33	int2/inta0_n	54	p2.5/bclk0	75	a13
13	hold	34	int3/inta1_n	55	p2.3/sint1	76	ad6
14	test_n	35	int4	56	p2.4/cts1_n	77	a14
15	lock_n	36	pdtmr	57	p2.0/rxd1	78	ad7
16	dt/r_n	37	resin_n	58	p2.1/txd1	79	a15
17	nmi	38	resout	59	p2.2/bclk1	80	a16
18	ready	39	Not Connected	60	Not Connected	81	a17
19	p1.7/gcs7_n	40	oscout	61	ad0	82	a18
20	p1.6/gcs6_n	41	clkin	62	a8	83	a19/once_n
21	p1.5/gcs5_n	42	V_{cc}	63	V_{ss}	84	V_{ss}

2.1.3 PLCC Physical Dimensions

The physical dimensions for the 84 PLCC are as shown in Figure 3.



Legend:

Symbol	Min	Nom	Max
A	0.165″	–	0.180″
A1	0.090″	–	0.120″
D	–	1.190″	–
D1	–	1.154″	–
E	–	1.190″	–
E1	–	1.154″	–
F	–	1.110″	–
F1	–	1.110″	–

Note: The bottom package is bigger than the top package by 0.004 inches (0.002 inches per side). Bottom package dimensions follow those stated in this drawing.

Figure 3. 84-Pin PLCC Physical Package Dimensions

2.1.4 IA186EB 80 PQFP Package

The pinout for the IA186EB 80 PQFP Package is as shown in Figure 4. The corresponding pinout is provided in Table 3.

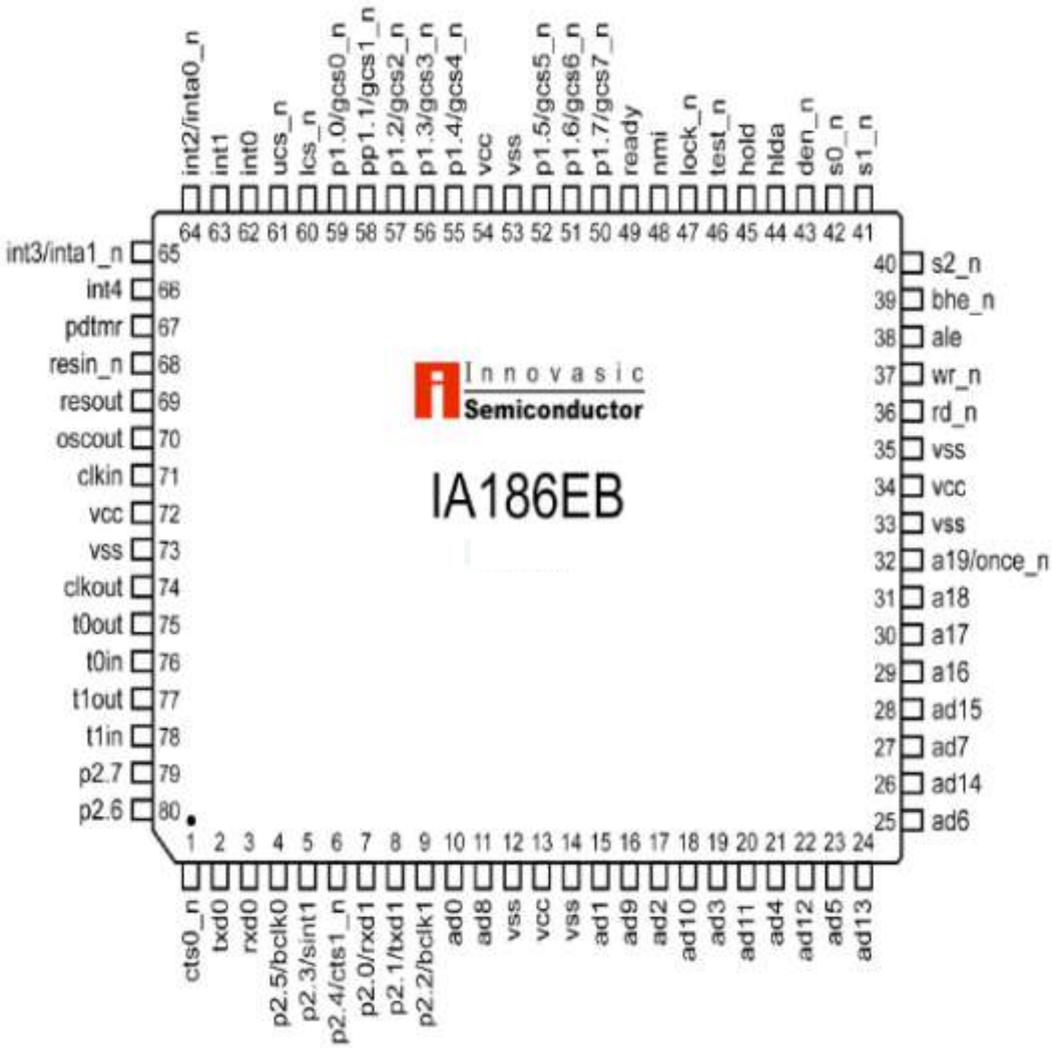


Figure 4. IA186EB 80-Pin PQFP Package Diagram

Table 3. IA186EB 80-Pin PQFP Pin Listing

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	cts0_n	21	ad4	41	s1_n	61	ucs_n
2	txd0	22	ad12	42	s0_n	62	int0
3	rxd0	23	ad5	43	den_n	63	int1
4	p2.5/bclk0	24	ad13	44	hlda	64	int2/inta0_n
5	p2.3/sint1	25	ad6	45	hold	65	int3/inta1_n
6	p2.4/cts1_n	26	ad14	46	test_n	66	int4
7	p2.0/rxd1	27	ad7	47	lock_n	67	pdtmr
8	p2.1/txd1	28	ad15	48	nmi	68	resin_n
9	p2.2/bclk1	29	a16	49	ready	69	resout
10	ad0	30	a17	50	p1.7/gcs7_n	70	oscout
11	ad8	31	a18	51	p1.6/gcs6_n	71	clkin
12	Vss	32	a19/once_n	52	p1.5/gcs5_n	72	Vcc
13	Vcc	33	Vss	53	Vss	73	Vss
14	Vss	34	Vcc	54	Vcc	74	clkout
15	ad1	35	Vss	55	p1.4/gcs4_n	75	t0out
16	ad9	36	rd_n	56	p1.3/gcs3_n	76	t0in
17	ad2	37	wr_n	57	p1.2/gcs2_n	77	t1out
18	ad10	38	ale	58	pp1.1/gcs1_n	78	t1in
19	ad3	39	bhe_n	59	p1.0/gcs0_n	79	p2.7
20	ad11	40	s2_n	60	lcs_n	80	p2.6

2.1.5 IA188EB 80 PQFP Package

The pinout for the IA188EB 80 PQFP Package is as shown in Figure 5. The corresponding pinout is provided in Table 4.

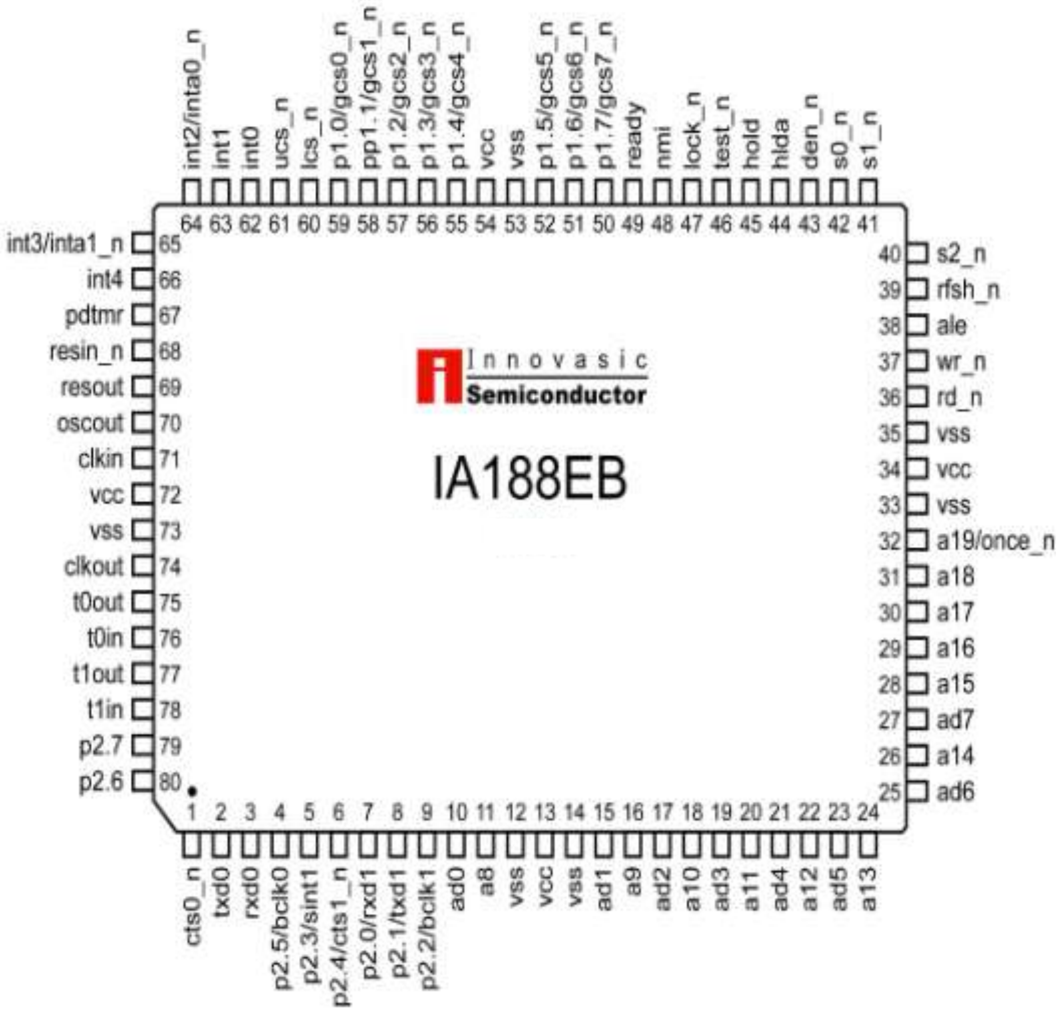


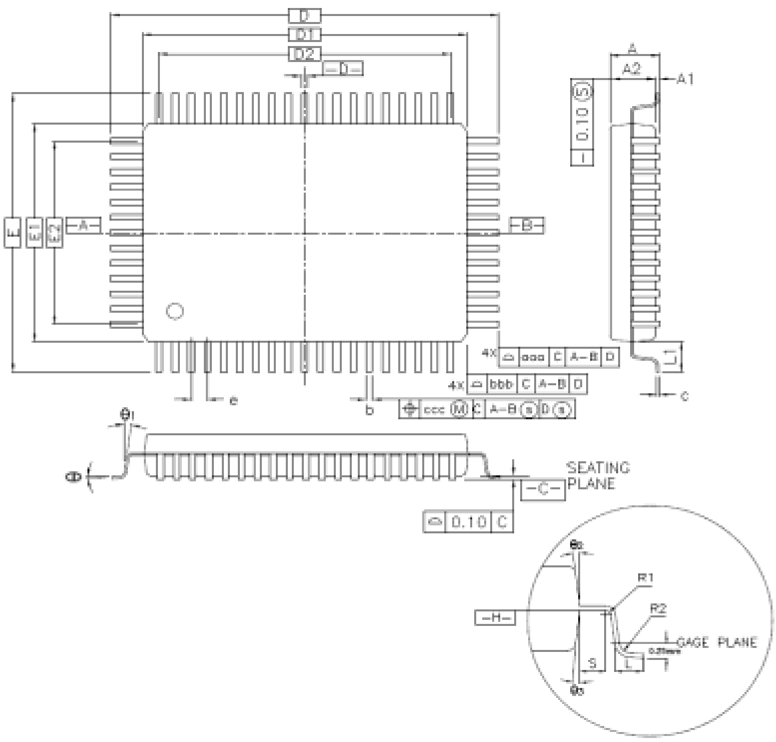
Figure 5. IA188EB 80-Pin PQFP Package Diagram

Table 4. IA188EB 80-Pin PQFP Pin Listing

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	cts0_n	21	ad4	41	s1_n	61	ucs_n
2	txd0	22	a12	42	s0_n	62	int0
3	rxd0	23	ad5	43	den_n	63	int1
4	p2.5/bclk0	24	a13	44	hlda	64	int2/inta0_n
5	p2.3/sint1	25	ad6	45	hold	65	int3/inta1_n
6	p2.4/cts1_n	26	a14	46	test_n	66	int4
7	p2.0/rxd1	27	ad7	47	lock_n	67	pdtmr
8	p2.1/txd1	28	a15	48	nmi	68	resin_n
9	p2.2/bclk1	29	a16	49	ready	69	resout
10	ad0	30	a17	50	p1.7/gcs7_n	70	oscout
11	a8	31	a18	51	p1.6/gcs6_n	71	clkin
12	Vss	32	a19/once_n	52	p1.5/gcs5_n	72	Vcc
13	Vcc	33	Vss	53	Vss	73	Vss
14	Vss	34	Vcc	54	Vcc	74	clkout
15	ad1	35	Vss	55	p1.4/gcs4_n	75	t0out
16	a9	36	rd_n	56	p1.3/gcs3_n	76	t0in
17	ad2	37	wr_n	57	p1.2/gcs2_n	77	t1out
18	a10	38	ale	58	pp1.1/gcs1_n	78	t1in
19	ad3	39	rfsh_n	59	p1.0/gcs0_n	79	p2.7
20	a11	40	s2_n	60	lcs_n	80	p2.6

2.1.6 PQFP Physical Dimensions

The physical dimensions for the 80 PQFP are as shown in Figure 6.



Legend:

Symbol	Millimeter Min	Millimeter Nom	Millimeter Max	Inch Min	Inch Nom	Inch Max
A	–	–	3.40	–	–	0.134
A1	0.25	–	–	0.010	–	–
A2	2.55	2.72	3.05	0.100	0.107	0.120
D		23.90 Basic			0.941 Basic	
D1		20.00 Basic			0.787 Basic	
E		17.90 Basic			0.705 Basic	
E1		14.00 Basic			0.551 Basic	
R2	0.013	–	0.30	0.005	–	0.012
R1	0.013	–	–	0.005	–	–
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	–	–	0°	–	–
θ2, θ3[a]		7° REF			7° REF	
θ2, θ3[b]		15° REF			15° REF	
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1		1.95 REF			0.077 REF	
S	0.40	–	–	0.016	–	–
b	0.30	0.35	0.45	0.012	0.014	0.018
e		0.80 BSC			0.031 BSC	
D2		18.40 REF			0.724	
E2		12.00 REF			0.472	
Tolerances of Form and Position						
aaa		0.25			0.010	
bbb		0.20			0.008	
ccc		0.20			0.008	

[a]Alloy 42 L/F.
[b]Copper L/F.

Notes:
1. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimension D1 and E1 do not include mold mismatch and are determined a datum plane –H– .
2. Dimension b does not include dambar protrusion. Allowable dambar protrusion will not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located on the lower radius of the lead foot.

Figure 6. 80-Pin PQFP Physical Package Dimensions

2.1.7 IA186EB 80 LQFP Package

The pinout for the IA186EB 80 LQFP Package is as shown in Figure 7. The corresponding pinout is provided in Table 5.

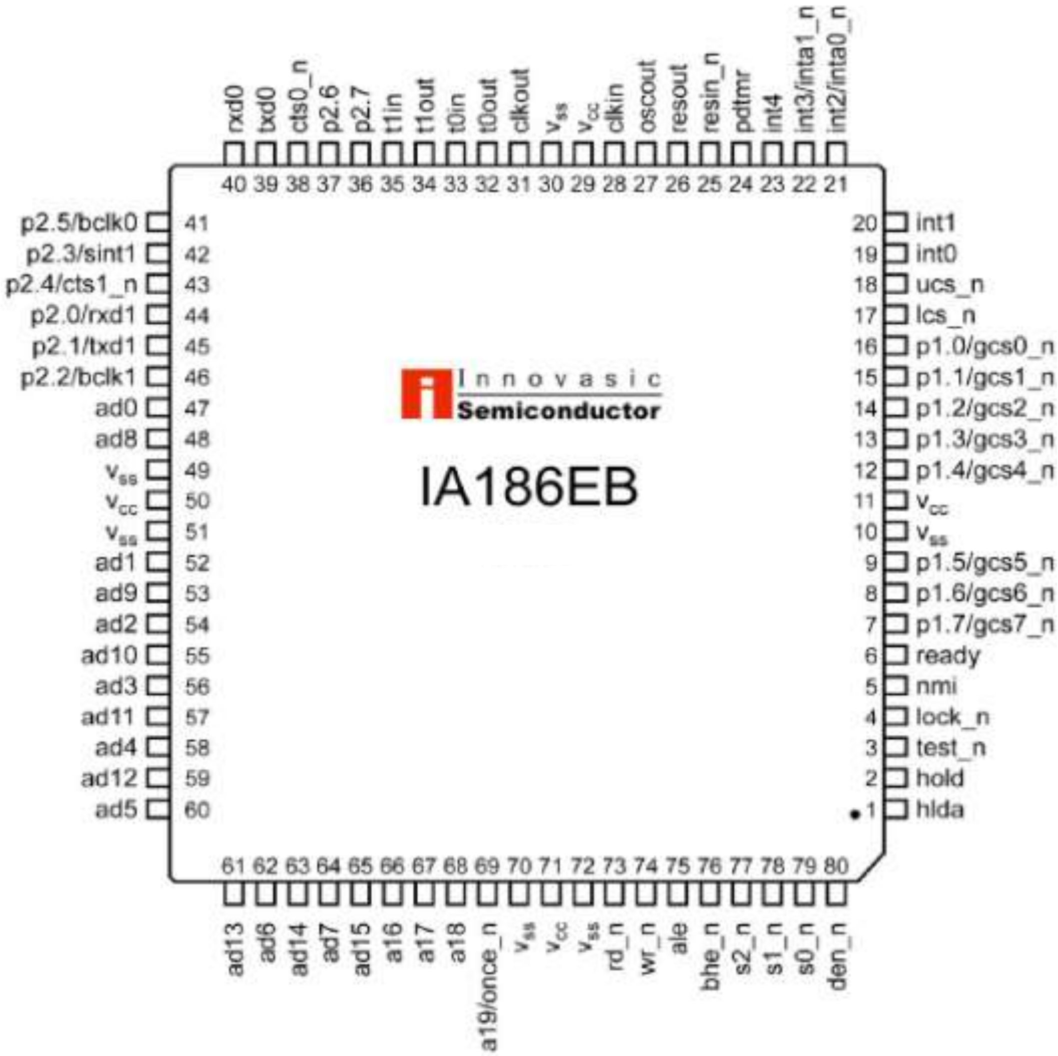


Figure 7. IA186EB 80-Pin LQFP Package Diagram

Table 5. IA186EB 80-Pin LQFP Pin Listing

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	hlda	21	int2/inta0_n	41	p2.5/bclk0	61	ad13
2	hold	22	int3/inta1_n	42	p2.3/sint1	62	ad6
3	test_n	23	int4	43	p2.4/cts1_n	63	ad14
4	lock_n	24	pdtmr	44	p2.0/rxd1	64	ad7
5	nmi	25	resin_n	45	p2.1/txd1	65	ad15
6	ready	26	resout	46	p2.2/bclk1	66	a16
7	p1.7/gcs7_n	27	oscout	47	ad0	67	a17
8	p1.6/gcs6_n	28	clkin	48	ad8	68	a18
9	p1.5/gcs5_n	29	V_{cc}	49	V_{ss}	69	a19/once_n
10	V_{ss}	30	V_{ss}	50	V_{cc}	70	V_{ss}
11	V_{cc}	31	clkout	51	V_{ss}	71	V_{cc}
12	p1.4/gcs4_n	32	t0out	52	ad1	72	V_{ss}
13	p1.3/gcs3_n	33	t0in	53	ad9	73	rd_n
14	p1.2/gcs2_n	34	t1out	54	ad2	74	wr_n
15	p1.1/gcs1_n	35	t1in	55	ad10	75	ale
16	p1.0/gcs0_n	36	p2.7	56	ad3	76	bhe_n
17	lcs_n	37	p2.6	57	ad11	77	s2_n
18	ucs_n	38	cts0_n	58	ad4	78	s1_n
19	int0	39	txd0	59	ad12	79	s0_n
20	int1	40	rxd0	60	ad5	80	den_n

2.1.8 IA188EB 80 LQFP Package

The pinout for the IA188EB 80 LQFP Package is as shown in Figure 8. The corresponding pinout is provided in Table 6.

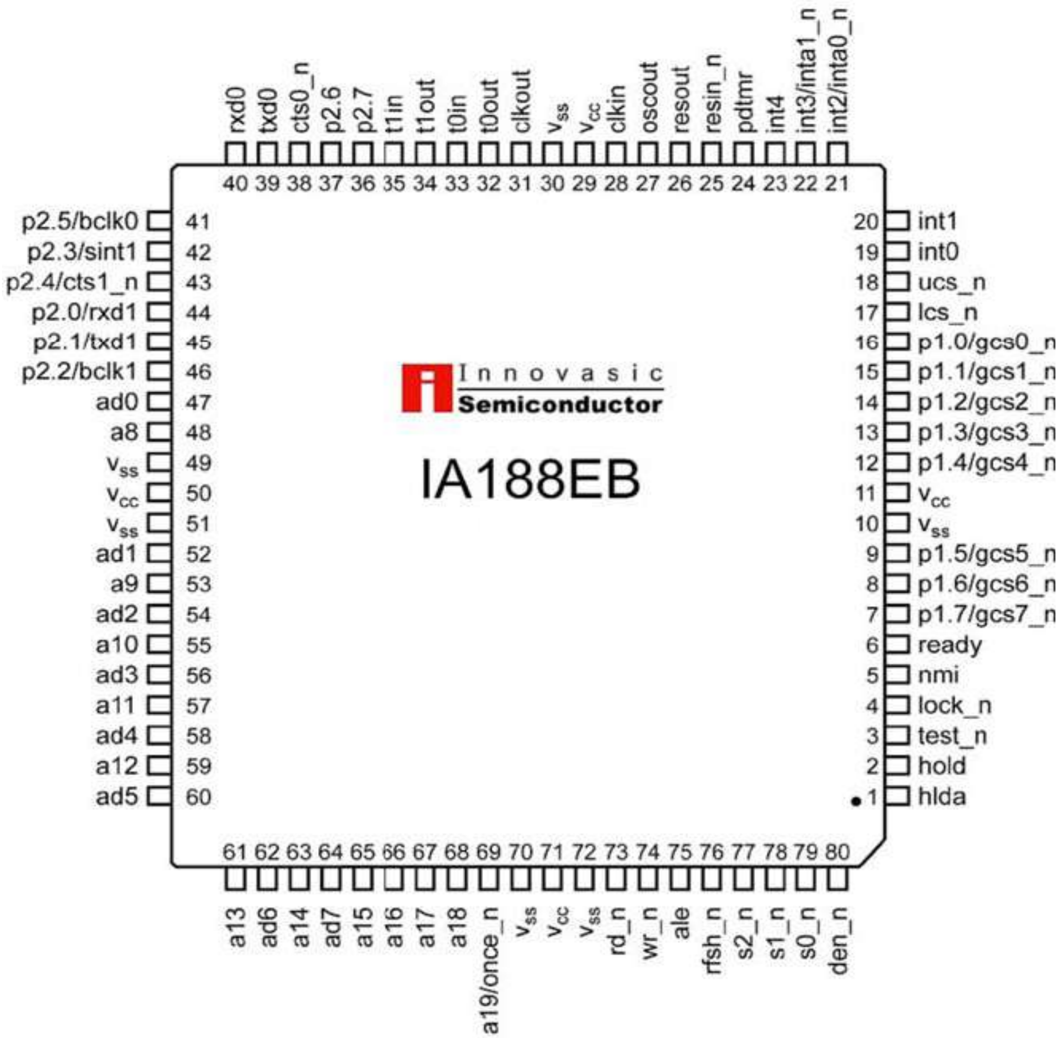


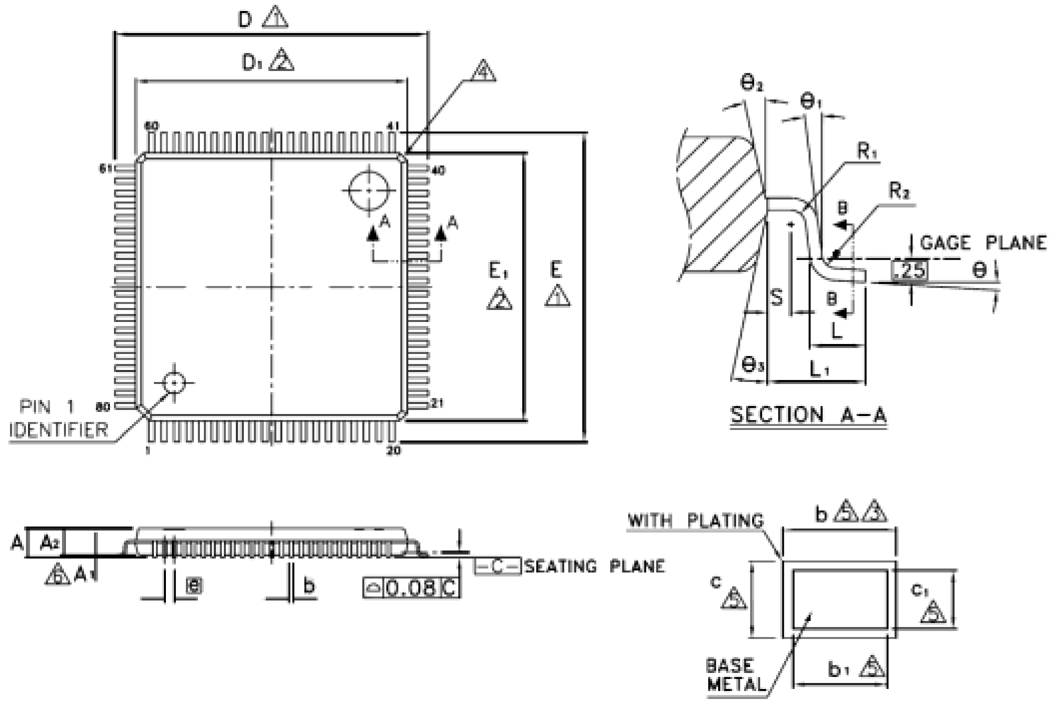
Figure 8. IA188EB 80-Pin LQFP Package Diagram

Table 6. IA188EB 80-Pin LQFP Pin Listing

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	hlda	21	int2/inta0_n	41	p2.5/bclk0	61	ad13
2	hold	22	int3/inta1_n	42	p2.3/sint1	62	ad6
3	test_n	23	int4	43	p2.4/cts1_n	63	ad14
4	lock_n	24	pdtmr	44	p2.0/rxd1	64	ad7
5	nmi	25	resin_n	45	p2.1/txd1	65	ad15
6	ready	26	resout	46	p2.2/bclk1	66	a16
7	p1.7/gcs7_n	27	oscout	47	ad0	67	a17
8	p1.6/gcs6_n	28	clkin	48	ad8	68	a18
9	p1.5/gcs5_n	29	V_{cc}	49	V_{ss}	69	a19/once_n
10	V_{ss}	30	V_{ss}	50	V_{cc}	70	V_{ss}
11	V_{cc}	31	clkout	51	V_{ss}	71	V_{cc}
12	p1.4/gcs4_n	32	t0out	52	ad1	72	V_{ss}
13	p1.3/gcs3_n	33	t0in	53	ad9	73	rd_n
14	p1.2/gcs2_n	34	t1out	54	ad2	74	wr_n
15	p1.1/gcs1_n	35	t1in	55	ad10	75	ale
16	p1.0/gcs0_n	36	p2.7	56	ad3	76	bhe_n
17	lcs_n	37	p2.6	57	ad11	77	s2_n
18	ucs_n	38	cts0_n	58	ad4	78	s1_n
19	int0	39	txd0	59	ad12	79	s0_n
20	int1	40	rxd0	60	ad5	80	den_n

2.1.9 LQFP Physical Dimensions

The physical dimensions for the 80 LQFP are as shown in Figure 9.



Legend:

Symbol	Dimension in mm Min	Nom	Max	Dimension in Inch Min	Mom	Max
A	–	–	1.60	–	–	0.063
A_1	0.05	–	0.15	0.002	–	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	–	0.20	0.004	–	0.008
c_1	0.09	–	0.16	0.004	–	0.006
D		14.00 BSC			0.551 BSC	
D_1		12.00 BSC			0.472 BSC	
E		14.00 BSC			0.551 BSC	
E_1		12.00 BSC			0.472 BSC	
e		0.50 BSC			0.020 BSC	
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1		1.00 REF			0.039 REF	
R_1	0.08	–	–	0.003	–	–
R_2	0.08	–	0.20	0.003	–	0.008
S	0.20	–	–	0.008	–	–
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°

1. To be determined at seating plane C.
2. Dimensions D1 and E1 do not include mold protrusion. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Dimension b does not include dambar protrusion. Dambar cannot be located on the lower radius of the foot.
4. Exact shape of each corner is optional.
5. These dimensions apply to the flat section of the lead between 0.10 and 0.25mm from the lead tip.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.

Notes:
1. Exact shape of each corner is optional.
2. Controlling dimension: mm.

Figure 9. 80-Pin LQFP Physical Package Dimensions

2.2 IA186EB Pin/Signal Descriptions

Descriptions of the pin and signal functions for the IA186EB microcontroller are provided in Table 7.

Several of the IA186EB pins have different functions depending on the operating mode of the device. Each of the different signals supported by a pin is listed and defined in Table 7—indexed alphabetically in the first column of the table. Additionally, the name of the pin associated with the signal as well as the pin numbers for the PLCC, LQFP, and PQFP packages are provided in the "Pin" column. If the signal and pin names are the same, a dash is provided in the "Pin-Name" column. Signals not used in a specific package type are designated "NA."

Table 7. IA186EB Pin/Signal Descriptions

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
a16	a16	80	66	29	**a**ddress Bits [**16–19**]. Input/Output. These pins provide the four most-significant bits of the Address Bus. During the address portion of the IA186EB bus cycle, Address Bits [16–19] are presented on the bus and can be latched using the ale signal (see table entry). During the data portion of the IA186EB bus cycle, these lines are driven to a logic 0.
a17	a17	81	67	30	
a18	a18	82	68	31	
a19	**a19**/once_n	83	69	32	
ad0	ad0	61	47	10	**a**ddress/**d**ata Bits [**0–15**]. Input/Output. These pins provide the multiplexed Address Bus and Data Bus. During the address portion of the IA186EB bus cycle, Address Bits [0–15] are presented on the bus and can be latched using the ale signal (see next table entry). During the data portion of the IA186EB bus cycle, 8- or 16-bit data are present on these lines.
ad1	ad1	66	52	15	
ad2	ad2	68	54	17	
ad3	ad3	70	56	19	
ad4	ad4	72	58	21	
ad5	ad5	74	60	23	
ad6	ad6	76	62	25	
ad7	ad7	78	64	27	
ad8	ad8	62	48	11	
ad9	ad9	67	53	16	
ad10	ad10	69	55	18	
ad11	ad11	71	57	20	
ad12	ad12	73	59	22	
ad13	ad13	75	61	24	
ad14	ad14	77	63	26	
ad15	ad15	79	65	28	

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
ale	ale	6	75	38	**a**ddress **l**atch **e**nable. Output. Active High. This signal is used to latch the address information during the address portion of a bus cycle.
bclk0	p2.5/**bclk0**	54	41	4	**b**aud **cl**oc**k**, Serial Port **0**. Input. The **bclk0** pin can be used to provide an alternate clock source for Serial Port 0. The input clock rate cannot be greater than one-half the operating frequency of the IA186EB.
bclk1	p2.2/**bclk1**	59	46	9	**b**aud **cl**oc**k**, Serial Port **1**. Input. The **bclk1** pin can be used to provide an alternate clock source for Serial Port 1. The input clock rate cannot be greater than one-half the operating frequency of the IA186EB.
bhe_n bhe_n is multi-plexed with refresh_n	bhe_n bhe_n is multi-plexed with refresh_n	7	76	39	**b**yte **h**igh **e**nable. Output. Active Low. When **bhe_n** is asserted (low), it indicates that the bus cycle in progress is transferring data over the upper half of the data bus. Additionally, **bhe_n** and **ad0** encode the following bus information: ad0 / bhe_n / Bus Status 0 / 0 / Word Transfer 0 / 1 / Even Byte Transfer 1 / 0 / Odd Byte Transfer 1 / 1 / Refresh Operation Note: bhe_n is multiplexed with refresh_n.
busy	test_n/**busy**	14	3	46	**busy**. Input. Active High. When the **busy** input is asserted, it causes the IA186EB to suspend operation during the execution of the Intel 80C187 Numerics Coprocessor instructions. Operation resumes when the pin is sampled low.

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
clkin	clkin	41	28	71	**cl**ock **in**put. Input. The **clkin** pin is the input connection for an external clock. An external oscillator operating at two times the required processor operating frequency can be connected to this pin. If a crystal is used to supply the clock, it is connected between the **clkin** pin and the **oscout** pin (see oscout table entry). When a crystal is connected, it drives an internal Pierce oscillator to the IA186EB.
clkout	clkout	44	31	74	**cl**ock **out**put. Output. The **clkout** pin provides a timing reference for inputs and outputs of the IA186EB. This clock output is one-half the input clock (**clkin**) frequency. The **clkout** signal has a 50% duty cycle, transitioning every falling edge of **clkin**.
cts0_n	cts0_n	51	38	1	**c**lear **t**o **s**end, Serial Port **0**. Input. Active Low. When this input is high (i.e., not asserted), data transmission from Serial Port 0 is inhibited. When the signal is asserted (low), data transmission is permitted.
cts1_n	p2.4/**cts1_n**	56	43	6	**c**lear **t**o **s**end, Serial Port **1**. Input. Active Low. When this input is high (i.e., not asserted), data transmission from Serial Port 1 is inhibited. When the signal is asserted (low), data transmission is permitted.
den_n	den_n	11	80	43	**d**ata **e**nable. Output. Active Low. This signal is used to enable of bidirectional transceivers in a buffered system. The **den_n** signal is asserted (low) only when data are to be transferred on the bus.
dt/r_n	dt/r_n	16	NA	NA	**d**ata **t**ransmit/**r**eceive. Output. This signal is used to control the direction of data flow for bidirectional buffers in a buffered system. When **dt/r_n** is high, the direction indicated is transmit; when **dt/t_n** is low, the direction indicated is receive.
error_n	error_n	3	NA	NA	**error**. Input. Active Low. When this signal is asserted (low), it indicates that the last numerics coprocessor operation resulted in an exception condition.

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
gcs0_n	p1.0/**gcs0_n**	28	16	59	**g**eneric **c**hip **s**elect **n** (n = 0–7). Output. Active Low. When programmed and enabled, each of these pins provide a chip select signal that will be asserted (low) whenever the address of a memory or I/O bus cycle is within the address space programmed for that output.
gcs1_n	p1.1/**gcs1_n**	27	15	58	
gcs2_n	p1.2/**gcs2_n**	26	14	57	
gcs3_n	p1.3/**gcs3_n**	25	13	56	
gcs4_n	p1.4/**gcs4_n**	24	12	55	
gcs5_n	p1.5/**gcs5_n**	21	9	52	
gcs6_n	p1.6/**gcs6_n**	20	8	51	
gcs7_n	p1.7/**gcs7_n**	19	7	50	
hlda	hlda	12	1	44	**h**o**l**d **a**cknowledge. Output. Active High. When **hlda** is asserted (high), it indicates that the IA186EB has relinquished control of the local bus to another bus master in response to a HOLD request (see next table entry). When **hlda** is asserted, the IA186EB data bus and control signals are floated, allowing another bus master to drive the signals directly.
hold	hold	13	2	45	**hold**. Input. Active High. This signal is a request indicating that an external bus master wishes to gain control of the local bus. The IA186EB will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.
int0 (input)	int0 (input)	31	19	62	**interrupt n** (n = 04). Input/Output. Active High. These maskable inputs interrupt program flow and cause execution to continue at an interrupt vector of a specific interrupt type as follows: **int0**: Type 12 **int1**: Type 13 **int2**: Type 14 **int3**: Type 15 **int4**: Type 17 To allow interrupt expansion, **int0** and **int1** can be used with the interrupt acknowledge signals **inta0_n** and **inta1_n** (see next table entries) to serve as external interrupt inputs or interrupt acknowledge outputs.
int1 (input)	int1 (input)	32	20	63	
int2	**int2**/inta0_n	33	21	64	
int3	**int3**/inta1_n	34	22	65	
int4 (input)	int4 (input)	35	23	66	
inta0_n	int2/**inta0_n**	33	21	64	**int**errupt **a**cknowledge **0**. Input/Output. Active Low. This pin provides an interrupt acknowledge handshake in response to an interrupt request on the **int0** pin (see previous table entry).

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
inta1_n	int3/**inta1_n**	34	22	65	**int**errupt **a**cknowledge **1**. Input/Output. Active Low. This pin provides an interrupt acknowledge handshake in response to an interrupt request on the **int1** pin (see previous table entry).
lcs_n	lcs_n	29	17	60	**l**ower **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.
lock_n	lock_n	15	4	47	**lock**. Output. Active Low. When asserted (low), this signal indicates that the bus cycle in progress is cannot be interrupted. While **lock_n** is active, the IA186EB will not service bus requests such as HOLD. When **resin_n** is active, this pin is weakly held high and must not be driven low.
ncs_n	ncs_n	60	NA	NA	**n**umerics **c**oprocessor **s**elect. Output. Active Low. This signal is asserted (low) when the IA186EB accesses an Intel 80C187 Numerics Coprocessor.
nmi	nmi	17	5	48	**n**on-**m**askable **i**nterrupt. Input. Active High. When the **nmi** signal is asserted (high) it causes a Type 2 interrupt to be serviced by the IA186EB. Note: The assertion of **nmi** is latched internally by the IA186EB.
once_n	a19/**once_n**	83	69	32	**on**-**c**ircuit **e**mulation. Input. Active Low. Note: ONCE Mode is used for device testing. If the **once_n** pin is driven low during a reset operation, all IA186EB output and input/output pins are placed in a high-impedance state. This pin is weakly held high while **resin_n** is active.

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
oscout	oscout	40	27	70	**osc**illator **out**put. Output. The **oscout** pin is the output connection for an external crystal that drives the IA186EB internal Pierce oscillator. (When an external crystal is used, it is connected between this pin and the **clkin** pin. See **clkin** table entry.) Note: If an external oscillator or clock source is used to drive the IA186EB instead of a crystal, **oscout** must be left unconnected (i.e., must be floated). When the IA186EB is operating in the ONCE mode, **oscout** does not float.
p1.0	**p1.0**/gcs0_n	28	16	59	**p**ort **1**, Bit [N] (N = **0**–**7**). Output. Each pin of Port 1, **p1.0**–**p1.7**, can function individually as a general-purpose output line.
p1.1	**p1.1**/gcs1_n	27	15	58	
p1.2	**p1.2**/gcs2_n	26	14	57	
p1.3	**p1.3**/gcs3_n	25	13	56	
p1.4	**p1.4**/gcs4_n	24	12	55	
p1.5	**p1.5**/gcs5_n	21	9	52	
p1.6	**p1.6**/gcs6_n	20	8	51	
p1.7	**p1.7**/gcs7_n	19	7	50	
p2.0	**p2.0**/rxd1	57	44	7	**p**ort **2**, Bit [**0**]. Input. This pin functions as a general-purpose input line.
p2.1	**p2.1**/txd1	58	45	8	**p**ort **2**, Bit [**1**]. Output. This pin functions as a general-purpose output line.
p2.2	**p2.2**/bclk1	59	46	9	**p**ort **2**, Bit [**2**]. Input. This pin functions as a general-purpose input line.
p2.3	**p2.3**/sint1	55	42	5	**p**ort **2**, Bit [**3**]. Output. This pin functions as a general-purpose output line.
p2.4	**p2.4**/cts1_n	56	43	6	**p**ort **2**, Bit [**4**]. Input. This pin functions as a general-purpose input line.
p2.5	**p2.5**/bclk0	54	41	4	**p**ort **2**, Bit [**5**]. Input. This pin functions as a general-purpose input line.
p2.6	p2.6	50	37	80	**p**ort **2**, Bit [**6**]. Input/Output (open drain). This pin functions as a general-purpose bidirectional input/output line.
p2.7	p2.7	49	36	79	**p**ort **2**, Bit [**7**]. Input/Output (open drain). This pin functions as a general-purpose bidirectional input/output line.

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
pdtmr	pdtmr	36	24	67	**p**ower-**d**own **t**i**m**e**r**. Input/Output (push-pull). Note: The IA186EB enters Powerdown Mode when the PWRDN bit in the Power Control Register is set to 1 and a HALT instruction is executed. Exit from the Powerdown Mode occurs upon receipt of a non-maskable interrupt (i.e., assertion of the **nmi** input) or a reset (i.e., assertion of the **resin_n** input). The **pdtmr** pin, which is normally connected to an external capacitor, determines the amount of time that the IA186EB waits before resuming normal operation after an exit from the Powerdown when a non-maskable interrupt is received—essentially a delay between the assertion of the **nmi** input and the enabling of the IA186EB internal clocks. The delay required depends on the start-up characteristics of the crystal oscillator. The **pdtmr** pin does not apply when the Powerdown Mode is exited by the receipt of a reset (i.e., the assertion **resin_n**).
pereq	pereq	39	NA	NA	numerics co**p**rocessor **e**xternal **req**uest. Input. Active High. When asserted (high), this signal indicates that a data transfer between an Intel 80C187 Numerics Coprocessor.and memory is pending.
rd_n	rd_n	4	73	36	**r**ea**d**. Output. Active Low. When asserted (low), **rd_n** indicates that the accessed memory or I/O device must drive data from the location being accessed onto the data bus.
ready	ready	18	6	49	**ready**. Input. Active High. When asserted (high) the **ready** line indicates a bus-cycle completion. This signal must be active to terminate any bus cycle unless the IA186EB Chip-Select Unit is being used, in which case, **ready** is ignored.
resin_n	resin_n	37	25	68	**res**et **in**put. Input. Active Low. When **resin_n** is asserted (low), the IA186EB immediately terminates any bus cycle in progress and assumes an initialized state. All pins are driven to a known state, and **resout** (see next table entry) is asserted.

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

<table>
<tr><th rowspan="2">Signal</th><th colspan="4">Pin</th><th rowspan="2">Description</th></tr>
<tr><th>Name</th><th>PLCC</th><th>PQFP</th><th>LQFP</th></tr>
<tr><td>resout</td><td>resout</td><td>38</td><td>26</td><td>69</td><td>reset output. Output. Active High. When resout is asserted, it indicates that the IA186EB is being reset. The resout signal will remain active (high) as long as resin_n remains active (low).</td></tr>
<tr><td>rxd0</td><td>rxd0</td><td>53</td><td>40</td><td>3</td><td>Receive (rx) data, Serial Port 0. Input/Output. This pin is the serial data input for Serial Port 0. During synchronous serial communications, rxd0 is bidirectional and functions an output for data transmission (txd0 becomes the clock).</td></tr>
<tr><td>rxd1</td><td>p2.0/rxd1</td><td>57</td><td>44</td><td>7</td><td>Receive (rx) data, Serial Port 1. Input/Output. This pin is the serial data input for Serial Port 1. During synchronous serial communications, rxd0 is bidirectional and functions an output for data transmission (txd0 becomes the clock).</td></tr>
<tr><td>s0_n</td><td>s0_n</td><td>10</td><td>79</td><td>42</td><td rowspan="3">status (n = 0–2). Output. During a bus cycle the status (i.e., type) of cycle is encoded on these lines as follows:

s2_n s1_n s0_n Bus Cycle Status
0 0 0 Interrupt Acknowledge
0 0 1 Read I/O
0 1 0 Write I/O
0 1 1 Processor HALT
1 0 0 Queue Instruction Fetch
1 0 1 Read Memory
1 1 0 Write Memory
1 1 1 No Bus Activity</td></tr>
<tr><td>s1_n</td><td>s1_n</td><td>9</td><td>78</td><td>41</td></tr>
<tr><td>s2_n</td><td>s2_n</td><td>8</td><td>77</td><td>40</td></tr>
<tr><td>sint1</td><td>p2.3/sint1</td><td>55</td><td>42</td><td>5</td><td>serial interrupt, Serial Port 1. Output. Active High. When sint1 is asserted (high), it indicates that Serial Port 1 requires service.</td></tr>
<tr><td>t0in</td><td>t0in</td><td>46</td><td>33</td><td>76</td><td>timer 0 input. Input. Depending on the Timer Mode programmed for Timer 0, this input is used either as clock input or a control signal.</td></tr>
<tr><td>t0out</td><td>t0out</td><td>45</td><td>32</td><td>75</td><td>timer 0 output. Output. Depending on the Timer Mode programmed for Timer 0, this output can provide a single clock or a continuous waveform.</td></tr>
<tr><td>t1in</td><td>t1in</td><td>48</td><td>35</td><td>78</td><td>timer 1 input. Input. Depending on the Timer Mode programmed for Timer 1, this input is used either as clock input or a control signal.</td></tr>
</table>

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
t1out	t1out	47	34	77	**t**imer **1 out**put. Output. Depending on the Timer Mode programmed for Timer 1, this output can provide a single clock or a continuous waveform.
test_n	**test_n**/busy	14	3	46	**test**. Input. Active Low. When the **test_n** input is high (i.e., not asserted), it causes the IA186EB to suspend operation during the execution of the WAIT instruction. Operation resumes when the pin is sampled low (asserted).
txd0	txd0	52	39	2	Transmit (**tx**) **d**ata, Serial Port **0**. Output. This pin is the serial data output for Serial Port 0. During synchronous serial communications, **txd0** becomes the transmit clock (**rxd0** functions as an output for data transmission).
txd1	p2.1/**txd1**	58	45	8	Transmit (**tx**) **d**ata, Serial Port **1**. Output. This pin is the serial data output for Serial Port 1. During synchronous serial communications, **txd0** becomes the transmit clock (**rxd1** functions as an output for data transmission).
ucs_n	ucs_n	30	18	61	**u**pper **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.
v_{cc}	v_{cc}	1, 23, 42, 64	11, 29, 50, 71	13, 34, 54, 72	Power (**v_{cc}**). This pin provides power for the IA186EB device. It must be connected to a +5V DC power source.
v_{ss}	v_{ss}	2, 22, 43, 63, 65, 84	10, 30, 49, 51, 70, 72	12, 14, 33, 35, 53, 73	Ground (**v_{ss}**). This pin provides the digital ground (0V) for the IA186EB. It must be connected to a v_{ss} board plane.
wr_n	wr_n	5	74	37	**wr**ite. Output. Active Low. When asserted (low), **wr_n** indicates that data available on the data bus are to be latched into the accessed memory or I/O device.

2.3 IA188EB Pin/Signal Descriptions

Descriptions of the pin and signal functions for the IA188EB microcontroller are provided in Table 8.

Several of the IA188EB pins have different functions depending on the operating mode of the device. Each of the different signals supported by a pin is listed and defined in Table 8—indexed alphabetically in the first column of the table. Additionally, the name of the pin associated with the signal as well as the pin numbers for the PLCC, LQFP, and LQFP packages are provided in the "Pin" column. If the signal and pin names are the same, no entry is provided in the "Pin-Name" column.

Table 8. IA188EB Pin/Signal Descriptions

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
a8	a8	62	48	11	**a**ddress Bits [**819**]. Input/Output. These pins provide the 12 most-significant bits of the Address Bus. During the entire IA188EB bus cycle, Address Bits [8–19] are presented on the bus and can be latched using the **ale** signal (see table entry).
a9	a9	67	53	16	
a10	a10	69	55	18	
a11	a11	71	57	20	
a12	a12	73	59	22	
a13	a13	75	61	24	
a14	a14	77	63	26	
a15	a15	79	65	28	
a16	a16	80	66	29	
a17	a17	81	67	30	
a18	a18	82	68	31	
a19	**a19**/once_n	83	69	32	
ad0	ad0	61	47	10	**a**ddress/**d**ata Bits [**0**–**7**]. Input/Output. These pins provide a multiplexed Address Bus and Data Bus. During the address portion of the IA188EB bus cycle, Address Bits [0–7] are presented on the bus and can be latched using the **ale** signal (see next table entry). During the data portion of the IA188EB bus cycle, 8-bit data are present on these lines.
ad1	ad1	66	52	15	
ad2	ad2	68	54	17	
ad3	ad3	70	56	19	
ad4	ad4	72	58	21	
ad5	ad5	74	60	23	
ad6	ad6	76	62	25	
ad7	ad7	78	64	27	
ale	ale	6	75	38	**a**ddress **l**atch **e**nable. Output. Active High. This signal is used to latch the address information during the address portion of a bus cycle.
bclk0	p2.5/**bclk0**	54	41	4	**b**aud **cl**oc**k**, Serial Port **0**. Input. The **bclk0** pin can be used to provide an alternate clock source for Serial Port 0. The input clock rate cannot be greater than one-half the operating frequency of the IA188EB.

Table 8. IA188EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
bclk1	p2.2/**bclk1**	59	46	9	**b**aud **cl**oc**k**, Serial Port **1**. Input. The **bclk1** pin can be used to provide an alternate clock source for Serial Port 1. The input clock rate cannot be greater than one-half the operating frequency of the IA188EB.
clkin	clkin	41	28	71	**cl**ock **in**put. Input. The **clkin** pin is the input connection for an external clock. An external oscillator, operating at two times the required processor operating frequency, can be connected to this pin. If a crystal is used to supply the clock, it is connected between the **clkin** pin and the **oscout** pin (see **oscout** table entry). When a crystal is connected, it drives an internal Pierce oscillator to the IA188EB.
clkout	clkout	44	31	74	**cl**oc**k out**put. Output. The **clkout** pin provides a timing reference for inputs and outputs of the IA188EB. This clock output is one-half the input clock (**clkin**) frequency. The **clkout** signal has a 50% duty cycle, transitioning every falling edge of **clkin**.
cts0_n	cts0_n	51	38	1	**c**lear **t**o **s**end, Serial Port **0**. Input. Active Low. When this input is high (i.e., not asserted), data transmission from Serial Port 0 is inhibited. When the signal is asserted (low), data transmission is permitted.
cts1_n	p2.4/**cts1_n**	56	43	6	**c**lear **t**o **s**end, Serial Port **1**. Input. Active Low. When this input is high (i.e., not asserted), data transmission from Serial Port 1 is inhibited. When the signal is asserted (low), data transmission is permitted.
den_n	den_n	11	80	43	**d**ata **en**able. Output. Active Low. This signal is used to enable of bidirectional transceivers in a buffered system. The **den_n** signal is asserted (low) only when data are to be transferred on the bus.
dt/r_n	dt/r_n	16	NA	NA	**d**ata **t**ransmit**/r**eceive. Output. This signal is used to control the direction of data flow for bidirectional buffers in a buffered system. When **dt/r_n** is high, the direction indicated is transmit; when **dt/t_n** is low, the direction indicated is receive.

Table 8. IA188EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
gcs0_n	p1.0/**gcs0_n**	28	16	59	**g**eneric **c**hip **s**elect **n** (n = 0–7). Output. Active Low. When programmed and enabled, each of these pins provide a chip select signal that will be asserted (low) whenever the address of a memory or I/O bus cycle is within the address space programmed for that output.
gcs1_n	p1.1/**gcs1_n**	27	15	58	
gcs2_n	p1.2/**gcs2_n**	26	14	57	
gcs3_n	p1.3/**gcs3_n**	25	13	56	
gcs4_n	p1.4/**gcs4_n**	24	12	55	
gcs5_n	p1.5/**gcs5_n**	21	9	52	
gcs6_n	p1.6/**gcs6_n**	20	8	51	
gcs7_n	p1.7/**gcs7_n**	19	7	50	
hlda	hlda	12	1	44	**h**o**l**d **a**cknowledge. Output. Active High. When **hlda** is asserted (high), it indicates that the IA188EB has relinquished control of the local bus to another bus master in response to a HOLD request (see next table entry). When **hlda** is asserted, the IA188EB data bus and control signals are floated, allowing another bus master to drive the signals directly.
hold (input)	hold (input)	13	2	45	**hold**. Input. Active High. This signal is a request indicating that an external bus master wishes to gain control of the local bus. The IA188EB will relinquish control of the local bus between instruction boundaries not conditioned by a lock prefix.
int0 (input)	int0 (input)	31	19	62	**int**errupt N (N = **0**–**4**). Input/Output. Active High. These maskable inputs interrupt program flow and cause execution to continue at an interrupt vector of a specific interrupt type as follows: **int0**: Type 12 **int1**: Type 13 **int2**: Type 14 **int3**: Type 15 **int4**: Type 17 To allow interrupt expansion, **int0** and **int1** can be used with the interrupt acknowledge signals **inta0_n** and **inta1_n** (see next table entries) to serve as external interrupt inputs or interrupt acknowledge outputs.
int1 (input)	int1 (input)	32	20	63	
int2	**int2**/inta0_n	33	21	64	
int3	**int3**/inta1_n	34	22	65	
int4 (input)	int4 (input)	35	23	66	
inta0_n	int2/**inta0_n**	33	21	64	**int**errupt **a**cknowledge **0**. Output. Active Low. This pin provides an interrupt acknowledge handshake in response to an interrupt request on the **int0** pin (see previous table entry).

Table 8. IA188EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
inta1_n	int3/**inta1_n**	34	22	65	**int**errupt **a**cknowledge **1**. Input/Output. Active Low. This pin provides an interrupt acknowledge handshake in response to an interrupt request on the **int1** pin (see previous table entry).
lcs_n	lcs_n	29	17	60	**l**ower **c**hip **s**elect. Input/Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.
lock_n	lock_n	15	4	47	**lock**. Output. Active Low. When asserted (low), this signal indicates that the bus cycle in progress is cannot be interrupted. While **lock_n** is active, the IA188EB will not service bus requests such as HOLD. When **resin_n** is active, this pin is weakly held high and must not be driven low.
nmi	nmi	17	5	48	**n**on-**m**askable **i**nterrupt. Input. Active High. When the **nmi** signal is asserted (high), it causes a Type 2 interrupt to be serviced by the IA188EB. Note: The assertion of **nmi** is latched internally by the IA188EB.
once_n	a19/**once_n**	83	69	32	**on**-**c**ircuit **e**mulation. Input. Active Low. Note: ONCE Mode is used for device testing. If the **once_n** pin is driven low during a reset operation, all IA188EB output and input/output pins are placed in a high-impedance state. This pin is weakly held high while **resin_n** is active.
oscout	oscout	40	27	70	**osc**illator **out**put. Output. The **oscout** pin is the output connection for an external crystal that drives the IA188EB internal Pierce oscillator. (When an external crystal is used, it is connected between this pin and the **clkin** pin—see **clkin** table entry.) Note: If an external oscillator or clock source is used to drive the IA188EB instead of a crystal, **oscout** must be left unconnected (i.e., must be floated). When the IA188EB is operating in the ONCE mode, **oscout** does not float.

Table 8. IA188EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
p1.0	**p1.0**/gcs0_n	28	16	59	**p**ort **1**, Bit [N] (N = **0**–**7**). Output. Each pin of Port 1, **p1.0**–**p1.7**, can function individually as a general-purpose output line.
p1.1	**p1.1**/gcs1_n	27	15	58	
p1.2	**p1.2**/gcs2_n	26	14	57	
p1.3	**p1.3**/gcs3_n	25	13	56	
p1.4	**p1.4**/gcs4_n	24	12	55	
p1.5	**p1.5**/gcs5_n	21	9	52	
p1.6	**p1.6**/gcs6_n	20	8	51	
p1.7	**p1.7**/gcs7_n	19	7	50	
p2.0	**p2.0**/rxd1	57	44	7	**p**ort **2**, Bit [**0**]. Input. This pin functions as a general-purpose input line.
p2.1	**p2.1**/txd1	58	45	8	**p**ort **2**, Bit [**1**]. Output. This pin functions as a general-purpose output line.
p2.2	**p2.2**/bclk1	59	46	9	**p**ort **2**, Bit [**2**]. Input. This pin functions as a general-purpose input line.
p2.3	**p2.3**/sint1	55	42	5	**p**ort **2**, Bit [**3**]. Output. This pin functions as a general-purpose output line.
p2.4	**p2.4**/cts1_n	56	43	6	**p**ort **2**, Bit [**4**]. Input. This pin functions as a general-purpose input line.
p2.5	**p2.5**/bclk0	54	41	4	**p**ort **2**, Bit [**5**]. Input. This pin functions as a general-purpose input line.
p2.6	p2.6	50	37	80	**p**ort **2**, Bit [**6**]. Input/Output (open drain). This pin functions as a general-purpose bidirectional input/output line.
p2.7	p2.7	49	36	79	**p**ort **2**, Bit [**7**]. Input/Output (open drain). This pin functions as a general-purpose bidirectional input/output line.

Table 8. IA188EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
pdtmr	pdtmr	36	24	67	**P**ower-**d**own **tim**e**r**. Input/Output (push-pull). Note: The IA188EB enters Powerdown Mode when the PWRDN bit in the Power Control Register is set to 1 and a HALT instruction is executed. Exit from the Powerdown Mode occurs upon receipt of a non-maskable interrupt (i.e., assertion of the **nmi** input) or a reset (i.e., assertion of the **resin_n** input). The **pdtmr** pin, which is normally connected to an external capacitor, determines the amount of time that the IA188EB waits before resuming normal operation after an exit from the Powerdown when a non-maskable interrupt is received—essentially a delay between the assertion of the **nmi** input and the enabling of the IA188EB internal clocks. The delay required depends on the start-up characteristics of the crystal oscillator. The **pdtmr** pin does not apply when the Powerdown Mode is exited by the receipt of a reset (i.e., the assertion **resin_n**).
rd_n	rd_n	4	73	36	**r**ea**d**. Output. Active Low. When asserted (low), **rd_n** indicates that the accessed memory or I/O device must drive data from the location being accessed onto the data bus.
ready	ready	18	6	49	**ready**. Input. Active High. When asserted (high) the **ready** line indicates the completion of a bus cycle. This signal must be active to terminate any bus cycle unless the IA188EB Chip-Select Unit is being used, in which case, **ready** is ignored.
resin_n	resin_n	37	25	68	**res**et **in**put. Input. Active Low. When **resin_n** is asserted (low), the IA188EB immediately terminates any bus cycle in progress and assumes an initialized state. All pins are driven to a known state, and **resout** (see next table entry) is asserted.
resout	resout	38	26	69	**res**et **out**put. Output. Active High. When **resout** is asserted, it indicates that the IA188EB is being reset. The **resout** signal will remain active (high) as long as **resin_n** remains active (low).
rfsh_n	rfsh_n	7	76	39	**r**e**f**re**sh**. Output. Active Low. When **rfsh_n** is asserted (low), it indicates that a refresh cycle is in progress.

Table 8. IA188EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
rxd0	rxd0	53	40	3	Receive (**rx**) **d**ata, Serial Port **0**. Input/Output. This pin is the serial data input for Serial Port 0. During synchronous serial communications, **rxd0** is bidirectional and functions an output for data transmission (**txd0** becomes the clock).
rxd1	p2.0/**rxd1**	57	44	7	Receive (**rx**) **data**, Serial Port **1**. Input/Output. This pin is the serial data input for Serial Port 1. During synchronous serial communications, **rxd0** is bidirectional and functions an output for data transmission (**txd0** becomes the clock).
s0_n	s0_n	10	79	42	**s**tatus**N** (N = 0–2). Output. During a bus cycle the status (i.e., type) of cycle is encoded on these lines as follows: **s2_n** **s1_n** **s0_n** Bus Cycle Status 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Processor HALT 1 0 0 Queue Instruction Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 No Bus Activity
s1_n	s1_n	9	78	41	
s2_n	s2_n	8	77	40	
sint1	p2.3/**sint1**	55	42	5	**s**erial **int**errupt, Serial Port **1**. Output. Active High. When **sint1** is asserted (high), it indicates that Serial Port 1 requires service.
t0in	t0in	46	33	76	**t**imer **0 in**put. Input. Depending on the Timer Mode programmed for Timer 0, this input is used either as clock input or a control signal.
t0out	t0out	45	32	75	**t**imer **0 out**put. Output. Depending on the Timer Mode programmed for Timer 0, this output can provide a single clock or a continuous waveform.
t1in	t1in	48	35	78	**t**imer **1 in**put. Input. Depending on the Timer Mode programmed for Timer 1, this input is used either as clock input or a control signal.
t1out	t1out	47	34	77	**t**imer **1 out**put. Output. Depending on the Timer Mode programmed for Timer 1, this output can provide a single clock or a continuous waveform.

Table 8. IA188EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
test_n	test_n	14	3	46	**test**. Input. Active Low. When the **test_n** input is high (i.e., not asserted), it causes the IA188EB to suspend operation during the execution of the WAIT instruction. Operation resumes when the pin is sampled low (asserted).
txd0	txd0	52	39	2	Transmit (**tx**) **d**ata, Serial Port **0**. Output. This pin is the serial data output for Serial Port 0. During synchronous serial communications, **txd0** becomes the transmit clock (**rxd0** functions as an output for data transmission).
txd1	p2.1/txd1	58	45	8	Transmit (**tx**) **d**ata, Serial Port **1**. Output. This pin is the serial data output for Serial Port 1. During synchronous serial communications, **txd0** becomes the transmit clock (**rxd1** functions as an output for data transmission).
ucs_n	ucs_n	30	18	61	**u**pper **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.
v_{cc}	v_{cc}	1, 23, 42, 64	11, 29, 50, 71	13, 34, 54, 72	Power (**v_{cc}**). This pin provides power for the IA188EB device. It must be connected to a +5V DC power source.
v_{ss}	v_{ss}	2, 22, 43, 63, 65, 84	10, 30, 49, 51, 70, 72	12, 14, 33, 35, 53, 73	Ground (**v_{ss}**). This pin provides the digital ground (0V) for the IA188EB. It must be connected to a **v_{ss}** board plane.
wr_n	wr_n	5	74	37	**wr**ite. Output. Active Low. When asserted (low), **wr_n** indicates that data available on the data bus are to be latched into the accessed memory or I/O device.

3. Maximum Ratings, Thermal Characteristics, and DC Parameters

For the Innovasic Semiconductor IA186EB and IA188EB microcontrollers, the absolute maximum ratings, thermal characteristics, and DC parameters are provided in Tables 9 through 11, respectively.

Table 9. IA186EB and IA188EB Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65°C to +150°C
Case Temperature under Bias	−65°C to +120°C
Supply Voltage with Respect to v_{ss}	−0.5V to +6.5V
Voltage on Pins other than Supply with Respect to v_{ss}	−0.5V to +(Vcc + 0.5)V

Table 10. IA186EB and IA188EB Thermal Characteristics

Symbol	Characteristic	Value	Units
T_A	Ambient Temperature	-40°C to 85°C	°C
P_D	Power Dissipation	MHz × ICC × V/1000	W
Θ_{Ja}	84-Pin PLCC Package	30.7	°C/W
	80-Pin PQFP Package	46	
	80-Pin LQFP Package	52	
T_J	Average Junction Temperature	$T_A + (P_D \times \Theta_{Ja})$	°C

Table 11. IA186EB and IA188EB DC Parameters

Symbol	Parameter	Min	Max	Units	Notes
5.0V Operation V_{CC}	Supply Voltage	4.5	5.5	V	–
3.3V Operation V_{CC}	Supply Voltage	3.0	3.6	V	–
V_{IL}	Input Low Voltage	−0.5	0.3 V_{CC}	V	input hysteresis on resin_n = 0.50V
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} + 0.5	V	–
V_{OL}	Output Low Voltage Vcc = 5.5V or 3.6V	–	0.45	V	I_{OL} = 3 mA
V_{OH}	Output High Voltage Vcc = 5.5V or 3.6V	V_{CC} – 0.5	–	V	I_{OH} = −2 mA
I_{LEAK}	Input Leakage Current for Pins: ad15–ad0, ad7–ad0 (IA188EB), ready, hold, resin_n; clkin, test_n, nmi, int4–int0, t0in, t1in, rdx0, bclk0_n, cts0_n, rxd1, bclk1_n, cts1_n, p2.6, p2.7	–	± 15	µA	0V ≤ V_{IN} ≤ V_{CC}
	Input Leakage Current for Pins: error_n, pereq	± 0.275	± 7	mA	0V ≤ V_{IN} ≤ V_{CC}
	Input Leakage Current for Pins: a19/once_n, a18–a16, lock_n	− 0.275	−5.0	mA	V_{IN} =0.7 V_{CC}
I_{LO}	Output Leakage Current	–	± 15	µA	0.45 ≤ V_{OUT} ≤ V_{CC}
I_{CC}	Supply Current Cold (RESET) Vcc = 5.5V	–	4.6	mA/mHz	–
	Supply Current Cold (RESET) Vcc = 3.6V	–	2.2	mA/mHz	–
I_{ID}	Supply Current (IDLE)	–	91	mA	–
I_{PD}	Supply Current Powerdown		100	µA	–
C_{IN}	Input Pin Capacitance	0	15	pF	T_F = 1 MHz
C_{OUT}	Output Pin Capacitance	0	15	pF	T_F = 1 MHz
Operating temperature is -40°C to +85°C.					

4. Functional Description

4.1 Device Architecture

Architecturally, the IA186EB and IA188EB microcontrollers include the following functional modules:

- Bus Interface Unit
- Clock Generator
- Interrupt Control Unit
- Timer/Counter Unit
- Serial Communications Unit
- Chip-Select Unit
- I/O Port Unit
- Refresh Control Unit
- Power Management Unit

A functional block diagram of the IA186EB/IA188EB is shown in Figure 10. Descriptions of the functional modules are provided in the following subsections.

4.1.1 Bus Interface Unit

The IA186EB/IA188EB bus controller that generates local bus control signals and uses a hold/hlda protocol to share the local bus with other bus masters. The bus controller generates 20 address bits, read and write control signals, and bus-cycle status information. A ready input is used to extend a bus cycle beyond the minimum four clock cycles.

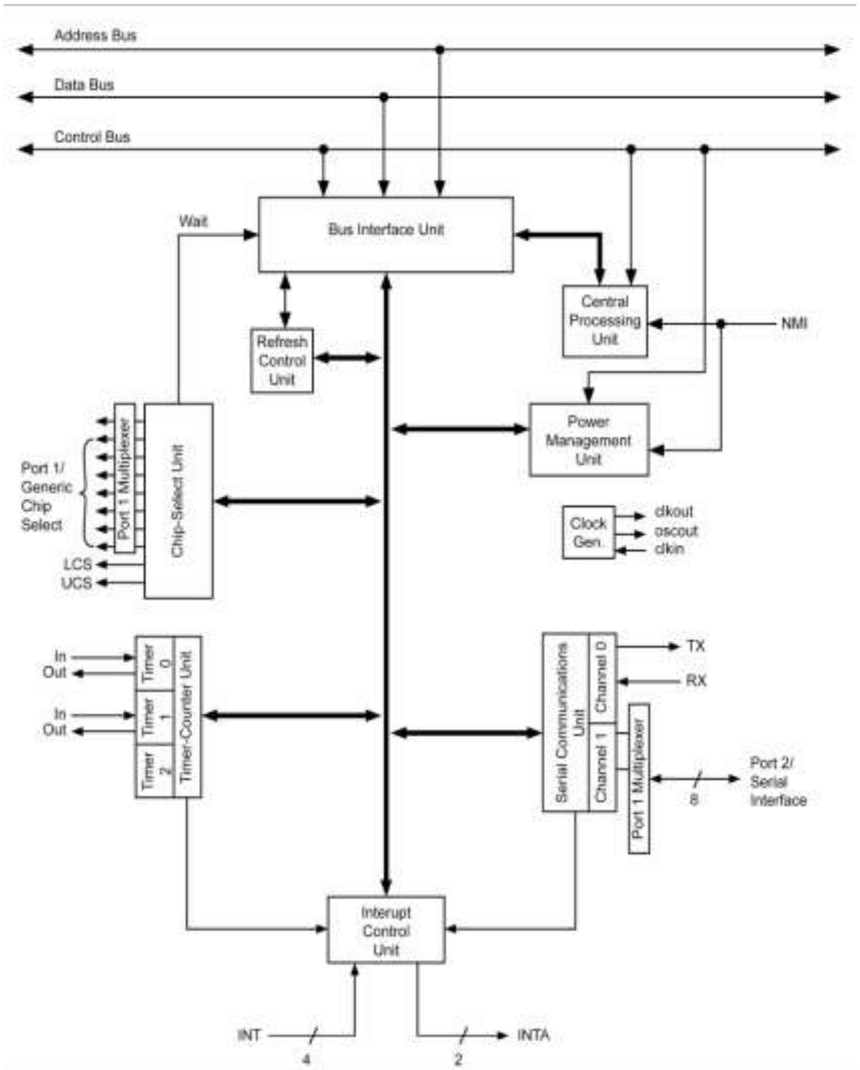


Figure 10. IA186EB/IA188EB Functional Block Diagram

4.1.2 Clock Generator

The IA186EB/IA188EB uses an on-chip clock generator to supply internal and external clocks. The clock generator makes use of a crystal oscillator and includes a divide-by-two counter.

Figure 11 shows the various operating modes of the clock circuit. The clock circuit can use either a parallel resonant fundamental mode crystal network (A) or a third-overtone mode crystal network (B), or it can be driven by an external clock source (C).

The following parameters are recommended when choosing a crystal:

- Temperature Range
  - Application Specific
  - ESR (Equivalent Series Resistance): 40Ω max
  - C0 (Shunt Capacitance of Crystal): 7.0 pF max
  - CL (Load Capacitance): 20 pF ± 2 pF
  - Drive Level: 1 mW max

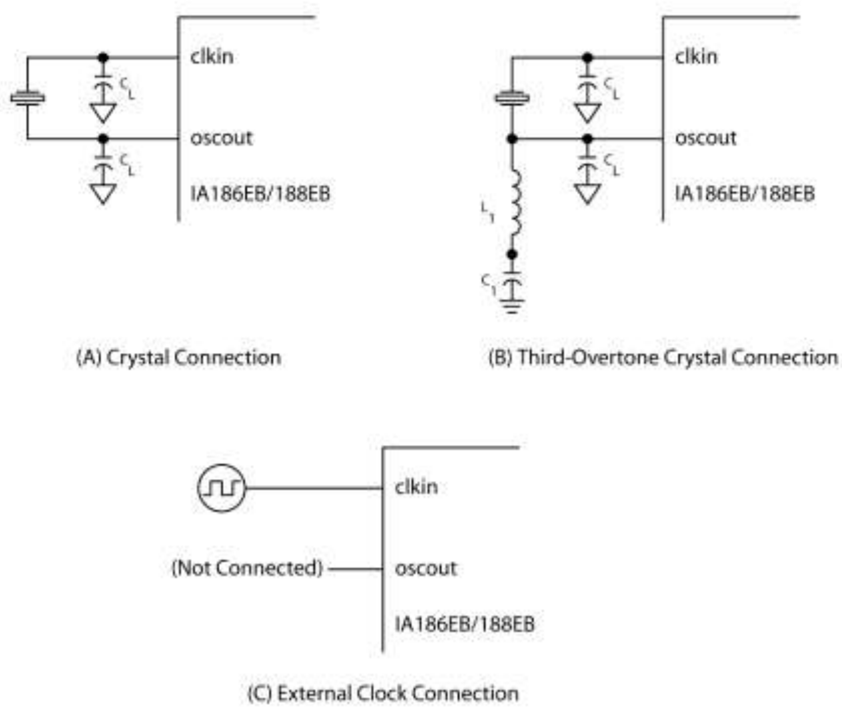


Figure 11. Clock Circuit Connection Options

4.1.3 Interrupt Control Unit

The IA186EB/IA188EB can receive interrupts from a number of sources, both internal and external. The interrupt control unit serves to merge these requests on a priority basis, for individual service by the CPU. Each interrupt source can be independently masked by the Interrupt Control Unit (ICU) or all interrupts can be globally masked by the CPU.

Internal interrupt sources include the Timers and Serial Channel 0. External interrupt sources come from the five input pins int0–int4. The NMI interrupt pin is not controlled by the ICU and is passed directly to the CPU. Although the Timer and Serial channel each have only one request input to the ICU, separate vector types are generated to service individual interrupts within the Timer and Serial channel units.

4.1.4 Timer/Counter Unit

The IA186EB/IA188EB Timer/Counter Unit (TCU) provides three 16-bit programmable timers. Two of these are highly flexible and are connected to external pins for control or clocking. A third timer is not connected to any external pins and can only be clocked internally. However, it can be used to clock the other two timer channels. The TCU can be used to count external events, time external events, generate non-repetitive waveforms, and generate timed interrupts, etc.

4.1.5 Serial Communications Unit

The Serial Control Unit (SCU) of the IA186EB/IA188EB contains two independent channels. Each channel is identical in operation except that only Channel 0 is supported by the integrated interrupt controller (Channel 1 has an external interrupt pin). Each channel has its own baud rate generator that is independent of the Timer/Counter Unit, and can be internally or externally clocked at up to one half the IA186EB/IA188EB operating frequency.

Independent baud rate generators are provided for each of the serial channels. For the asynchronous modes, the generator supplies an 8x baud clock to both the receive and transmit register logic. A 1x baud clock is provided in the synchronous mode.

4.1.6 Chip-Select Unit

The IA186EB/IA188EB Chip-Select Unit (CSU) integrates logic that provides up to ten programmable chip-selects to access both memories and peripherals. In addition, each chip select can be programmed to automatically insert additional clocks (wait-states) into the current bus cycle and automatically terminate a bus cycle independent of the condition of the ready input pin.

4.1.7 I/O Port Unit

The I/O Port Unit (IPU) on the IA186EB/IA188EB supports two 8-bit channels of input, output, or input/output operation. Port 1 is multiplexed with the chip select pins and is output only. Most of Port 2 is multiplexed with the serial channel pins. Port 2 pins are limited to either an output or input function, depending on the operation of the serial pin it is multiplexed with.

4.1.8 Refresh Control Unit

The Refresh Control Unit (RCU) automatically generates a periodic memory read bus cycle to keep dynamic or pseudo-static memory refreshed. A 9-bit counter controls the number of clocks between refresh requests.

A 12-bit address generator is maintained by the RCU and is presented on the a1–a12 address lines during the refresh bus cycle. Address Bits [a13–a19] are programmable to allow the refresh address block to be located on any 8-Kbyte boundary.

4.1.9 Power Management Unit

The IA186EB/IA188EB Power Management Unit (PMU) is provided to control the power consumption of the device. The PMU provides three power modes: Active, Idle, and Powerdown.

Active Mode indicates that all units on the IA186EB/IA188EB are functional and the device consumes maximum power (depending on the level of peripheral operation). Idle Mode freezes the clocks of the execution and bus units at a logic zero state (all peripherals continue to operate normally).

The Powerdown mode freezes all internal clocks at a logic zero level and disables the crystal oscillator. All internal registers hold their values provided V_{CC} is maintained. Current consumption is reduced to just transistor junction leakage.

4.2 Peripheral Architecture

The IA186EB/IA188EB has integrated several common system peripherals with a CPU core to create a compact, yet powerful system. The integrated peripherals are designed to be flexible and provide logical interconnections between supporting units (e.g., the interrupt control unit supports interrupt requests from the timer/counters or serial channels). The list of integrated peripherals includes:

- 7-Input Interrupt Control Unit
- 3-Channel Timer/Counter Unit
- 2-Channel Serial Communications Unit
- 10-Output Chip-Select Unit
- I/O Port Unit

- Refresh Control Unit
- Power Management Unit

The registers associated with each integrated peripheral are contained within a 128 × 16 register file called the Peripheral Control Block (PCB). The PCB can be located in either memory or I/O space on any 256-byte address boundary.

Table 12 provides a list of the registers associated with the PCB.

Table 12. Peripheral Control Block Registers

PCB Offset	Function	PCB Offset	Function	PCB Offset	Function	PCB Offset	Function
00H	Reserved	40H	Timer2 Count	80H	GCS0 Start	C0H	Reserved
02H	End Of Interrupt	42H	Timer2 Compare	82H	GCS0 Stop	C2H	Reserved
04H	Poll	44H	Reserved	84H	GCS1 Start	C4H	Reserved
06H	Poll Status	46H	Timer2 Control	86H	GCS1 Stop	C6H	Reserved
08H	Interrupt Mask	48H	Reserved	88H	GCS2 Start	C8H	Reserved
0AH	Priority Mask	4AH	Reserved	8AH	GCS2 Stop	CAH	Reserved
0CH	In-Service	4CH	Reserved	8CH	GCS3 Start	CCH	Reserved
0EH	Interrupt Request	4EH	Reserved	8EH	GCS3 Stop	CEH	Reserved
10H	Interrupt Status	50H	Port 1 Direction	90H	GCS4 Start	D0H	Reserved
12H	Timer Control	52H	Port 1 Pin	92H	GCS4 Stop	D2H	Reserved
14H	Serial Control	54H	Port 1 Control	94H	GCS5 Start	D4H	Reserved
16H	INT4 Control	56H	Port 1 Latch	96H	GCS5 Stop	D6H	Reserved
18H	INT0 Control	58H	Port 2 Direction	98H	GCS6 Start	D8H	Reserved
1AH	INT1 Control	5AH	Port 2 Pin	9AH	GCS6 Stop	DAH	Reserved
1CH	INT2 Control	5CH	Port 2 Control	9CH	GCS7 Start	DCH	Reserved
1EH	INT3 Control	5EH	Port 2 Latch	9EH	GCS7 Stop	DEH	Reserved

Table 12. Peripheral Control Block Registers *(Continued)*

PCB Offset	Function	PCB Offset	Function	PCB Offset	Function	PCB Offset	Function
20H	Reserved	60H	Serial0 Baud	A0H	LCS Start	E0H	Reserved
22H	Reserved	62H	Serial0 Count	A2H	LCS Stop	E2H	Reserved
PCB Offset	Function	PCB Offset	Function	PCB Offset	Function	PCB Offset	Function
24H	Reserved	64H	Serial0 Control	A4H	UCS Start	E4H	Reserved
26H	Reserved	66H	Serial0 Status	A6H	UCS Stop	E6H	Reserved
28H	Reserved	68H	Serial0 RBUF	A8H	Relocation	E8H	Reserved
2AH	Reserved	6AH	Serial0 TBUF	AAH	Reserved	EAH	Reserved
2CH	Reserved	6CH	Reserved	ACH	Reserved	ECH	Reserved
2EH	Reserved	6EH	Reserved	AEH	Reserved	EEH	Reserved
30H	Timer0 Count	70H	Serial1 Baud	B0H	Refresh Base	F0H	Reserved
32H	Timer0 Compare A	72H	Serial1 Count	B2H	Refresh Time	F2H	Reserved
34H	Timer0 Compare B	74H	Serial1 Control	B4H	Refresh Control	F4H	Reserved
36H	Timer0 Control	76H	Serial1 Status	B6H	Reserved	F6H	Reserved
38H	Timer1 Count	78H	Serial1 RBUF	B8H	Power Control	F8H	Reserved
3AH	Timer1 Compare A	7AH	Serial1 TBUF	BAH	Reserved	FAH	Reserved
3CH	Timer1 Compare B	7CH	Reserved	BCH	Step ID	FCH	Reserved
3EH	Timer1 Control	7EH	Reserved	BEH	Reserved	FEH	Reserved

4.3 Reference Documents

Additional information on the operation and programming of the 80C186EB/80C188EB can be found in the following Intel publications:

- 80C186EB/80C188EB and 80L186EB/80L188EB 16-Bit High-Integration Embedded Processors (272433-006)
- 80C186EB/80C188EB Microprocessor User's Manual (270830-00n)

5. AC Specifications

This chapter defines the AC specifications of the IA186EB/IA188EB. Input characteristics are provided in Figure 12 and Tables 13 and 14. Output characteristics are provided in Figure 13 and Tables 15 and 16. Relative timing characteristics are provided in Figure 14 and Table 17. Clock input and clock output timing characteristics are provided in Figure 18 and Tables 18 and 19. Additional timing information is provided in Chapter 7, Bus Timing, and Chapter 8, Instruction Execution Times.

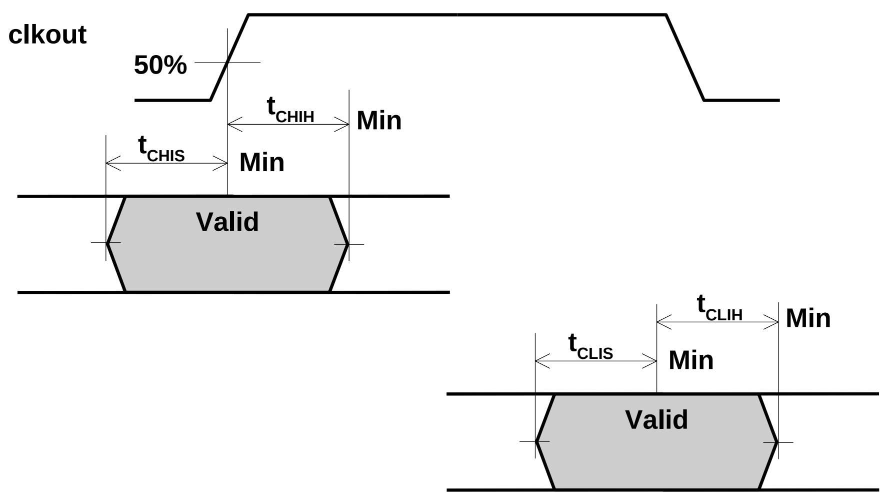


Figure 12. AC Input Characteristics

For specific 5.0- and 3.3-volt characteristics, refer to Tables 13 and 14, respectively.

Table 13. AC Input Characteristics for 5.0-Volt Operation

Symbol	Pins	Min	Max	Units
t_{CHIS}	test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n, p2.6, p2.7	10	–	ns
t_{CHIH}	test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n	3	–	ns
t_{CLIS}	ad15–ad0, ad7–ad0 (IA188EB), ready	10	–	ns
t_{CLIS}	hold, pereq, error_n	10	–	ns
t_{CLIH}	ad15–ad0, ad7–ad0 (IA188EB), ready	3	–	ns
t_{CLIH}	hold, pereq, error_n	3	–	ns

Table 14. AC Input Characteristics for 3.3-Volt Operation

Symbol	Pins	Min	Max	Units
t_{CHIS}	test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n, p2.6, p2.7	10	–	ns
t_{CHIH}	test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n	3	–	ns
t_{CLIS}	ad15–ad0, ad7–ad0 (IA188EB), ready	10	–	ns
t_{CLIS}	hold, pereq, error_n	10	–	ns
t_{CLIH}	ad15–ad0, ad7–ad0 (IA188EB), ready	3	–	ns
t_{CLIH}	hold, pereq, error_n	3	–	ns

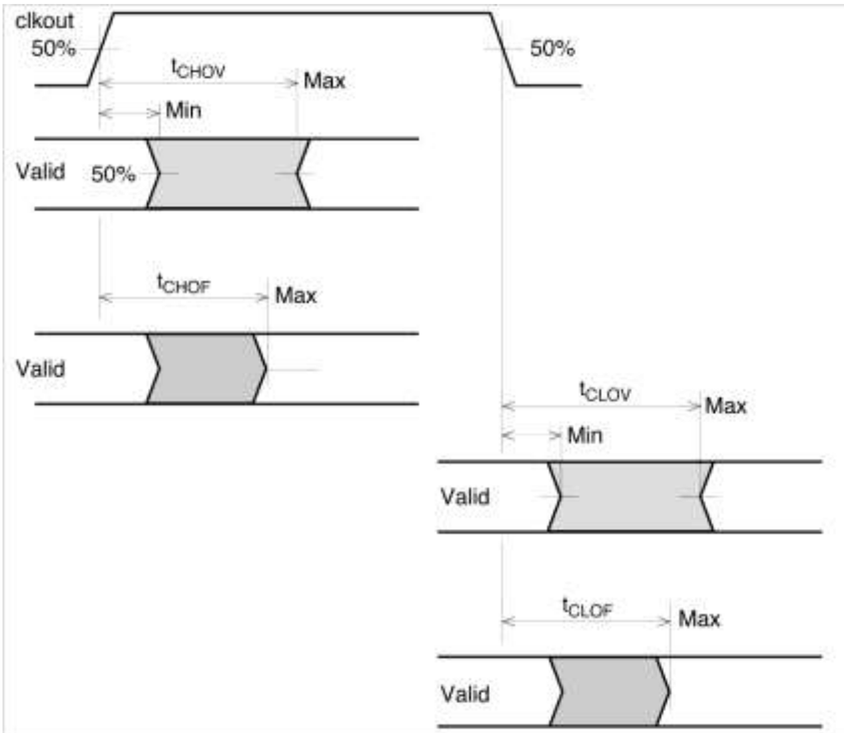


Figure 13. AC Output Characteristics

For specific 5.0- and 3.3-volt characteristics, refer to Tables 15 and 16, respectively.

Table 15. AC Output Characteristics for 5.0-Volt Operation

Symbol	Parameter	Min	Max	Units
t_{CHOV}	ale, s2–s0_n, den_n, dt/r_n, bhe_n, rfsh_n (IA188EB), lock_n, a19–a16	3	17	ns
	gcs0–gcs7_n, lcs_n, ucs_n, ncs_n, rd_n, wr_n	3	20	ns
t_{CLOV}	bhe_n, rfsh_n (IA188EB), den_n, lock_n, resout, hlda, t0out, t1out, a19–a16	3	17	ns
	rd_n , wr_n, gcs7–gcs0_n, lcs_n, ucs_n, ad15–ad0, ad7–ad0 (IA188EB), a15–a8 (IA188EB), ncs_n, inta1_n–inta0_n, s2_n–s0_n	3	20	ns
t_{CHOF}	re_n, wr_n, bhe_n, rfsh_n (IA188EB), dt/r_n, lock_n, s2_n–s0_n, a19–a16	0	20	ns
t_{CLOF}	den_n, ad15–ad0, ad7–ad0 (IA188EB), a15–a8 (IA188EB)	0	20	ns

Table 16. AC Output Characteristics for 3.3-Volt Operation

Symbol	Parameter	Min	Max	Units
t_{CHOV}	ale, s2–s0_n, den_n, dt/r_n, bhe_n, rfsh_n (IA188EB), lock_n, a19–a16	3	25	ns
	gcs0–gcs7_n, lcs_n, ucs_n, ncs_n, rd_n, wr_n	3	30	ns
t_{CLOV}	bhe_n, rfsh_n (IA188EB), den_n, lock_n, resout, hlda, t0out, t1out, a19–a16	3	25	ns
	rd_n , wr_n, gcs7–gcs0_n, lcs_n, ucs_n, ad15–ad0, ad7–ad0 (IA188EB), a15–a8 (IA188EB), ncs_n, inta1_n–inta0_n, s2_n–s0_n	3	30	ns
t_{CHOF}	re_n, wr_n, bhe_n, rfsh_n (IA188EB), dt/r_n, lock_n, s2_n–s0_n, a19–a16	0	30	ns
t_{CLOF}	den_n, ad15–ad0, ad7–ad0 (IA188EB), a15–a8 (IA188EB)	0	30	ns

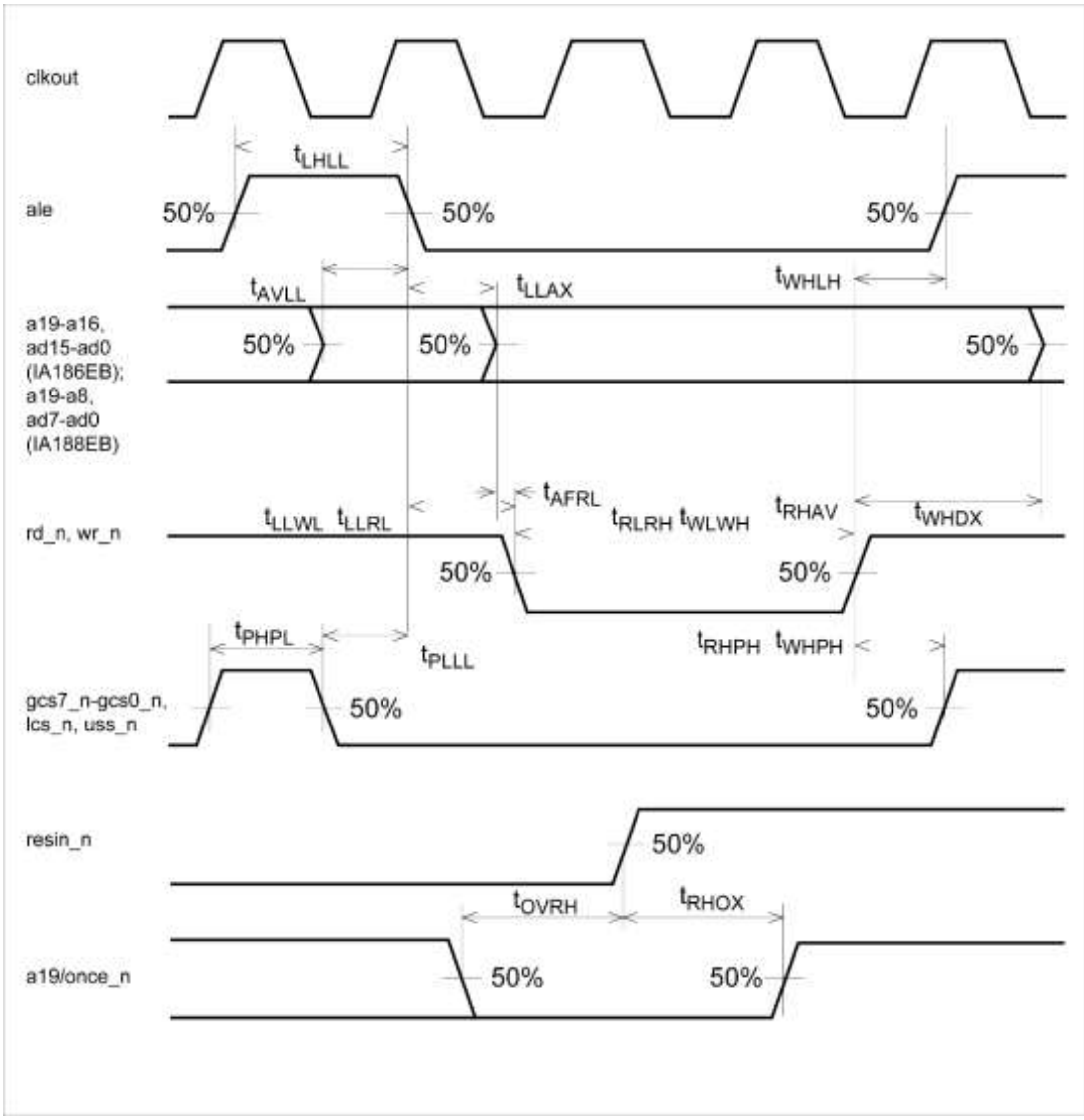


Figure 14. Relative Timing Characteristics

For specific relative timing characteristics, refer to Table 17.

Table 17. Relative Timing Characteristics

Symbol	Parameter	Min	Max	Units
t_{LHLL}	ale Rising to ale Falling	t – 15	–	ns
t_{AVLL}	Address Valid to ale Falling	½t –10	–	ns
t_{PLLL}	Chip Selects Valid to ale Falling	½t –10	–	ns
t_{LLAX}	Address Hold from ale Falling	½t –10	–	ns
t_{LLWL}	ale Falling to wr_n Falling	½t –15	–	ns
t_{LLRL}	ale Falling to rd_n Falling	½t –15	–	ns
t_{WHLH}	wr_n Rising to ale Rising	½t –10	–	ns
t_{AFRL}	Address Float to rd_n Falling	0	–	ns
t_{RLRH}	rd_n Falling to rd_n Rising	(2t) – 5	–	ns
t_{WLWH}	wr_n Falling to wr_n Rising	(2t) – 5	–	ns
t_{RHAV}	rd_n Rising to Address Active	t – 15	–	ns
t_{WHDX}	Output Data Hold after wr_n Rising	t – 15	–	ns
t_{WHPH}	wr_n Rising to Chip Select Rising	½t –10	–	ns
t_{RHPH}	rd_n Rising to Chip Select Rising	½t –10	–	ns
t_{PHPL}	cs_n inactive to cs_n active	½t –10	–	ns
t_{OVRH}	once_n Active to resin_n Rising	t	–	ns
t_{RHOX}	once_n Hold to resin_n Rising	t	–	Ns

5.1 AC Test Conditions

The AC specifications are tested with the 50-pF load shown in Figure 15. Specifications are measured at the $V_{CC}/2$ crossing point unless otherwise specified. The derating curves of Figures 16 and 17 show how timings vary with load capacitance.

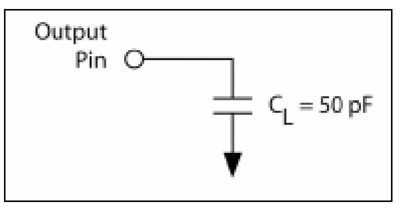


Figure 15. AC Test Load

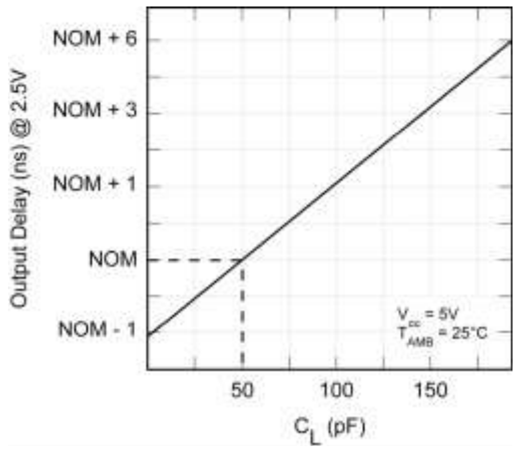


Figure 16. Typical Output Delay Variations Versus Load Capacitance

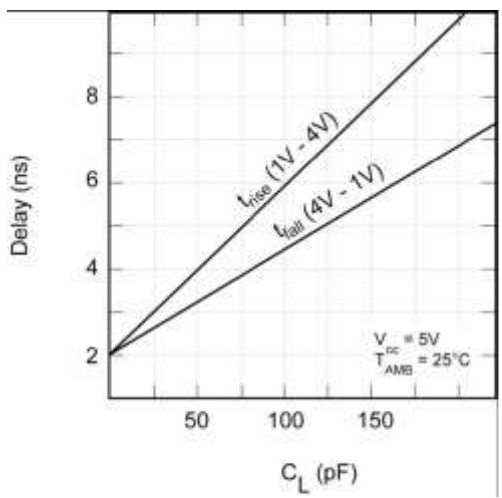


Figure 17. Typical Rise and Fall Variations Versus Load Capacitance

5.2 Clock Input and Clock Output Timing Characteristics

For clock input and clock output timing characteristics for both 5.0- and 3.3-volt operation, see Tables 18 and 19, respectively.

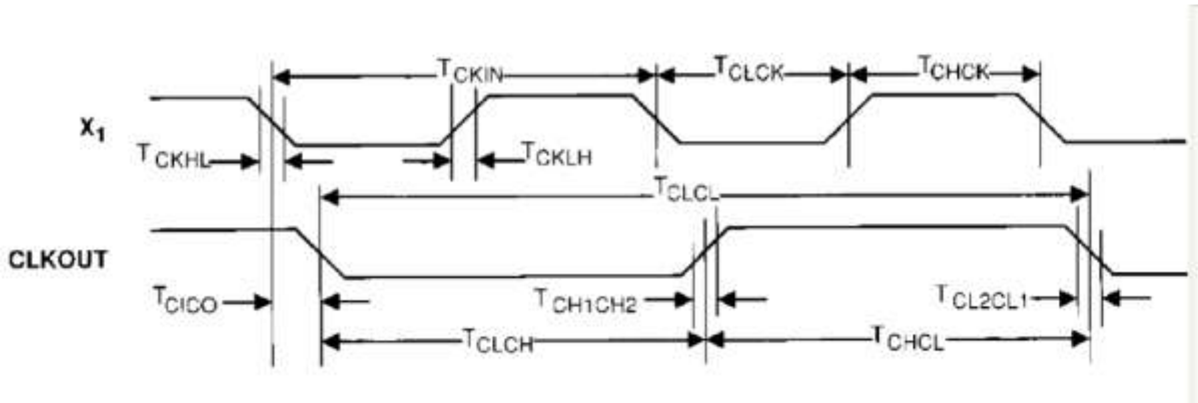


Figure 18. Clock Input and Clock Output Timing Characteristics

Table 18. Clock Input and Clock Output Timing Characteristics for 5.0-Volt Operation

Item	Symbol	Parameter	Min	Max	Units	Notes
–	XTF	clkin Frequency	0	66.67	MHz	–
1	TCKIN	clkin Period	15	∞	ns	–
2	TCHCK	clkin High Time	6.5	∞	ns	Measure for VIH for high time, NIL for low time.
3	TCLCK	clkin Low Time	6.5	∞	ns	Measure for VIH for high time, NIL for low time.
4	TCKLH	clkin Rise Time	1	5	ns	Only required to guarantee ICC. Maximum limits are bounded for TC, TCH, and TCL.
5	TCKHL	clkin Fall Time	1	5	ns	Only required to guarantee ICC. Maximum limits are bounded for TC, TCH, and TCL.
6	TCICO	clkin to clkout Delay	0	11.5	ns	Specified for a 50-pF load. See Figure 17 for capacitive derating information.
7	TCLCL	clkout Period	–	2TCKIN	ns	–
8	TCHCL	clkout High Time	(TCLCL/2) – 5	(TCLCL/2) + 5	ns	Measure for VIH for high time, NIL for low time.
9	TCCCH	clkout Low Time	(TCLCL/2) – 5	(TCLCL/2) + 5	ns	Measure for VIH for high time, NIL for low time.
10	TCH1CH2	clkout Rise Time	1	6	ns	Specified for a 50-pF load. See Figure 17 for rise and fall times outside 50 pF.
11	TCL2CL1	clkout Fall Time	1	6	ns	Specified for a 50-pF load. See Figure 17 for rise and fall times outside 50 pF.

Table 19. Clock Input and Output Characteristics for 3.3-Volt Operation

Item	Symbol	Parameter	Min	Max	Units	Notes
–	XTF	clkin Frequency	0	55.5	MHz	–
1	TC	clkin Period	18	∞	ns	–
2	TCH	clkin High Time	8	∞	ns	Measure for VIH for high time, NIL for low time.
3	TCL	clkin Low Time	8	∞	ns	Measure for VIH for high time, NIL for low time.
4	TCR	clkin Rise Time	1	5	ns	Only required to guarantee ICC. Maximum limits are bounded for TC, TCH and TCL.
5	TCF	clkin Fall Time	1	5	ns	Only required to guarantee ICC. Maximum limits are bounded for TC, TCH and TCL.
6	XTCD	clkin to clkout Delay	0	14.5	ns	Specified for a 50-pF load. See Figure 17 for capacitive derating information.
7	T	clkin Period	–	2TC	ns	–
8	TPH	clkin High Time	(T/2) – 5	(T/2) + 5	ns	Measure for VIH for high time, NIL for low time.
9	TPL	clkin Low Time	(T/2) – 5	(T/2) + 5	ns	Measure for VIH for high time, NIL for low time.
10	TPR	clkin Rise Time	1	6	ns	Specified for a 50-pF load. See Figure 17 for rise and fall times outside 50 pF.
11	TPF	clkin Fall Time	1	6	ns	Specified for a 50-pF load. See Figure 17 for rise and fall times outside 50 pF.

5.3 Serial Port Mode 0 Timing Characteristics

Serial Port Mode 0 timing characteristics are illustrated in Figure 19 and collected in Table 20.

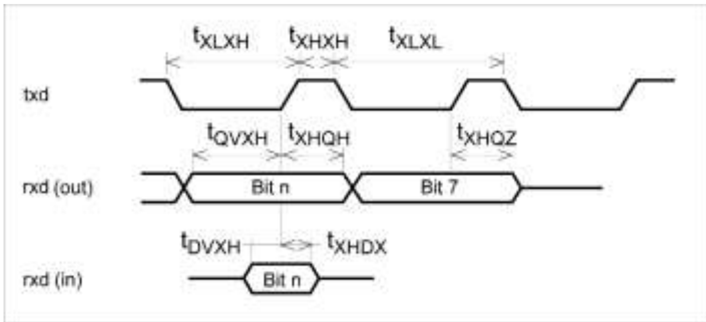


Figure 19. Serial Port Mode 0 Timing Characteristics

Table 20. Serial Port Mode 0 Timing Characteristics

Symbol	Parameter	Minimum	Maximum	Units
t_{XLXL}	txd Clock Period	t (n +1)	–	ns
t_{XLXH}	txd Clock Low to Clock High (n > 1)	2t – 35	2t + 35	ns
t_{XLXH}	txd Clock Low to Clock High (n = 1)	t – 35	t + 35	ns
t_{XHXL}	txd Clock High to Clock Low (n > 1)	(n – 1) t – 35	(n – 1) t + 35	ns
t_{XHXL}	txd Clock High to Clock Low (n = 1)	t – 35	t + 35	ns
t_{QVXH}	rxd Output Data Setup to txd Clock High (n > 1)	(n – 1) t – 35	–	ns
t_{QVXH}	rxd Output Data Setup to txd Clock High (n = 1)	t – 35	–	ns
t_{XHQX}	rxd Output Data Hold after txd Clock High (n > 1)	2t – 35	–	ns
t_{XHQX}	rxd Output Data Hold after txd Clock High (n = 1)	t – 35	–	ns
t_{XHQZ}	rxd Output Data Float after Last txd Clock High	–	t + 20	ns
t_{DVXH}	rxd Input Data Setup to txd Clock High	t + 20	–	ns
t_{XHDX}	rxd Input Data Hold after txd Clock High	0	–	ns

6. Reset Operation

The IA186EB/IA188EB will perform a reset operation any time the resin_n pin is active. Figure 20 shows the reset sequence when power is applied to the IA186EB/IA188EB. An external clock connected to clkin must not exceed the V_{CC} threshold being applied to the processor. This is normally not a problem if the clock driver is supplied with the same V_{CC} that supplies the processor. When attaching a crystal to the device, resin_n must remain active until both V_{CC} and clkout are stable (the length of time is application-specific and depends on the startup characteristics of the crystal circuit). The resin_n pin is designed to operate correctly using an RC reset circuit, but the designer must ensure that the ramp time for V_{CC} is not so long that resin_n is never really sampled at a logic low level when V_{CC} reaches minimum operating conditions.

Note: Failure to assert resin_n while the device is powering up will result in unpredictable operation.

Figure 21, Warm Reset Timing, shows the timing sequence when resin_n is applied after V_{cc} is stable and the device has been operating. Any bus operation that is in progress at the time resin_n is asserted will terminate immediately.

While resin_n is active, bus signals lock_n, a19/once_n, and a18–a16 are configured as inputs and weakly held high by internal pull-up transistors. Only a19/ once_n can be overdriven to a low-to-enable ONCE Mode.

7. Bus Timing

Figures 20 through 28 present the various bus cycles that are generated by the processor. The figures show the relationship of the various bus signals to clkout. Together with the information present in AC Characteristics, the figures allow the user to determine all the critical timing analysis needed for a given application.

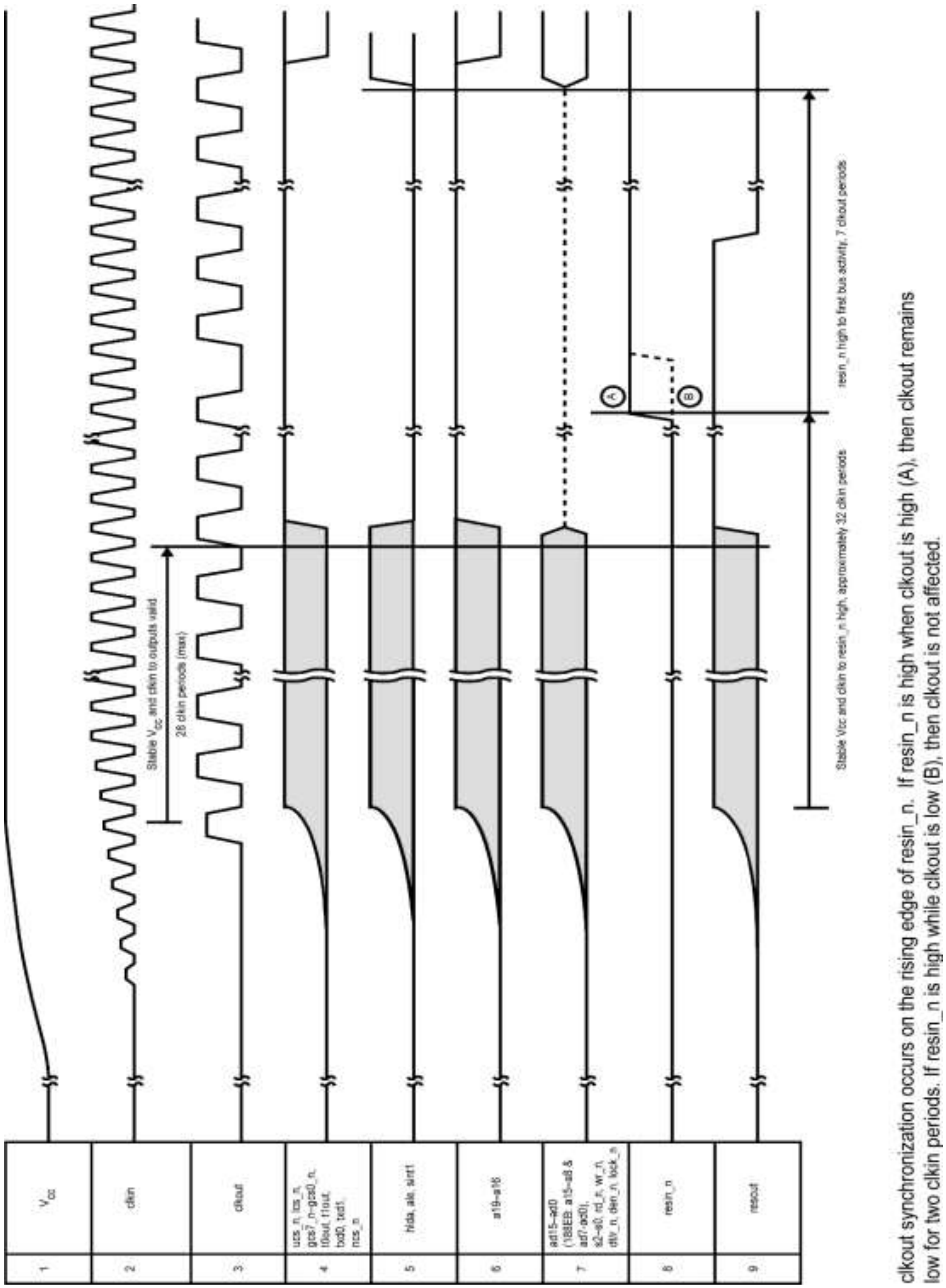


Figure 20. Cold Reset Timing

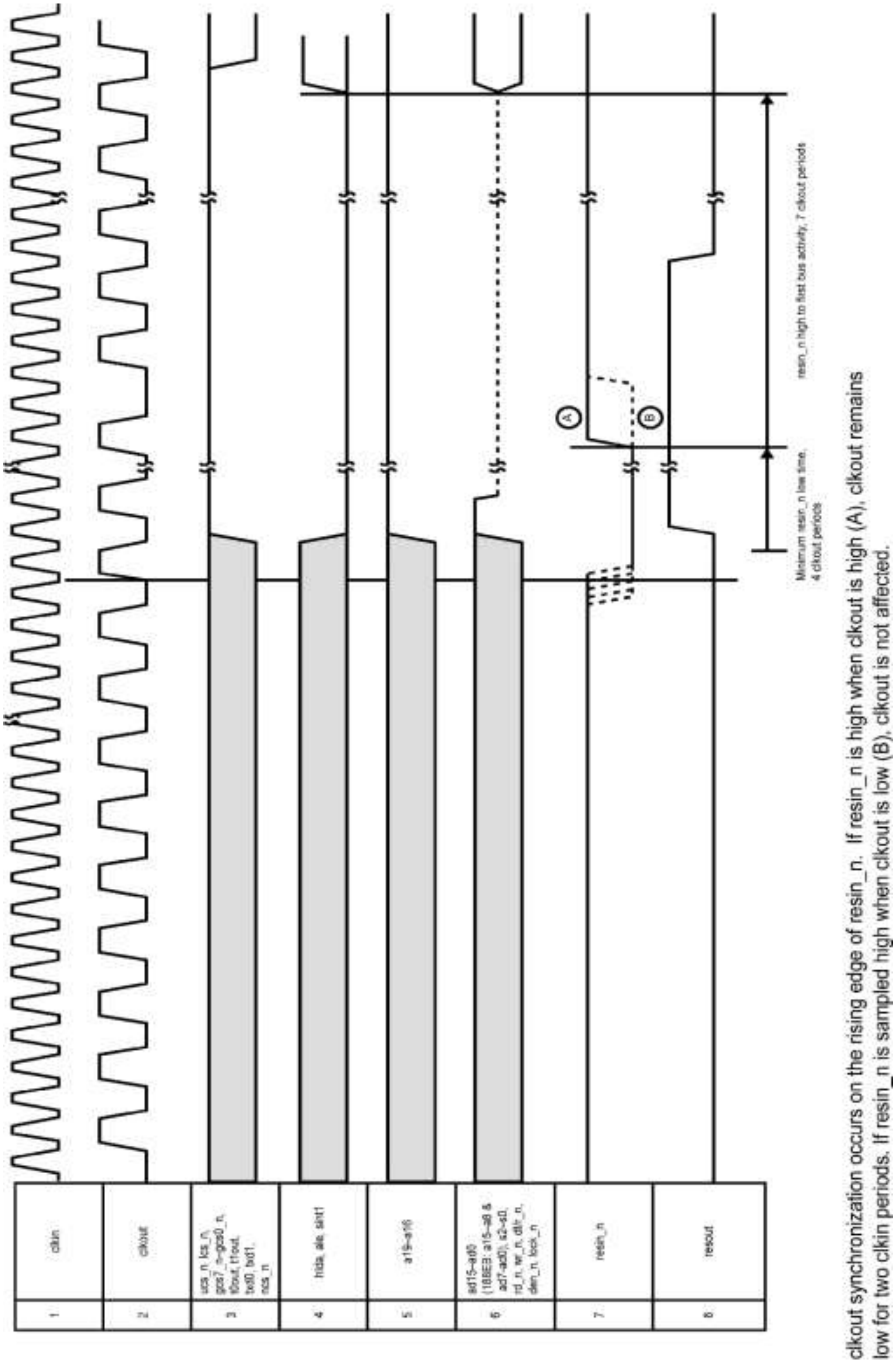


Figure 21. Warm Reset Timing

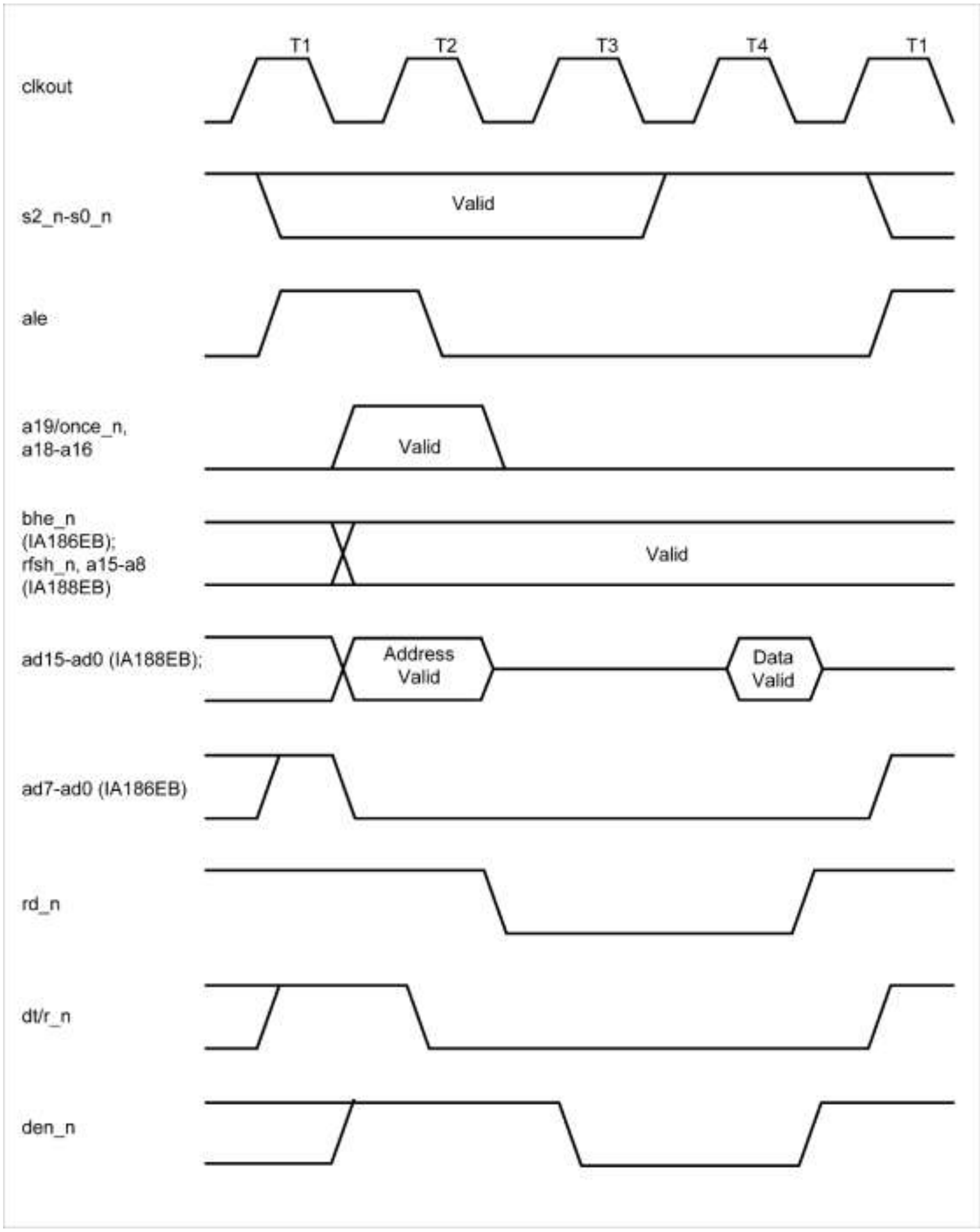


Figure 22. Read, Fetch, and Refresh Cycle Timing

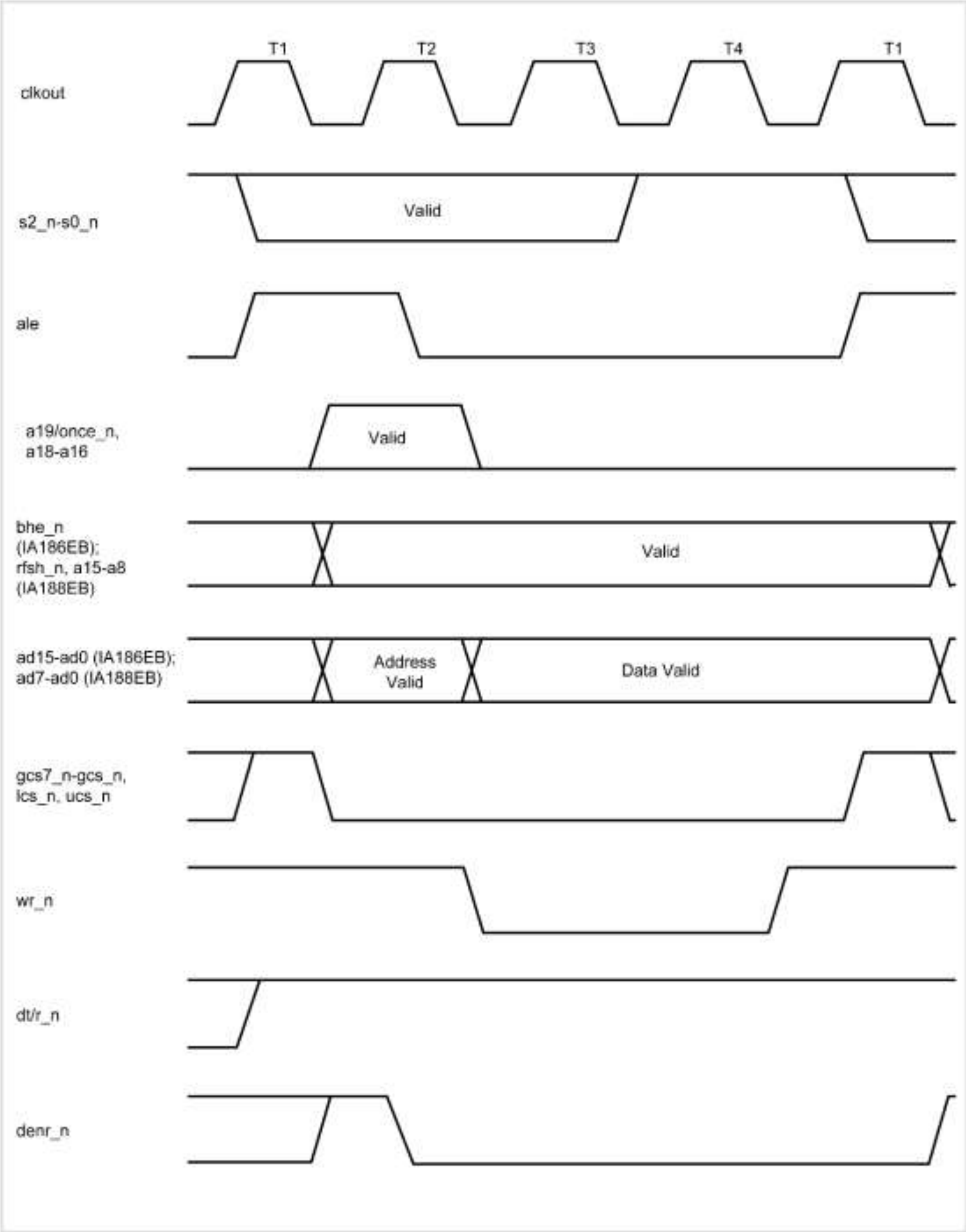


Figure 23. Write Cycle Timing

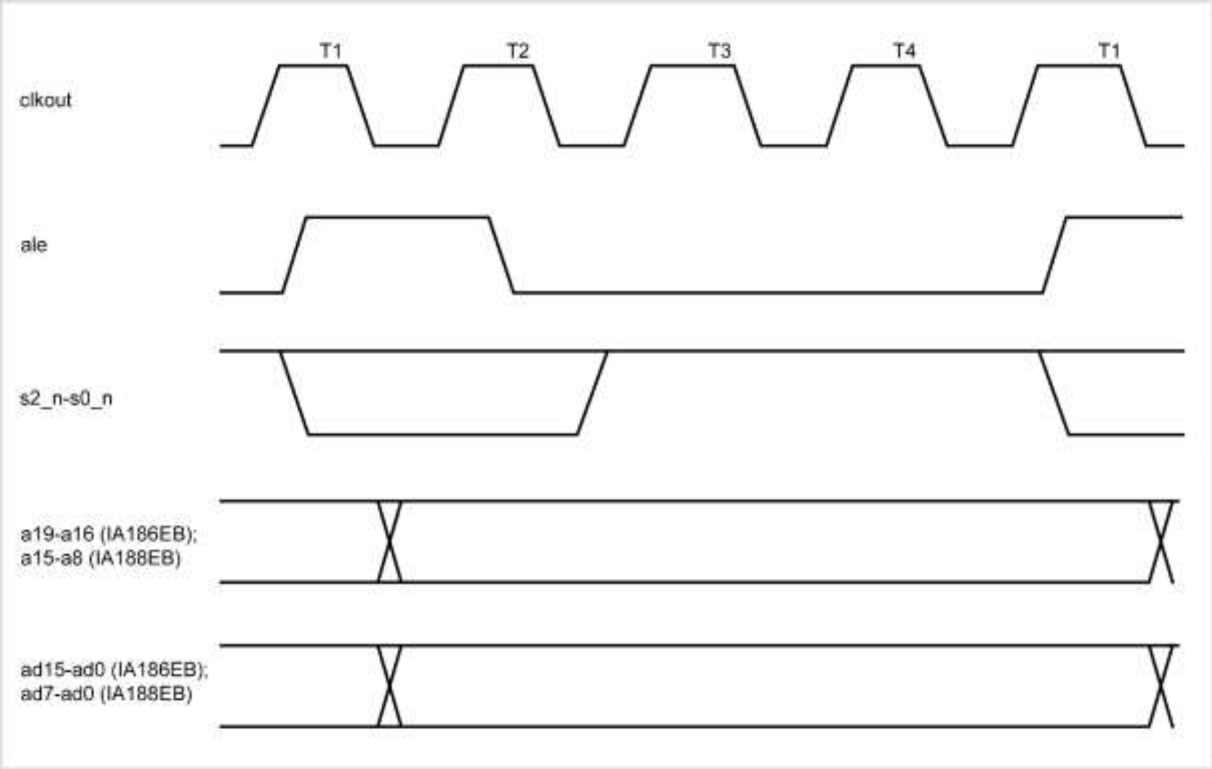


Figure 24. Halt Cycle Timing

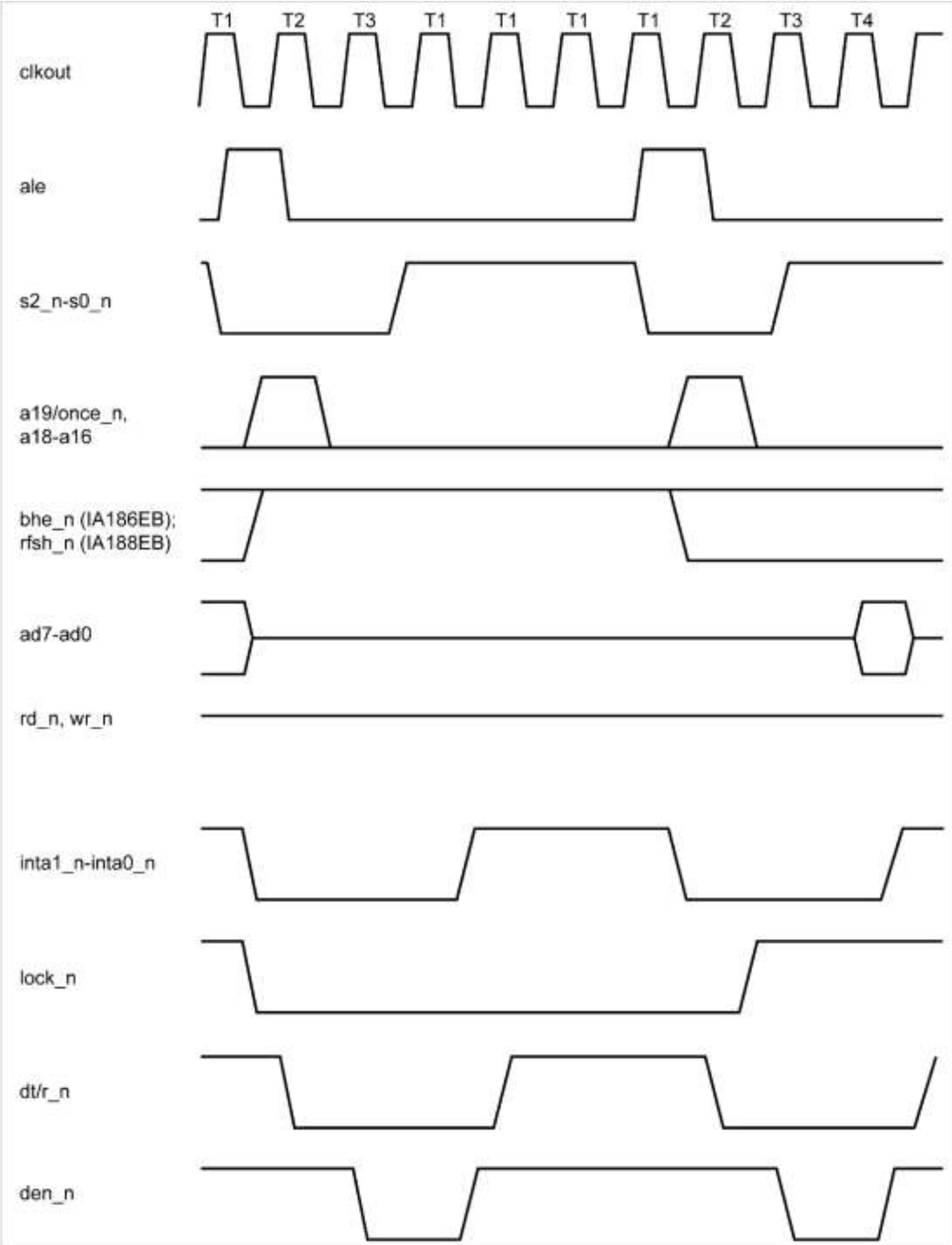


Figure 25. Interrupt Acknowledge (inta1_n, inta0_n) Cycle Timing

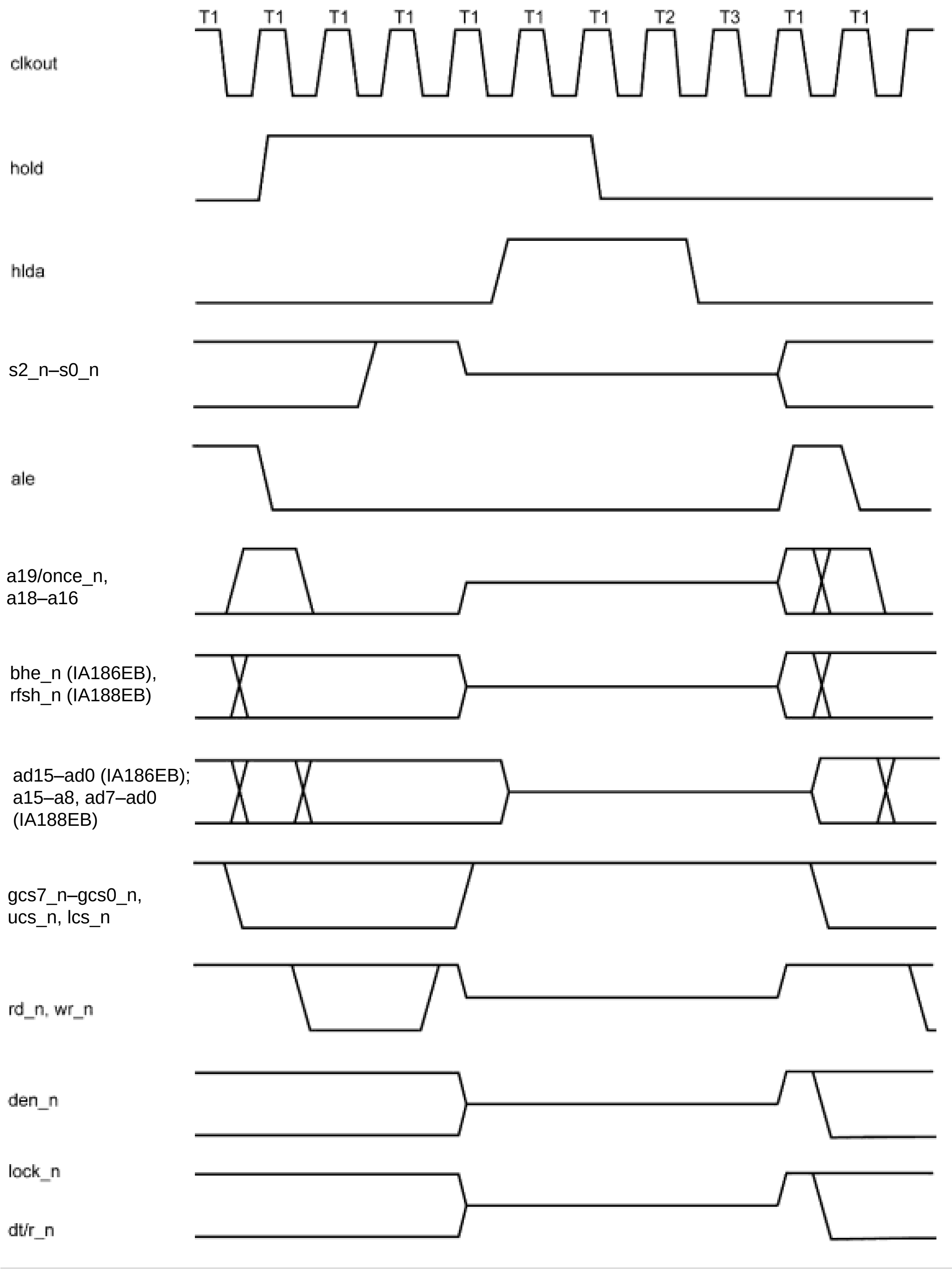


Figure 26. hold/hlda Timing

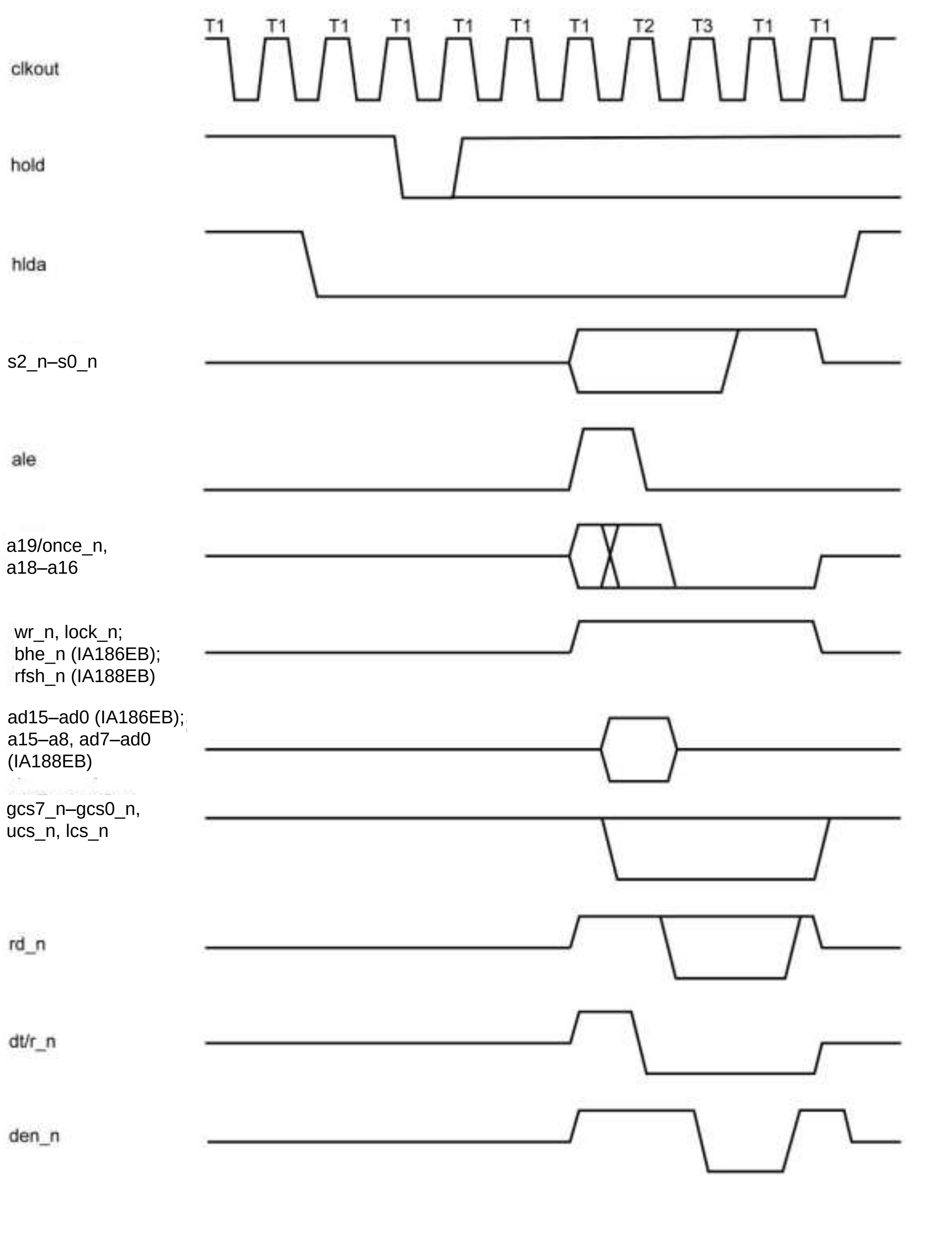


Figure 27. Refresh During Hold Acknowledge Timing

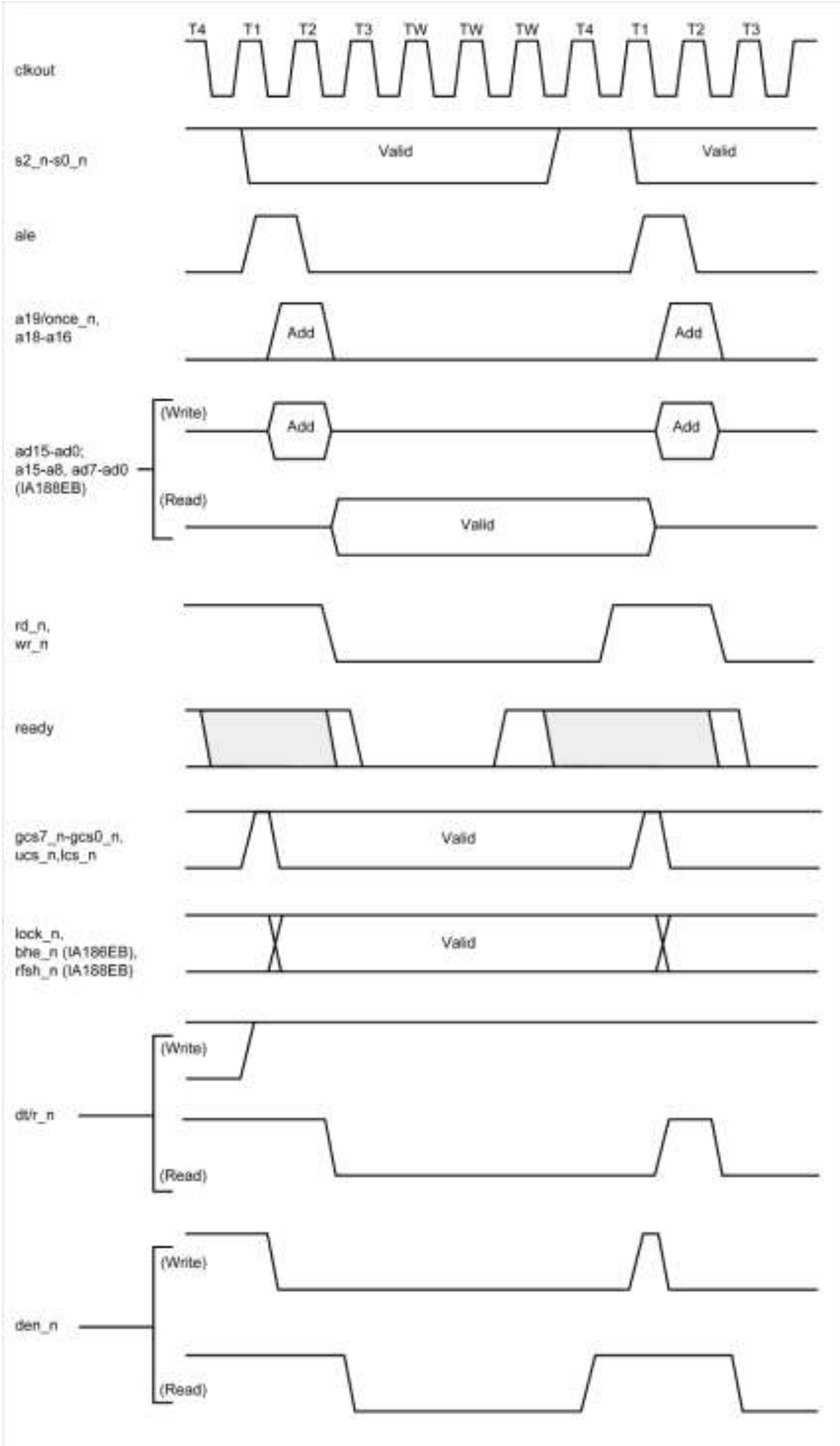


Figure 28. Ready Timing

8. Instruction Execution Times

Table 21 provides IA186EB and IA188EB execution times, mnemonic instruction, and additional information on execution, if required.

Table 21. Instruction Set Timing

Instruction	Clock Cycles		Comments
	IA186EB	IA188EB	
AAA	8	8	–
AAD	15	15	–
AAM	19	19	–
AAS	7	7	–
ADC Immediate to accumulator	3/4	3/4	8-bit/16-bit
ADC Immediate to register/memory	4/16	4/16[a]	register/memory
ADC Register/memory with register to either	3/10	3/10[a]	
ADD Immediate to accumulator	3/4	3/4	8-bit/16-bit
ADD Immediate to register/memory	4/16	4/16[a]	register/memory
ADD Register/memory with register either	3/10	3/10[a]	
AND Immediate to accumulator	3/4	3/4[a]	8-bit/16-bit
AND Immediate to register/memory	4/16	4/16[a]	register/memory
AND Register/memory and register to either	3/10	3/10[a]	
BOUND	33–35	33–35	–
CALL Direct intersegment	23	31	–
CALL Direct within segment	15	19	–
CALL Indirect intersegment	38	54	–
CALL Register/memory indirect with segment	13/19	17/27	register/memory
CBW	2	2	–
CLC	2	2	–
CLD	2	2	–
CLI	2	2	–
CMC	2	2	–
CMP Immediate with accumulator	3/4	3/4	8-bit/16-bit
CMP Immediate with register/memory	3/10	3/10[a]	register/memory
CMP Register with register/memory	3/10	3/10[a]	
CMP Register/memory with register	3/10	3/10[a]	

[a]Number of clock cycles for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

Table 21. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186EB	IA188EB	
CMPS	22	22[a]	–
CMPS (repeated *n* times)	5+22*n*	5+22*n*[a]	–
CS	2	2	–
CWD	4	4	–
DAA	4	4	–
DAS	4	4	–
DEC Register	3	3	–
DEC Register/memory	3/14	3/15[a]	register/memory
DIV Memory-Byte	35	35	–
DIV Memory-Word	44	44[a]	–
DIV Register-Byte	29	29	–
DIV Register-Word	38	38	–
DS	2	2	–
ENTER L − 0	15	19	–
ENTER L − 1	25	29	–
ENTER L > 1	22+16(*n*−1)	22+16(*n*−1)	–
ES	2	2	–
HLT	2	2	–
IDIV Memory-Byte	50–58	50–58	–
IDIV Memory-Word	59–67	59–67[a]	–
IDIV Register-Byte	44–52	44–52	–
IDIV Register-Word	53–61	53–61	–
IMUL Immediate (signed)	22–25/29–32	22–25/29–32	register/memory
IMUL Memory-Byte	31–34	31–34	–
IMUL Memory-Word	40–43	40–43[a]	–
IMUL Register-Byte	25–28	25–28	–
IMUL Register-Word	34–37	34–37	–
IN Fixed port	10	10[a]	–
IN Variable port	8	8[a]	–
INC Register	3	3	–
INC Register/memory	3/15	3/15[a]	register/memory
INS	14	14	–
INS (repeated *n* times)	8+8*n*	8+8*n*[a]	–
INT Type specified	47	47	–
INT Type 3	45	45	–
INTO	48/4	48/4	INTO taken/INTO not taken
IRET	28	28	–

[a]Number of clock cycles for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

Table 21. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles IA186EB	Clock Cycles IA188EB	Comments
JA	4/13	4/13	Jump not taken/Jump taken
JAE	4/13	4/13	
JB	4/13	4/13	
JBE	4/13	4/13	
JCXZ	5/15	5/15	
JE	4/13	4/13	
JG	4/13	4/13	
JGE	4/13	4/13	
JL	4/13	4/13	
JLE	4/13	4/13	Jump not taken/Jump taken
JMP Register/memory indirect within segment	11/17	11/21	
JMP Direct intersegment	14	14	–
JMP Direct within segment	14	14	–
JMP Indirect inter-segment	26	34	–
JMP Short/long	14	14	–
JNA	4/13	4/13	Jump not taken/Jump taken
JNAE	4/13	4/13	
JNB	4/13	4/13	
JNBE	4/13	4/13	
JNE	4/13	4/13	
JNG	4/13	4/13	
JNGE	4/13	4/13	
JNL	4/13	4/13	
JNLE	4/13	4/13	
JNO	4/13	4/13	
JNP	4/13	4/13	
JNS	4/13	4/13	
JNZ	4/13	4/13	
JO	4/13	4/13	
JP	4/13	4/13	
JPE	4/13	4/13	
JPO	4/13	4/13	
JS	4/13	4/13	
JZ	4/13	4/13	
LAHF	2	2	–
LDS	18	26	–
LEA	6	6	–
LEAVE	8	8	–
LES	18	26	–

[a]Number of clock cycles for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

Table 21. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186EB	IA188EB	
LOCK	2	2	–
LODS	12	12[a]	–
LODS (repeated *n* times)	6+11*n*	6+11*n*[a]	–
LOOP	6/16	6/16	–
LOOPE	6/16	6/16	Loop not taken/Loop taken
LOOPNE	6/16	6/16	
LOOPNZ	6/16	6/16	
LOOPZ	6/16	6/16	Loop not taken/Loop taken
MOV Accumulator to memory	9	9[a]	–
MOV Immediate to register	3/4	3/4	8-bit/16-bit
MOV Immediate to register/memory	12/13	12/13	register/memory
MOV Memory to accumulator	8	8[a]	–
MOV Register to Register/Memory	2/12	2/12[a]	register/memory
MOV Register/memory to register	2/9	2/9[a]	
MOV Register/memory to segment register	2/9	2/13	
MOV Segment register to register/memory	2/11	2/15	
MOVS	14	14[a]	–
MOVS (repeated *n* times)	8+8*n*	8+8*n*[a]	–
MUL Memory-Byte	32–34	32–34	–
MUL Memory-Word	41–43	41–43[a]	–
MUL Register-Byte	26–28	26–28	–
MUL Register-Word	35–37	35–37	–
NEG	3/10	3/10[a]	register/memory
NOP	3	3	–
NOT	3/10	3/10[a]	register/memory
OR Immediate to accumulator	3/4	3/4[a]	8-bit/16-bit
OR Immediate to register/memory	4/16	4/16[a]	register/memory
OR Register/memory and register to either	3/10	3/10[a]	
OUT Fixed port	9	9[a]	–
OUT Variable port	7	7[a]	–
OUTS	14	14	–
OUTS (repeated *n* times)	8+8*n*	8+8*n*[a]	–
POP Memory	20	24	–
POP Register	10	14	–
POP Segment register	8	12	–
POPA	51	83	–
POPF	8	12	–
PUSH Immediate	10	14	–

[a]Number of clock cycles for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

Table 21. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186EB	IA188EB	
PUSH Memory	16	20	–
PUSH Register	10	14	–
PUSH Segment register	9	13	–
PUSHA	36	68	–
PUSHF	9	13	–
RET Inter-segment	22	30	–
RET Inter-segment adding immediate to SP	25	33	–
RET Within segment	16	20	–
RET Within segment adding immediate to SP	18	22	–
ROL Register/Memory by 1	2/15	2/15	register/memory
ROL Register/Memory by CL	5+n/17+n	5+n/17+n	
ROL Register/Memory by Count	5+n/17+n	5+n/17+n	register/memory
ROR Register/Memory by 1	2/15	2/15	
ROR Register/Memory by CL	5+n/17+n	5+n/17+n	
ROR Register/Memory by Count	5+n/17+n	5+n/17+n	
SAHF	3	3	–
SBB Immediate from accumulator	3/4	3/4[a]	8-bit/16-bit
SBB Immediate from register/memory	4/16	4/16[a]	register/memory
SBB Register/memory and register to either	3/10	3/10[a]	
SCAS	15	15[a]	–
SCAS (repeated *n* times)	5+15*n*	5+15*n*[a]	–
SHL Register/Memory by 1	2/15	2/15	–
SHL Register/Memory by CL	5+n/17+*n*	5+n/17+*n*	register/memory
SHL Register/Memory by Count	5+n/17+*n*	5+n/17+*n*	
SHR Register/Memory by 1	2/15	2/15	
SHR Register/Memory by CL	5+n/17+*n*	5+n/17+*n*	
SHR Register/Memory by Count	5+n/17+*n*	5+n/17+*n*	
SS	2	2	–
STC	2	2	–
SUB Immediate from accumulator	3/4	3/4	8-bit/16-bit
SUB Immediate from register/memory	4/16	4/16[a]	register/memory
SUB Register/memory and register to either	3/10	3/10[a]	
STD	2	2	–
STI	2	2	–

[a]Number of clock cycles for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

Table 21. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186EB	IA188EB	
STOS	10	10[a]	–
STOS (repeated n times)	6+9n	6+9n	–
TEST Immediate data and accumulator	3/4	3/4	8-bit/16-bit
TEST Immediate data and register/memory	4/10	4/10[a]	register/memory
TEST Register/memory and register	3/10	3/10[a]	
WAIT	6	6	test_n = 0
XCHG Register with accumulator	3	3	
XCHG Register/memory with register	4/17	4/17[a]	register/memory
XLAT	11	15	–
XOR Immediate to accumulator	3/4	3/4	8-bit/16-bit
XOR Immediate to register/memory	4/16	4/16[a]	register/memory
XOR Register/memory and register to either	3/10	3/10[a]	–

[a]Number of clock cycles for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

9. Innovasic Part Number Cross-Reference

Tables 22 through 24 cross-reference the Innovasic part number with the corresponding Intel part number.

Table 22. Innovasic Part Number Cross-Reference for the PLCC

Innovasic Part Number	Intel Part Number	Package Type	Temperature Grades
IA186EB-PLC84I-R-00 lead free (RoHS-compliant)	EE80C186EB25 EE80C186EB20 EN80C186EB25 EN80C186EB20 EN80C186EB13 N80C186EB25 N80C186EB20 N80C186EB13 TN80C186EB25 TN80C186EB20 TN80C186EB13 N80L186EB16 N80L186EB13 TN80L186EB16 TN80L186EB13 EN80L186EB13	84-Pin PLCC	Commercial and industrial
IA188EB-PLC84I-R-00 lead free (RoHS-compliant)	EE80C188EB25 EE80C188EB20 EE80C188EB13 EN80C188EB25 EN80C188EB20 EN80C188EB13 N80C188EB25 N80C188EB20 N80C188EB13 TN80C188EB25 TN80C188EB20 TN80C188EB13 EE80L188EB16 EN80L188EB13 N80L188EB16 N80L188EB13 TN80L188EB16 TN80L188EB13	84-Pin PLCC	Commercial and industrial

Table 23. Innovasic Part Number Cross-Reference for the PQFP

Innovasic Part Number	Intel Part Number	Package Type	Temperature Grades
IA186EB-PQF80I-R-00 lead free (RoHS-compliant)	EG80C186EB25 ES80C186EB20 ES80C186EB13 S80C186EB25 S80C186EB20 S80C186EB13 TS80C186EB25 TS80C186EB20 TS80C186EB13 EG80L186EB16 EG80L186EB13 S80L186EB16 S80L186EB13 TS80L186EB16 TS80L186EB13	80-Pin PQFP	Commercial and industrial
IA188EB-PQF80I-R-00 lead free (RoHS-compliant)	EG80C188EB25 ES80C188EB20 S80C188EB25 S80C188EB20 S80C188EB13 TS80C188EB25 TS80C188EB20 TS80C188EB13 ES80L188EB13 TS80L188EB16 TS80L188EB13	80-Pin PQFP	Commercial and industrial

Table 24. Innovasic Part Number Cross-Reference for the LQFP

Innovasic Part Number	Intel Part Number	Package Type	Temperature Grades
IA186EB-PLQ80I-R-00 lead free (RoHS-compliant)	YW80C186EB25 YW80C186EB20 SB80C186EB25 SB80C186EB20 SB80C186EB13 YW80L186EB16 YW80L186EB13 SB80L186EB16 SB80L186EB13	80-Pin LQFP	Commercial and industrial
IA188EB-PLQ80I-R-00 lead free (RoHS-compliant)	YW80C188EB25 YW80C188EB20 SB80C188EB25 SB80C188EB20 SB80C188EB13 YW80L188EB16 YW80L188EB13 SB80L188EB16 SB80L188EB13	80-Pin LQFP	Commercial and industrial

10. Errata

The following errata are associated with Version 00 of the IA186EB/IA188EB. A workaround to the identified problem has been provided where possible.

10.1 Summary

Table 25 presents a summary of errata.

Table 25. Summary of Errata

Errata No.	Problem	Ver. 00
1	Alternate Mode (TxCON[1] == 1) for timer 0 and 1 has some functional issues.	Exists
2	When the extension byte (mod field) is set to "11," some instructions will cause the CPU to hang.	Exists
3	When the chip is put in SFNM mode for INT0 or INT1, the LVL bit is automatically set for those interrupts.	Exists
4	Timer 2 will stop or not start counting.	Exists
5	Write does not occur when counter is actively counting.	Exists
6	Program Counter can become corrupted if an interrupt occurs.	Exists
7	Bound instruction uses bad data when index addresses are on odd boundary in memory.	Exists

10.2 Detail

Errata No. 1

Problem: Alternate Mode (TxCON[1] == 1) for timer 0 and 1 has some functional issues.

Description:

- TxOUT will continuously toggle at 1/2 CLKOUT regardless of count register values.
- The maxcount compare will not work. The live count will compare against TxCMPA and TxCMPB in alternate cycles. This could cause a compare (and the associated interrupt, or switch the intended compare, or stop counting altogether) to occur early or not at all.

- The TxOUT pin may start in the wrong state if the user writes to TxCON register Bit [12].
- When in retrigger mode, Timer 1 will not function correctly. Input pulses on T0IN will cause counter to begin counting.

Workaround: None.

Errata No. 2

Problem: When the extension byte (mod field) is set to "11," some instructions will cause the CPU to hang.

Description: Although there are faster versions of each instruction (these are not commonly used by compilers), the following instructions will cause the CPU to hang when the extension byte (mod field) is set to "11":

- 8D (LEA)
- 8F (POP memory)
- C6 (MOV immediate8 to memory/register)
- C7 (MOV immediate16 to memory/register)
- FE (PUSH memory)
- FF (PUSH memory)

Workaround: Substitute instructions in the following table.

Instruction	Workaround
8D (LEA)	Use MOV register (89 or 8B)
8F (POP memory)	Use POP register (0101_0xxx)
C6 (MOV immediate8 to memory/register)	Use MOV immediate8 to register (1011_0xxx)
C7 (MOV immediate16 to memory/register)	Use MOV immediate16 to register (1011_1xxx)
FE (PUSH memory)	Use PUSH register (0101_0xxx)
FF (PUSH memory)	Use PUSH register (0101_0xxx)

Errata No. 3

Problem: When the chip is put in SFNM mode for INT0 or INT1, the LVL bit is automatically set for those interrupts.

Workaround: None.

Errata No. 4

Problem: Timer 2 will stop or not start counting.

Description: Writing a logic “1” to unused bits in the timer control register can cause the timer to stop counting or to never start counting.

Workaround: Do not write a logic “1” to any unused or reserved bits in the timer control register.

Errata No. 5

Problem: Write does not occur when counter is actively counting.

Description: If a timer incremented its count register to the currently active compare register during a write to that count register, the write would not occur.

Workaround: Do not write count register while that counter is actively counting.

Errata No. 6

Problem: Program Counter can become corrupted if an interrupt occurs.

Description: If an interrupt occurs during the decode stage of a TEST instruction using an opcode of the form 1111_0111_1100_0xxx, the Program Counter could become corrupted upon returning from the interrupt handler.

Workaround: None.

Errata No. 7

Problem: Bound instruction uses bad data when index addresses are on odd boundary in memory.

Description: BOUND instruction will use bad data if index address LSB is a “1” in memory.

Workaround: None.

Revision History

Table 26 presents the sequence of revisions to document IA211080214.

Table 26. Revision History

Date	Revision	Description	Page(s)
July 30, 2008	00	First edition released.	NA
October 13, 2008	01	Pin number range “ad15–a8” corrected to “a15–a8” in Figures 26 and 27. Errata No. 4 added. [Also cover page, header, footer, and errata chapter reformatted to meet publication standards.]	66, 67, 78, 79, 80, 81
January 14, 2009	02	Updated errata table for Version 00 – added 3 errata (#5 – 7).	81, 83

11. For Additional Information

The Innovasic Semiconductor IA186EB and IA188EB microcontrollers are form, fit, and function replacements for the original Intel® 80C186EB, 80C188EB, 80L186EB, and 80L188EB 16-bit high-integration embedded processors.

The Innovasic Support Team wants our information to be complete, accurate, useful, and easy to understand. Please feel free to contact our experts at Innovasic at any time with suggestions, comments, or questions.

Innovasic Support Team
3737 Princeton NE
Suite 130
Albuquerque, NM 87107

(505) 883-5263
Fax: (505) 883-5477
Toll Free: (888) 824-4184
E-mail: support@innovasic.com
Website: http://www.Innovasic.com