

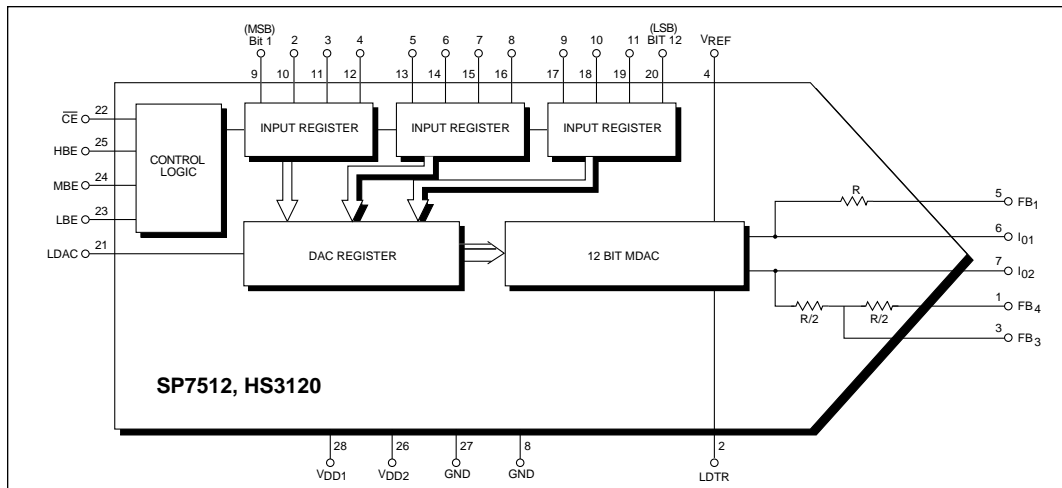
Double-Buffered 12-Bit Multiplying DAC

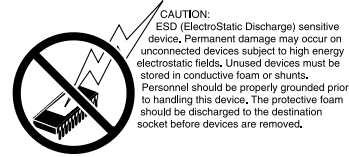
- Monolithic Construction
- 12-Bit Resolution
- 0.01% Non-Linearity
- Four-Quadrant Multiplication
- Latch-up Protected
- Low Power – 30mW
- Single +15V Power Supply



DESCRIPTION...

The **SP7512** and **HS3120** are precision 12-bit multiplying DACs, double-buffered for easy interfacing with microprocessor busses. Both unipolar and bipolar operation can be accommodated with a minimum of external components. The **SP7512** is available for use in commercial and industrial temperature ranges, packaged in a 28-pin SOIC. The **HS3120** is available in commercial and military temperature ranges, packaged in a 28-pin side-brazed DIP.





SPECIFICATIONS

(Typical @ 25°C, nominal power supply, $V_{REF} = +10V$, unipolar, unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DIGITAL INPUT					
Resolution	12			Bits	<p>The input coding is complementary binary if I_{O2} is used.</p> <p>Digital input voltage must not exceed supply voltage or go below $-0.5V$; "0" $< 0.8V$; $2.4V < "1" \leq V_{DD}$</p> <p>All strobes are level triggered. See Timing Diagram; GBD*</p> <p>All strobes are level triggered. See Timing Diagram; GBD*</p> <p>All strobes are level triggered. See Timing Diagram; GBD*</p>
2-Quad, Unipolar Coding		Binary & Comp. Binary			
4-Quad, Bipolar Coding		Offset Binary			
Logic Compatibility		CMOS, TTL			
Input Current			± 1	μA	
Data Set-up Time	250			ns	
Strobe Width	250			ns	
Data Hold Time	0			ns	
REFERENCE INPUT					
Voltage Range			± 25	V	
Input Impedance	4		12	KOhms	
ANALOG OUTPUT					
Scale Factor	62.5		187.5	$\mu A/V_{REF}$	<p>Using the internal feedback resistor and an external op amp.</p> <p>At 25°C; the output leakage current will create an offset voltage at the external op amps output. It doubles every 10°C temperature increase.</p>
Scale Factor Accuracy		± 0.4		%	
Output Leakage			10	nA	
Output Capacitance				pF	
C_{OUT1} , all inputs high		80		pF	
C_{OUT1} , all inputs low		40		pF	
C_{OUT2} , all inputs high		40		pF	
C_{OUT2} , all inputs low		80		pF	
STATIC PERFORMANCE					
Integral Linearity			± 0.015	% FSR	
SP7512BN/KN, HS3120-2					
Differential Linearity			± 0.024	%FSR	
SP7512BN/KN, HS3120-2					
Monotonicity		Guaranteed to 12 bits			
SP7512BN/KN, HS3120-2					
STABILITY					$(T_{MIN}$ to $T_{MAX})$
Scale Factor			2	ppm FSR/°C	Note 1
Integral Linearity			0.2	ppm FSR/°C	
Differential Linearity			0.2	ppm FSR/°C	
STABILITY					$(T_{MIN}$ to $T_{MAX})$
Monotonicity Temp. Range				°C	
SP7512KN, HS3120C-__	0		+70	°C	
SP7512BN	-40		+85	°C	
HS3120B-__	-55		+125	°C	

SPECIFICATIONS (continued)

(Typical @ 25°C, nominal power supply, $V_{REF} = +10V$, unipolar unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DYNAMIC PERFORMANCE					
Digital Small Signal Settling		1.0		μS	to 0.01% (strobed) ($V_{REF} = 20V_{pp}$)
Full Scale Transition Settling		2.0		μS	
Reference Feedthrough Error		<1		mV	
@ 1kHz				mV	Delay times are twice the amount shown at $T_A = +125^\circ C$
@ 10kHz		2		mV	
Delay to output					
from Bits input		100		ns	
from LDAC		200		ns	
from CE		120		ns	
POWER SUPPLY (V_{DD})					
Operating Voltage		+15 \pm 5%		V	specifications guaranteed
Voltage Range	+5		+16	V	
Current			2.5	mA	
Rejection Ratio			0.002	%/%	
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
SP7512K	0		+70	$^\circ C$	
SP7512B	-40		+85	$^\circ C$	
HS3120-C	0		+70	$^\circ C$	
HS3120-B	-55		+125	$^\circ C$	
HS3120-B/883	-55		+125	$^\circ C$	
Storage Temperature	-65		+150	$^\circ C$	
Package					
SP7512_N		28-pin SOIC			
HS3120-C		28-pin Plastic DIP			
HS3120-B		28-pin Side-Brazed DIP			

Notes:

- Using the internal feedback resistor, output leakage current creates an offset, which doubles every 10°C rise in temperature.

PIN ASSIGNMENTS

- Pin 1 – FB₄ – Feedback Bipolar Operation
 - Pin 2 – LDTR – Ladder Termination
 - Pin 3 – FB₃ – Feedback Bipolar Operation
 - Pin 4 – V_{REF} – Reference Voltage Input
 - Pin 5 – FB₁ – Feedback, Unipolar/Bipolar
 - Pin 6 – I_{O1} – Current out into virtual ground
 - Pin 7 – I_{O2} – Current out-complement of I_{O1}
 - Pin 8 – V_{SS} – Ground, Analog and DAC Register
 - Pin 9 – DB₁₁ – MSB, Data Bit 1
 - Pin 10 – DB₁₀ – Data Bit 2
 - Pin 11 – DB₉ – Data Bit 3
 - Pin 12 – DB₈ – Data Bit 4
 - Pin 13 – DB₇ – Data Bit 5
 - Pin 14 – DB₆ – Data Bit 6
 - Pin 15 – DB₅ – Data Bit 7
 - Pin 16 – DB₄ – Data Bit 8
 - Pin 17 – DB₃ – Data Bit 9
 - Pin 18 – DB₂ – Data Bit 10
 - Pin 19 – DB₁ – Data Bit 11
 - Pin 20 – DB₀ – LSB, Data Bit 12
 - Pin 21 – LDAC – Transfers data from input to DAC register; a logic “0” latches data into registers; a logic “1” allows data to change (transfer to) register.
 - Pin 22 – $\overline{\text{CE}}$ – Chip Enable, active low
 - Pin 23 – LBE – Bit 12 to Bit 9 Enable
 - Pin 24 – MBE – Bit 8 to Bit 5 Enable
 - Pin 25 – HBE – Bit 4 to Bit 1 Enable
 - Pin 26 – V_{DD2} – Supply Analog and DAC Register
 - Pin 27 – V_{SS1} – Ground input latches
 - Pin 28 – V_{DD1} – Supply input latches
- NOTE: Pins 8 and 27, and pins 26 and 28 must be connected externally.

FEATURES...

The **SP7512** and **HS3120** are precision 12-bit multiplying DACs with internal two-stage input storage registers for easy interfacing with microprocessor busses. The DACs are implemented as a one-chip CMOS circuit with a resistor ladder network designed for 0.01% linearity without laser trimming.

The input registers are sectioned into 3 segments of 4 bits each, all individually addressable. The DAC-register, following the input registers, is a parallel 12-bit register for holding the DAC data while the input registers are updated. Only the data held in the DAC register determines the analog output value of the converter.

The **SP7512** and **HS3120** have been designed for great flexibility in connecting to bus-oriented systems. The 12 data inputs are organized into 3 independent addressable 4-bit input registers such that the DACs can be connected to either a 4, 8 or 16-bit data bus. The control logic of the DACs includes chip enable and latch enable inputs for flexible memory mapping. All controls are level-triggered to allow static or dynamic operation.

A total of 5 output lines are provided on the DACs to allow unipolar and bipolar output connection with a minimum of external components. The feedback resistor is internal. The resistor ladder network termination is externally available, thus eliminating an external resistor for the 1 LSB offset in bipolar mode.

The **SP7512** is available for use in commercial and industrial temperature ranges, packaged in

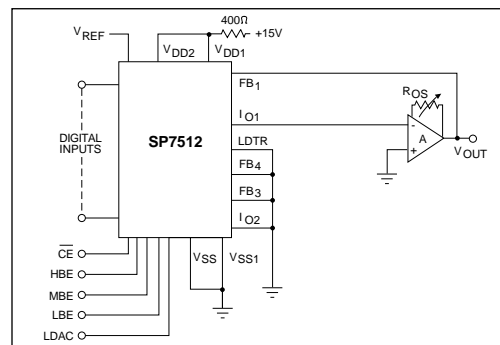


Figure 1. Unipolar Operation

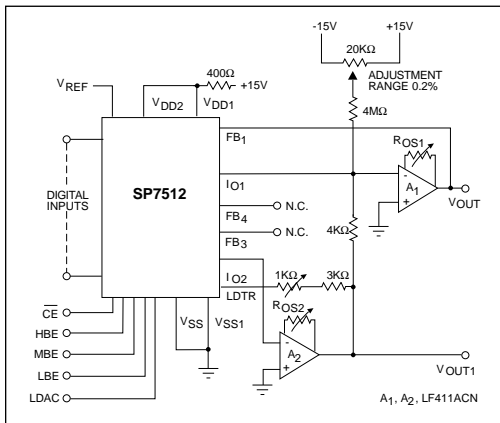


Figure 2. Bipolar Operation

a 28-pin SOIC. The **HS3120** is available in commercial and military temperature ranges, packaged in a 28-pin side-braced DIP. For product processed and screened to the requirements of MIL-M-38510 and MIL-STD-883C, please consult the factory (**HS3120B** only).

APPLICATIONS INFORMATION

Unipolar Operation

Figure 1 shows the interconnections for unipolar operation. Connect I_{O1} and FB_1 as shown in diagram. Tie I_{O2} (Pin 7), FB_3 (Pin 3), and FB_4 (Pin 1) to Ground (Pin 8). To maintain specified linearity, external amplifiers must be zeroed. This is best done with V_{REF} set to zero and, with the DAC register loaded with all bits at zero, adjust R_{OS} for $V_{OUT} = 0V$

TRANSFER FUNCTION (N=12)

BINARY INPUT	UNIPOLAR OUTPUT	BIPOLAR OUTPUT
111...111	$-V_{REF} (1 - 2^{-N})$	$-V_{REF} (1 - 2^{-(N-1)})$
100...001	$-V_{REF} (1/2 + 2^{-N})$	$-V_{REF} (2^{-(N-1)})$
100...000	$-V_{REF} / 2$	0
011...111	$-V_{REF} (1/2 - 2^{-N})$	$V_{REF} (2^{-(N-1)})$
000...000	0	V_{REF}

Table 1. Transfer Function

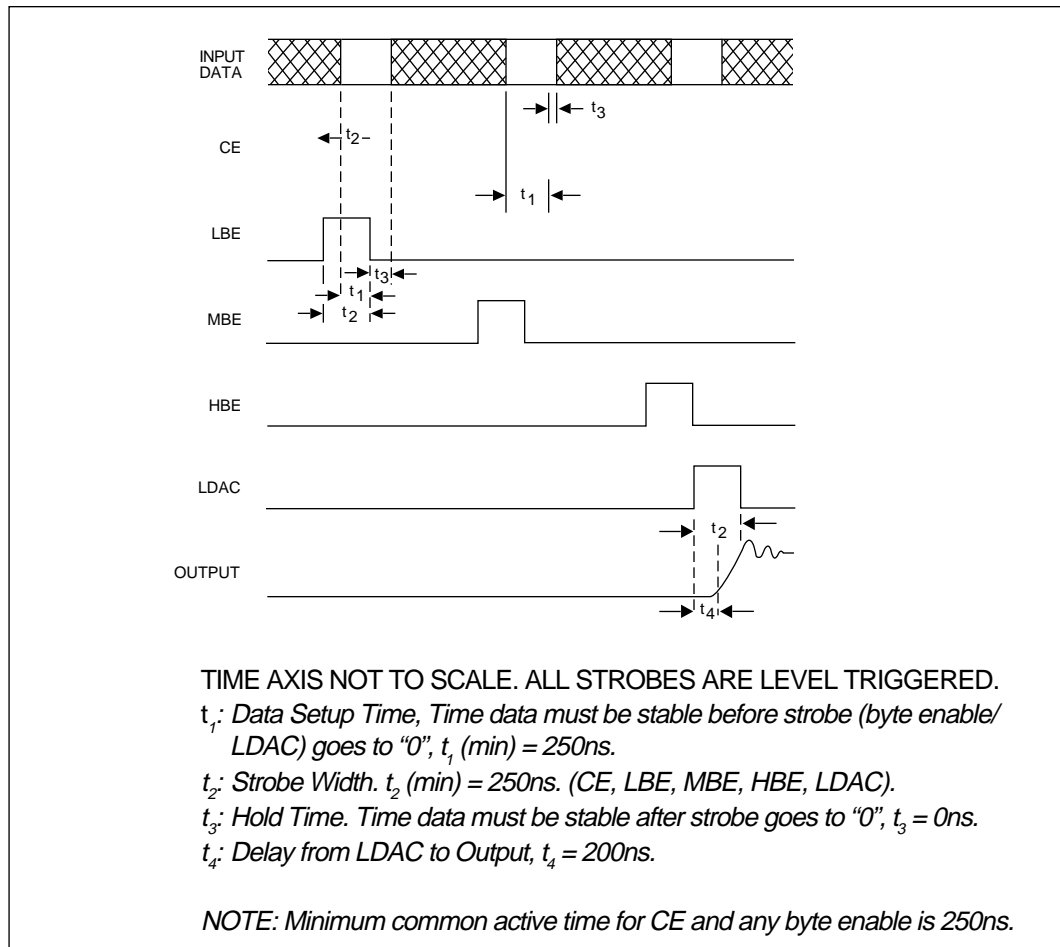
Bipolar Operation

Figure 2 shows the interconnections for bipolar operation. Connect I_{O1} , I_{O2} , FB_1 , FB_3 , FB_4 as shown in diagram. Tie $LDTR$ to I_{O2} . To maintain specified linearity, external amplifiers must be zeroed. This is best done with V_{REF} set to zero and, the DAC register loaded with $10...0$ (MSB = 1), set R_{OS2} for $V_{OUT1} = 0V$. Then set R_{OS1} for $V_{OUT} = 0V$.

Grounding

Connect all GND pins to system analog ground and tie this to digital ground. All unused input pins must be grounded.

TIMING



ORDERING INFORMATION

Model	Monotonicity	Temperature Range	Package
Double-Buffered 12-Bit Multiplying DAC			
SP7512BN	12-Bit	-40°C to +85°C	28-pin, 0.3" SOIC
SP7512KN	12-Bit	0°C to +70°C	28-pin, 0.3" SOIC
HS3120C-2N	12-Bit	0°C to +70°C	28-pin, 0.6" Plastic DIP
HS3120C-2Q	12-Bit	0°C to +70°C	28-pin, 0.6" Side-Brazed DIP
HS3120B-2Q	12-Bit	-55°C to +125°C	28-pin, 0.6" Side-Brazed DIP
HS3120B-2/883	12-Bit	-55°C to +125°C	28-pin, 0.6" Side-Brazed DIP