

**100MHz, JFET Input, High Slew Rate, Uncompensated, Operational Amplifier**

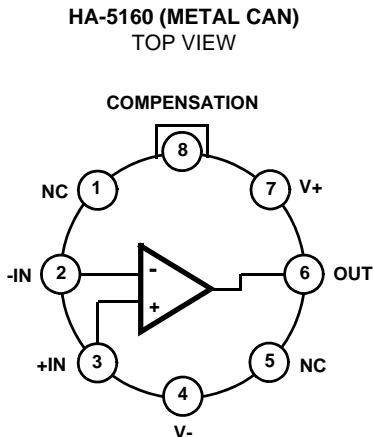
The HA-5160 is a wideband, uncompensated, operational amplifier with FET/Bipolar technologies and Dielectric Isolation. This monolithic amplifier features superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excellent input characteristics. This device has excellent phase margin at a closed loop gain of 10 without external compensation.

The HA-5160 offers a number of important advantages over similar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics, the Intersil devices have nearly constant slew rate, bandwidth, and settling characteristics over the operating temperature range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. Note also that Intersil specified all parameters at ambient (rather than junction) temperature to provide the designer meaningful data to predict actual operating performance.

Complementing the HA-5160's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and a very high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications. The HA-5160 provides excellent performance for applications which require both precision and high speed performance.

Military version (/883) data sheets are available upon request.

**Pinout**



NOTE: Case connected to V-.

**Features**

- Wide Gain Bandwidth ( $A_V \geq 10$ ) . . . . . 100MHz
- High Slew Rate . . . . . 120V/ $\mu$ s
- Settling Time . . . . . 280ns
- Power Bandwidth . . . . . 1.9MHz
- Offset Voltage . . . . . 1.0mV
- Bias Current . . . . . 20pA
- Compensation Pin for Unity Gain Capability

**Applications**

- Video and RF Amplifiers
- Data Acquisition
- Pulse Amplifiers
- Precision Signal Generation

**Ordering Information**

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA2-5160-5	HA2-5160-5	0 to 75	8 Pin Metal Can	T8.C

**Absolute Maximum Ratings**

Voltage Between V+ and V- ..... 40V  
 Differential Input Voltage ..... 40V  
 Peak Output Current ..... Full Short Circuit Protection

**Operating conditions**

Temperature Ranges  
 HA-5160-5 ..... 0°C to 75°C  
 Supply Voltage Range (Typical) ..... ±7V to ±18V

**Thermal Information**

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  (°C/W)  $\theta_{JC}$  (°C/W)  
 Metal Can Package ..... 155 67  
 Maximum Junction Temperature ..... 175°C  
 Maximum Storage Temperature Range ..... -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) ..... 300°C

**Die Characteristics**

Number of Transistors ..... 82  
 Substrate Potential (Powered Up) ..... Floating

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications**  $V_{SUPPLY} = \pm 15V$ , Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage		25	-	1	3	mV
		Full	-	3	5	mV
Offset Voltage Average Drift		Full	-	20	-	µV/°C
Bias Current		25	-	20	50	pA
		Full	-	5	10	nA
Offset Current		25	-	2	10	pA
		Full	-	2	5	nA
Input Capacitance		25	-	5	-	pF
Input Resistance		25	-	10 <sup>12</sup>	-	Ω
Common Mode Range		Full	±10	±11	-	V
<b>TRANSFER CHARACTERISTICS</b>						
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$ , $R_L = 2k\Omega$	25	75	150	-	kV/V
		Full	60	100	-	kV/V
Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	Full	74	80	-	dB
Minimum Stable Gain		25	10	-	-	V/V
Gain Bandwidth Product	$A_V \geq 10$	Full	-	100	-	MHz
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage Swing	$R_L = 2k\Omega$	25	±10	±11	-	V
		Full	±10	±11	-	V
Output Current	$V_{OUT} = \pm 10V$	25	±10	±20	-	mA
Output Short Circuit Current		25	-	±35	-	mA
Full Power Bandwidth (Note 2)	$V_{OUT} = \pm 10V$ , $R_L = 2k\Omega$	25	1.6	1.9	-	MHz
Output Resistance	Open Loop	25	-	50	-	Ω
<b>TRANSIENT RESPONSE</b> (Note 3)						
Rise Time	$A_V = +10$	25	-	20	-	ns
Slew Rate	$A_V = +10$	25	100	120	-	V/µs
Settling Time (Note 4)	$A_V = -10$	25	-	280	-	ns

**Electrical Specifications**  $V_{SUPPLY} = \pm 15V$ , Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY CHARACTERISTICS</b>						
Supply Current		Full	-	8	10	mA
Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 20V$	25	74	86	-	dB

NOTES:

- Full Power Bandwidth guaranteed, based on slew rate measurement using:  $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$ .
- Refer to Test circuits section of the data sheet.
- Settling Time is measured to 0.2% of final value for a 10V output step.

**Test Circuits and Waveforms**

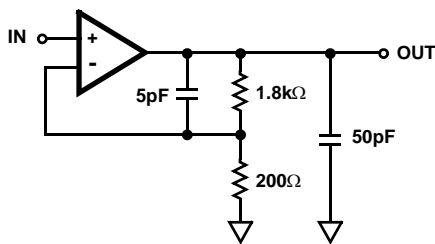
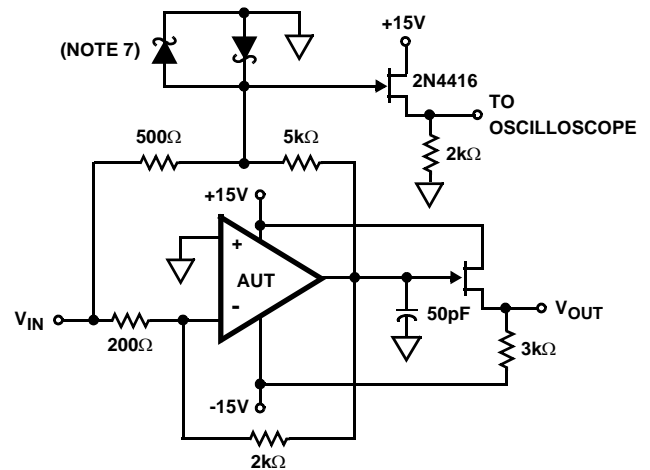


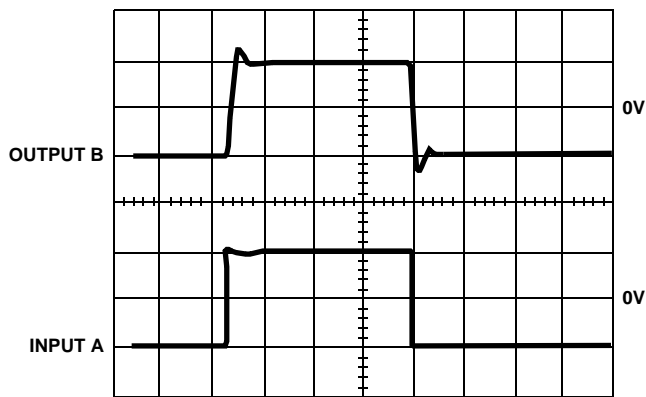
FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



NOTES:

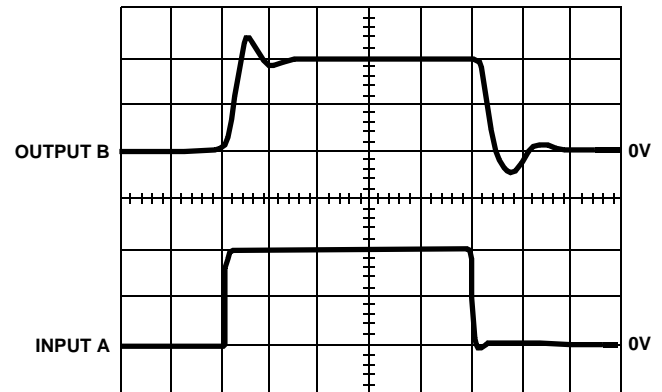
- $A_V = -10$ .
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 2. SETTLE TIME TEST CIRCUIT



Vertical Scale: A = 0.5V/Div., B = 5V/Div.  
Horizontal Scale: 500ns/Div.

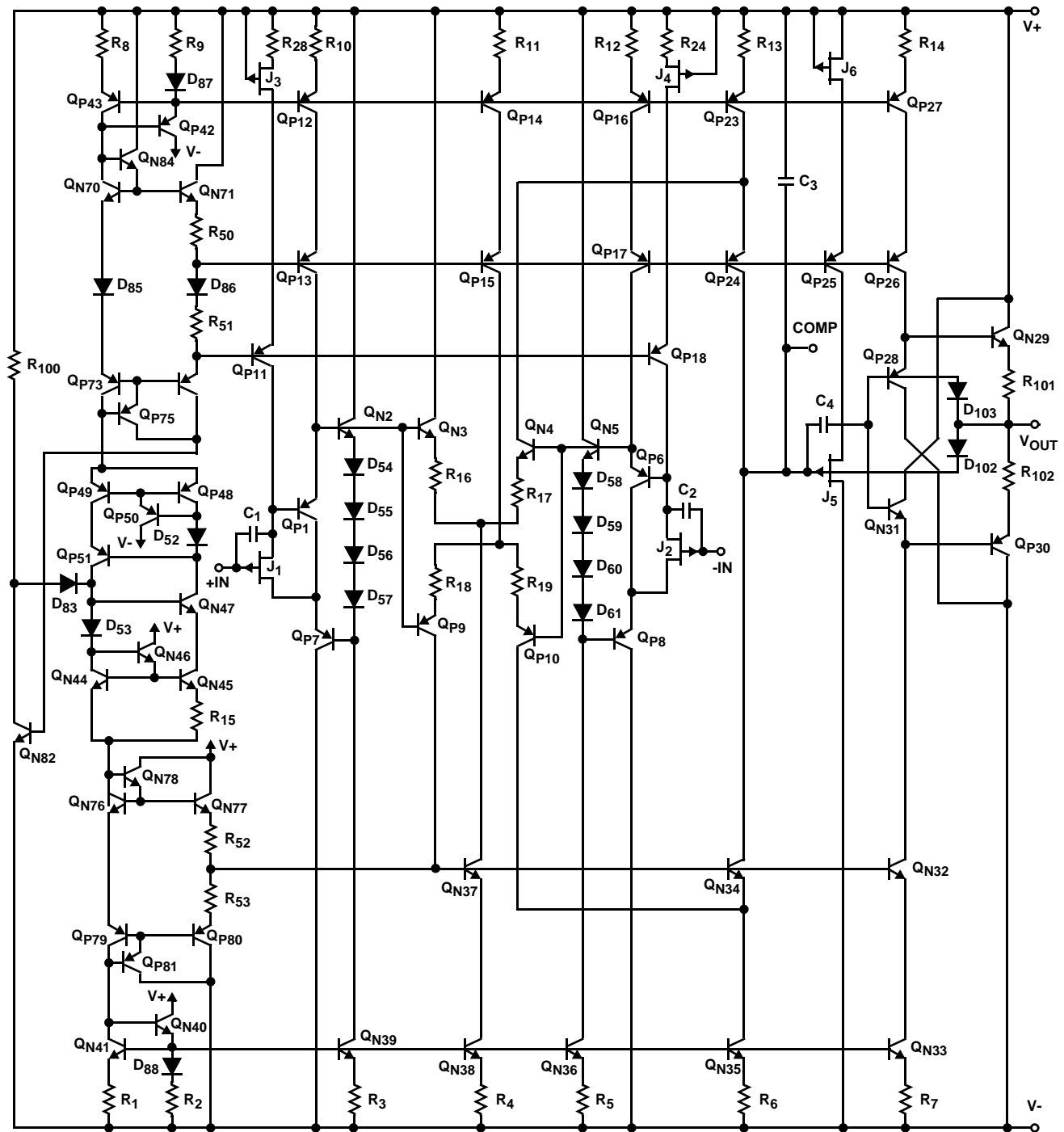
LARGE SIGNAL RESPONSE



Vertical Scale: A = 10mV/Div., B = 100mV/Div.  
Horizontal Scale: 100ns/Div.

SMALL SIGNAL RESPONSE

Schematic Diagram



**Application Information**

**Power Supply Decoupling**

Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01µF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

**Stability**

The phase margin of the HA-5160 will be improved by connecting a small capacitor (>10pF) between the output and the inverting input of the device. This small capacitor compensates for the input capacitance of the FET.

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**Capacitive Loads**

When driving large capacitive loads (>100pF), it is suggested that a small resistor (~100Ω) be connected in series with the output of the device and inside the feedback loop.

**Power Supply Minimum**

The absolute supply minimum is ±6V and the safe level is ±7V.

**Typical Applications** SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY (NOTE)

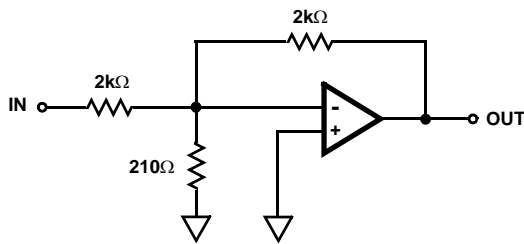
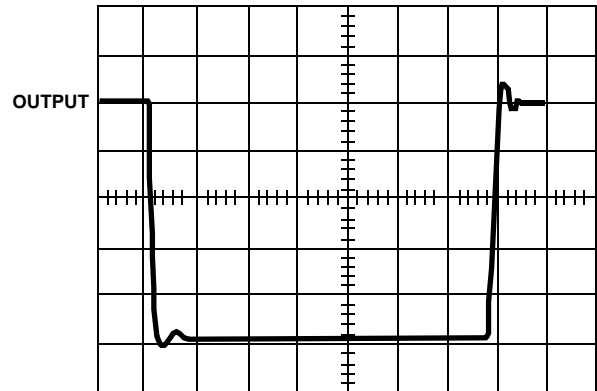


FIGURE 3A. INVERTING UNITY GAIN CIRCUIT



Vertical Scale: 2V/Div.  
Horizontal Scale: 500ns/Div.

FIGURE 3B. INVERTING UNITY GAIN PULSE RESPONSE

FIGURE 3. GAIN OF -1

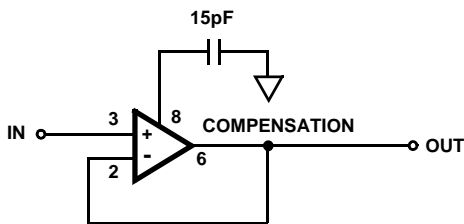
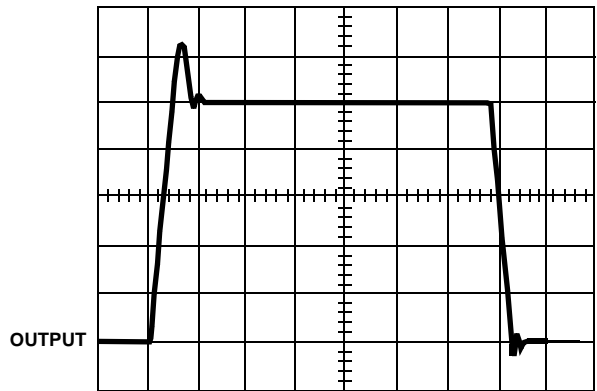


FIGURE 4A. NONINVERTING UNITY GAIN CIRCUIT



Vertical Scale: 2V/Div.  
Horizontal Scale: 500ns/Div.

FIGURE 4B. NONINVERTING UNITY GAIN PULSE RESPONSE

FIGURE 4. GAIN OF +1

NOTE: Values were determined experimentally for optimum speed and settling time.

Typical Performance Curves

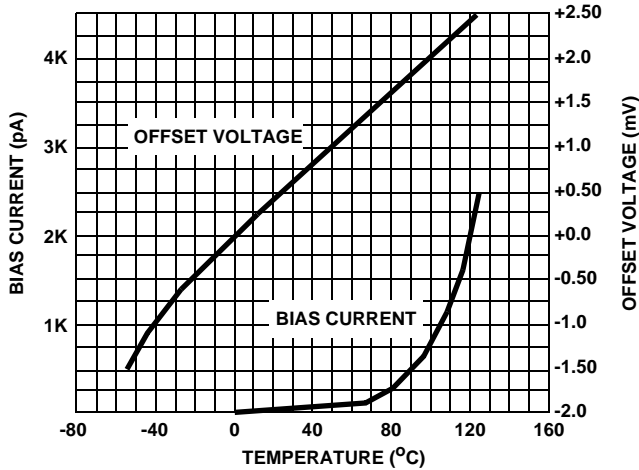


FIGURE 5. INPUT OFFSET VOLTAGE AND BIAS CURRENT vs TEMPERATURE

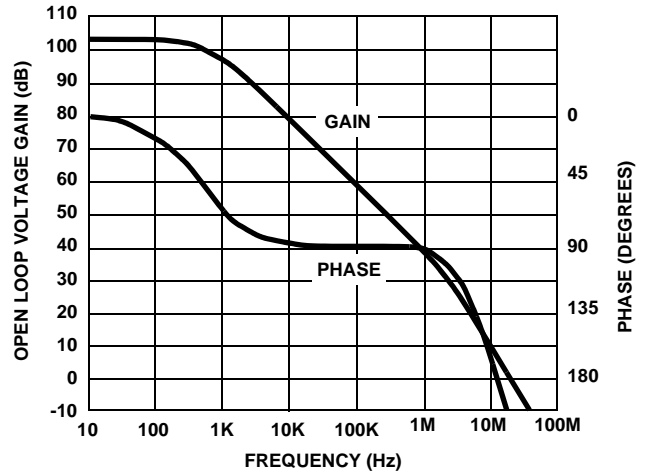


FIGURE 6. OPEN LOOP FREQUENCY RESPONSE

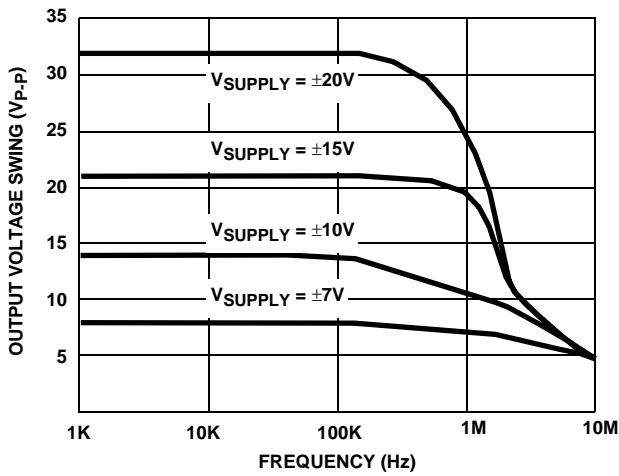


FIGURE 7. OUTPUT VOLTAGE SWING vs FREQUENCY

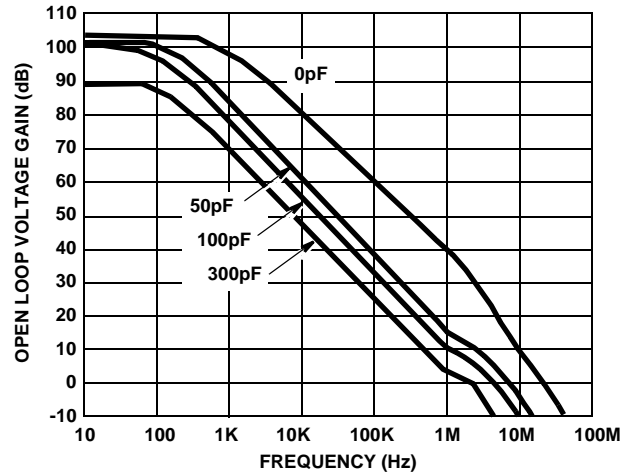


FIGURE 8. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS COMPENSATION CAPACITANCES

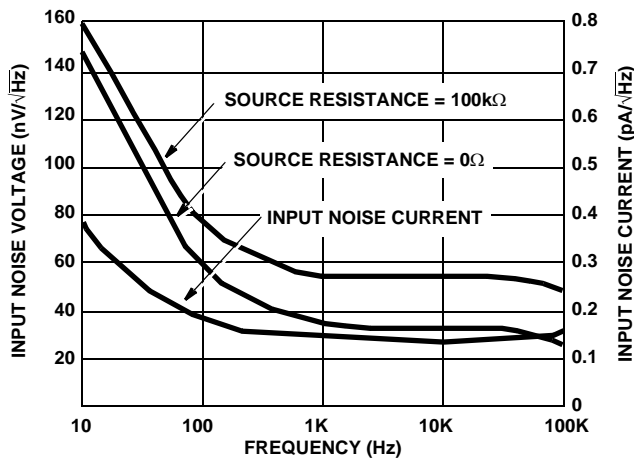


FIGURE 9. INPUT NOISE VOLTAGE AND NOISE CURRENT vs FREQUENCY

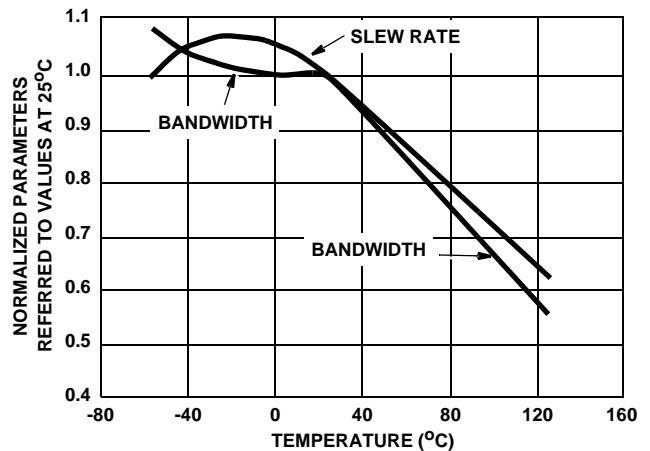


FIGURE 10. NORMALIZED AC PARAMETERS vs TEMPERATURE

Typical Performance Curves (Continued)

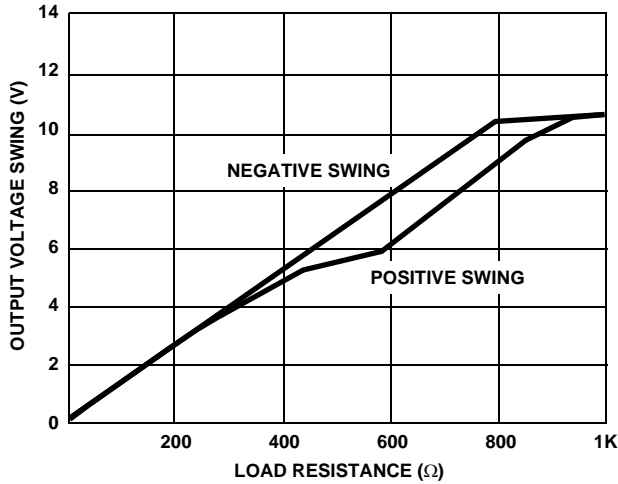


FIGURE 11. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

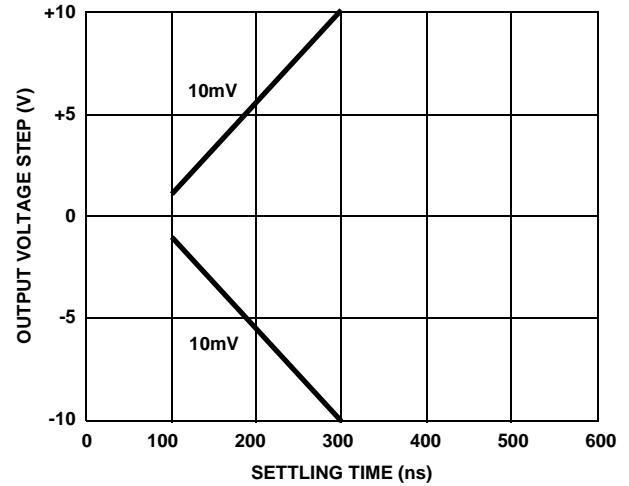


FIGURE 12. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

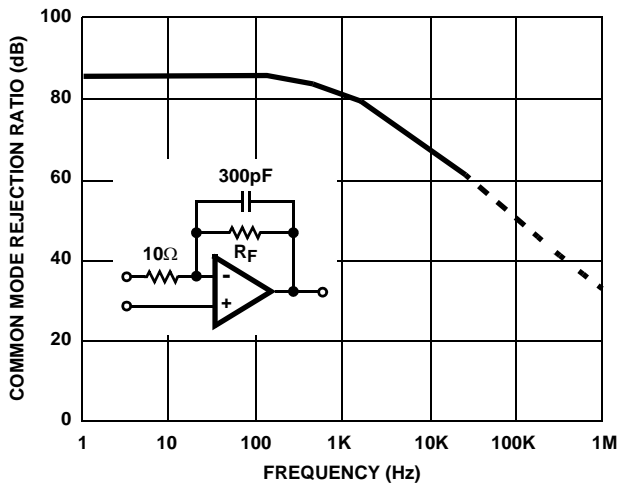


FIGURE 13. COMMON MODE REJECTION RATIO vs FREQUENCY

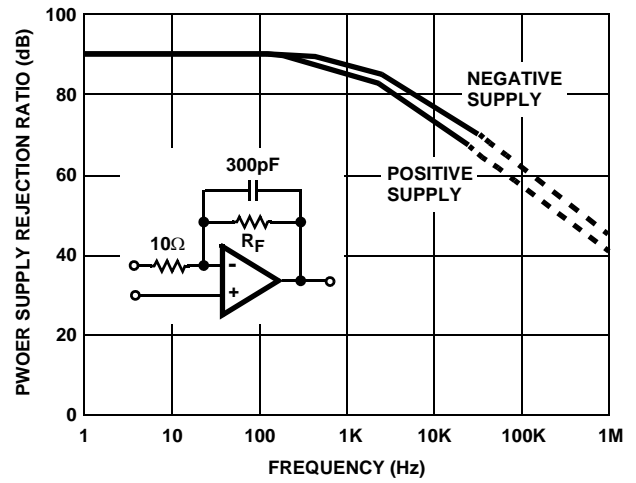


FIGURE 14. POWER SUPPLY REJECTION RATIO vs FREQUENCY

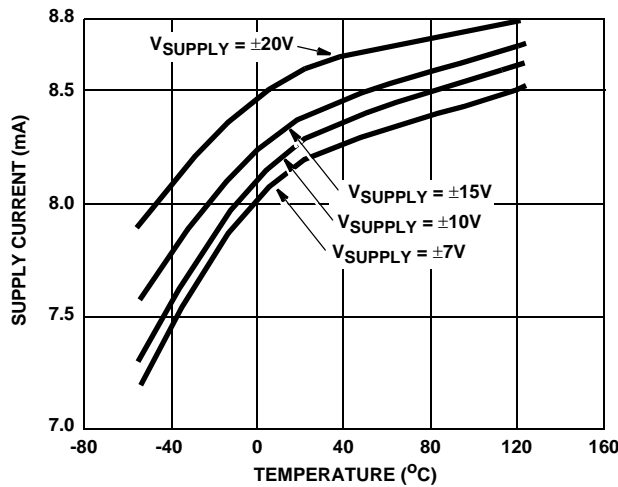
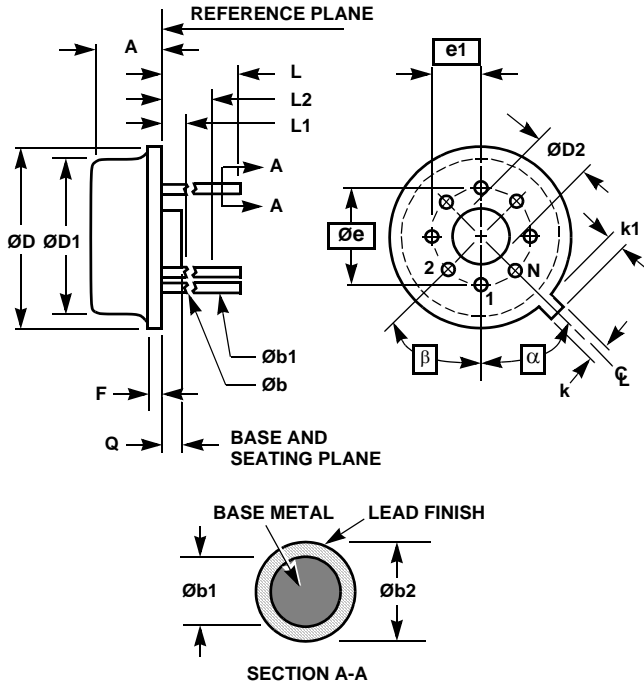


FIGURE 15. POWER SUPPLY CURRENT vs TEMPERATURE

**Metal Can Packages (Can)**



**T8.C MIL-STD-1835 MACY1-X8 (A1)  
8 LEAD METAL CAN PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	0.110	0.160	2.79	4.06	-
e	0.200 BSC		5.08 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	45° BSC		45° BSC		3
β	45° BSC		45° BSC		3
N	8		8		4

Rev. 0 5/18/94

**NOTES:**

- (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
- Measured from maximum diameter of the product.
- α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N - 1 places) from α, looking at the bottom of the package.
- N is the maximum number of terminal positions.
- Dimensioning and tolerancing per ANSI Y14.5M - 1982.
- Controlling dimension: INCH.

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Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

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