EClamp3343C
USB 2.0 & USB OTG EMI/RFI Filter, Termination, and ESD Protection

PROTECTION PRODUCTS - EMIClamp™

Description

The EClamp™3343C is designed to satisfy the termination and filtering requirements of USB On the Go (OTG) and USB 2.0 low and full speed operation. The termination is set by a 33 ohm resistor. The filtering and edge rate control is accomplished with 47pF capacitors on each USB data line. This device is also designed to provide electrostatic discharge (ESD) protection in excess of 15kV (Air) and 8kV (Contact) per IEC 61000-4-2, level 4 on both data (D+, D-) lines as well as the voltage bus and ID pins.

USB upstream and downstream port are identified by terminating the data lines with either a pull up resisitor or pull down resistor. This device may be used on either type of port by changing the pin connections. For upstream applications, separate bumps are provided for protection of the VBus line (5.25V) and the pull up resistor connection to the 3.3V supply (V_{TRM}) as required by the USB specification. For downstream applications, this device also supplies the option for 15kΩ pulldown resistors on the D+ and D- line.

For USB OTG applications, the device can be configured as upstream(peripheral) by connecting a 1.5kΩ pull-up resistor from the D+ line to the 3.3V supply. To configure the device as a downstream(host), 15kΩ pull-down resistors are connected from both the D+ and D- lines to ground. TVS diodes provide ESD protection of both (D+ and D-) data lines, the ID pin, and the voltage bus (V_{BUS}).

Features

- Compliant to **USB 1.1, USB2.0** (low and full speed) and **USB OTG** requirements
- ESD protection for USB power (V_{BUS}), ID, and data lines (D+ & D-) to **IEC 61000-4-2 Level 4**
- 33 Ohm series resistor
- Connections for both 1.5K Ohm pull up resistors and 15K Ohm pull down resistors
- Separate connections for 5.25V V_{BUS} and 3.3V supply voltage
- Low TVS operating voltage (5.25V)
- Low leakage current
- Solid-state technology

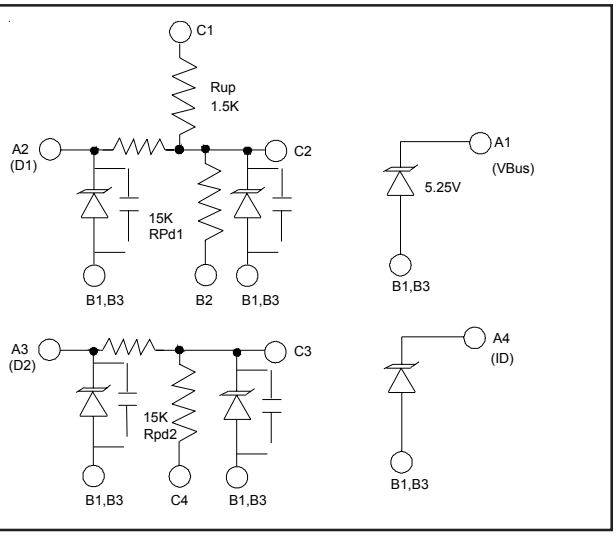
Mechanical Characteristics

- 11-bump, 0.5mm pitch, flip chip
- Bump Diameter: 315+/-20 µm
- Non-conductive top side coating
- Marking : Orientation Mark and Marking Code
- Packaging : Tape and Reel per EIA 481

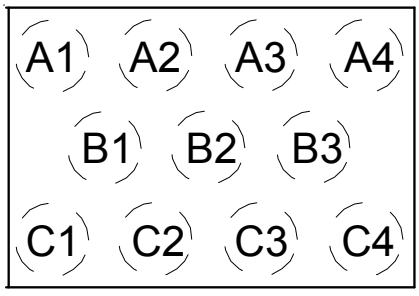
Applications

- USB OTG
- USB 2.0 Upstream Ports (Low and Full Speed)
- USB 2.0 Downstream Ports (Low and Full Speed)
- Cellular Handsets
- Set Top Box
- Portable Electronics
- PC Peripherals

Circuit Diagram



Schematic & PIN Configuration



11-Bump Flip Chip TVS (Top/Ball Down View)

Maximum Ratings

Rating	Symbol	Value	Units
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	>15 >8	kV
Junction Temperature	T_J	125	°C
Operating Temperature	T_{op}	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics

EClamp3343C						
Parameter	**Symbol**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
TVS Reverse Stand-Off Voltage	V_{RWM}				5.25	V
TVS Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	6			V
TVS Reverse Leakage Current	I_R	V_{RWM}= 5.25V, T=25 °C V_{Bus} and ID pin & Ground			5	µA
TVS Reverse Leakage Current	I_R	V_{RWM}= 3.3V, T=25 °C Between any data pin (D+, D-) and Ground			1	µA
Series Resistance	R_S	Each Line	30	33	36	Ohms
Pull Up Resistance	R_{PU}		1.35	1.5	1.65	kOhms
Pulldown Resistance	R_{PD}		13.5	15	16.5	kOhms
Total Capacitance	C_{TOT}	Input or Output to Ground V_R = 0V, f = 1MHz		47	60	pF

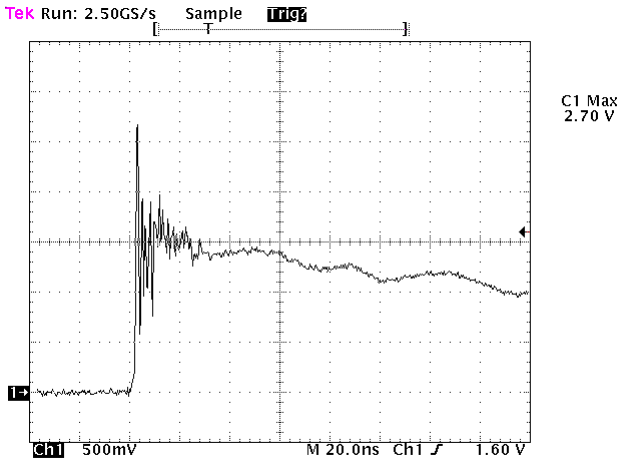
Pin Identification

Pin	Identification
A1	Vbus
A2	D1 In
A3	D2 In
A4	ID
B1	Gnd
B2	R_{down1}

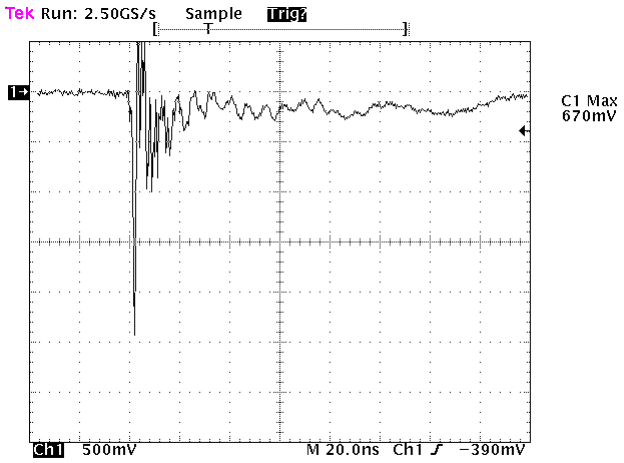
Pin	Identification
B3	Gnd
C1	R_{up}
C2	D1 Out
C3	D2 Out
C4	R_{down2}

Typical Characteristics

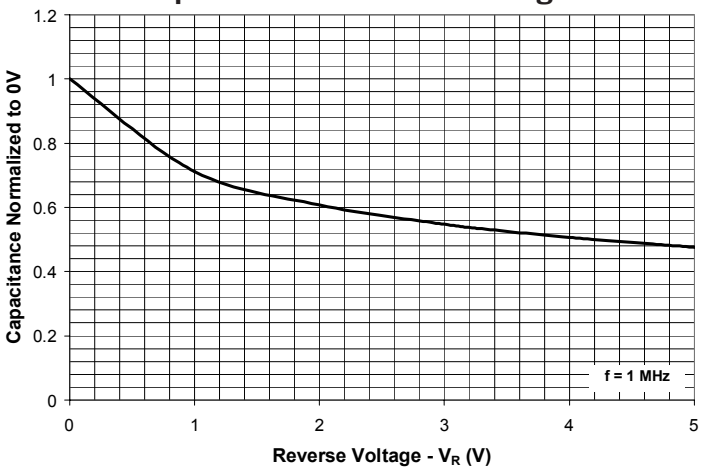
ESD Clamping (+8kV Contact)



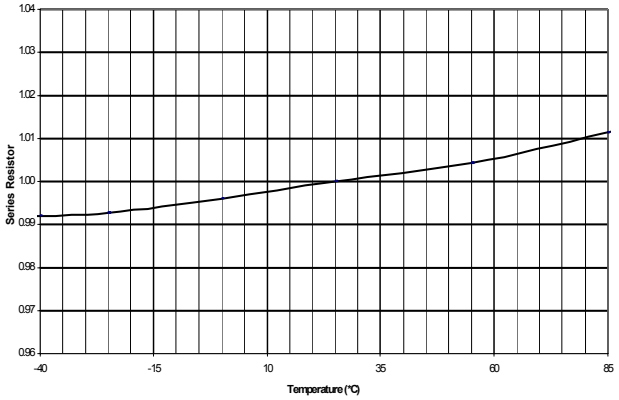
ESD Clamping (-8kV Contact)



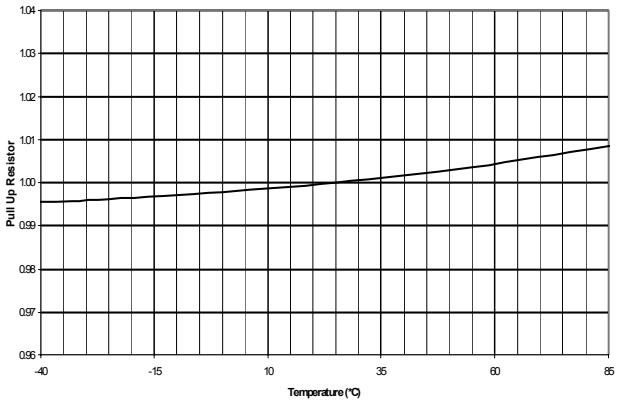
Capacitance vs. Reverse Voltage



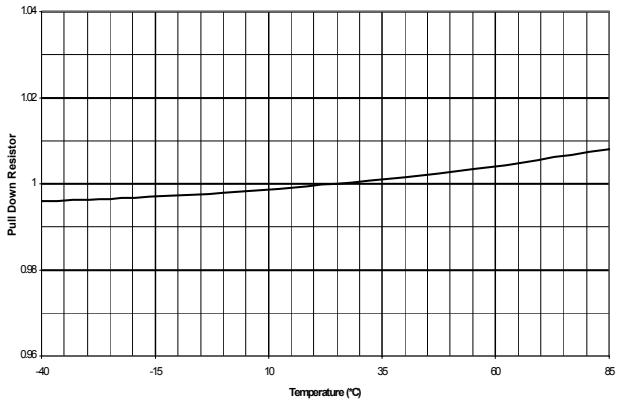
Normalized Series Resistance vs. Temperature



Normalized Pull Up Resistance vs. Temperature



Normalized Pull Down Resistance vs. Temperature



Applications Information

The EClamp3343C is designed for termination and ESD/EMI protection of USB ports operating to 12Mb/s. This includes USB 1.1, USB 2.0 (low and full speed options) and USB OTG. The device includes the necessary pull up and pull down resistors to configure standard USB ports for either upstream or down stream configuration. The device pin configuration is shown in Figure 1. Since USB is a hot plug system, the potential for an ESD discharge into the USB port is high. ESD protection is provided on the D+ and D- data lines. Options for ESD protection on the voltage bus and ID (USB OTG) pins are also included. All ESD protection meets the requirements of IEC 61000-4-2, Level 4. The device connection options are detailed below.

Figure 1. Device Pin Connections

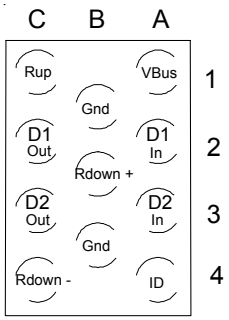
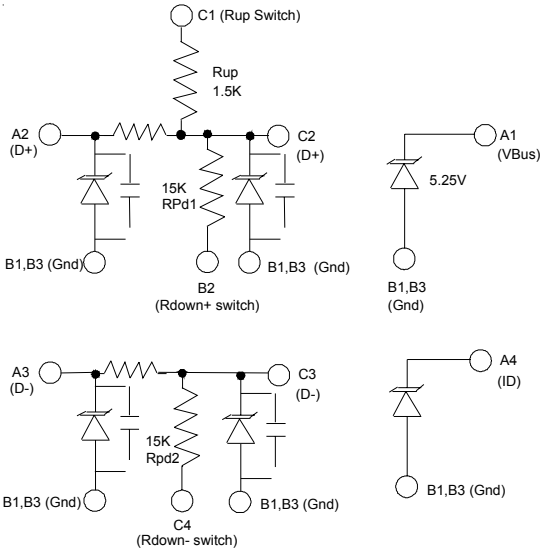


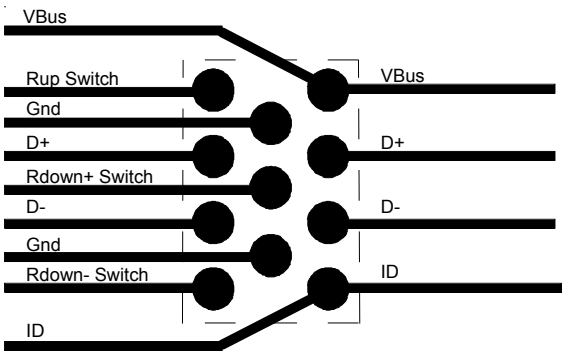
Figure 2. USB OTG Schematic



USB OTG

USB OTG provides a solution for point-to-point communication between portable devices. As such, USB OTG devices have to be able to switch between host and peripheral roles. Figure 2 shows schematically the R and C configuration for a USB OTG port. Figure 3 shows the layout to connect the ECalmp3343C for a USB OTG application. The USB OTG transceiver can configure the device via an external switch connected between the pull up resistor at C1 and the pull down resistors at B2 and C4. An upstream (peripheral) connection would select the pull up resistor while a downstream (host) connection would select the two pull down resistors. When in use, the pull up resistor is connected to the 3.3 volt regulated USB voltage (V_{TERM}). The unregulated USB voltage bus connection should be made at bump A1. ESD protection is achieved at this connection by a TVS with a rated stand-off voltage of 5.25 volts per the USB specification. An ID pin is used to identify the device as host or peripheral by taking the connection low (host) or high (peripheral). ESD protection is provided for this connection with a 5 volt TVS at bump A4. The input (connector side) of the D+ and D- data lines are connected at bumps A2 and A3 respectively. The outputs (Transceiver side) are connected at bumps C2 and C3 respectively. Each of these lines is terminated with a 33 Ohm resistor. Each line also features a dual stage of ESD protection. Ground connections are made at bumps B1 and B3.

Figure 3. USB OTG Layout



Applications Information

USB Upstream Ports

Upstream (peripheral) ports are identified with a 1.5k Ohm pull up resistor on the D+ line (for full speed operation) and on the D- line (for low speed). The pull up resistor should be connected to the 3.3 volt regulated USB voltage (V_{TERM}). The unregulated USB voltage bus connection should be made at bump A1. ESD protection is achieved at this connection by a TVS with a rated stand-off voltage of 5.25 volts per the USB specification. The input (connector side) of the D+ and D- data lines are connected at bumps A2 and A3. For full speed ports, D+ is connected to A2 and D- is connected to A3 as shown in Figure 4 and 5. For low speed ports, D- is connected to A2 and D+ is connected to A3 as shown in Figure 6 and 7. The outputs (Transceiver side) are connected at bumps C2 and C3 respectively. Each of these lines is terminated with a 33 Ohm resistor. Each line also features a dual stage of ESD protection. Bumps B2, C4, and A4 are not connected. Ground connections are made at bumps B1 and B3.

Figure 4. USB Upstream Schematic (Full Speed)

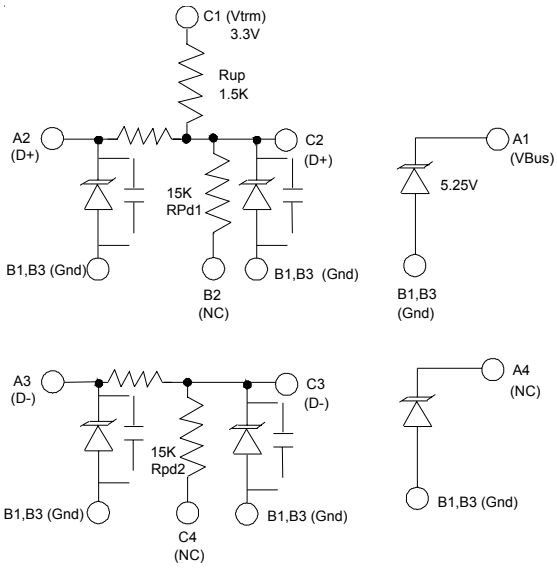


Figure 5. USB Upstream Layout (Full Speed)

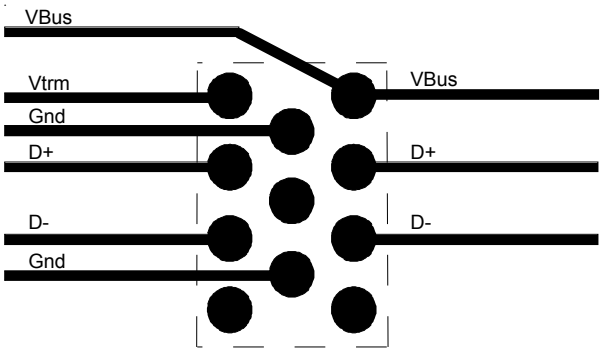


Figure 6. USB Upstream Schematic (Low Speed)

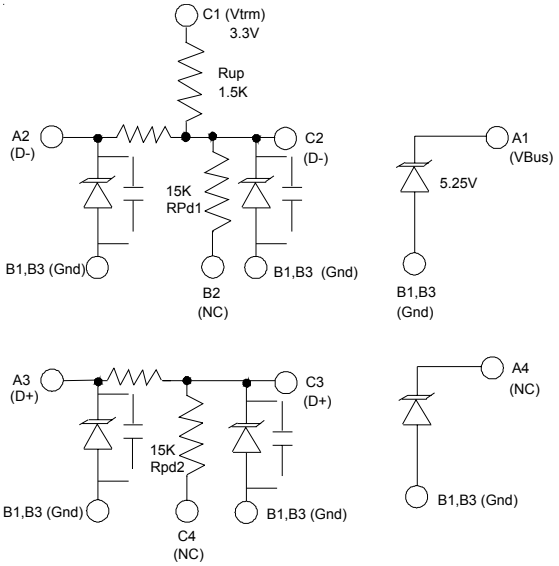
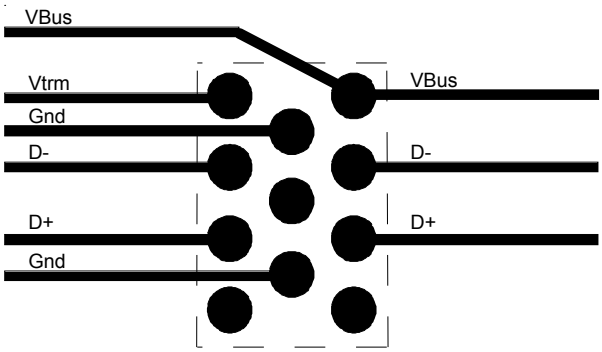


Figure 7. USB Upstream Layout (Low Speed)



USB Downstream Ports

USB downstream (host) ports are identified by 15k Ohm pull down resistors on both the D+ and D- lines as shown in Figure 8. The pull down resistors are made available by connecting bumps B2 and C4 to ground. Bumps B1 and B3 should also be tied to ground. Bumps C1 and A4 are not connected. An example layout in shown in Figure 9. All other connections are as described in the upstream port section.

Figure 8. USB Downstream Schematic

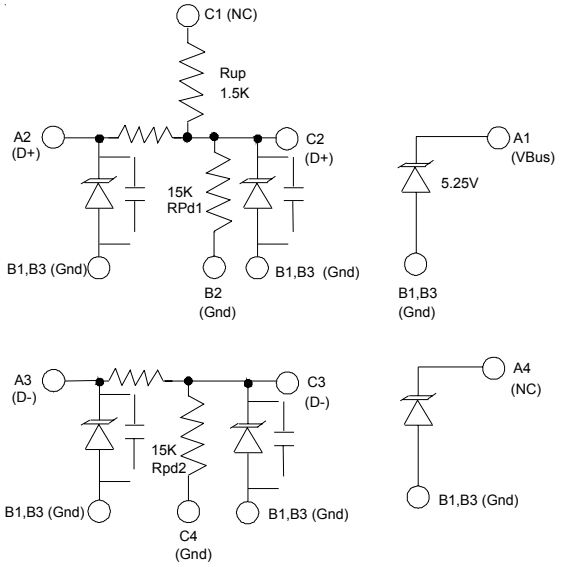
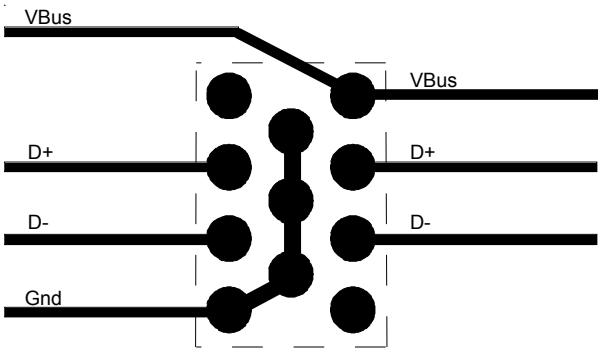


Figure 9. USB Downstream Layout



Applications Information

Designing with Flip Chip TVS

When designing with flip chip TVS devices, certain precautions and design considerations have to be observed to ensure for maximum solder joint reliability. These include solder pad definition, board finish, and assembly parameters.

Printed Circuit Board Mounting

Non-solder mask defined (NSMD) land patterns are recommended for mounting flip chip devices. Solder mask defined (SMD) pads produce stress points at the solder mask to solder ball interface that can result in solder joint cracking when exposed to extreme fatigue conditions. The recommended pad size is 0.275 ± 0.010 mm with a minimum solder mask opening of 0.325 mm.

Grid Courtyard

The recommended grid placement courtyard is 2.0 x 1.4 mm. The grid courtyard is intended to encompass the land pattern and the component body that is centered in the land pattern. When placing parts on a PCB, the highest recommended density is when one courtyard touches another.

Printed Circuit Board Finish

A uniform board finish is critical for good assembly yield. Two finishes that provide uniform surface coatings are immersion nickel gold and organic surface protectant (OSP). A non-uniform finish such as hot air solder leveling (HASL) can lead to mounting problems and should be avoided.

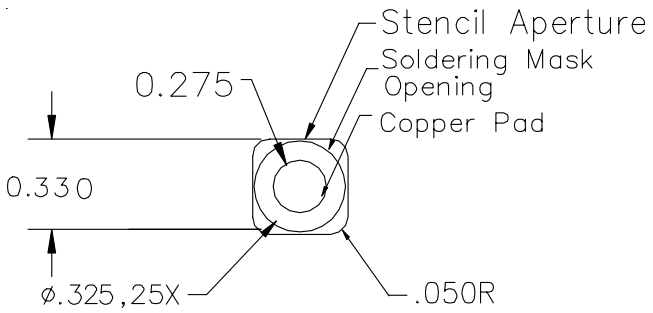
Stencil Design

A properly designed stencil is key to achieving adequate solder volume without compromising assembly yields. A 0.100mm to 0.200mm thick, laser cut, electro-polished stencil with 0.330mm apertures corners with rounded corners is recommended.

Reflow Profile

The flip chip TVS can be assembled using the reflow requirements for IPC/JEDEC standard J-STD-020 for assembly of small body components. During reflow, the component will self-align itself on the pad.

Recommended NSMD Pad and Stencil Aperture

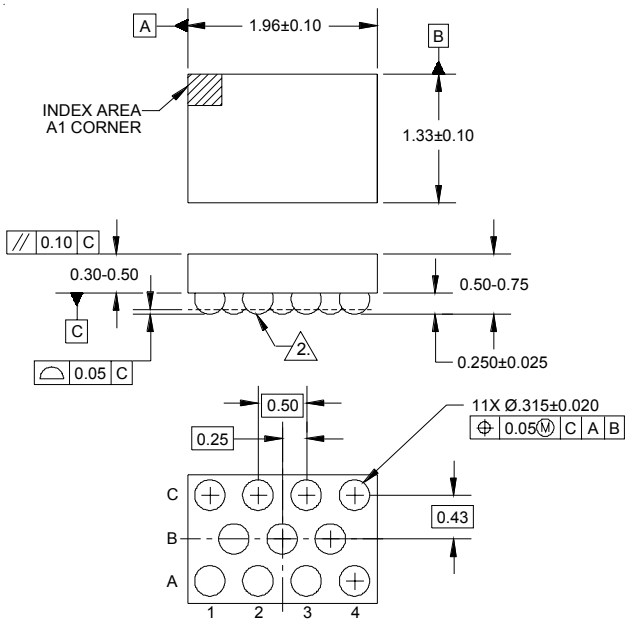


Assembly Guideline for Pb-Free Soldering

The following are recommendations for the assembly of this device:

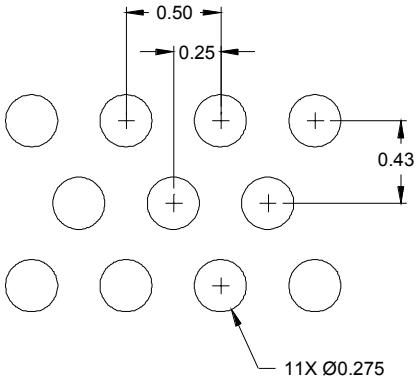
Assembly Parameter	Recommendation
Solder Ball Composition	95.5Sn/3.8Ag/0.7Cu
Solder Stencil Design	Same as the SnPb design
Solder Stencil Thickness	0.100 mm to 0.200 mm
Solder Paste Composition	Sn Ag (3-4) Cu (0.5-0.9)
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	per JEDEC J-STD-020
PCB Solder Pad Design	Same as the SnPb Design
PCB Pad Finish	OSP or AuNi

Outline Drawing - 11 Bump Flip Chip



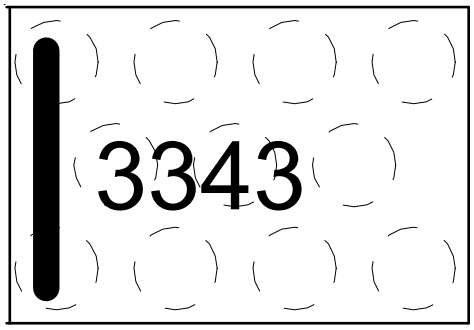
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS
2. Sn63/Pb37 FOR STANDARD DEVICES OR Sn95.5/Ag3.8/Cu0.7 FOR Pb-FREE DEVICES.

Land Pattern - 11 Bump Flip Chip



NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking



Top View Showing Laser Mark

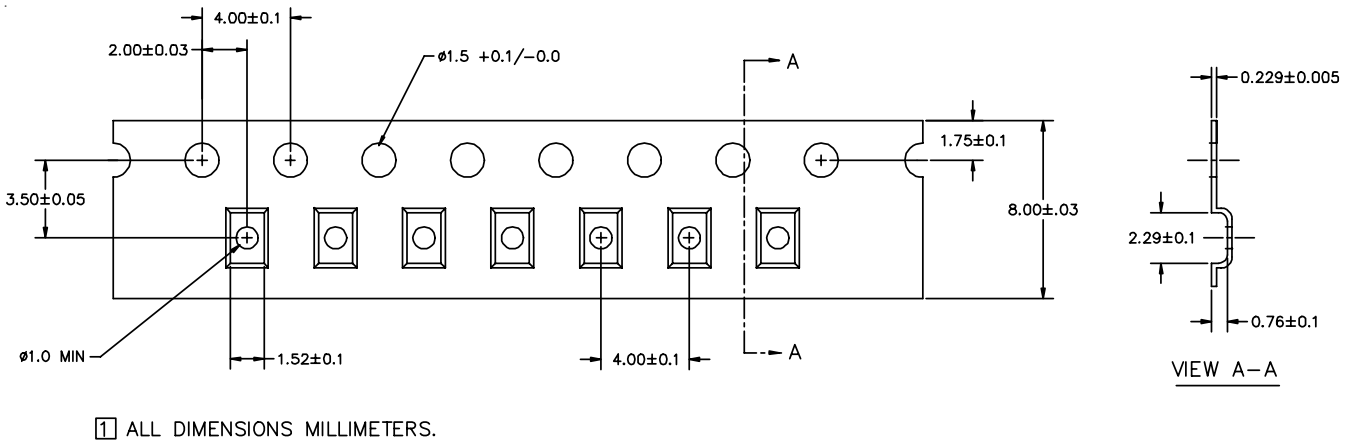
Top Coating: The top (non-bump side) of the device is a white non-conductive coating. The coating is laser markable and increases mechanical durability. This material is compliant with UL 94V-0 flammability requirements.

Ordering Information

Part Number	Solder Ball Composition	Qty per Reel	Reel Size
EClamp3343C.WC	SnPb	3000	7 Inch
EClamp3343C.WCT	SnAgCu	3000	7 Inch

EMIClamp and EClamp are marks of Semtech Corporation

Tape and Reel Specification



Tape Specifications

Contact Information

Semtech Corporation
Protection Products Division
200 Flynn Rd., Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804