

PROTECTION PRODUCTS - EMIClamp™

Description

The EClamp™2340C is a low pass filter array with integrated TVS diodes. It is designed to suppress unwanted EMI/RFI signals and provide electrostatic discharge (ESD) protection in portable electronic equipment. This state-of-the-art device utilizes solid-state silicon-avalanche technology for superior clamping performance and DC electrical characteristics. They have been optimized for **protection of color LCD panels** in cellular phones and other portable electronics.

The device consists of ten identical circuits comprised of TVS diodes for ESD protection, and a resistor - capacitor network for EMI/RFI filtering. A series resistor value of 100Ω and a capacitance value of 18pF is used to achieve 20dB minimum attenuation from 800MHz to 3GHz. Each line features two stages of TVS diode protection. The TVS diodes provide effective suppression of ESD voltages in excess of 15kV (air discharge) and 8kV (contact discharge) per IEC 61000-4-2, level 4.

The device is a 25-bump, 0.5mm pitch flip chip array with a 5x5 bump grid. It measures 2.6 x 2.6 x 0.65mm. The solder bumps have a nominal diameter of 0.315mm.

Features

- ◆ Flip Chip bidirectional EMI/RFI filter with integrated ESD protection
- ◆ ESD protection to **IEC 61000-4-2 (ESD) Level4, +/-15kV (air), +/-8kV (contact)**
- ◆ Filter performance: 20dB minimum attenuation 800MHz to 3GHz
- ◆ TVS working voltage: 5V
- ◆ Resistor: 100 Ohms
- ◆ Input Capacitance: 18pF (VR = 2.5V_{DC})
- ◆ Protection and filtering for ten lines
- ◆ Solid-state technology

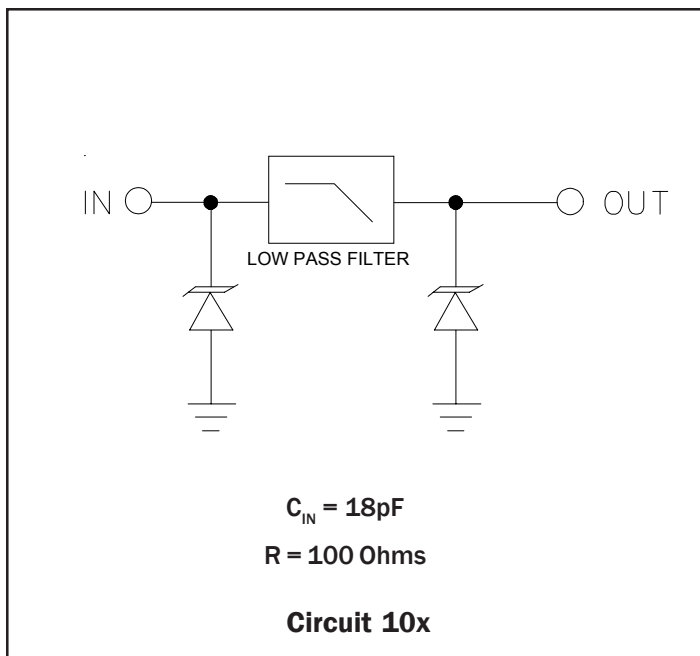
Mechanical Characteristics

- ◆ JEDEC MO-211, 0.50 mm pitch flip chip
- ◆ Nominal Dimensions: 2.6 x 2.6 x 0.65 mm
- ◆ Bump Diameter: 315+/-20 μm
- ◆ Non-conductive top side coating
- ◆ Marking : Mark code, lot code, orientation mark
- ◆ Packaging : Tape and Reel per EIA 481

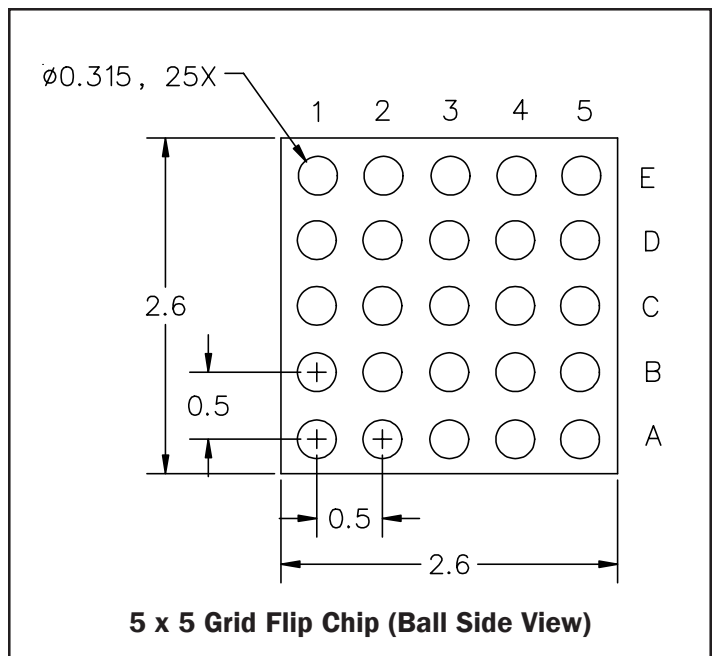
Applications

- ◆ Color LCD Panel Protection
- ◆ Cell Phone CCD Camera Lines
- ◆ Personal Digital Assistants (PDA's)

Circuit Diagram



PIN Configuration



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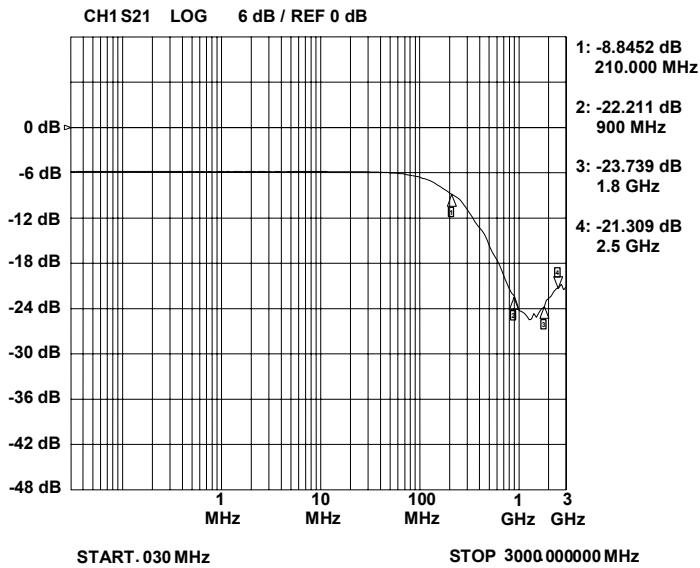
Absolute Maximum Rating

Rating	Symbol	Value	Units
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	+/- 15 +/- 15	kV
Junction Temperature	T_J	125	°C
Operating Temperature	T_{op}	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

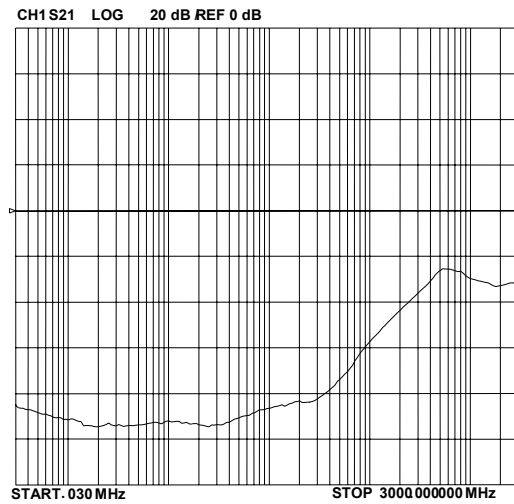
Electrical Characteristics (T=25°C)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
TVS Reverse Stand-Off Voltage	V_{RWM}				5	V
TVS Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	6	8	10	V
TVS Reverse Leakage Current	I_R	$V_{RWM} = 3.0V$			0.5	μA
Total Series Resistance	R	Each Line	85	100	115	Ohms
Total Capacitance	C_{in}	Input to Ground, Each Line $V_R = 0V, f = 1MHz$			27	pF
Total Capacitance	C_{in}	Input to Ground, Each Line $V_R = 2.5V, f = 1MHz$			18	pF

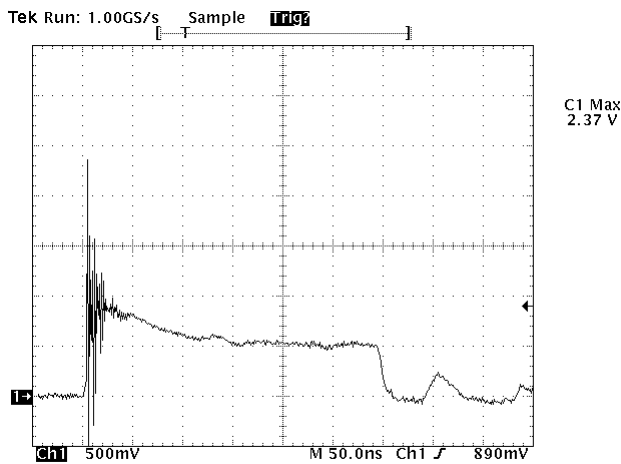
Typical Insertion Loss S21 (Each Line)



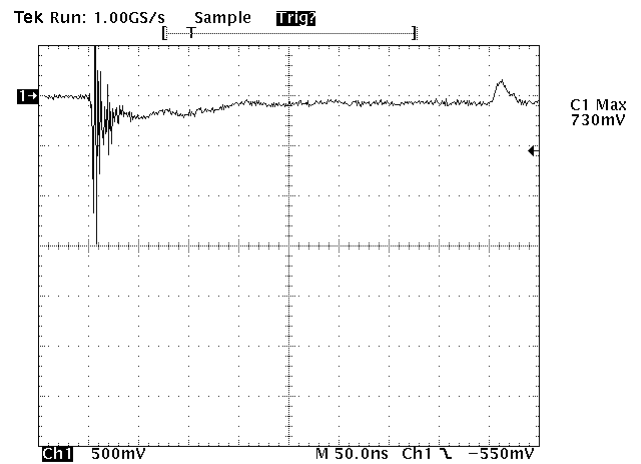
Analog Crosstalk (Each Line)



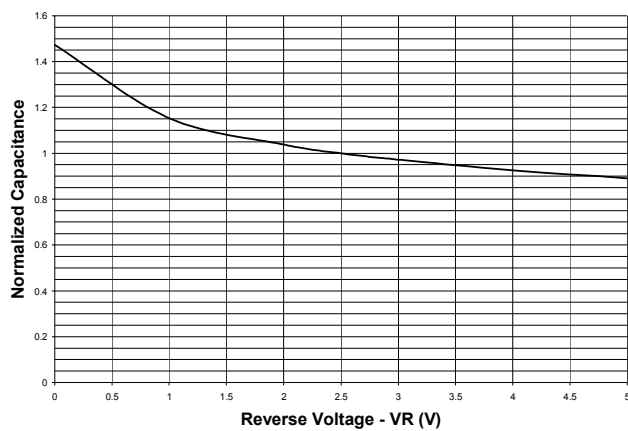
ESD Clamping (+8kV Contact)



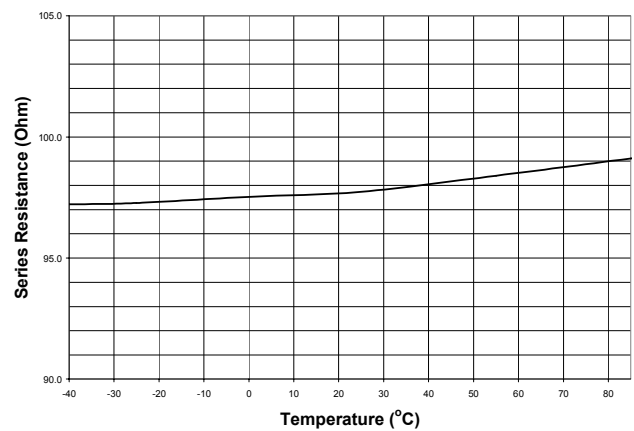
ESD Clamping (-8kV Contact)



Capacitance vs. Reverse Voltage (Normalized to 2.5 volts)



Series Resistance vs. Temperature



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Applications Information

Device Connection Options

The EClamp2340C has solder bumps located in a 5 x 5 matrix layout on the active side of the device. The bumps are designated by the numbers 1 - 5 along the horizontal axis and letters A - E along the vertical axis. The input of the lines to be protected are connected at bumps A1 - A5 and B1 - B5. The line outputs are connected at bumps D1 - D5 and E1 - E5. Bumps C1 - C5 are connected to ground. All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces.

Flip Chip TVS

Flip chip TVS devices are wafer level chip scale packages. They eliminate external plastic packages and leads and thus result in a significant board space savings. Manufacturing costs are minimized since they do not require an intermediate level interconnect or interposer layer for reliable operation. They are compatible with current pick and place equipment further reducing manufacturing costs. Certain precautions and design considerations have to be observed however for maximum solder joint reliability. These include solder pad definition, board finish, and assembly parameters.

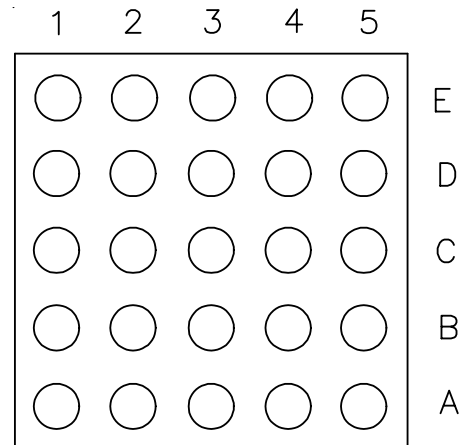
Printed Circuit Board Mounting

Non-solder mask defined (NSMD) land patterns are recommended for mounting flip chip devices. Solder mask defined (SMD) pads produce stress points at the solder mask to solder ball interface that can result in solder joint cracking when exposed to extreme fatigue conditions. The recommended pad size is 0.275 ± 0.010 mm with a minimum solder mask opening of 0.325 mm.

Grid Courtyard

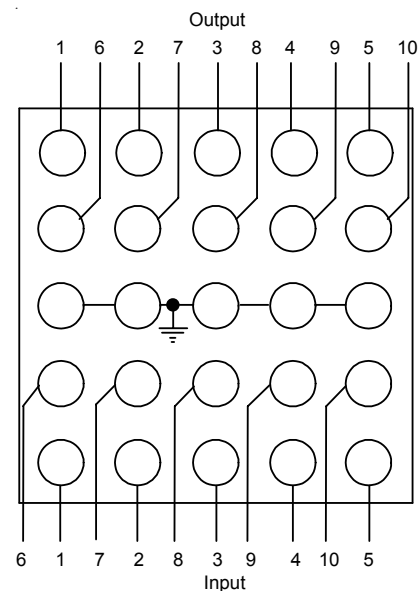
The recommended grid placement courtyard is 2.7 x 2.7 mm. The grid courtyard is intended to encompass the land pattern and the component body that is centered in the land pattern. When placing parts on a PCB, the highest recommended density is when one courtyard touches another.

Pin Identification and Configuration (Ball Side View)



Pin	Identification
A1 - A5	Input, Lines 1, 2, 3, 4, 5
B1 - B5	Input, Lines 6, 7, 8, 9, 10
C1 - C5	Ground
D1 - D5	Output, Lines 6, 7, 8, 9, 10
E1 - E5	Output, Lines 1, 2, 3, 4, 5

Layout Example (Ball Side View)



Printed Circuit Board Finish

A uniform board finish is critical for good assembly yield. Two finishes that provide uniform surface coatings are immersion nickel gold and organic surface protectant (OSP). A non-uniform finish such as hot air solder leveling (HASL) can lead to mounting problems and should be avoided.

Stencil Design

A properly designed stencil is key to achieving adequate solder volume without compromising assembly yields. A 0.100mm thick, laser cut, electro-polished stencil with 0.330mm apertures corners with rounded corners is recommended.

Reflow Profile

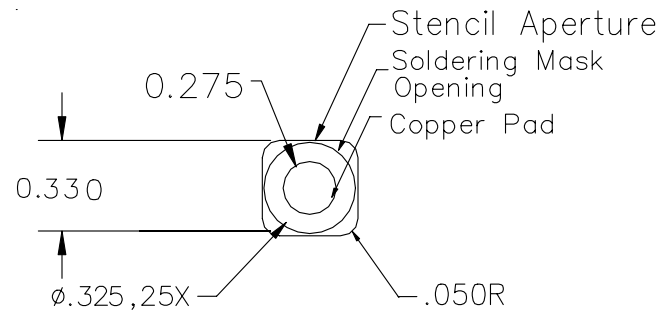
The flip chip TVS can be assembled using the reflow requirements for IPC/JEDEC standard J-STD-020 for assembly of small body components. During reflow, the component will self-align itself on the pad.

Circuit Board Layout Recommendations for Suppression of ESD

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

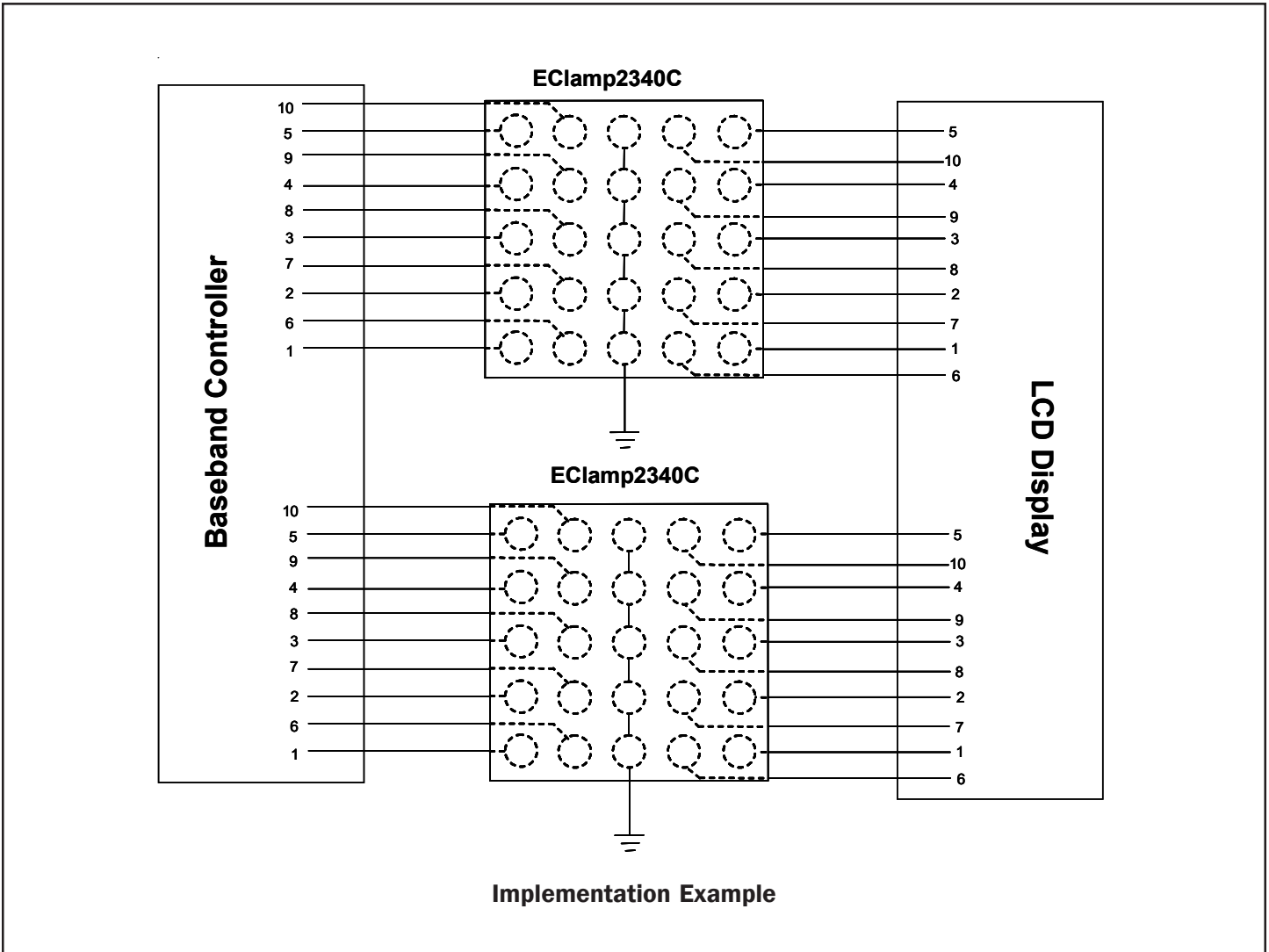
Recommended NSMD Pad and Stencil Aperture



Assembly Guideline for Pb-Free Soldering

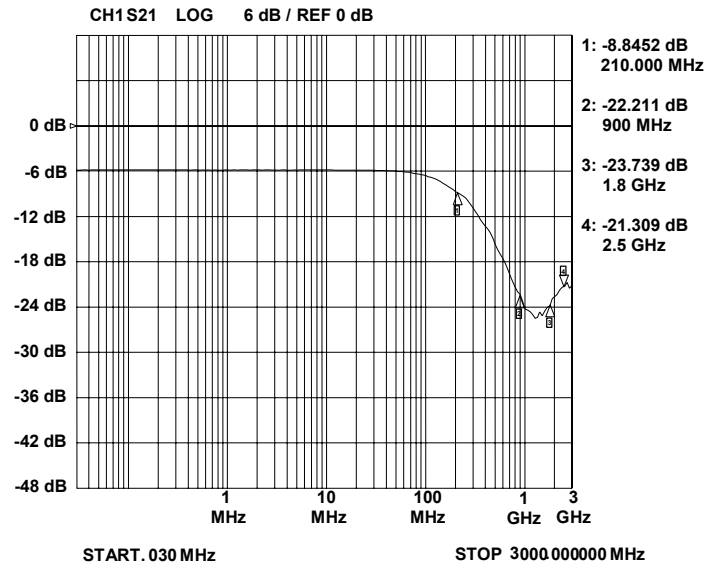
The following are recommendations for the assembly of this device:

Assembly Parameter	Recommendation
Solder Ball Composition	95.5Sn/3.8Ag/0.7Cu
Solder Stencil Design	Same as the SnPb design
Solder Stencil Thickness	0.100 mm (0.004")
Solder Paste Composition	Sn Ag (3-4) Cu (0.5-0.9)
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	per JEDEC J-STD-020
PCB Solder Pad Design	Same as the SnPb Design
PCB Pad Finish	OSP or AuNi

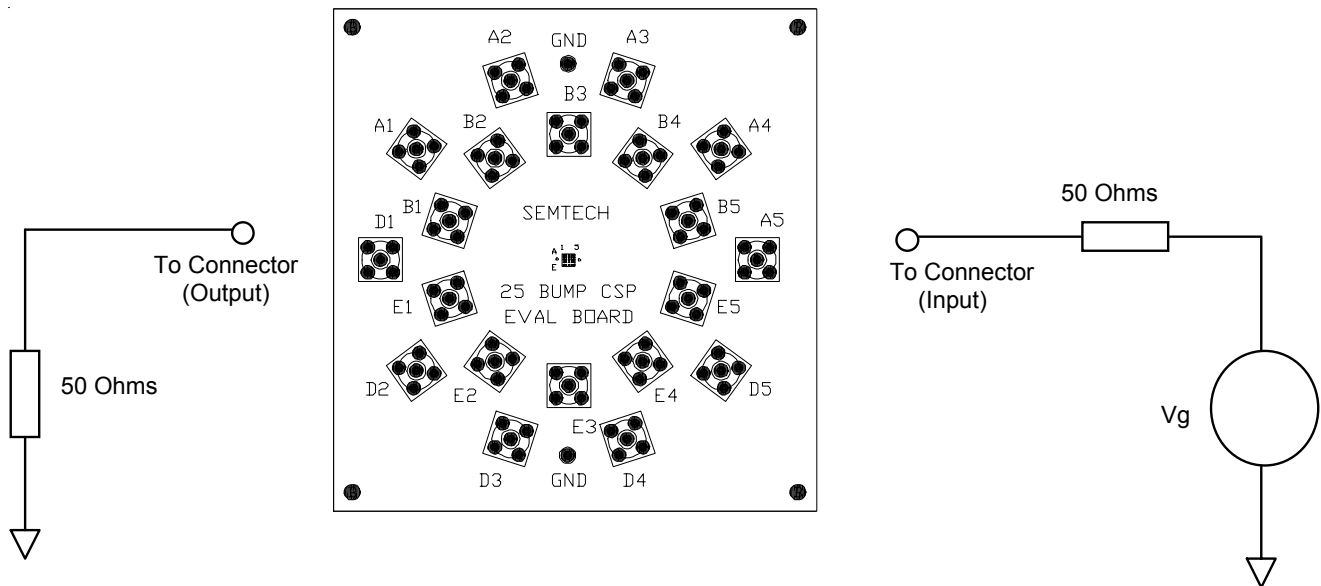


Insertion Loss

The insertion loss of the device is the ratio of the power delivered to the load with and without the filter in the circuit. This parameter is dependent upon the impedance of the source and the load. The standard impedance of test equipment that is used to measure filter frequency response is 50Ω . In order to obtain an accurate measurement of the filter performance, an evaluation board with 50Ω transmission lines are used. The test conditions for the *EClamp2340C* are shown below. The evaluation board contains SMA connectors at each of the circuits inputs and outputs. The connections are made with 50Ω traces. An HP 8753E network analyzer with an internal spectrum analyzer and tracking generator is used. This equipment has the capability to sweep the device from 3kHz to 3GHz. The analyzer's source (R_s) impedance is equal to the load (R_L) impedance which is equal to 50Ω .



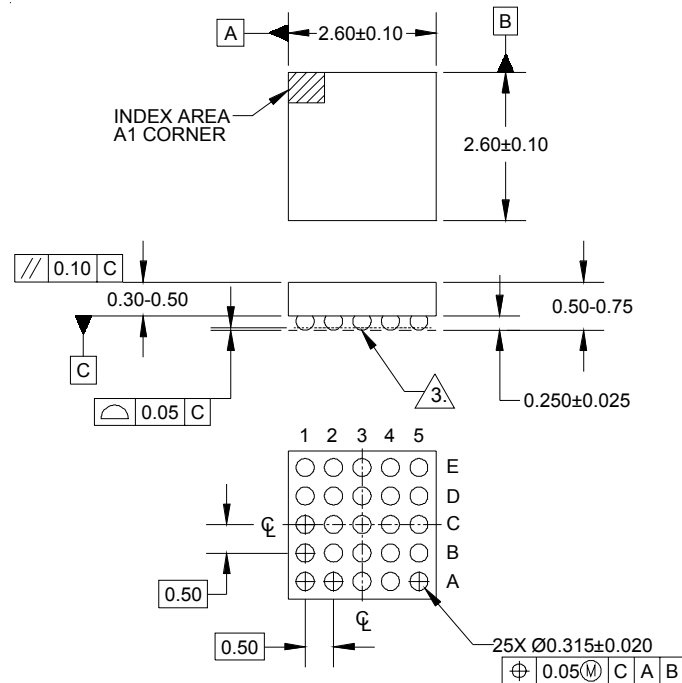
Insertion Loss S21



Insertion Loss Measurement Conditions

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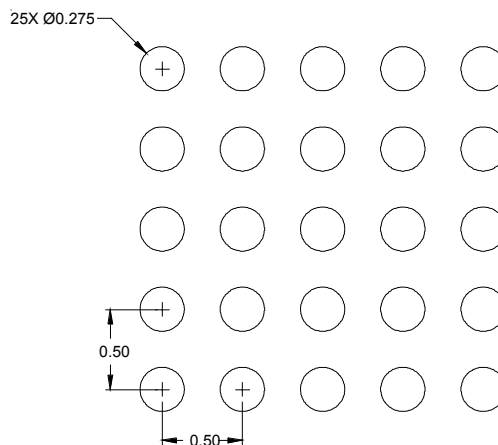
Outline Drawing



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS
2. REFERENCE JEDEC REGISTRATION MO-211.
3. Sn63/Pb37 FOR STANDARD DEVICES OR Sn95.5/Ag3.8/Cu0.7 FOR Pb-FREE DEVICES.

Land Pattern

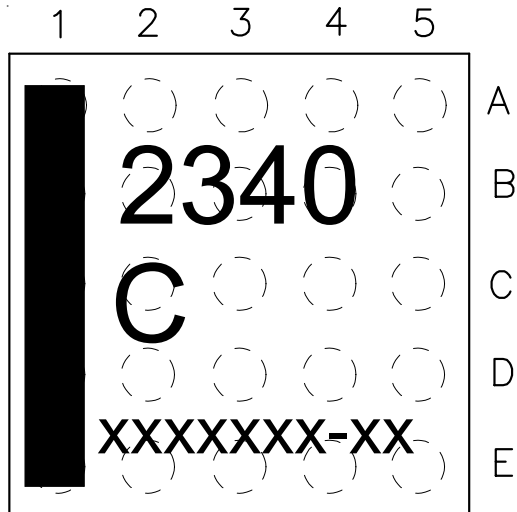


NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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Marking



Top View Showing Laser Mark

Note: xxxxxx-xx = Wafer Lot Code

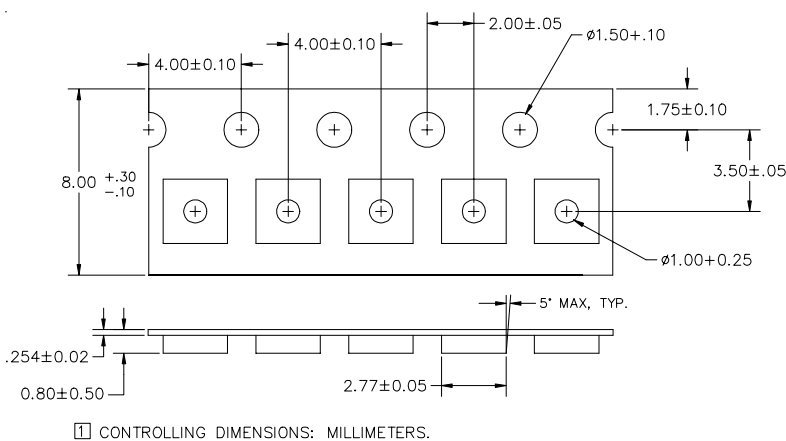
Top Coating: The top (non-bump side) of the device is a white non-conductive coating. The coating is laser markable and helps prevent die chipping during the PCB assembly process. This material is compliant with UL 94V-0 flammability requirements.

Ordering Information

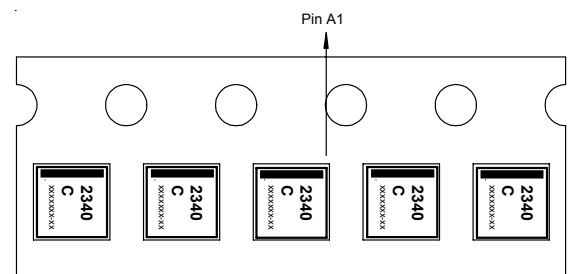
Part Number	Solder Ball Composition	Qty per Reel	Reel Size
EClamp2340C.WC	SnPb	3000	7 Inch
EClamp2340C.WCT	SnAgCu	3000	7 Inch

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Tape and Reel Specification



Tape Specifications



Device Orientation in Tape

Contact Information

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