Data Sheet

CX3000
0.35um Structured ASIC

Product Description

The CX3000, 0.35µm Structured ASIC product family offers cost-effective, rapid turnaround of ASIC devices. Using ChipX's innovative architecture, flexible manufacturing alternatives are available that permit options for rapid turnaround time and scalable volume production. The CX3000 product services those applications requiring ASIC performance in the networking, communications, computing, and industrial marketplace.

Key Features and Benefits

- Structured ASIC architecture
- Low NRE and start-up costs
- Fast time to production
- 21K to 200K usable logic gates (2 input NAND gate equivalent)
- 0.3µW/MHz/Gate @ 3.3V
- 5V and 3.3V core voltage
- Rich I/O libraries (2308 cells)
- Programmable I/O pads for power, ground, or I/O
- 5V drive or 3.3V drive with 5V tolerance (5V tolerant compliant I/O requires a reference bias voltage)
- 3.3V PCI-compliant at 66MHz
- Differential input support modes
- Configurable embedded synchronous memory
- 16K to 352K bits of single-port or dual-port SRAM or ROM
- 290MHz SRAM worst-case operation @ 3.3V for single-port and dual-port RAM
- 4 APLL
- >200MHz worst-case operation @ 3.3V
- Verilog/VHDL synthesis and simulation support
- DRC utilities (Check_all)
- Clock Tree Synthesis (CTS) with <500ps clock-skew
- Automatic cross-talk handling
- Memory BIST generator

The CX3000 ASIC Family

Available products in the CX3000 product family are shown in Table 1.

Table 1 CX3000 Products

Base Array	Usable ASIC Gates (K)	Embedded Memory (K bits)	Max Memory Instantiations	APLL	Max I/O
CX3041	21	48	6	4	160
CX3061	33	64	8	4	208
CX3141	68	96	12	4	304
CX3301	150	144	16	4	432
CX3303	150	144	18	4	432
CX3403	200	352	44	4	528
CX3072	40	32	4	4	128
CX3122	70	48	6	4	160
CX3422	200	96	12	4	304

Note: Each memory block can be used as one dual-port memory or two single-port memories. Max I/O include both signals and power/ground.

CX3000 Cell Library

- Synopsys DC Support
- Low power flip-flops
- Built-in scan MUX in flip-flops
- Multiplexers, decoders
- Tri-state/drive cells

Power Pin Assignment

All I/O cells are programmable as VDD, VSS, input, output, or bidirectional. This flexibility allows the user to properly ratio power pins with output drive requirements or to match specific pin-out when replacing existing devices.

Input and Output Bidirectional Cells

The CX3000 library contains a large selection of input, output, and bidirectional cells that accommodate a wide range of designs. Input cells can be personalized with internal pull-up or pull-down resistors and with or without hysteresis. Output cells include slew rate control, current drive capability from 2mA to 12mA, as well as N channel and P channel open drains. If required, outputs can be used in parallel to enable increased drive capability. Each I/O can be programmed independently for 3.3V or 5V.

Recommended Operating Conditions

Table 2, 3, and 4 provide data related to absolute maximum ratings, recommended operating conditions, and DC characteristics over operating conditions.

Table 2 Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{DD}	Core supply voltage	-0.3	4.6	V
V_{DDIO} (3.3V)	I/O supply voltage	-0.3	4.6	V
V_{DDIO} (5V)	I/O supply voltage	-0.3	6.5	V
V_{IN}	DC input voltage range	VSS -0.3	VDDWELL[1] +0.3	V
T_J	Junction temperature	—	150	°C
T_{STG}	Storage temperature	-65	150	°C
T_{SOL}	Soldering lead temperature (10 seconds)	—	210	°C

1. VDDWELL is 3.3V or 5V, depending on the highest voltage in the system.

Table 3 Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{DD}	Supply voltage (3.3V)	Commercial (0°C ≤ T_J ≤ 100°C)	3.0	3.6	V
		Industrial (-40°C ≤ T_J ≤ 115°C)	3.0	3.6	V
		Military (-55°C ≤ T_J ≤ 125°C)	3.0	3.6	V
V_{DD}	Supply voltage (5V)	Commercial (0°C ≤ T_J ≤ 100°C)	4.75	5.25	V
		Industrial (-40C ≤ T_J ≤ 115°C)	4.75	5.25	V
		Military (-55°C ≤ T_J ≤ 125°C)	4.5	5.5	V
V_{IH}	Input high voltage	TTL inputs	2.0	V_{DD}	V
		CMOS inputs	0.7 V_{DD}	V_{DD}	V
V_{IL}	Input low voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	0.3 V_{DD}	V
T_{in}	Input signal transition time		—	10	ns

Table 4 DC Characteristics Over Operating Conditions

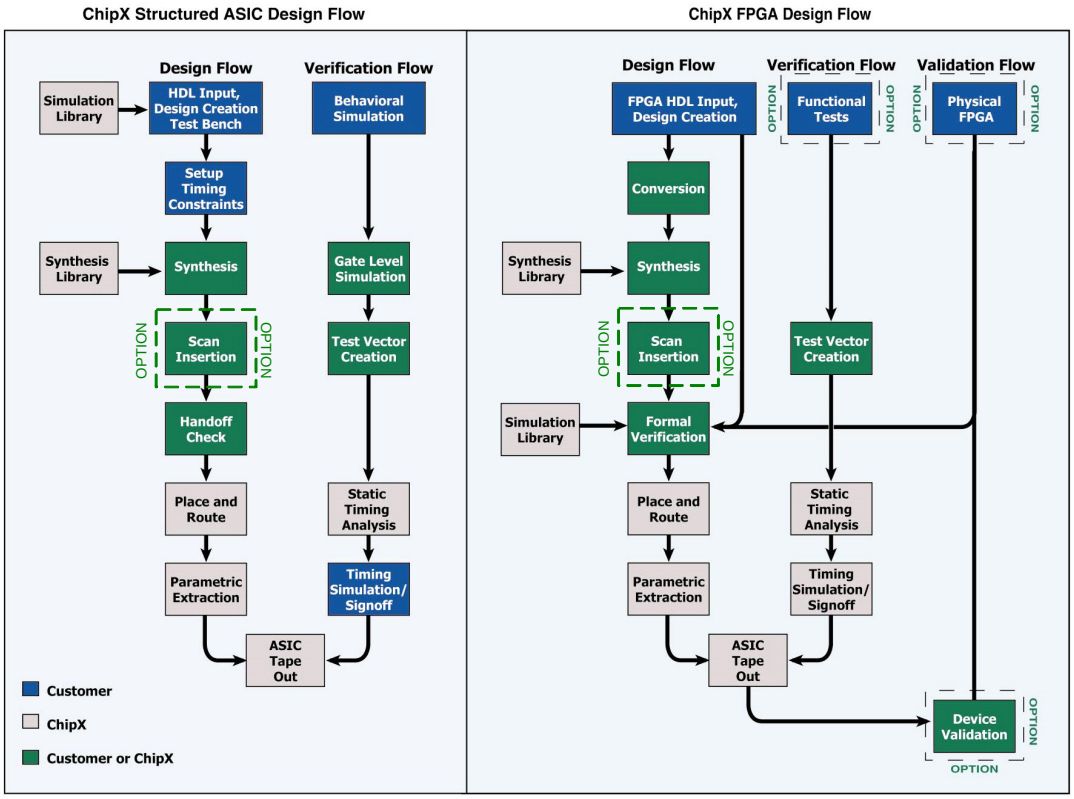
Symbol	Description		Min	Max	Units
V_{OH}	Output high voltage	TTL outputs	2.7	—	V
		CMOS outputs	V_{DD} -0.8	—	V
V_{OL}	Output low voltage	TTL outputs	—	0.5	V
		CMOS outputs	—	0.5	V
I_{IN}	Input leakage current		-10	10	µA
C_{IN}	Input capacitance	QFP packages	—	—	Refer to web site
		BGA packages	—	—	

Design Flow

ChipX spends considerable development effort to ensure that taping out a design to a Structured ASIC is a simple, painless, and risk-free endeavor. ChipX provides an on-line downloadable design kit in both Verilog and VHDL with complete libraries and a design-flow script which leads users through the development process in a logical, linear fashion, ensuring trouble-free product

development every time. The ChipX Design Toolkit checks design constraints, I/O rules, typical, min and max case timing, glitches, contention and handoff database completeness. Our standard ASIC and FPGA design flows are shown in Figure 1.

Figure 1 ChipX Structured ASIC and FPGA Design Flows



RTL or FPGA Netlist Handoff

An increasing number of customers prefer to handoff their RTL designs early and let ChipX perform the entire timing closure loop, including synthesis and final simulations. ChipX can also convert obsolete design netlists, FPGA bitmaps, and even well-specified concept designs into prototypes rapidly and reliably.

Packaging and Test

ChipX uses world-class external packaging and test facilities in the United States and Taiwan to assemble and complete commercial, industrial or military testing and qualification of products. The CX3000 product line is supported by a vast standard packaging library that includes the most popular DIP, QFP, BGA, fine-pitch BGA, and PGA package sizes. For special applications, multi-chip modules or hard-to-find hermetic or BGA package sizes, ChipX's experienced custom package design staff can create a package or pinout to your specifications.

ChipX, Inc. www.chipx.com Tel: 408-988-2445 Toll Free: 1-800-95-CHIPX Fax: 408-988-2449
Email: moreinfo@chipx.com 2323 Owen Street Santa Clara, California USA 95054