# AS5243

**DataSheet**

## Programmable 360º Magnetic Angle Encoder With Absolute SSI And Analog Outputs

## 1 General Description

The AS5243 is a contactless magnetic angle encoder for accurate measurement up to 360º and includes two AS5143 devices in a punched stacked leadframe.

It is a system-on-chip, combining integrated Hall elements, analog front end and digital signal processing in a single device.

The AS5243 provides a digital 10-bit as well as a programmable analog output that is directly proportional to the angle of a magnet, rotating over the chip.

The analog output can be configured in many ways, including user programmable angular range, adjustable output voltage range, voltage or current output, etc.

An internal voltage regulator allows operation of the AS5243 from 3.3V or 5.0V supplies.

The AS5243 is fully automotive qualified to AEC-Q100, grade 1.

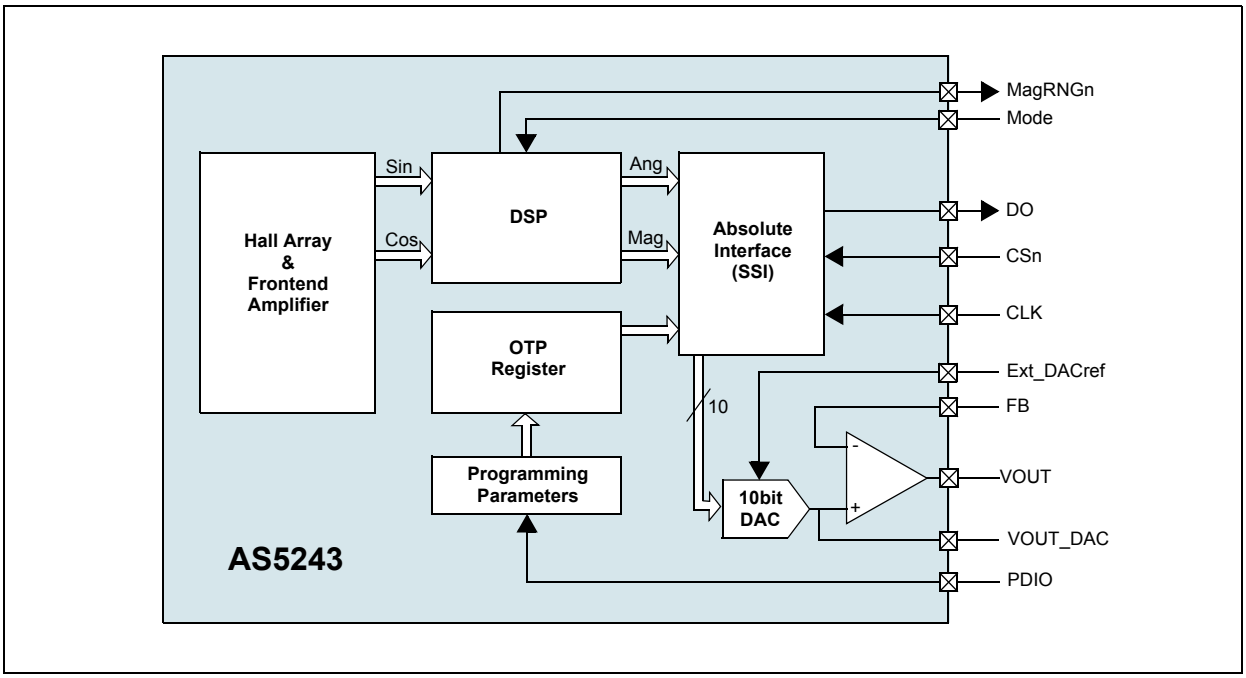
## 2 Key Features

- User programmable zero position
- Digital serial 10-bit absolute output
- 10-bit Analog output with programmable angle down to 0.088º/step
- Failure detection mode for magnet field strength and loss of power supply
- Serial read-out of multiple interconnected AS5243 devices using daisy chain mode
- Mode input for optimizing noise vs. speed
- Alignment mode for magnet placement guidance
- Wide temperature range: - 40ºC to +150ºC
- Small package: QFN32LD(7x7)
- Unique Chip Identifier

## 3 Applications

The AS5243 is ideal for applications with an angular travel range from a few degrees up to a full turn of 360º. The device is suitable for automotive applications like Throttle position sensors, Gas/brake pedal position sensing, Headlight position control, Contactless rotary position sensing, Front panel rotary switches and Replacement of potentiometers.

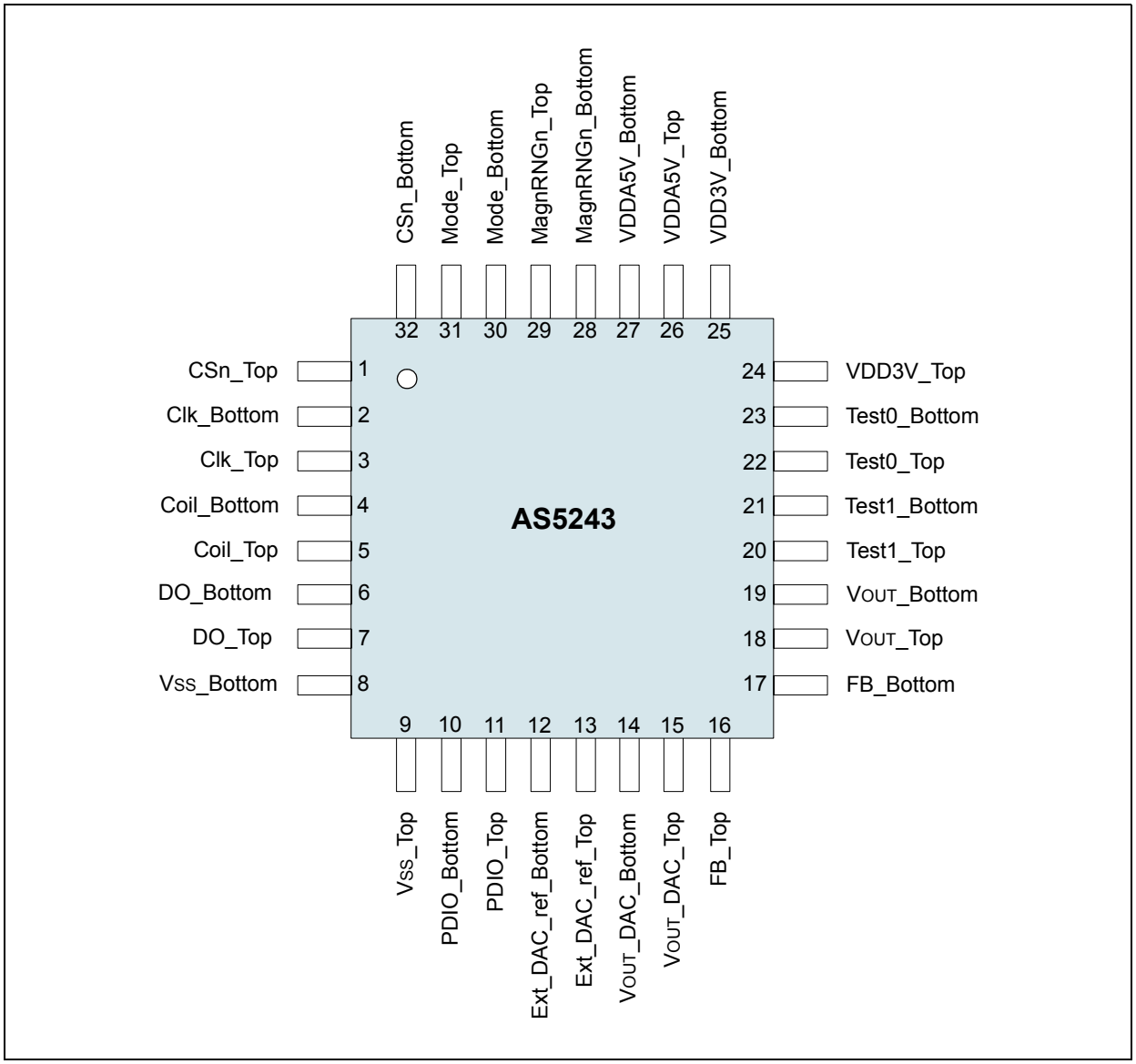
*Figure 1. Block Diagram*



## Contents

# 4 Pin Assignments

*Figure 2. Pin Assignments (Top View)*



## Pin Descriptions

*Table 1. Pin Descriptions*

| Pin Name | Pin Number | Description |
|---|---|---|
| CSn | 1,32 | **Chip Select.** Active low. Schmitt-Trigger input, internal pull-up resistor (~50kΩ). This pin selects a device for serial data transmission over the SSI interface. A “logic high” at CSn forces output DO to digital tri-state. |
| CLK | 2,3 | **SSI Clock Input.** Schmitt-Trigger input. Clock input for serial data transmission over the SSI interface. |
| Coil | 4,5 | For internal use. Must be left unconnected. |
| DO | 6,7 | **SSI Data Output.** Serial data output during data transmission over the SSI interface. |
| VSS | 8,9 | Negative Supply Voltage (GND). |
| PDIO | 10,11 | **OTP Programming Input and Data Input for Daisy Chain mode.** Internal pull-down resistor (~74kΩ). Should be connected to VSS if programming is not used. This pin is used to program the different operation modes, as well as the zero-position in the OTP register. This pin is also used as a digital input to shift serial data through the device in Daisy Chain Configuration. |
| Ext_DAC_ref | 12,13 | **DAC Reference.** This pin is the external voltage reference input for the Digital-to-Analog Converter (DAC). If selected, the analog output voltage on pin 12 (VOUT) will be ratiometric to the voltage on this pin. |
| VOUT_DAC | 14,15 | **Ratio metric analog output voltage of DAC** in different modes. VOUT_DAC is the unbuffered output of the asdDAC. This pin may be used to connect an external OPAMP, etc. to the DAC. |
| FB | 16,17 | **Feedback.** This pin is the inverting input of the OPAMP buffer stage. Access to this pin allows various OPAMP configurations. |
| VOUT | 18,19 | **Amplified analog output voltage of DAC.** This pin is the analog output pin. The analog output is a DC voltage, ratiometric to VDD5V (3.0 – 5.5V) or an external voltage source and proportional to the angle. |
| Test1 | 20,21 | For internal use. Must be left unconnected. |
| Test0 | 22,23 | For internal use. Must be left unconnected. |
| VDD3V3 | 24,25 | **Supply Pins.** 3V-Regulator Output for internal core, regulated from VDD5V. Connect to VDD5V for 3V supply voltage. Do not load externally. |
| VDD5V | 26,27 | **Supply Pins.** Positive Supply Voltage, 3.0 to 5.5 V. |
| MagRNGn | 28,29 | **Magnet Field Magnitude RaNGe warning.** Active low. Indicates that the magnetic field strength is outside of the recommended limits. It is an open-drain output that is pulled to VSS when the magnetic field is out of the recommended range (45mT to 75mT). The chip will still continue to operate, but with reduced performance, when the magnetic field is out of range. When this pin is low, the analog output at pins #10 and #12 will be 0V to indicate the out-of-range condition. |
| Mode | 30,31 | **Mode input.** Select between low noise (open, low) and high speed (high) mode. Internal pull-down resistor. |

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# 5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 7 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*Table 2. Absolute Maximum Ratings*

| Parameter | Min | Max | Units | Comments |
|---|---|---|---|---|
| DC supply voltage at pin VDD5V | -0.3 | 7 | V | |
| DC supply voltage at pin VDD3V3 | | 5 | V | |
| Input pin voltage ($V_{IN}$) | -0.3 | VDD5V +0.3 | V | Pins MagRNGn, Mode, CSn, CLK, DO, $V_{OUT}$_DAC, FB, Vout |
| | -0.3 | 5 | | Pin Ext_DAC_ref |
| | -0.3 | 7.5 | | Pin PDIO |
| Input current (latchup immunity) | -100 | 100 | mA | Norm: EIA/JESD78 ClassII Level A |
| Electrostatic discharge (ESD) | | ±2 | kV | Norm: JESD22-A114E |
| Storage temperature | -55 | 150 | ºC | Min -67ºF; Max +257ºF |
| Body temperature (Lead-free package) | | 260 | ºC | t=20 to 40s, Norm: IPC/JEDEC J-Std-020C Lead finish 100% Sn “matte tin” |
| Humidity non-condensing | 5 | 85 | % | |
| Ambient Temperature ($T_{AMB}$) | -40 | +150 | ºC | -40ºF…+257ºF |

# 6 Electrical Characteristics

TAMB = -40 to 150ºC, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation), unless otherwise noted.

*Table 3. Electrical Characteristics*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| RES | Resolution[1] | 0.352 deg | | | 10 | bit |
| $INL_{opt}$ | Integral non-linearity (optimum)[2] | Maximum error with respect to the best line fit. Verified at optimum magnet placement, TAMB =25ºC | | | ±0.5 | deg |
| $INL_{temp}$ | Integral non-linearity (optimum) | Maximum error with respect to the best line fit. Verified at optimum magnet placement, TAMB = -40 to +150ºC | | | ±0.9 | deg |
| INL | Integral non-linearity | Best line fit = ($Err_{max}$ – $Err_{min}$) / 2 Over displacement tolerance with 6mm diameter magnet, TAMB = -40 to +150ºC | | | ±1.4 | deg |
| DNL | Differential non-linearity[3] | 10bit, no missing codes | | | ±0.176 | deg |
| TN | Transition noise[4] | 1 sigma, fast mode (pin MODE = 1) | | | 0.06 | Deg RMS |
| | | 1 sigma, slow mode (pin MODE=0 or open) | | | 0.03 | |
| Hyst | Hysteresis | Incremental modes only | | | | |
| $V_{on}$ | Power-on reset thresholds On voltage; 300mV typ. hysteresis | DC supply voltage 3.3V (VDD3V3) | 1,37 | 2.2 | 2.9 | V |
| $V_{off}$ | Power-on reset thresholds Off voltage; 300mV typ. hysteresis | | 1.08 | 1.9 | 2.6 | |
| $t_{PwrUp}$ | Power-up time Until offset compensation finished, OCF = 1, Angular Data valid | fast mode (pin MODE=1) | | | 20 | ms |
| | | slow mode (pin MODE=0 or open) | | | 80 | |
| $t_{delay}$ | System propagation delay absolute output : delay of ADC and DSP | fast mode (pin MODE=1) | | | 96 | µs |
| | | slow mode (pin MODE=0 or open) | | | 384 | |
| $f_{S,mode0}$ | Internal sampling rate for absolute output | TAMB = 25ºC, slow mode (pin MODE=0 or open) | 2.48 | 2.61 | 2.74 | kHz |
| | | TAMB = -40 to +150ºC, slow mode (pin MODE=0 or open) | 2.35 | 2.61 | 2.87 | |
| $f_{S,mode1}$ | Internal sampling rate for absolute output | TAMB = 25ºC, fast mode (pin MODE =1) | 9.90 | 10.42 | 10.94 | kHz |
| | | TAMB = -40 to +150ºC, : fast mode (pin MODE =1) | 9.38 | 10.42 | 11.46 | |
| CLK | Read-out frequency | Max. clock frequency to read out serial data | >0 | | 1 | MHz |
| **Operating Conditions** | | | | | | |
| $I_{supp}$ | Supply Current | | | 16 | 21 | mA |
| VDD5V | Supply voltage at pin VDD5V | 5V Operation | 4.5 | 5.0 | 5.5 | V |
| VDD3V3 | Voltage regulator output voltage at pin VDD3V3 | | 3.0 | 3.3 | 3.6 | |

*Table 3. Electrical Characteristics (Continued)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VDD5V | Supply voltage at pin VDD5V | 3.3V Operation (pin VDD5V and VDD3V3 connected) | 3.0 | 3.3 | 3.6 | V |
| VDD3V3 | Supply voltage at pin VDD3V3 | | 3.0 | 3.3 | 3.6 | |
| **DC Characteristics for Digital Inputs and Outputs** | | | | | | |
| CMOS Schmitt-Trigger Inputs: CLK, CSn (internal Pull-up), Mode (internal Pull-down) | | | | | | |
| $V_{IH}$ | High level input voltage | Normal operation | 0.7 *VDD5V | | | V |
| $V_{IL}$ | Low level input voltage | | | | 0.3 *VDD5V | V |
| $V_{Ion} - V_{Ioff}$ | Schmitt Trigger hysteresis | | 1 | | | V |
| $I_{LEAK}$ | Input leakage current | Pin CLK, VDD5V = 5.0V | -1 | | 1 | µA |
| $I_{iL}$ | Pull-up low level input current | Pin CSn, VDD5V= 5.0V | -30 | | -100 | |
| $I_{iH}$ | Pull-up high level input current | Pin Mode, VDD5V= 5.0V | 30 | | 100 | |
| CMOS Input : Program Input (Prog) | | | | | | |
| $V_{IH}$ | High level input voltage | | 0.7 *VDD5V | | 5 | V |
| $V_{PROG}$ | High level input voltage | During programming | Refer to Programming Conditions | | | V |
| $V_{IL}$ | Low level input voltage | | | | 0.3 *VDD5V | V |
| $I_{iL}$ | Pull-down high level input current | VDD5V:5.5V | | | 100 | µA |
| CMOS Output Open Drain: MagRNGn | | | | | | |
| $V_{OL}$ | Low level output voltage | | | | $V_{SS}$+0.4 | V |
| $I_O$ | Output current | VDD5V:4.5V | | | 4 | mA |
| | | VDD5V:3V | | | 2 | |
| $I_{OZ}$ | Open drain leakage current | | | | 1 | µA |
| Tristate CMOS Output: DO | | | | | | |
| $V_{OH}$ | High level output voltage | | VDD5V -0.5 | | | V |
| $V_{OL}$ | Low level output voltage | | | | $V_{SS}$+0.4 | V |
| $I_O$ | Output current | VDD5V:4.5V | | | 4 | mA |
| | | VDD5V:3V | | | 2 | |
| $I_{OZ}$ | Tri-state leakage current | | | | 1 | µA |
| Digital-to-Analog Converter | | | | | | |
| | Resolution | | | 10 | | bit |
| $V_{OUTM1}$ | Output Range | ClampMdEn = 0 (default) 0…100% $V_{REF}$ (default) | 0 | | $V_{REF}$ | V |
| $V_{OUTM2}$ | | ClampMdEn = 1 10…90% $V_{REF}$ | 0.10 *$V_{REF}$ | | 0.90 *$V_{REF}$ | |
| $R_{OutDAC}$ | Output Resistance | Unbuffered Pin DACout (#10) | | | 8 | kΩ |

*Table 3. Electrical Characteristics (Continued)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{REF}$ | DAC reference voltage (DAC full scale range) | RefExt EN = 1<br>DAC reference = external<br>Pin: DACref (#9) | 0.2 | | VDD3V3 - 0.2 | V |
| | | RefExtEn = 0 (default)<br>DAC reference = internal | | | VDD5V / 2 | |
| $INL_{DAC}$ | Integral Non-Linearity | Non-Linearity of DAC and OPAMP; -40…+150ºC, For all analog modes: 1LSB = $V_{REF}$ / 1024 | | | ±1.5 | LSB |
| $DNL_{DAC}$ | Differential Non-Linearity | | | | ±0.5 | |
| Hyst | Analog output hysteresis | All analog modes | | | 1 | LSB |
| | | OR1,OR0 = 00 (default)<br>At 360º -0º transition, 360º mode only | | | 2 | |
| OPAMP Output Stage | | | | | | |
| VDD5V | Power Supply Range | | 3.0 | | 5.5 | V |
| CL | Parallel Load Capacitance | | | | 100 | pF |
| RL | Parallel Load Resistance | 3.3V Operation | 4.7 | | | kΩ |
| A0 | Open Loop Gain | | 92 | 130 | 144 | dB |
| VosOP | Offset Voltage RTI | 3 sigma | -5 | | 5 | mV |
| $V_{OUT}L$ | Output Range Low | Linear range of analog output | | | 0.05 *VDD5V | V |
| $V_{OUT}H$ | Output Range High | | 0.95 *VDD5V | | | |
| $I_{sink}$ | Current capability sink | Permanent short circuit current: $V_{OUT}$ to VDD5V | 4.8 | | 50 | mA |
| $I_{source}$ | Current capability source | Permanent short circuit current: $V_{OUT}$ to $V_{SS}$ | 4.6 | | 66 | |
| $V_{noise}$ | Output noise | Over full temperature range; BW= 1Hz…10MHz, Gain = 2x | 160 | 220 | 490 | µVrms |
| Gain | OPAMP gain (non-inverting) | Internal; OTP: FB_int EN = 1 | | 2 | | |
| | | External OTP: FB_int EN = 0 (default)<br>With external resistors, pins $V_{OUT}$ [#12] and FB [#11]: (see Figure 14) | 1 | | 4 | |
| **Magnetic Input Specification** (Two-pole cylindrical diametrically magnetized source) | | | | | | |
| $d_{mag}$ | Diameter | Recommended magnet: Ø 6mm x 2.5mm for cylindrical magnets | 4 | 6 | | mm |
| $t_{mag}$ | Thickness | | 2.5 | | | |
| $B_{pk}$ | Magnetic input field amplitude | Required vertical component of the magnetic field strength on the die's surface, measured along a concentric circle with a radius of 1.1mm | 45 | | 75 | mT |
| $B_{off}$ | Magnetic offset | Constant magnetic stray field | | | ±10 | mT |
| | Field non-linearity | Including offset gradient | | | 5 | % |
| $f_{mag\_abs}$ | Input frequency (rotational speed of magnet) | Absolute mode: 600 rpm @ readout of 1024 positions (see Table 10) | | | 10 | Hz |
| $f_{mag\_inc}$ | | Incremental mode: no missing pulses at rotational speeds of up to 10,000 rpm (see Table 10) | | | 166 | Hz |

*Table 3. Electrical Characteristics (Continued)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Disp | Displacement Radius | Max. offset between defined device center and magnet axis | | | 0.25 | mm |
| | Recommended magnet material and temperature drift | NdFeB (Neodymium Iron Boron) | | -0.12 | | %/K |
| | | SmCo (Samarium Cobalt) | | -0.035 | | |
| **Programming Conditions** | | | | | | |
| $t_{Prog\ enable}$ | Programming enable time | Time between rising edge at Prog pin and rising edge of CSn | 2 | | | µs |
| $t_{Data\ in}$ | Write data start | | 2 | | | µs |
| $t_{Data\ in\ valid}$ | Write data valid | Write data at the rising edge of $CLK_{PROG}$ | 250 | | | ns |
| $t_{Load\ PROG}$ | Load programming data | | 3 | | | µs |
| $t_{PrgR}$ | Rise time of VPROG before CLK PROG | | 0 | | | µs |
| $t_{PrgH}$ | Hold time of VPROG after CLK PROG | | 0 | | 5 | µs |
| $CLK_{PROG}$ | Write data – programming CLK PROG | | | | 250 | kHz |
| $t_{PROG}$ | CLK pulse width | During programming; 16 clock cycles | 1.8 | 2 | 2.2 | µs |
| $t_{PROG\ finished}$ | Hold time of Vprog after programming | Programmed data is available after next power-on | 2 | | | µs |
| $V_{PROG}$ | Programming voltage | Must be switched off after zapping | 7.3 | 7.4 | 7.5 | V |
| $V_{ProgOff}$ | Programming voltage off level | Line must be discharged to this level | 0 | | 1 | V |
| $I_{PROG}$ | Programming current | During programming | | | 130 | mA |
| $CLK_{Aread}$ | Analog read CLK | Analog readback mode | | | 100 | kHz |
| $V_{programmed}$ | Programmed zener voltage (log.1) | $V_{REF}$ - $V_{PROG}$ during analog readback mode; Refer Analog Readback Mode on page 25 | | | 100 | mV |
| $V_{unprogrammed}$ | Unprogrammed zener voltage (log. 0) | | 1 | | | V |

1. Digital Interface
2. Integral Non-Linearity (INL) is the maximum deviation between actual position and indicated position.
3. Differential Non-Linearity (DNL) is the maximum deviation of the step length from one position to the next.
4. Transition Noise (TN) is the repeatability of an indicated position.

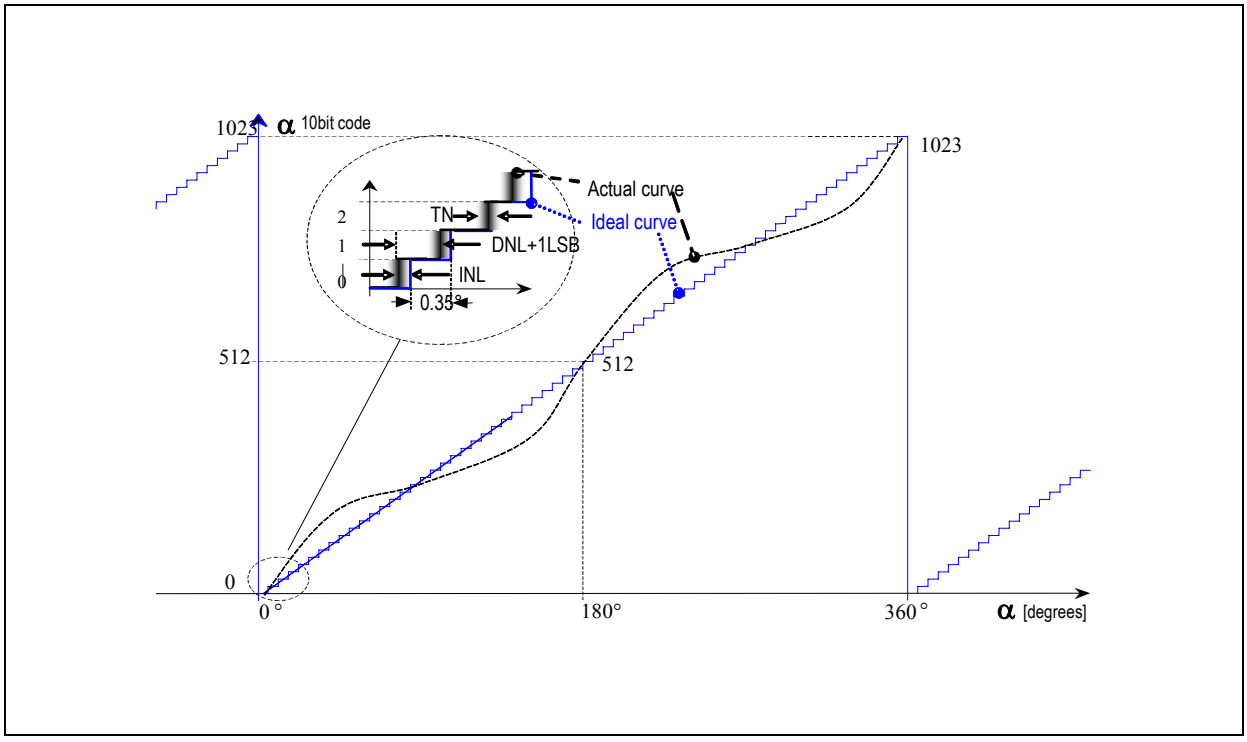
## Timing Characteristics

TAMB = -40 to +150 ºC, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation), unless otherwise noted.

*Table 4. Timing Characteristics*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Synchronous Serial Interface (SSI)** | | | | | | |
| $t_{DO\ active}$ | Data output activated (logic high) | Time between falling edge of CSn and data output activated | | | 100 | ns |
| $t_{CLK\ FE}$ | First data shifted to output register | Time between falling edge of CSn and first falling edge of CLK | 500 | | | ns |
| $T_{CLK/2}$ | Start of data output | Rising edge of CLK shifts out one bit at a time | 500 | | | ns |
| $t_{DO\ valid}$ | Data output valid | Time between rising edge of CLK and data output valid | 357 | 375 | 394 | ns |
| $t_{DO\ tristate}$ | Data output tristate | After the last bit DO changes back to “tristate” | | | 100 | ns |
| $t_{CSn}$ | Pulse width of CSn | CSn =high; To initiate read-out of next angular position | 500 | | | ns |
| $f_{CLK}$ | Read-out frequency | Clock frequency to read out serial data | >0 | | 1 | MHz |

*Figure 3. Integral and Differential Non-Linearity (exaggerated curve)*



# 7 Detailed Description

The AS5243 is manufactured in a CMOS standard process and uses a spinning current Hall technology for sensing the magnetic field distribution across the surface of the chip. The integrated Hall elements are placed in a circle around the center of the device and deliver a voltage representation of the magnetic field perpendicular to the surface of the IC. Through Sigma-Delta Analog / Digital Conversion and Digital Signal-Processing (DSP) algorithms, the AS5243 provides accurate high-resolution absolute angular position information. For this purpose a Coordinate Rotation Digital Computer (CORDIC) calculates the angle and the magnitude of the Hall array signals. The DSP is also used to indicate movements of the magnet towards or away from the chip and to indicate, when the magnetic field is outside of the recommended range (status bits = MagInc, MagDec;  hardware pin = MagRngn). A small low cost diametrically magnetized (two-pole) standard magnet, centered over the chip, is used as the input device.

The AS5243 senses the orientation of the magnetic field and calculates a 10-bit binary code. This code can be accessed via a Synchronous Serial Interface (SSI). In addition, the absolute angular representation is converted to an analog signal, ratiometric to the supply voltage. The analog output can be configured in many ways, such as 360º / 180º / 90º or 45º angular range, external or internal DAC reference voltage, 0-100% *VDD or 10-90% *VDD analog output range, external or internal amplifier gain setting. The various output modes as well as a user programmable zero position can be programmed in an OTP register. As long as no programming voltage is applied to pin PDIO, the new setting may be overwritten at any time and will be reset to default when power is cycled. To make the setting permanent, the OTP register must be programmed by applying a programming voltage.

The AS5243 is tolerant to magnet misalignment and unwanted external magnetic fields due to differential measurement technique and Hall sensor conditioning circuitry. It is also tolerant to airgap and temperature variations due to Sin-/Cos- signal evaluation.

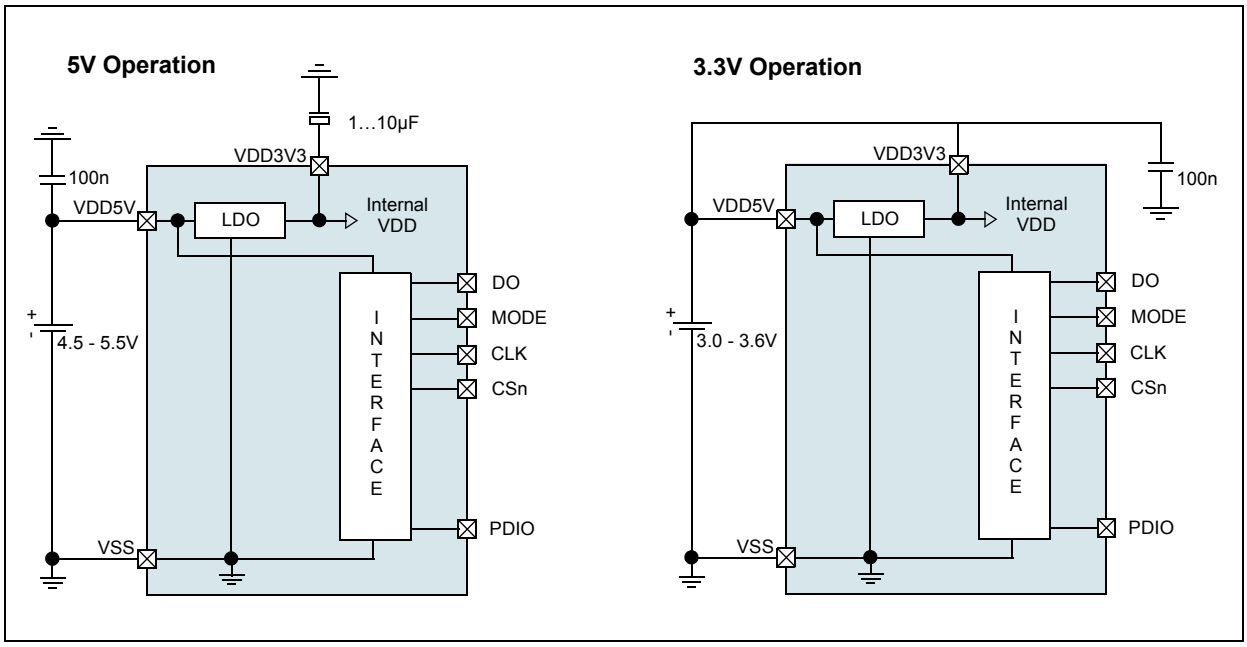
## 3.3V / 5V Operation

The AS5243 operates either at 3.3V ±10% or at 5V ±10%. This is made possible by an internal 3.3V Low-Dropout (LDO) Voltage regulator. The core supply voltage is always taken from the LDO output, as the internal blocks are always operating at 3.3V. For 3.3V operation, the LDO must be bypassed by connecting VDD3V3 with VDD5V (see Figure 4).

For 5V operation, the 5V supply is connected to pin VDD5V, while VDD3V3 (LDO output) must be buffered by a 1...10µF capacitor, which should be placed close to the supply pin (see Figure 4). The VDD3V3 output is intended for internal use only It should not be loaded with an external load.

The voltage levels of the digital interface I/O's correspond to the voltage at pin VDD5V, as the I/O buffers are supplied from this pin. A buffer capacitor of 100nF is recommended in both cases close to pin VDD5V. Note that pin VDD3V3 must always be buffered by a capacitor. It must not be left floating, as this may cause an instable internal 3.3V supply voltage, which may lead to larger than normal jitter of the measured angle.

*Figure 4. Connections for 5V / 3.3V Supply Voltages*




## 10-bit Absolute Synchronous Serial Interface (SSI)

The serial data transmission timing is outlined in Figure 5: if CSn changes to logic low, Data Out (DO) will change from high impedance (tri-state) to logic high and the read-out sequence will be initiated. After a minimum time $t_{CLK\ FE}$, data is latched into the output shift register with the first falling edge of CLK. Each subsequent rising CLK edge shifts out one bit of data. The serial word contains 16 bits, the first 10 bits are the angular information D[9:0], the subsequent 6 bits contain system information, about the validity of data such as OCF, COF, LIN, Parity and Magnetic Field status (increase / decrease / out of range). A subsequent measurement is initiated by a logic “high” pulse at CSn with a minimum duration of $t_{CSn}$. Data transmission may be terminated at any time by pulling CSn = high.

### Serial Data Contents

**D9:D0** – Absolute angular position data (MSB is clocked out first).

**OCF** – (Offset Compensation Finished). Logic high indicates that the Offset Compensation Algorithm has finished and data is valid.

**COF** – (Cordic Overflow). Logic high indicates an out of range error in the CORDIC part. When this bit is set, the data at D9:D0 is invalid. The absolute output maintains the last valid angular value. This alarm may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

**LIN** – (Linearity Alarm). Logic high indicates that the input field generates a critical output linearity. When this bit is set, the data at D9:D0 may still be used, but can contain invalid data. This warning may be resolved by bringing the magnet within the X-Y-Z tolerance limits. Data D9:D0 is valid, when the status bits have the following configurations:

*Table 5. Status Bit Outputs*

| OCF | COF | LIN | MagINC | MagDEC | Parity |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | even checksum of bits 1:15 |
| | | | 0 | 1 | |
| | | | 1 | 0 | |

**MagINC** – (Magnitude Increase) becomes HIGH, when the magnet is pushed towards the IC, thus increasing the magnetic field strength.

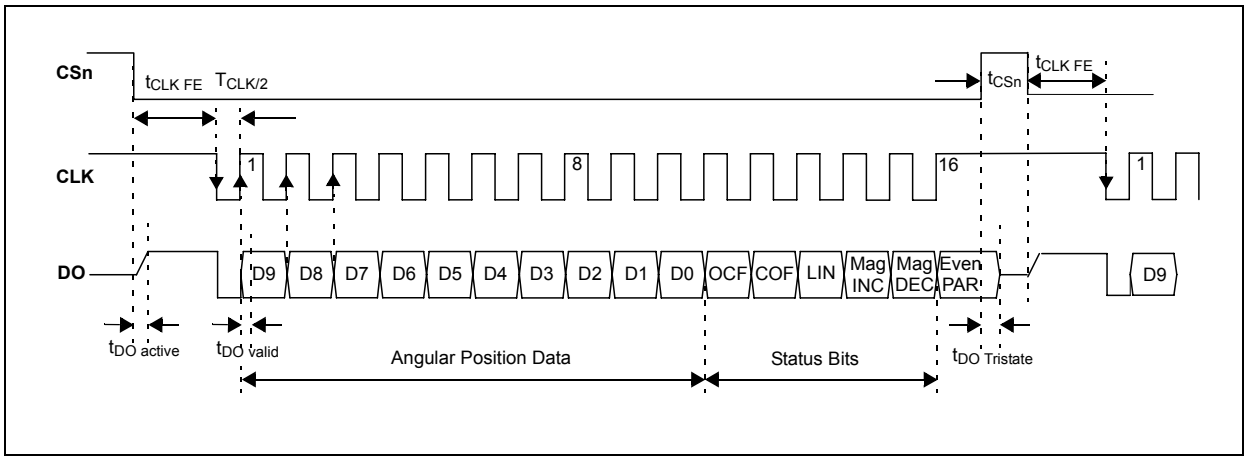
**MagDEC** – (Magnitude Decrease) becomes HIGH, when the magnet is pulled away from the IC, thus decreasing the magnetic field strength.

Signal “HIGH” for both MagINC and MagDEC indicate a magnetic field that is out of the allowed range (see Table 6).

**Note:** Pin 28,29 (MagRngn) is a combination of MagINC and MagDEC. It is active low via an open drain output and requires an external pull-up resistor. If the magnetic field is in range, this output is turned off, (logic “high”).

**Even Parity** – A bit for transmission error detection of bits 1to 15 (D9 to D0, OCF, COF, LIN, MagINC, MagDEC). The absolute angular output is always set to a resolution of 10 bit / 360º. Placing the magnet above the chip, angular values increase in clockwise direction by default.

*Figure 5. Synchronous Serial Interface with Absolute Angular Position Data*




## Z-Axis Range Indication (Push Button Feature, Red/Yellow/Green Indicator)

The AS5243 provides several options of detecting movement and distance of the magnet in the vertical (Z-) direction. Signal indicators MagINC, MagDEC and LIN are available as status bits in the serial data stream, while MagRngn is an open-drain output that indicates an out-of range status (on in YELLOW or RED range). Additionally, the analog output provides a safety feature in the form that it will be turned off when the magnetic field is too strong or too weak (RED range). The serial data is always available, the red/yellow/green status is indicated by the status bits as shown below.

*Table 6. Magnetic Field Strength Indicators*

| SSI Status Bits | | | Hardware Pins | | Description |
|---|---|---|---|---|---|
| MagINC | MagDEC | LIN | MagRNGn | Analog Output | |
| 0 | 0 | 0 | Off | Enabled | No distance change<br>Magnetic Input Field OK (GREEN range, ~45…75mT). |
| 0 | 1 | 0 | Off | Enabled | Distance increase, GREEN range; Pull-function. This state is dynamic and only active while the magnet is moving away from the chip. |
| 1 | 0 | 0 | Off | Enabled | Distance decrease, GREEN range; Push- function. This state is dynamic and only active while the magnet is moving towards the chip. |
| 1 | 1 | 0 | On | Enabled | YELLOW Range: Magnetic field is ~ 25…45mT or ~75…135mT. The AS5243 may still be operated in this range, but with slightly reduced accuracy. |
| 1 | 1 | 1 | On | Disabled | RED Range: Magnetic field is ~<25mT or >~135mT. The analog output will be turned off in this range by default. It can be enabled permanently by OTP programming. Refer Diagnostic Output Mode on page 17. It is still possible to use the absolute serial interface in the red range, but not recommended. |

## Mode Input Pin

The absolute angular position is sampled at a rate of 10.4kHz (t=96µs) in fast mode and at a rate of 2.6kHz (t=384µs) in slow mode. These modes are selected by pin MODE (#30,31). The mode input pin activates or deactivates an internal filter, which is used to reduce the digital jitter and consequently the analog output noise.

Activating the filter by pulling Mode = LOW or leaving it open reduces the transition noise to <0.03° rms. At the same time, the sampling rate is reduced to 2.6kHz and the signal propagation delay is increased to 384µs. This mode is recommended for high precision, low speed and ≤360° applications.

Deactivating the filter by setting Mode = HIGH increases the sampling rate to 10.4kHz and reduces the signal propagation delay to 96µs. The transition noise will increase to <0.06° rms. This mode is recommended for higher speed and full scale = 360° applications. Switching the MODE pin affects the following parameters:

*Table 7. Mode Pin Settings*

| Parameter | slow mode (Pin MODE = 0 or open) | fast mode (Pin MODE = 1) |
|---|---|---|
| Sampling rate | 2.61 kHz (383µs) | 10.42 kHz (95.9µs) |
| Transition noise (1 sigma) | ≤ 0.03° rms | ≤ 0.06° rms |
| Propagation delay | 384µs | 96µs |
| Startup time | 20ms | 80ms |

Pin MODE should be set at power-up. A mode change during operation is not recommended.

## Daisy Chain Mode

The Daisy Chain Mode allows connection of several AS5243's in series, while still keeping just one digital input for data transfer (See "Data IN" in Figure 6). This mode is accomplished by connecting the data output (DO; pin 6,7) to the data input (PDIO; pin 10,11) of the subsequent device. The serial data of all connected devices is read from the DO pin of the first device in the chain.

The length of the serial bit stream increases with every connected device, it is n * (16+1) bits: E.g. 34 bit for two devices, 51 bit for three devices, etc.

The last data bit of the first device (Parity) is followed by a dummy bit and the first data bit of the second device (D9), etc. (see Figure 7).

*Figure 6. Daisy Chain Hardware Configuration*

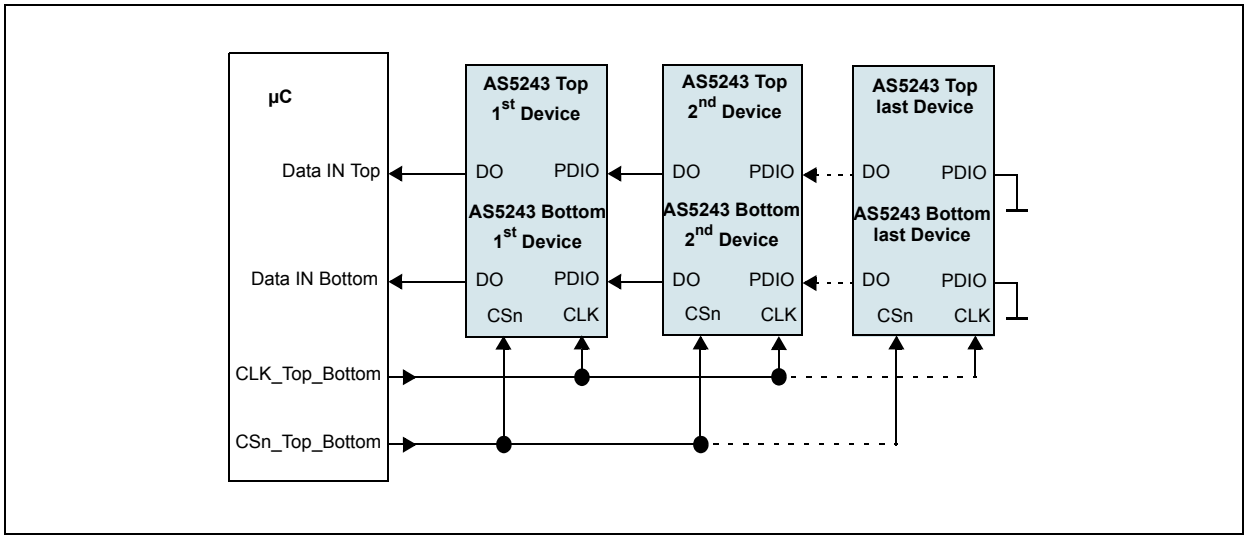
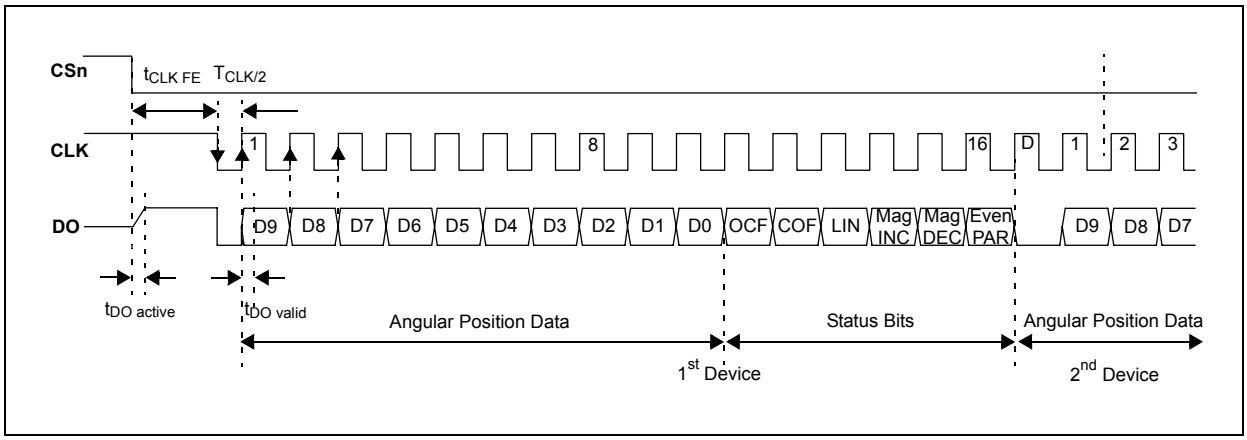


*Figure 7. Daisy Chain Data Transfer Timing Diagram*




## Analog Output

The analog output VOUT provides an analog voltage that is proportional to the angle of the rotating magnet and ratiometric to the supply voltage VDD5V (max.5.5V). It can source or sink currents up to ±1mA in normal operation (up to 66mA short circuit current). The analog output block consists of a digital angular range selector, a 10-bit Digital-to-Analog converter and an OPAMP buffer stage (see Figure 14).

The digital range selector allows a preselection of the angular range for 360º,180º,90º or 45º (see Table 10). Fine-tuning of the angular range can be accomplished by adjusting the gain of the OPAMP buffer stage. The reference voltage for the Digital-to-Analog converter (DAC) can be taken internally from VDD5V / 2. In this mode, the output voltage is ratiometric to the supply voltage. Alternatively, an external DAC reference can be applied at pin Ext_DAC_ref (#12,13). In this mode, the analog output is ratiometric to the external reference voltage.

An on-chip diagnostic feature turns the analog output off in case of an error (broken supply or magnetic field out of range; (see Table 6). The DAC output can be accessed directly at pin #14,15 VOUT_DAC. The addition of an OPAMP to the DAC output allows a variety of user configurable options, such as variable output voltage ranges and variable output voltage versus angle response. By adding an external transistor, the analog voltage output can be buffered to allow output currents up to hundred milliamperes or more. Furthermore, the OPAMP can be configured as constant current source.

As an OTP option, the DAC can be configured to 2 different output ranges:

1. **0……100% VDACref.** The reference point may be either taken from VDD5V/2 or from the external Ext_DAC_ref input. The 0…100% range allows easy replacement of potentiometers. Due to the nature of rail-to-rail outputs, the linearity will degrade at output voltages that are close to the supply rails.
2. **10…..90% VDACref.** This range allows better linearity, as the OPAMP is not driven to the rails. Furthermore, this mode allows failure detection, when the analog output voltage is outside of the normal operating range of 10…90%VDD, as in the case of broken supply or when the magnetic field is out of range and the analog output is turned off.

### Analog Output Voltage Modes

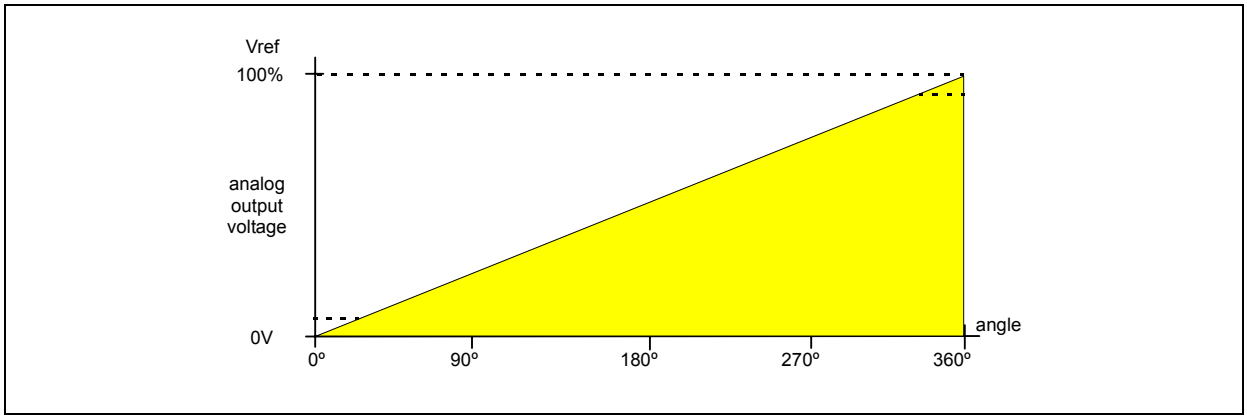
The Analog output voltage modes are programmable by OTP. Depending on the application, the analog output can be selected as rail-to-rail output or as clamped output with 10%-90% VDD5V. The output is ratiometric to the supply voltage (VDD5V), which can range from 3.0V to 5.5V. If the DAC reference is switched to an external reference (pin Ext_DAC_ref), the output is ratiometric to the external reference.

#### *Full Scale Mode*

This output mode provides a ratiometric DAC output of (0% to 100%)x Vref *), amplified by the OPAMP stage (default = internal 2x gain, (see Figure 14).

**Note:** For simplification, Figure 8 describes a linear output voltage from rail to rail (0V to VDD). In practice, this is not feasible due to saturation effects of the OPAMP output driver transistors. The actual curve will be rounded towards the supply rails (as indicated in Figure 8).

*Figure 8. Analog Output, Full Scale Mode (shown for 360º mode)*

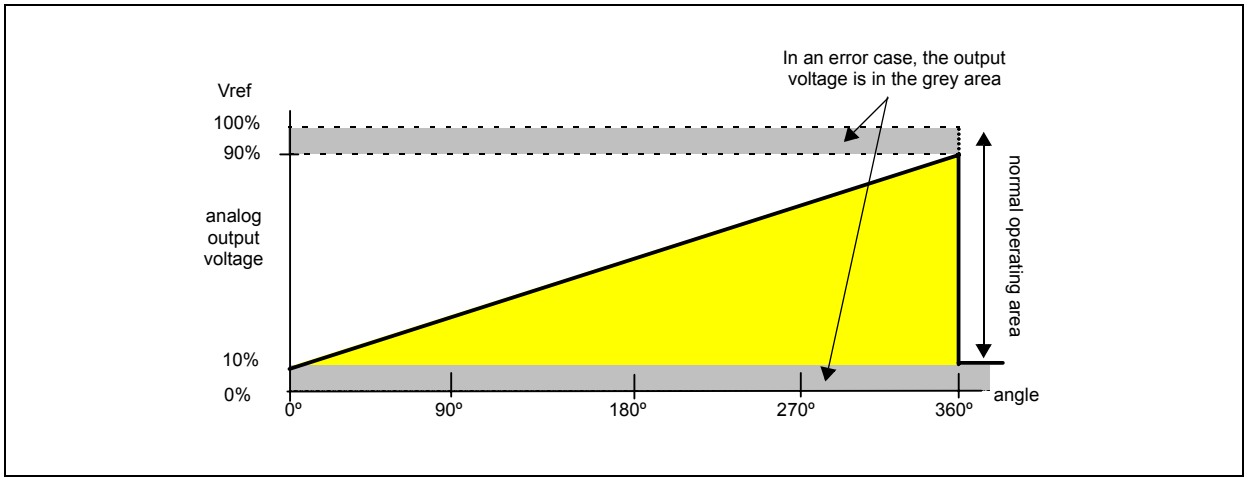



**Note:** Figure 8 and Figure 9 are shown for 360º operation. See Table 10 for further angular range programming options.

### *Diagnostic Output Mode*

In Diagnostic Output Mode (see Figure 9), the analog output of the internal DAC ranges from 10% - 90% Vref*). In an error case, either when the supply is interrupted or when the magnetic field is in the “red” range (see Table 6), the output is switched to 0V and thus indicates the error condition. It is possible to enable the analog output permanently (it will not be switched off even if the magnetic field is out of range). To enable this feature, an OTP bit in the factory setting must be set. The corresponding bit is FS6. See application note AS5040-20 (Extended features of OTP programming) for further details. The application note is available for download at the austriamicrosystems website.

*Figure 9. Diagnostic Output Mode*




The analog and digital outputs will have the following conditions:

*Table 8. Conditions for Analog and Digital Outputs*

| Status | DAC Output Voltage | SSI Digital Output |
|---|---|---|
| Normal operation | 10% - 90% $V_{REF}$[1] | #0 - #1023 (0º-360º), MagRNGn = 1 |
| Magnetic field out of range | < 10% $V_{REF}$, DAC output is switched to 0V | #0 - #1023 (0º-360º) Out of range is signaled in status bits: MagINC=MagDEC=LIN=1, MagRNGn= 0 |

*Table 8. Conditions for Analog and Digital Outputs*

| Status | DAC Output Voltage | SSI Digital Output |
|---|---|---|
| Broken positive power supply (VOUT pull down resistor at receiving side) | < 10% VDD[2] | With pull down resistor at DO (receiving side), all bits read by the SSI will be "0"-s, indicating a non-valid output. |
| Broken power supply ground (VOUT pull down resistor at receiving side) | < 10% VDD | |
| Broken positive power supply (VOUT pull up resistor at receiving side) | > 90% VDD | |
| Broken power supply ground (VOUT pull up resistor at receiving side) | > 90% VDD | |

1. VREF = Internal: ½ * VDD5V (pin #26,27) or external: $V_{DACref}$ (pin#12,13), depending on Ref_extEN bit in OTP (0=int., 1=ext.)
2. VDD = positive supply voltage at receiving side (3.0 – 5.5V).

## Programming the AS5243

**Note:** A detailed description of the austriamicrosystems low voltage polyfuse OTP programming method is given in Application Note AN5000-30, which can be downloaded from the austriamicrosystems website. The OTP programming description in this datasheet is for general information only.

After power-on, programming the AS5243 is enabled with the rising edge of CSn with PDIO = high and CLK = low. The AS5243 programming is a one-time-programming (OTP) method, based on polysilicon fuses. The advantage of this method is that a programming voltage of only 3.3V is required for programming. The OTP consists of 52 bits, of which 21 bits are available for user programming. The remaining 31 bits contain factory settings and a unique chip identifier (Chip-ID).

A single OTP cell can be programmed only once. By default, the cell is "0". A programmed cell will contain "1". While it is not possible to reset a programmed bit from "1" to "0", multiple OTP writes are possible, as long as only unprogrammed "0"-bits are programmed to "1". Independent of the OTP programming, it is possible to overwrite the OTP register temporarily with an OTP write command at any time. This setting will be cleared and overwritten with the hard programmed OTP settings at each power-up sequence or by a LOAD operation.

The OTP memory can be accessed in several ways:

- **Load Operation**: The Load operation reads the OTP fuses and loads the contents into the OTP register. Note that the Load operation is automatically executed after each power-on-reset.
- **Write Operation**: The Write operation allows a temporary modification of the OTP register. It does not program the OTP. This operation can be invoked multiple times, and will remain set while the chip is supplied with power and while the OTP register is not modified with another Write or Load operation.
- **Read Operation**: The Read operation reads the contents of the OTP register, for example to verify a Write command or to read the OTP memory after a Load command.
- **Program Operation**: The Program operation writes the contents of the OTP register permanently into the OTP ROM.
- **Analog Readback Operation**: The Analog Readback operation allows a quantifiable verification of the programming. For each programmed or unprogrammed bit, there is a representative analog value (in essence, a resistor value) that is read to verify whether a bit has been successfully programmed or not.

## OTP Memory Assignment

*Table 9. OTP Bit Assignment*

| Bit | Symbol | Function | |
|---|---|---|---|
| | mbit1 | Factory Bit | |
| 51 | OR0 | Output Range Selection | Customer Section |
| 50 | OR1 | | |
| 49 | ClampMdEn | VOUT Clamping | |
| 48 | RefExtEn | DAC Reference | |
| 47 | FbIntEn | OPAMP Feedback | |
| 46 | Z0 | 10 bit Zero Position | |
| : | : | | |
| 37 | Z9 | | |
| 36 | CCW | Direction | |
| 35 | RA0 | Redundancy Address | |
| : | : | | |
| 31 | RA4 | | |
| 30 | FS 0 | Factory Bit | Factory Section |
| : | FS 1 | Factory Bit | |
| 18 | FS12 | Factory Bit | |
| 17 | ChipID0 | 18 bit Chip ID | ID Section |
| 16 | ChipID1 | | |
| : | : | | |
| 0 | ChipID17 | | |
| | mbit0 | Factory Bit | |

## User Selectable Settings

The AS5243 allows programming of the following user selectable options:

- **CCW:** Counter Clockwise Bit.
  ccw=0 – angular value increases in clockwise direction.
  ccw=1 – angular value increases in counterclockwise direction.
- **Z [9:0]:** Programmable Zero / Index Position.
-
- **FB_intEN:** OPAMP gain setting – 0=external, 1=internal.
- **RefExtEN:** DAC reference – 0=internal, 1=external.
- **ClampMd EN:** Analog output span – 0=0-100%, 1=10-90%*VDD.
- **Output Range (OR0, OR1):** Analog Output Range Selection –

  [1:0] 00 = 360º 01 = 180º

  10 = 90º 11 = 45º

### OTP Default Setting

The AS5243 can also be operated without programming. The default, un-programmed setting is as listed below.

- **Output Range (OR0, OR1):** 00 = 360º
- **ClampMd EN:** Analog output span – 0=0-100%
- **RefExtEN:** DAC reference – 0=internal
- **FB_intEN:** OPAMP gain setting – 0=external.
- **Z [9:0]:** No Programmed Zero Position.
- **CCW:** 0 = Clockwise operation.
- **RA4 to RA0:** 0 = No OTP bit is selected.

### Redundant Programming Option

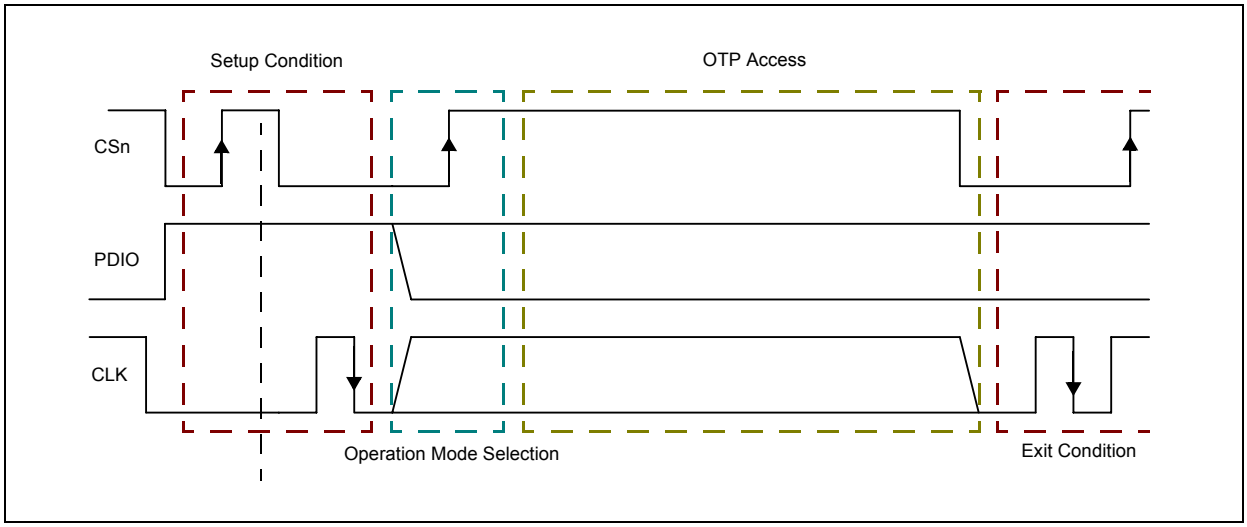
In addition to the regular programming, a redundant programming option is available. This option allows that one selectable OTP bit can be set to “1” (programmed state) by writing the location of that bit into a 5-bit address decoder. This address can be stored in bits RA5…0 in the OTP user settings.

Example: Setting RA5…0 to “00001” selects bit 51 = OR0, “00010” selects bit 50 = OR1, “10000” selects bit 36 = CCW, etc.

### OTP Register Entry and Exit Condition

To avoid accidental modification of the OTP during normal operation, each OTP access (Load, Write, Read, Program) requires a defined entry and exit procedure, using the CSn, PDIO and CLK signals as shown in Figure 10.

*Figure 10. OTP Access Timing Diagram*

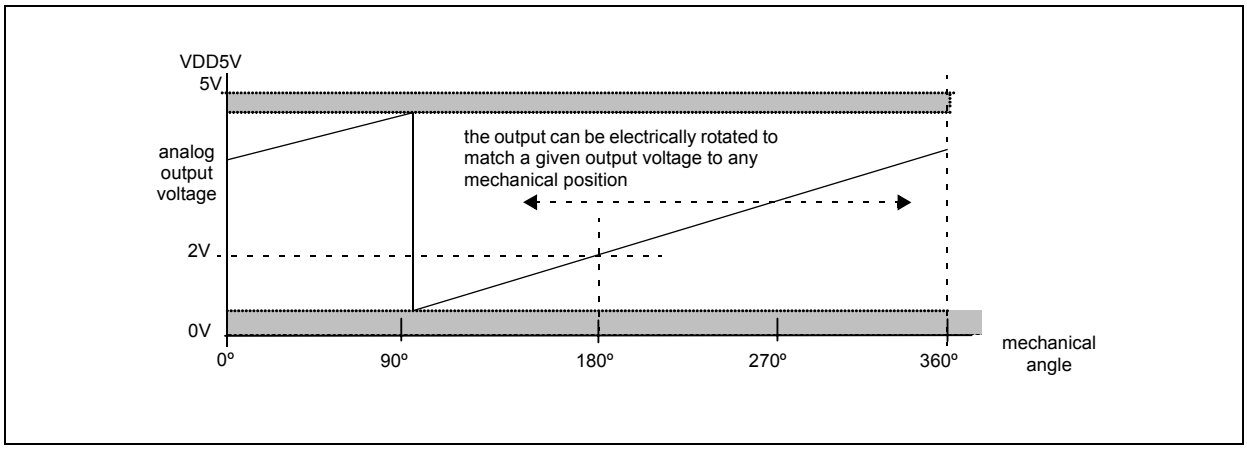



### Zero Position Programming

The AS5243 allows easy assembly of the system, as the actual angle of the magnet does not need to be considered. By OTP programming, any position can be assigned as the new permanent zero position with an accuracy of 0.35º (all modes). Using the same procedure, the AS5243 can be calibrated to assign a given output voltage to a given angle. With this approach, all offset errors (DAC + OPAMP) are also compensated for the calibrated position.

Essentially, for a given mechanical position, the angular measurement system is electrically rotated (by changing the Zero Position value in the OTP register), until the output matches the desired mechanical position. The example in Figure 11 below shows a configuration for 5V supply voltage and 10%-90% output voltage range. It is adjusted by Zero Position Programming to provide an analog output voltage of 2.0 Volts at an angle of 180º. The slope of the curve may be further adjusted by changing the gain of the OPAMP output stage and by selecting the desired angular range (360º /180º /90º /45º).

*Figure 11. Zero Position Programming (shown for 360º mode)*




## Alignment Mode

The alignment mode simplifies centering the magnet over the center of the chip to gain maximum accuracy. Alignment mode can be enabled with the falling edge of CSn while PDIO = logic high (Figure 12). The Data bits D9-D0 of the SSI change to a 10-bit displacement amplitude output. A high value indicates large X or Y displacement, but also higher absolute magnetic field strength. The magnet is properly aligned, when the difference between highest and lowest value over one full turn is at a minimum. Under normal conditions, a properly aligned magnet will result in a reading of less than 128 over a full turn. The MagRNGn indicators will be = 1 when the alignment mode reading is < 128. At the same time, both software bits MagINCn and MagDECn in the SSI stream will be pulled to high. A properly aligned magnet will therefore produce a MagINCn = MagDECn = 1 signal throughout a full 360º turn of the magnet. Stronger magnets or short gaps between magnet and IC may show values larger than 128. These magnets are still properly aligned as long as the difference between highest and lowest value over one full turn is at a minimum. The Alignment mode can be reset to normal operation by a power-on-reset (disconnect / re-connect power supply) or by a falling edge on CSn with PDIO = low.

*Figure 12. Enabling the Alignment Mode*

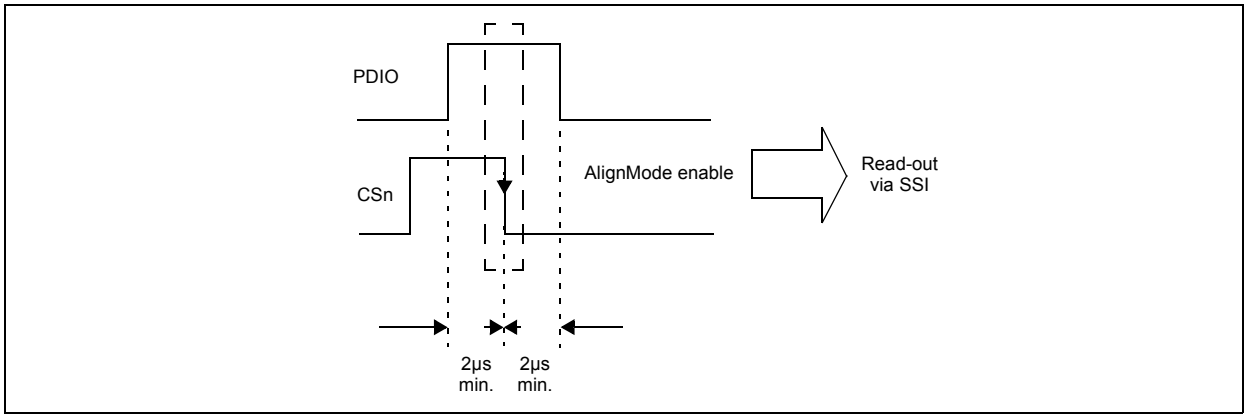
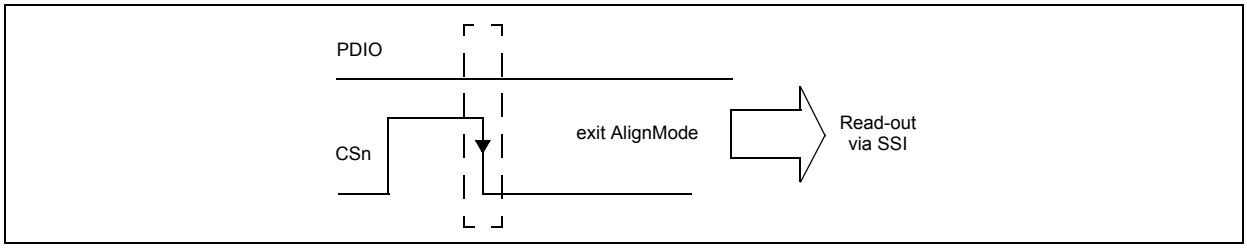



*Figure 13. Exiting Alignment Mode*



## Analog Mode Programming

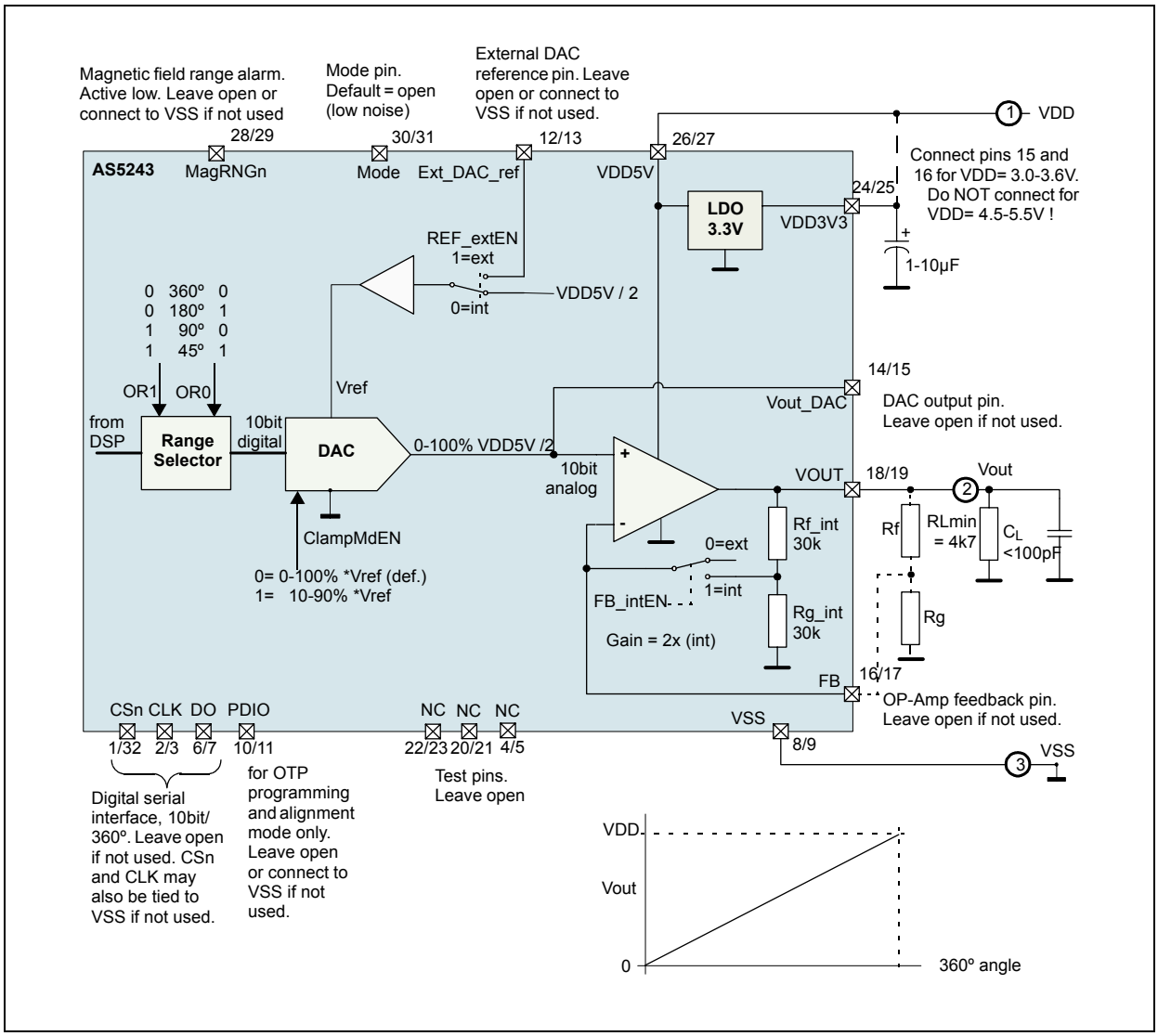
The analog output can be configured in many ways. It consists of following three major building blocks,

- a digital range preselector,
- a 10-bit Digital-to-Analog-Converter (DAC), and
- an OP-AMP buffer stage

In the default configuration (all OTP bits = 0), the analog output is set for 360º operation, internal DAC reference (VDD5V/2), external OPAMP gain, 0-100% ratiometric to VDD5V. Shown below is a typical example for a 0º-360º range, 0-5V output. The complete application requires only one external component, a buffer capacitor at VDD3V3 and has only 3 connections VDD, VSS and VOUT (connectors 1-3).

**Note:** The default setting for the OPAMP feedback path is, FB_intEn=0=external. The external resistors Rf and Rg must be installed. In the programmed state (FB_intEn=1=internal), these resistors do not need to be installed as the feedback path is internal (Rf_int and Rg_int).

*Figure 14. Analog Output Block Diagram*




*Angular Range Selector*

The Angular Range selector allows a digital pre-selection of the angular range. The AS5243 can be configured for a full scale angular range of 45º,90º,180º or 360º. In addition, the Output voltage versus angle response can be fine-tuned by setting the gain of the OP-AMP with external resistors and the maximum output voltage can be set in the DAC. The combination of these options allows to configure the operation range of the AS5243 for all angles up to 360º and output voltages up to 5.5V.

The response curve for the analog output is linear for the selected range (45º /90º /180º /360º). In addition, the slope is mirrored at 180º for 45º- and 90º- modes and has a step response at 270º for the 180º-mode. This allows the AS5243 to be used in a variety of applications. In these three modes, the output remains at VOUT,max and VOUT,min to avoid a sudden output change when the mechanical angle is rotated beyond the selected analog range. In 360º-mode, a jitter between VOUT,max and VOUT,min at the 360º point is also prevented due to a hysteresis.

*Table 10. Digital Range Selector Programming Option*

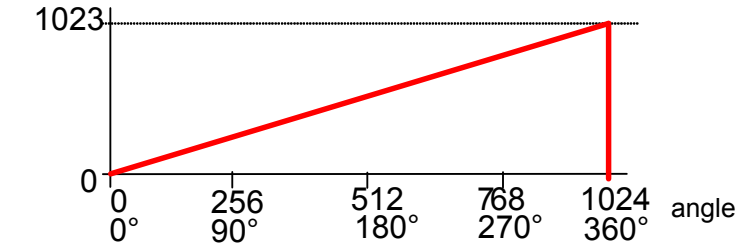
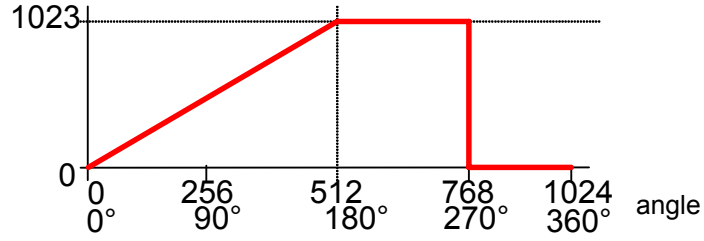
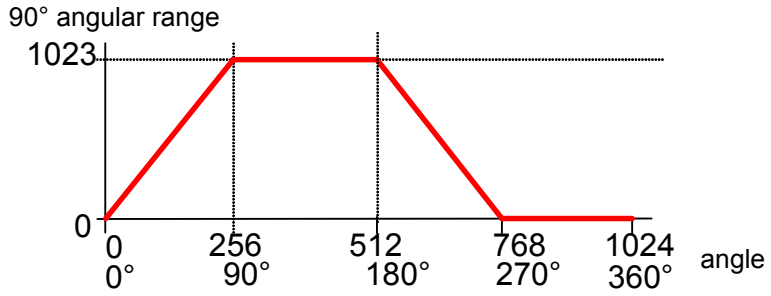
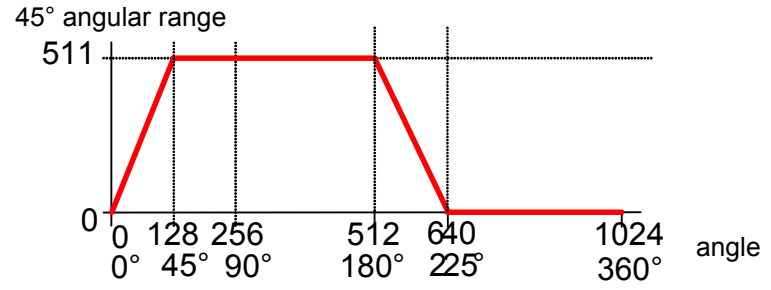
| Output Range1 | Output Range0 | Mode | Note |
|---|---|---|---|
| 0 | 0 | 360° angular range (default)<br>  | Default mode,<br>Analog resolution = 10bit (1024 steps) over 360º<br>Analog step size: 1LSB = 0.35º |
| 0 | 1 | 180° angular range<br>  | Analog resolution = 10bit (1024 steps) over 180º<br>Analog step size: 1LSB = 0.175º |

*Table 10. Digital Range Selector Programming Option*

| Output Range1 | Output Range0 | Mode | Note |
|---|---|---|---|
| 1 | 0 |  | Analog resolution = 10bit (1024 steps) over 90º<br><br>Analog step size: 1LSB = 0.088º |
| 1 | 1 |  | Analog resolution = 9bit (512 steps) over 45º<br><br>Analog step size: 1LSB = 0.088º |

### Repeated OTP Programming

Although a single AS5243 OTP register bit can be programmed only once (from 0 to 1), it is possible to program other, unprogrammed bits in subsequent programming cycles. However, a bit that has already been programmed should not be programmed twice. Therefore it is recommended that bits that are already programmed are set to “0” during a programming cycle.

### Non-permanent Programming

It is also possible to re-configure the AS5243 in a non-permanent way by overwriting the OTP register. This procedure is essentially a “Write Data” sequence (Refer to Programming the AS5243) without a subsequent OTP programming cycle. The “Write Data” sequence may be applied at any time during normal operation. This configuration remains set while the power supply voltage is above the power-on reset level (Refer to Electrical Characteristics). See Application Note AN5000-20 for further information.

### Digital-to-Analog Converter (DAC)

The DAC has a resolution of 10bit (1024 steps) and can be configured for the following options:

*Internal or External Reference*

The default DAC reference is the voltage at pin #26,27 (VDD5V) divided by 2 (see Figure 14). Using this reference, a system that has an output voltage ratiometric to the supply voltage can be built. Optionally, an external reference source, applied at pin#12,13 (Ext_DAC_ref) can be used. This programming option is useful for applications requiring a precise output voltage that is independent of supply fluctuations, for current sink outputs or for applications with a dynamic reference, e.g. attenuation of audio signals.

*0-100% or 10-90% Full Scale Range*

The reference voltage for the DAC is buffered internally. The recommended range for the external reference voltage is 0.2V to (VDD3V3 -0.2)V. The DAC output voltage will be switched to 0V, when the magnetic field is out of range, when the MagINC and MagDEC indicators are both =1 and the MagRNGn-pin (#28,29) will go low. The default full scale output voltage range is 0-100%*VDD5V. Due to limitations in the output stage of an OP-Amp buffer, it cannot drive the output voltage from 0-100% rail-to-rail. Without load, the minimum output voltage at 0º will be a few millivolts higher than 0V and the maximum output voltage will be slightly lower than VDD5V. With increasing load, the voltage drops will increase accordingly. As a programming option, an output range of 10-90%*VDD5V can be selected. In this mode, there is no saturation at the upper and lower output voltage limits like in the 0-100% mode and it allows failure detection as the output voltage will be outside the 10-90% limits, when the magnetic field is in the “red” range (VOUT=0V, see Table 6) or when the supply to the chip is interrupted (VOUT=0V or VDD5V). The unbuffered output of the DAC is accessible at pin #14,15 (VOUT_DAC). This output must not be loaded.

### OP-AMP Stage

The DAC output is buffered by a non-inverting Op-Amp stage. The amplifier is supplied by VDD5V (pin #26,27) and can hence provide output voltages up to 5V. By allowing access to the inverting input of the Op-Amp and with the addition of a few discrete components it can be configured in many ways, like high current buffer, current sink output, adjustable angle range, etc. Per default, the gain of the Op-Amp must be set by two external resistors (see Figure 14). Optionally, the fixed internal gain setting (2x) may be programmed by OTP, eliminating the need for external resistors.

#### *Output Noise*

The Noise level at the analog output depends on two states of the digital angular output:

1. **The digital angular output value is stable.** In this case, the output noise is the figure given as $V_{noise}$ in the Table on page 9. Note that the noise level is given for the default gain of 2x. For other gains, it must be scaled accordingly.
2. The digital output is at the edge of a step. In this case, the digital output may jitter between two adjacent values. The rate of jitter is specified as transition noise (refer to parameter ‘Transition Noise’ on page 7). The resulting output noise is calculated by:

$$V_{noise,Vout} = \frac{TN * VDD5V}{360} + V_{noise,OPAMP} \quad \text{(EQ 1)}$$

**Where:**
$V_{noise,Vout}$ = noise level at pin VOUT in Vrms
TN = transition noise (in ºrms)
VDD5V = Supply voltage VDD5V in V
$V_{noise,OPAMP}$ = noise level of OPAMP

### Application Examples

See Application Note AN5043-10 for AS5143 Application Examples.

## Analog Readback Mode

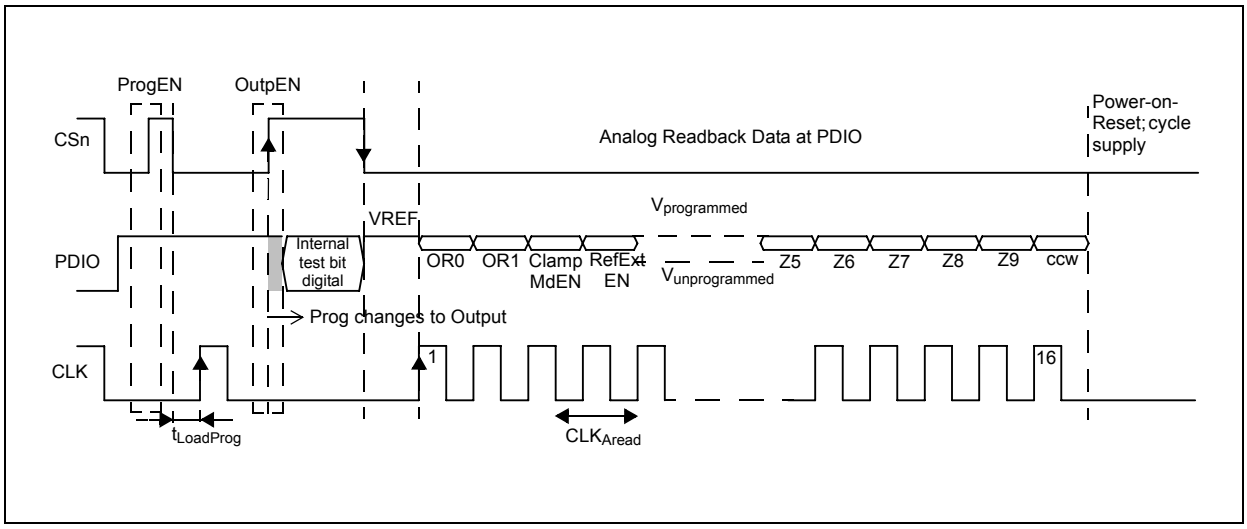
Non-volatile programming (OTP) uses on-chip zener diodes, which become permanently low resistive when subjected to a specified reverse current. The quality of the programming process depends on the amount of current that is applied during the programming process (up to 130mA). This current must be provided by an external voltage source. If this voltage source cannot provide adequate power, the zener diodes may not be programmed properly. In order to verify the quality of the programmed bits, an analog level can be read for each zener diode, giving an indication whether this particular bit was properly programmed or not.

To put the AS5243 in Analog Readback Mode, a digital sequence must be applied to pins CSn, PDIO and CLK as shown in Figure 15. The digital level for this pin depends on the supply configuration (3.3V or 5V; see 3.3V / 5V Operation on page 12). The second rising edge on CSn (OutpEN) changes pin PDIO to a digital output and the log high signal at pin PDIO must be removed to avoid collision of outputs (grey area in Figure 15).

The following falling slope of CSn changes pin PDIO to an analog output, providing a reference voltage VREF, that must be saved as a reference for the calculation of the subsequent programmed and unprogrammed OTP bits. Following this step, each rising slope of CLK outputs one bit of data in the reverse order as during programming, (see Figure 15: Output Range OR0 and -1, ClampMdEn, RefExtEn, FB_IntEn, Z0…Z9, ccw).

During analog readback, any capacitor at pin PDIO should be removed to allow a fast readout rate. The measured analog voltage for each bit must be subtracted from the previously measured VREF, and the resulting value gives an indication on the quality of the programmed bit: a reading of <100mV indicates a properly programmed bit and a reading of >1V indicates a properly unprogrammed bit. A reading between 100mV and 1V indicates a faulty bit, which may result in an undefined digital value, when the OTP is read at power-up. Following the 16th clock (after reading bit “ccw”), the chip must be reset by disconnecting the power supply.

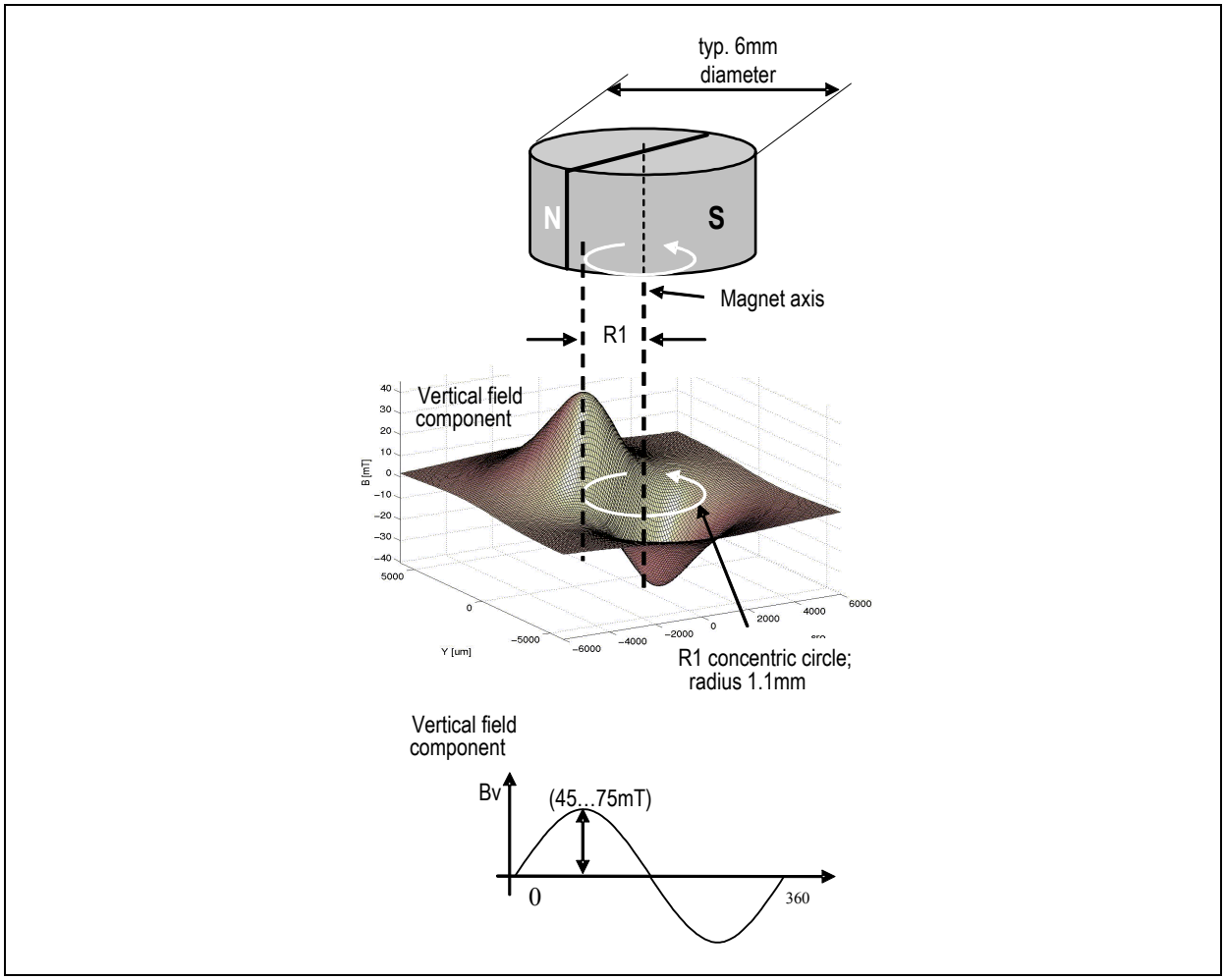
*Figure 15. Analog OTP Register Read*




## Choosing the Proper Magnet

Typically the magnet should be 6mm in diameter and ≥2.5mm in height. Magnetic materials such as rare earth AlNiCo, SmCo5 or NdFeB are recommended. The magnet’s field strength perpendicular to the die surface should be verified using a gauss-meter. The magnetic field $B_V$ at a given distance, along a concentric circle with a radius of 1.1mm (R1), should be in the range of ±45mT…±75mT, (see Figure 16).

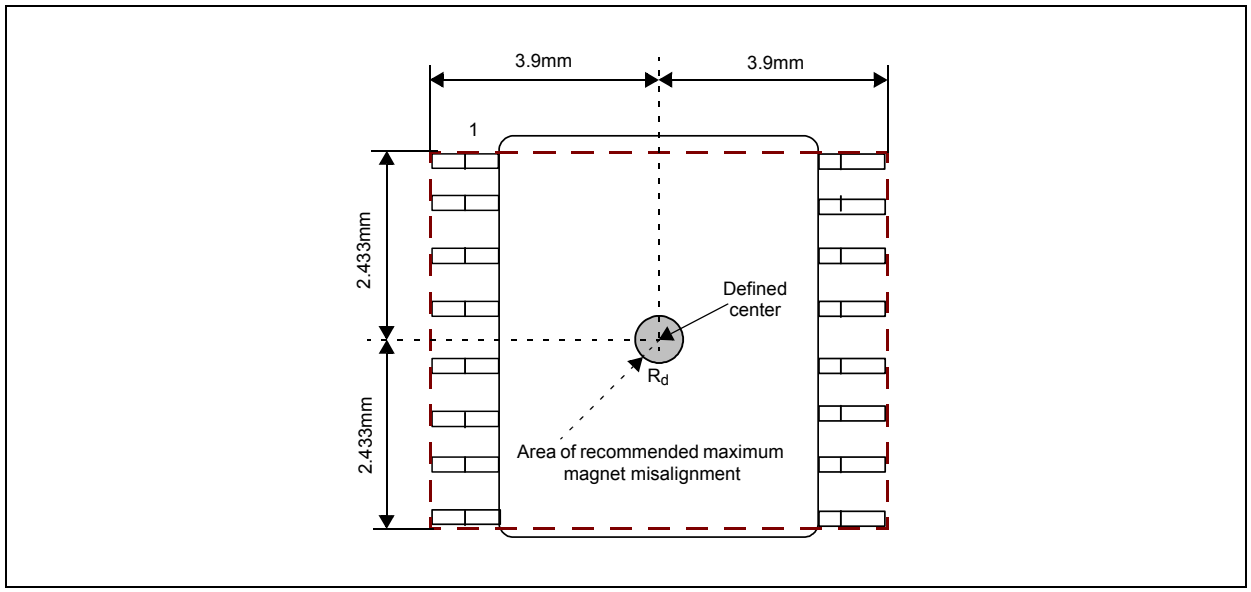
*Figure 16. Typical Magnet and Magnetic Field Distribution*




## Physical Placement of the Magnet

The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the IC package as shown in Figure 17 below.

*Figure 17. Defined IC Center and Magnet Displacement Radius*

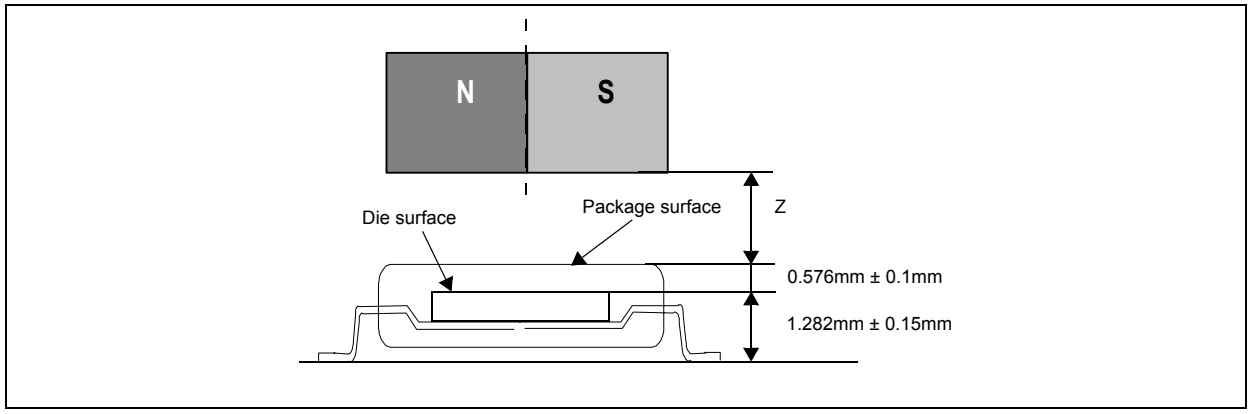



### *Magnet Placement*

The magnet's center axis should be aligned within a displacement radius $R_d$ of 0.25mm from the defined center of the IC with reference to the edge of pin #1 (see Figure 17). This radius includes the placement tolerance of the chip within the QFN32LD(7x7) package (+/- 0.235mm). The displacement radius $R_d$ is 0.485mm with reference to the center of the chip (see Alignment Mode on page 21).

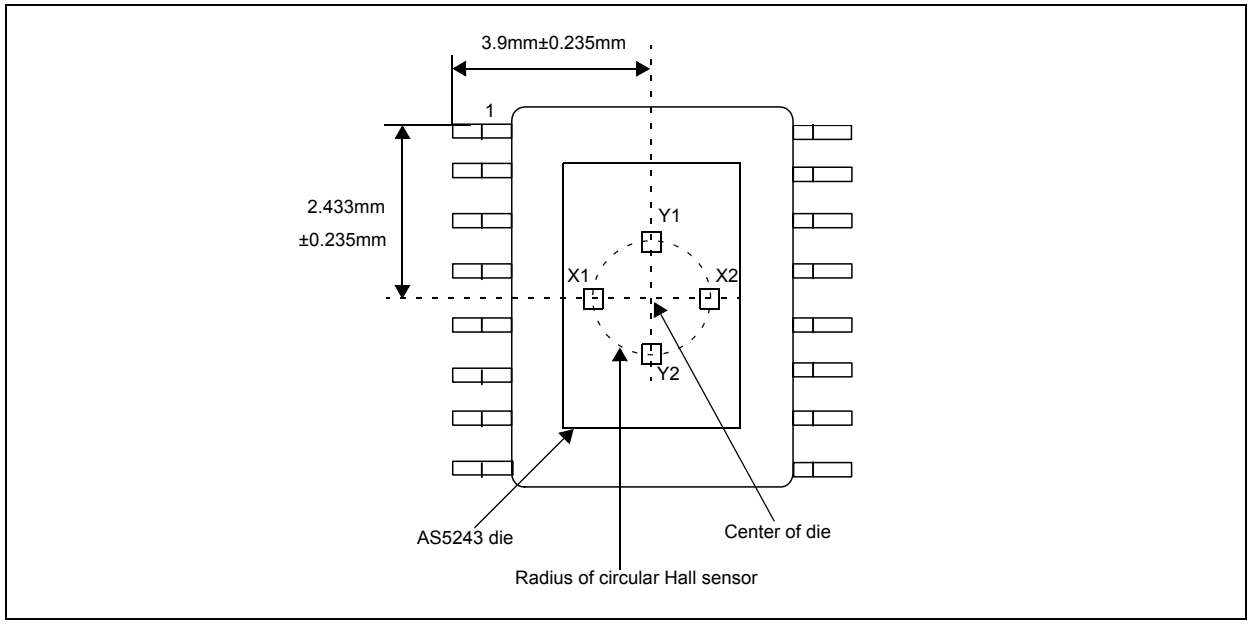
The vertical distance should be chosen such that the magnetic field on the die surface is within the specified limits (see Figure 16). The typical distance "z" between the magnet and the package surface is 0.5mm to 1.8mm with the recommended magnet (6mm x 3mm). Larger gaps are possible, as long as the required magnetic field strength stays within the defined limits. A magnetic field outside the specified range may still produce usable results, but the out-of-range condition will be indicated by MagRNGn (pin 28,29), which will be pulled low. At this condition, the angular data is still available over the digital serial interface (SSI), but the analog output will be turned off.

*Figure 18. Vertical Placement of the Magnet*



## Simulation Modeling

*Figure 19. Arrangement of Hall Sensor Array on Chip (principle)*




With reference to Figure 19, a diametrically magnetized permanent magnet is placed above or below the surface of the AS5243. The chip uses an array of Hall sensors to sample the vertical vector of a magnetic field distributed across the device package surface. The area of magnetic sensitivity is a circular locus of 1.1mm radius with respect to the center of the die. The Hall sensors in the area of magnetic sensitivity are grouped and configured such that orthogonally related components of the magnetic fields are sampled differentially. The differential signal Y1-Y2 will give a sine vector of the magnetic field. The differential signal X1-X2 will give an orthogonally related cosine vector of the magnetic field. The angular displacement ($\Theta$) of the magnetic source with reference to the Hall sensor array may then be modelled by:

$$\Theta = \arctan \frac{(Y1 - Y2)}{(X1 - X2)} \pm 0.5° \quad \text{(EQ 2)}$$

The ±0.5º angular error assumes a magnet optimally aligned over the center of the die and is a result of gain mismatch errors of the AS5243. Placement tolerances of the die within the package are ±0.235mm in X and Y direction, using a reference point of the edge of pin #1 (Figure 19). In order to neglect the influence of external disturbing magnetic fields, a robust differential sampling and ratiometric calculation algorithm has been implemented. The differential sampling of the sine and cosine vectors removes any common mode error due to DC components introduced by the magnetic source itself or external disturbing magnetic fields. A ratiometric division of the sine and cosine vectors removes the need for an accurate absolute magnitude of the magnetic field and thus accurate Z-axis alignment of the magnetic source.

The recommended differential input range of the magnetic field strength ($B_{(X1-X2)}$,$B_{(Y1-Y2)}$) is ±75mT at the surface of the die. In addition to this range, an additional offset of ±5mT, caused by unwanted external stray fields is allowed. The chip will continue to operate, but with degraded output linearity, if the signal field strength is outside the recommended range. Too strong magnetic fields will introduce errors due to saturation effects in the internal preamplifiers. Too weak magnetic fields will introduce errors due to noise becoming more dominant.

## Failure Diagnostics

The AS5243 also offers several diagnostic and failure detection features, which are discussed in detail further in the document.

### Magnetic Field Strength Diagnosis

**By Software:** The MagINC and MagDEC status bits will both be high when the magnetic field is out of range.

**By Hardware:** Pin #28,29 (MagRNGn) is a logical NAND-ed combination of the MagINC and MagDEC status bits. It is an open-drain output and will be turned on (= low with external pull-up resistor) when the magnetic field is out of range.

Pin #18,19 (VOUT) is the analog output of the DAC and OP-Amp. The analog output will be 0V, when the magnetic field is out of range (all analog modes).

### Power Supply Failure Detection

**By Software:** If the power supply to the AS5243 is interrupted, the digital data read by the SSI will be all “0”s. Data is only valid, when bit OCF is high, hence a data stream with all “0”s is invalid. To ensure adequate low levels in the failure case, a pull-down resistor (~10kΩ) should be added between pin DO and VSS at the receiving side.

**By Hardware:** The MagRNGn pin is an open drain output and requires an external pull-up resistor. In normal operation, this pin is high ohmic and the output is high. In a failure case, either when the magnetic field is out of range or the power supply is missing, this output will become low. To ensure an adequate low level in case of a broken power supply to the AS5243, the pull-up resistor (~10kΩ) must be connected to the positive supply at pin 26,27 (VDD5V).

## Angular Output Tolerances

### Accuracy; Digital Outputs

Accuracy is defined as the error between measured angle and actual angle. It is influenced by several factors:

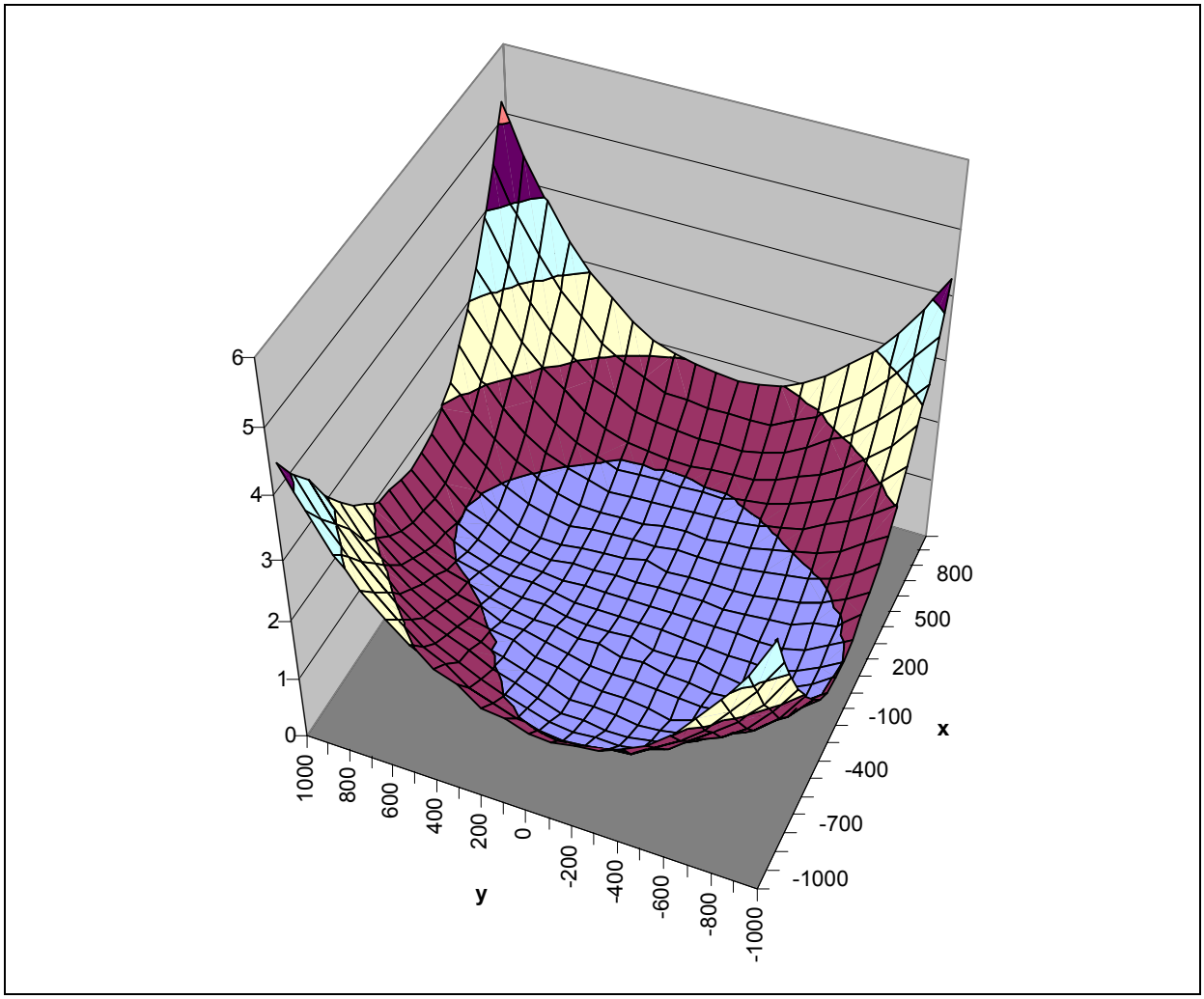
- The non-linearity of the analog-digital converters,
- Internal gain and mismatch errors,
- Non-linearity due to misalignment of the magnet.

As a sum of all these errors, the accuracy with centered magnet = ($Err_{max}$ – $Err_{min}$)/2 is specified as better than ±0.5 degrees @ 25ºC (see Figure 21). Misalignment of the magnet further reduces the accuracy. Figure 20 shows an example of a 3D-graph displaying non-linearity over XY-misalignment. The center of the square XY-area corresponds to a centered magnet (see dot in the center of the graph). The X- and Y- axis extends to a misalignment of ±1mm in both directions. The total misalignment area of the graph covers a square of 2x2 mm (79x79mil) with a step size of 100µm. For each misalignment step, the measurement as shown in Figure 21 is repeated and the accuracy ($Err_{max}$ – $Err_{min}$)/2 (e.g. 0.25º in Figure 21) is entered as the Z-axis in the 3D-graph.

### Accuracy; Analog Output

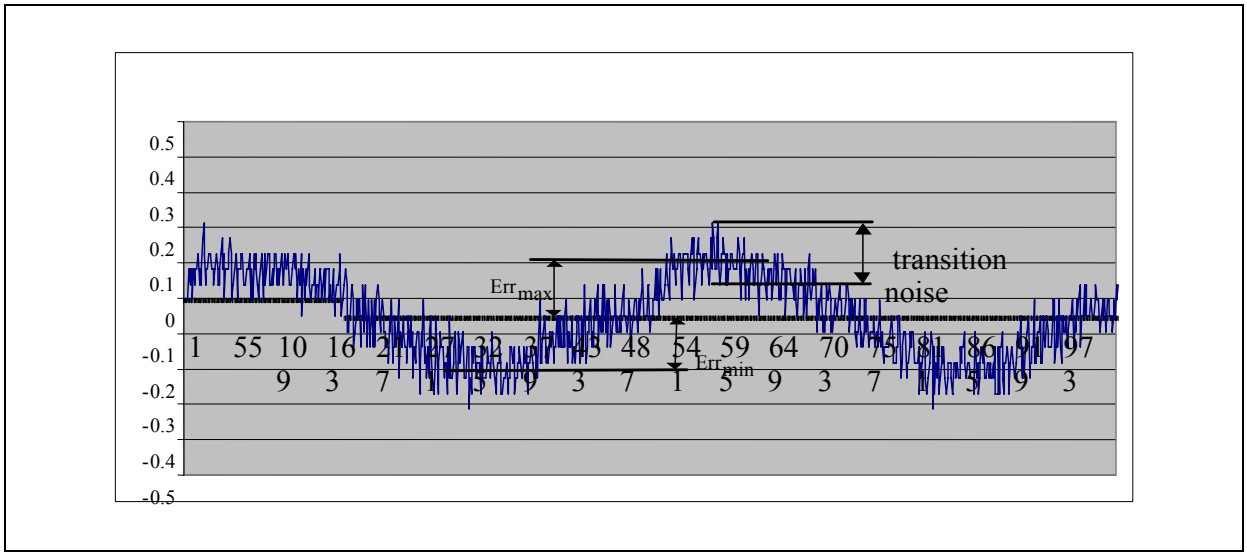
The analog output has the same accuracy as the digital output with the addition of the nonlinearities of the DAC and the OPAMP (±1LSB; see Table on page 8).

*Figure 20. Example of Linearity Error Over XY Misalignment*




The maximum non-linearity error on this example is better than ±1 degree (inner circle) over a misalignment radius of ~0.7mm. For volume production, the placement tolerance of the IC within the package (±0.235mm) must also be taken into account. The total nonlinearity error over process tolerances, temperature and a misalignment circle radius of 0.25mm is specified better than ±1.4 degrees. The magnet used for these measurement was a cylindrical NdFeB (Bomatec® BMN-35H) magnet with 6mm diameter and 2.5mm in height.

*Figure 21. Example of Linearity Error Over 360º*




## Transition Noise

Transition noise is defined as the jitter in the transition between two steps. Due to the nature of the measurement principle (Hall sensors + Preamplifier + ADC), there is always a certain degree of noise involved. This transition noise voltage results in an angular transition noise at the outputs. It is specified as 0.06 degrees rms (1 sigma)[1]. This is the repeatability of an indicated angle at a given mechanical position. The transition noise has different implications on the type of output that is used:

- **Absolute Output; SSI Interface:** The transition noise of the absolute output can be reduced by the user by applying an averaging of readings. An averaging of 4 readings will reduce the transition noise by 6dB or 50%, e.g. from 0.03ºrms to 0.015ºrms (1 sigma) in slow mode.
- **Analog Output:** Ideally, the analog output should have a jitter that is less than one digit. In 360º mode, both fast or slow mode may be selected for adequate low jitter. In 180º, 90º or 45º mode, where the step sizes are smaller, slow mode should be selected to reduce the output jitter.

## High Speed Operation

### *Sampling Rate*

The AS5243 samples the angular value at a rate of 10.42k samples per second (ksps) in fast mode and 2.61ksps in slow mode. Consequently, a new reading is performed each 96µs. (fast mode) or 384µs (slow mode). At a stationary position of the magnet, this sampling rate creates no additional error.

### *Absolute Mode*

With the given sampling rates, the number of samples (n) per turn for a magnet rotating at high speed can be calculated by

$$n = \frac{60}{rpm \cdot 96\mu s} \quad \text{for fast mode} \qquad \text{(EQ 3)}$$

$$n = \frac{60}{rpm \cdot 384\mu s} \quad \text{for slow mode} \qquad \text{(EQ 4)}$$

1. Statistically, 1 sigma represents 68.27% of readings; 3 sigma represents 99.73% of readings.

In practice, there is no upper speed limit. The only restriction is that there will be fewer samples per revolution as the speed increases. Regardless of the rotational speed, the absolute angular value is always sampled at the highest resolution.

*Table 11. Speed Performance*

| Fast Mode (pin Mode = 1) | Slow Mode (pin Mode = 0 or open) |
|---|---|
| 610rpm = 1024 samples / turn | 610rpm = 256 samples / turn |
| 1220rpm = 512 samples / turn | 1220rpm = 128 samples / turn |
| 2441rpm = 256 samples / turn | 2441rpm = 64 samples / turn |
| etc. | etc. |

## Output Delays

The propagation delay is the delay between the time that the sample is taken until it is available as angular data. This delay is 96µs in fast mode (pin Mode = high) and 384µs in slow mode (pin Mode = low or open). The analog output produces no further delay, the output voltage will be updated as soon as it is available. Using the SSI interface for data transmission, an additional delay must be considered, caused by the asynchronous sampling (0…$1/f_{sample}$) and the time it takes the external control unit to read and process the angular data from the AS5243.

### *Angular Error Caused by Propagation Delay*

A rotating magnet will therefore cause an angular error caused by the output delay. This error increases linearly with speed:

$$e_{sampling}\ (deg) = 6 * rpm * prop.delay \qquad (EQ\ 5)$$

**Where:**

$e_{sampling}$ = angular error [º]
rpm = rotating speed [rpm]
prop.delay = propagation delay [seconds]

**Note:** Since the propagation delay is known, it can be automatically compensated by the control unit processing the data from the AS5243.

## Internal Timing Tolerance

The AS5243 does not require an external ceramic resonator or quartz. All internal clock timings for the AS5243 are generated by an on-chip RC oscillator. This oscillator is factory trimmed to ±5% accuracy at room temperature (±10% over full temperature range). This tolerance influences the ADC sampling rate.

### *Absolute Output; SSI Interface*

A new angular value is updated every 96µs ±5% (Mode = 1) or 384µs ±5% (Mode = 0 or open).

## Temperature

### *Magnetic Temperature Coefficient*

One of the major benefits of the AS5243 compared to linear Hall sensors is that it is much less sensitive to temperature. While linear Hall sensors require a compensation of the magnet's temperature coefficients, the AS5243 automatically compensates for the varying magnetic field strength over temperature. The magnet's temperature drift does not need to be considered, as the AS5243 operates with magnetic field strengths from ±45…±75mT.

Example:

A NdFeB magnet has a field strength of 75mT @ -40ºC and a temperature coefficient of -0.12% per Kelvin. The temperature change is from –40º to +150º = 165K. The magnetic field change is: 165 x -0.12% = -19.8%, which corresponds to 75mT at –40ºC and 60mT at 150ºC.

In the above described scenario, the AS5243 can automatically compensate for the change in temperature related field strength. No user adjustment is required.

### *Accuracy Over Temperature*

The influence of temperature in the absolute accuracy is very low. While the accuracy is ≤ ±0.5º at room temperature, it may increase to ≤±0.9º due to increasing noise at high temperatures.

### *Timing Tolerance Over Temperature*

The internal RC oscillator is factory trimmed to ±5%. Over temperature, this tolerance may increase to ±10%. Generally, the timing tolerance has no influence in the accuracy or resolution of the system, as it is used mainly for internal clock generation.

# 8 Application Information

## Benefits of AS5243

- Complete system-on-chip
- Angle measurement with programmable range up to 360º
- High reliability due to non-contact magnetic sensing
- Ideal for applications in harsh environments
- Robust system, tolerant to magnet misalignment, airgap variations, temperature variations and external magnetic fields
- No calibration required
- Building of redundancy systems with plausibility checks

# 9 Package Drawings and Markings

The device is available in a QFN32LD(7x7) Package.

*Figure 22. Package Drawings*

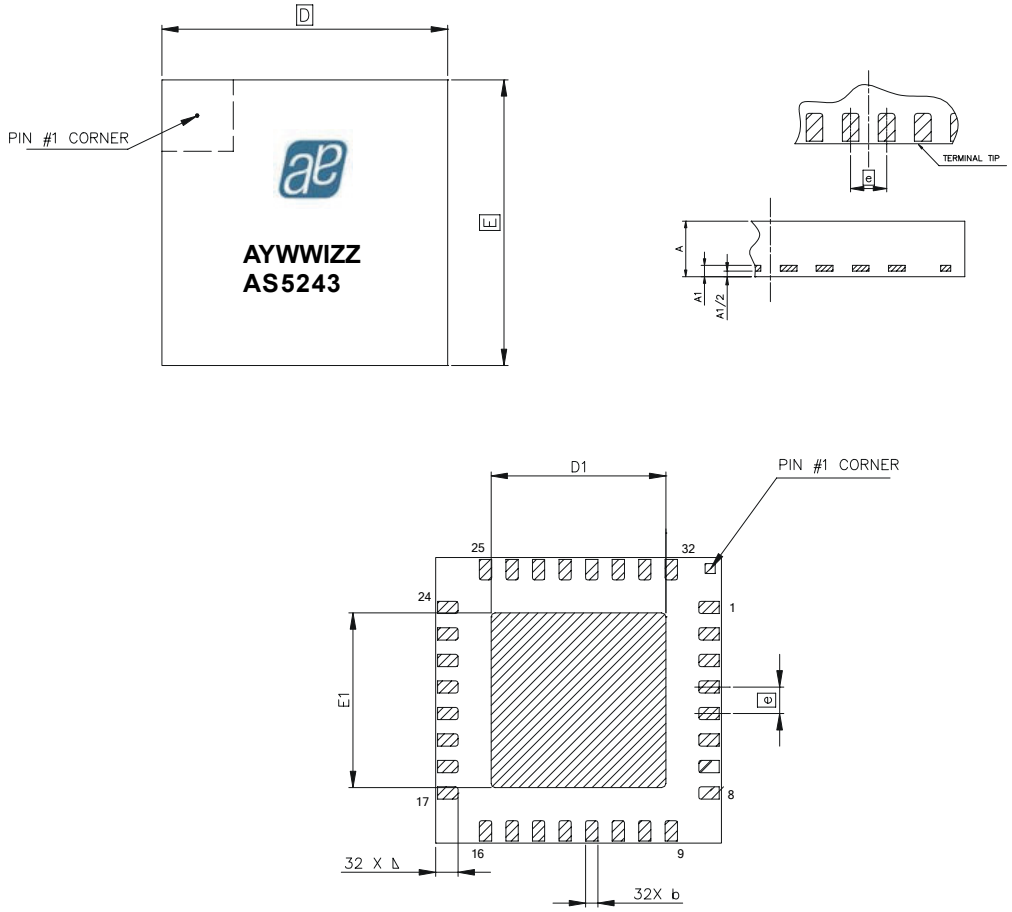



*Table 12. QFN-32 package dimensions*

| Symbol | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| D | | 7 BSC | | | 0.28 BSC | |
| E | | 7 BSC | | | 0.28 BSC | |
| D1 | 4.18 | 4.28 | 4.38 | 0.165 | 0.169 | 0.172 |
| E1 | 4.18 | 4.28 | 4.38 | 0.165 | 0.169 | 0.172 |
| L | 0.45 | 0.55 | 0.65 | 0.018 | 0.022 | 0.026 |
| b | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| e | | 0.65 BSC | | | 0.026 BSC | |
| A | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 |
| A1 | | 0.203 REF | | | 0.008 REF | |

# 10 Ordering Information

The devices are available as the standard products shown in Table 13.

*Table 13. Ordering Information*

| Model | Description | Delivery Form | Package |
|---|---|---|---|
| AS5243ASSU | | Tubes | QFN32 |
| AS5243ASST | | Tape and Reel | QFN32 |

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