1 General Description

The AS5030 is a contactless magnetic rotary encoder for accurate angular measurement over a full turn of 360°. It is a system-on-chip, combining integrated Hall elements, analog front end and digital signal processing in a single device.

To measure the angle, only a simple two-pole magnet, rotating over the center of the chip is required.

The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of 8 bit = 256 positions per revolution. This digital data is available as a serial bit stream and as a PWM signal.

In addition to the angle information, the strength of the magnetic field is also available as a 6-bit code.

Data transmission can be configured for 1-wire (PWM), 2-wires (CLK, DIO) or 3-wires (CLK, DIO, CS).

A software programmable (OTP) zero position simplifies assembly as the zero position of the magnet does not need to be mechanically aligned.

A Power Down Mode together with fast startup- and measurement cycles allows for very low average power consumption and makes the AS5030 also suitable for battery operated equipment.
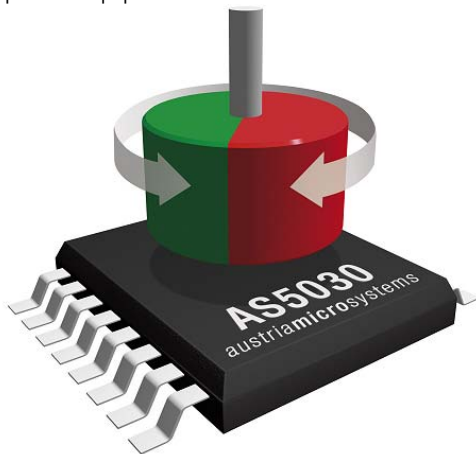

Figure 1: Typical arrangement of AS5030 and magnet

1.1 Benefits

- Complete system-on-chip, no calibration required

- Flexible system solution provides absolute serial and PWM output

- Ideal for applications in harsh environments due to magnetic sensing principle

- High reliability due to non-contact sensing

- Robust system, tolerant to horizontal misalignment, airgap variations, temperature variations and external magnetic fields

1.2 Key Features

- 360° contactless angular position encoding

- Two digital 8-bit absolute outputs:
    - Serial interface and
    - Pulse width modulated (PWM) output

- User programmable zero position

- High speed: up to 30,000 rpm

- Direct measurement of magnetic field strength allows exact determination of vertical magnet distance

- Serial read-out of multiple interconnected AS5030 devices using daisy chain mode

- Wide magnetic field input range: 20 ~ 80mT

- Wide temperature range: - 40°C to + 125°C

- Small Pb-free package: TSSOP 16

1.3 Applications

- Contactless rotary position sensing

- Rotary switches (human machine interface)

- AC/DC motor position control

- Robotics

- Encoder for battery operated equipment
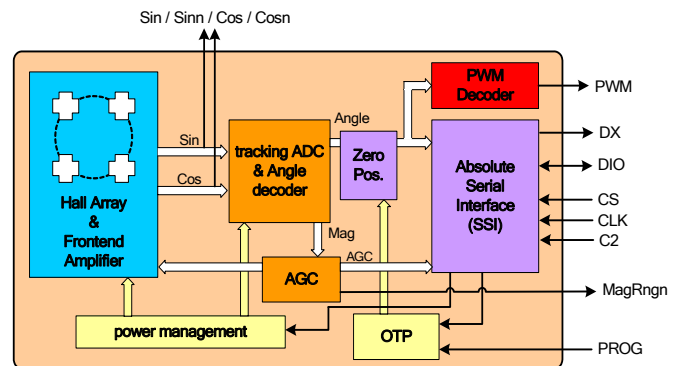
1.4 Block Diagram

Figure 2: AS5030 block diagram

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2   Package and Pinout

The AS5030 is available in a TSSOP16 package
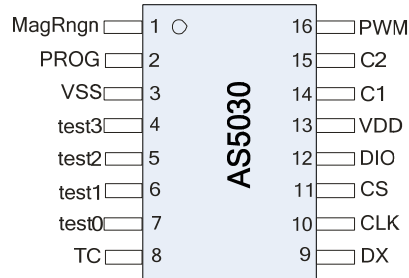
Figure 3: TSSOP-16 package and pin-out

Pin# TSSOP	Symbol	Type	Description
1	MagRngn	DO_T	Push-Pull output. Is HIGH when the magnetic field strength is too weak, e.g. due to missing magnet
2	Prog_DI	S	OTP Programming voltage supply pin. Leave open or connect to VDD if not used
3	VSS	S	Supply ground
4	T3_SINn	-	This pin is used for factory testing. For normal operation it must be left unconnected. Inverse SIN (Sinn) output in SIN/COS output mode
5	T2_SIN	-	This pin is used for factory testing. For normal operation it must be left unconnected. SIN output in SIN/COS mode
6	T1_COSn	-	This pin is used for factory testing. For normal operation it must be left unconnected. Inverse COS (Cosn) output in SIN/COS mode
7	T0_COS	-	This pin is used for factory testing. For normal operation it must be left unconnected. COS output in SIN/COS mode
8	TC	-	Test pin. Connect to VSS or leave unconnected
9	DX	DO	Digital output for 2-wire operation and Daisy Chain mode
10	CLK	DI_ST	Clock Input of Synchronous Serial Interface; Schmitt-Trigger input
11	CS	DI_ST	Chip Select for serial data transmission, active high; Schmitt-Trigger input, external pull-down resistor (~50kΩ) required in read-only mode
12	DIO	DIO	Data output / command input for digital serial interface
13	VDD	S	Positive supply voltage, 4.5V to 5.5V
14	C1	DI	Configuration input: connect to VSS for normal operation, connect to VDD to enable SIN-COS outputs. This pin is scanned at power-on-reset and at wakeup from one of the Ultra Low Power Modes
15	C2	DI	Configuration input: connect to VSS for 3-wire operation, connect to VDD for 2-wire operation. This pin is scanned at power-on-reset and at wakeup from one of the Ultra Low Power Modes
16	PWM	DO	Pulse Width Modulation output, 2µs pulse width per step (2µs ~ 512µs)

Table 1: Pin description

Pin types: S: supply pin   DO: digital output
               DI_ST: digital input / Schmitt-Trigger   DO_T: digital output / tri-state
               DIO: bi-directional digital pin   DI: digital input (standard CMOS; no pull-up or pull-down)

3   AS5030 Parameter and Features List

Parameter	Description
Supply Voltage	5V ± 10%
Supply Current	Low Power Mode, non-operational: typ. 1.4mA Ultra Low Power Mode, non-operational: typ. 30μA Normal operating mode: typ. 14mA.
Absolute Output; Serial Interface	21-bit Synchronous Serial Interface (SSI): 5 command bits, 2 data valid bits, 6 data bits for magnetic field strength, 8 data bits for angle. Configurable for 2-wire (Clock, Data) or 3-wire (Chip Select, Clock, Data) operation Daisy Chain mode for reading multiple encoders through a 2- or 3-wire interface. Zero Position Programming (OTP)
SSI Clock rate	≤ 6 MHz data clock rate, 250 ~ 500kHz during programming
2-wire Readout Mode	DIO and CLK signals. 0.1 ~ 6MHz clock rate. Synchronization through time-out of CLK signal.
Power Down Modes	Activated and deactivated by software commands. Low Power Mode: power down current = 1.4mA typ.; power up time <150μs Ultra Low Power Mode : power down current = 30μA typ.; power up time <500μs
Digital input cells	CLK, CS = Schmitt trigger inputs
SIN-COS mode	Sine, inverse Sine, Cosine and inverse Cosine outputs. 360° per period.
Maximum Speed	30,000 rpm with locked ADC
Resolution and Accuracy	Resolution = 8 bit (1.406°) Accuracy ≤ ± 2° with centered magnet
Transition Noise	0.24°rms (1 sigma)
PWM output	2.26μs / Step, PWM will be permanently low when angular data is not valid (e.g during startup).
Digital Output Current	4mA @ VDD = 5V (PWM, DIO, DX, MagRngn outputs)
OTP programming mode	Through serial interface with static programming voltage on pin #2 (PROG) 16-bit OTP programming register. OTP user programming options: Angular zero position: 8 bit Hall element sensitivity: 2 bit
Magnetic Field Range	Trimable in four steps with OTP programming (sensitivity) maximum/minimum ratio ~ 2.5:1. Field range window = 20 ~ 80mT (e.g. maximum sensitivity range = 20 ~ 48mT, minimum sensitivity range = 32 ~ 80mT
Non-Valid-Range indication	by hardware: MagRngn pin indicates locked condition of ADC by software: LOCK1&2 status bits indicate locked condition of ADC
Start upTimings	Start-up time after shutdown < 2ms Start-up time after power-down from Ultra Low Power Mode : < 500μs Start-up time after power-down from Low Power Mode : < 150μs
ESD protection	± 2kV
Operating Temperature	-40°C ~ +125 °C

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4   General Device Specifications

(operating conditions: T_{amb} = -40°C to +125°C, VDD5V = 4.5V ~ 5.5V, all voltages referenced to VSS, unless otherwise noted)

4.1   Absolute Maximum Ratings (non operating)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	VDD	-0.3	7	V	(1) Except during OTP programming
Input Pin Voltage	V_{in}	VSS - 0.5	VDD + 0.5	V	
Input Current (latch up immunity)	I_{scr}	-100	100	mA	Norm: Jedec 17
ESD		±2		kV	Norm: MIL 883 E method 3015
Package Thermal Resistance	Θ_{JA}		137	°C/W	Still Air / Single Layer PCB
			89	°C/W	Still Air / Multilayer PCB
Storage Temperature	T_{strg}	-55	125	°C	
Soldering conditions, Body temperature (Pb-free package)	T_{lead}		260	°C	T=20s to 40s, Norm: IPC/JEDEC J-Std-020C. Lead finish 100% Sn "matte tin"
Humidity non-condensing		5	85	%	

4.2   Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Positive Supply Voltage	VDD	4.5		5.5	V	
Operating Current	IDD		14	18	mA	No load on outputs. Minimum AGC (strong magnetic field)
			18	22		No load on outputs. Maximum AGC (weak or no magnetic field)
Power down current	I_{off}		1400	2000	µA	Low Power Mode
			30	120		Ultra Low Power Mode
Ambient Temperature	T_{amb}	-40		125	°C	-40°F ~ +257°F
Junction Temperature	T_J			140	°C	

4.3 System Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Note
Resolution	N		8		bit	
			1.406		°	
Power Up Time	T_{PwrUp}			1000	µs	Startup from zero; AGC not regulated
				3800		Startup from zero until regulated AGC
				500		Startup from Power Down Mode
				150		Startup from Low Power Mode
Propagation delay	t_{da}		15	17	µs	Analog signal path; over full temperature range
Tracking rate	t_{dd}	0.85	1.15	1.45	µs	step rate of tracking ADC; 1 step = 1.406°
Signal processing delay	t_{delay}		16.15	18.45	µs	Total signal processing delay, analog + digital (t_{da} + t_{dd})
Analog filter time constant	T	4.1	6.6	12.5	µs	Internal lowpass filter
Accuracy	INL_{cm}	-2		2	°	centered magnet
		-3		3		within horizontal displacement radius (4.4)
Transition noise	TN			0.235	°	rms (1 sigma)
Power-On-Reset levels	POR_r	3.5		4.5	V	VDD rising
	POR_f	3.0		4.5	V	VDD falling
	Hyst		500		mV	Hysteresis | POR_r -POR_f |

4.4   Magnet Specifications

Recommended magnet: NdFeB 35H B_R = 12.000 Gauss, Ø6mm x 2.5mm

Parameter	Symbol	Min	Typ	Max	Unit	Note
Magnet diameter	MD		6		mm	diametrically magnetized
Magnet thickness	MT		2.5		mm	
Magnetic Input Range	B_i	20		80	mT	at chip surface, on a radius of 1mm
Magnet rotation speed	v_i			30,000	rpm	to maintain locked state
Magnetic field high detection	B_{max}		52		mT	T_{amb}=25°C, AGC@lower limit, 1 sigma = 2.5mT
Magnetic field low detection	B_{min}		23			T_{amb}=25°C, AGC@upper limit, 1 sigma = 1.5mT
Hall Array radius			1		mm	over x/y chip center
vertical distance of magnet		0.5	1	1.8	mm	Recommended distance; operation outside this range is possible, accuracy may be reduced
Horizontal magnet displacement radius				0.25	mm	from diagonal package center
				0.5		from diagonal IC center
Recommended magnet material and temperature drift	tk_M		-0.12		%/K	NdFeB Material
			-0.035			SmCo Material

4.5   Magnetic Field Alarm Limits

Parameter	Symbol	Min	Typ	Max	Unit	Note
Magnetic field too low alarm limit	AGC_{FF}	20.3		23.6	mT	AGC = FF_H untrimmed, 25°C, 1sigma
Magnetic field too high alarm limit	AGC_0	44.5		52.2	mT	AGC = 0_H untrimmed, 25°C, 1sigma
Magnetic field alarm limit trim range		100		121	%	see 4.6
Temperature coefficient of alarm ranges[1]			0.052		%/K	Sensitivity increases with temperature which partly compensates the temperature coefficient of the magnet

4.6   Hall Element sensitivity options

Parameter	Symbol	Min	Typ	Max	Unit	Note
Hall Element sensitivity setting	sens		100		%	sens = 00 (default; low sensitivity; see 5.2.4)
			106			sens = 01
			113			sens = 10
			121			sens = 11 (high sensitivity)

4.7   Programming parameters

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Programming Voltage	V_{PROG}	8.0	8.5	V	static voltage at pin PROG
Programming Current	I_{PROG}		100	mA	
programming ambient temperature	$Tamb_{PROG}$	0	85	°C	during programming
Programming time	t_{PROG}	2	4	µs	timing is internally generated
Analog readback voltage	$V_{R,prog}$		0.5	V	during Analog Readback mode at pin PROG
	$V_{R,unprog}$	2.2	3.5		

4.8   DC Characteristics of Digital Inputs and Outputs

Parameter	Symbol	Min	Typ	Max	Unit	Note
CMOS Inputs: CLK, CS, DIO, C1, C2						
High level input voltage	VI_H	0.7*VDD			V	
Low level input voltage	VI_L			0.3*VDD	V	
Input leakage current	I_{LEAK}			1	µA	
CMOS Outputs: DIO, MagRngn, PWM, DX						
High level output voltage	VO_H	VDD-0.5			V	source current <4mA
Low level output voltage	VO_L			0.4	V	sink current <4mA
Capacitive load	CL			35	pF	
CMOS Tristate Output: DIO						
Tristate leakage current	IO_Z			1	µA	CS = low

4.9   8-bit PWM Output

Parameter	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
PWM resolution	N_{PWM}		8		bit	
			2		µs/step	
PWM pulse width	PW_{MIN}	1.66	2.26	2.85	µs	angle = 0° (00_H)
PWM pulse width	PW_{MAX}	427	578	731	µs	angle = 358.6° (FF_H)
PWM period	PW_P	428	581	734	µs	over full temperature range[1]
PWM frequency	f_{PWM}		1.72		kHz	=1 / PWM period
Digital hysteresis[2]	Hyst		1		bit	at change of rotation direction

Notes:
1) The tolerance of the absolute PWM pulse width and frequency can be eliminated by using the duty cycle $t_{ON}/(t_{ON}+t_{OFF})$ for angle measurement; see 4.18.
2) Hysteresis may be temporarily disabled by software: see 5.2.2

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4.10   Serial 8-bit Output

Parameter	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
3-wire interface						
Clock frequency	f_{CLK}			6	MHz	normal operation
	t_{CLK}	166.6			ns	
Clock frequency	$f_{clk,P}$	250		500	kHz	during OTP programming
2-wire interface						
Clock frequency	f_{CLK}	0.1		6	MHz	normal operation
	t_{CLK}	166.6		10,000	ns	
Clock frequency	$f_{clk,P}$	250		500	kHz	during OTP programming
Synchronization timeout	t_{TO}	16.6	27	34.3	ms	Rising edge of CLK to internally generated chip select on pin DX
Digital hysteresis[1]	Hyst		1		bit	at change of rotation direction

Note: 1) Hysteresis may be temporarily disabled by software: see 5.2.2

4.11   General Data Transmission Timings

Parameter	Symbol	Min	Max	Unit
rising CLK to CS	t0	15	-	ns
chip select to positive edge of CLK	t1	15	-	ns
chip select to drive bus externally	t2	-	-	ns
setup time command bit data valid to positive edge of CLK	t3	30		ns
hold time command bit data valid after positive edge of CLK	t4	30		ns
float time positive edge of CLK for last command bit to bus float	t5	30	CLK/2	ns
bus driving time positive edge of CLK for last command bit to bus drive	t6	CLK/2 +0	CLK/2 +30	ns
setup time data bit data valid to positive edge of CLK	t7	CLK/2 +0	CLK/2 +30	ns
hold time data bit data valid after positive edge of CLK	t8	CLK/2 +0	CLK/2 +30	ns
hold time chip select positive edge CLK to negative edge of chip select	t9	30		ns
bus floating time negative edge of chip select to float bus	t10	0	30	ns
hold time data bit @ write access data valid to positive edge of CLK	t11	50		ns
hold time data bit @ write access data valid after positive edge of CLK	t12	30		ns
bus floating time negative edge of chip select to float bus	t13		50	ns
Timeout period in 2-wire mode (from rising edge of CLK)	t_{TO}	20	24	µs

See the Figure 5 for the corresponding timing diagram.

4.12   Connecting the AS5030

The following examples show various ways to connect the AS5030 to an external controller:

4.13   Serial 3-Wire R/W Connection
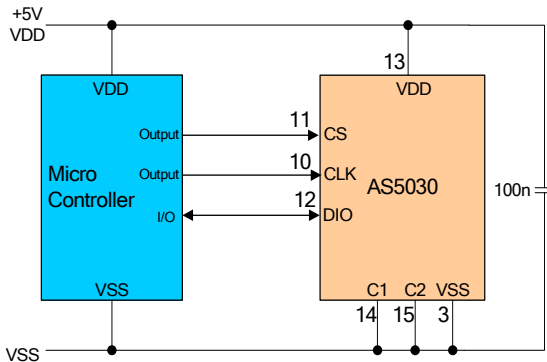
In this mode, the AS5030 is connected to the external controller via three signals:
Chip Select (CS), Clock (CLK) inputs and bi-directional DIO (Data In/Out) output.

The controller sends commands over the DIO pin at the beginning of each data transmission sequence, such as reading the angle or putting the AS5030 in and out of the reduced power modes.
A pull-down resistor (as shown in 4.14) is not required.
C1 and C2 are hardware configuration inputs. C1 must always be connected to VSS, C2 selects 3-wire mode (C2 = low) or 2-wire mode (C2 = high)

Figure 4: SSI read/write serial data transmission
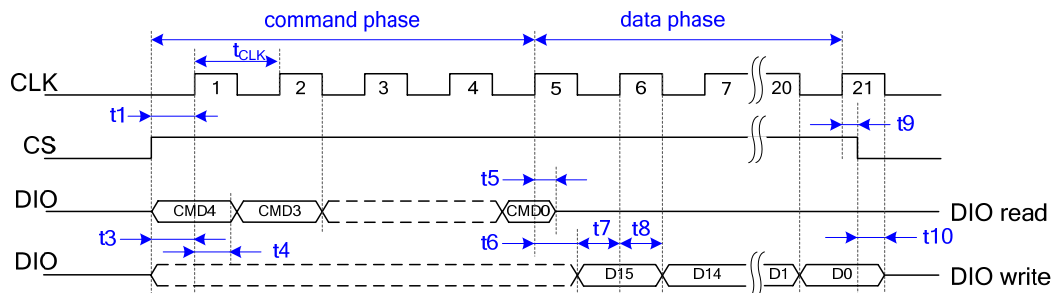
Figure 5: Timing diagram in 3-wire SSI R/W mode (timing values in 4.11: General Data Transmission Timings)

Serial bit sequence (16bit read/write):

Write Command					Read/Write Data															
C4	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
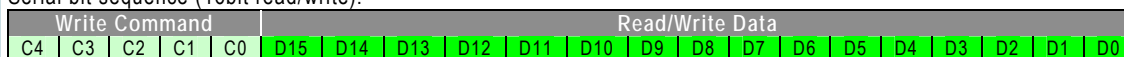
4.14   Serial 3-Wire Read-only Connection
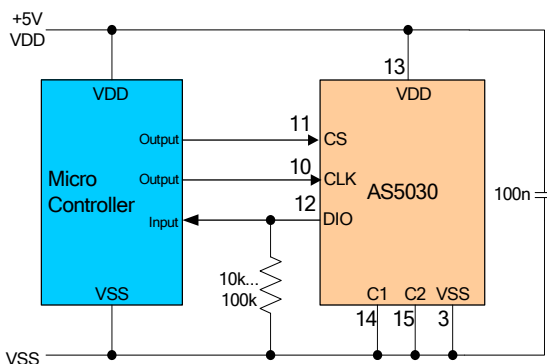
If the AS5030 is only used to provide the angular data (no power down or OTP access) this simplified connection is possible. The Chip Select (CS) and Clock (CLK) connection is the same as in the R/W mode (see 4.13), but only a digital input pin (not an I/O pin) is required for the DIO connection. As the first 5 bits of the data transmission are command bits sent to the AS5030, both the microcontroller and the AS5030 are configured as digital inputs during this phase. Therefore, a pull-down resistor must be added to make sure that the AS5030 reads "00000" as the first 5 bits which sets the Read_Angle command.

Note: all further application examples are shown in R/W mode, however read-only mode is also possible unless otherwise noted.

Figure 6: SSI read-only serial data transmission

2-or 3-wire read-only serial bit sequence (21bit read):

D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Read																				
0	0	0	0	0	C2	lock	AGC						Angle							
							D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

Figure 7: Timing diagram in 2-wire and 3-wire SSI mode

4.15   Serial 2-Wire Connection (R/W Mode)
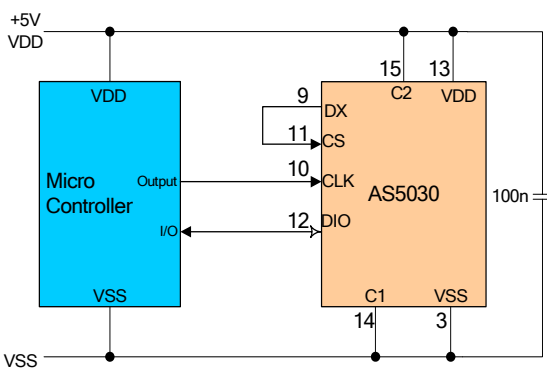
By connecting the configuration input C2 to VDD, the AS5030 is configured to 2-wire data transmission mode.

Only Clock (CLK) and Data (DIO) signals are required. A Chip Select (CS) signal is automatically generated by the DX output, when a time-out of CLK occurs (typ. 20µs).

Note: Read-only mode is also possible in this configuration

Figure 8: SSI R/W mode 2-wire data transmission
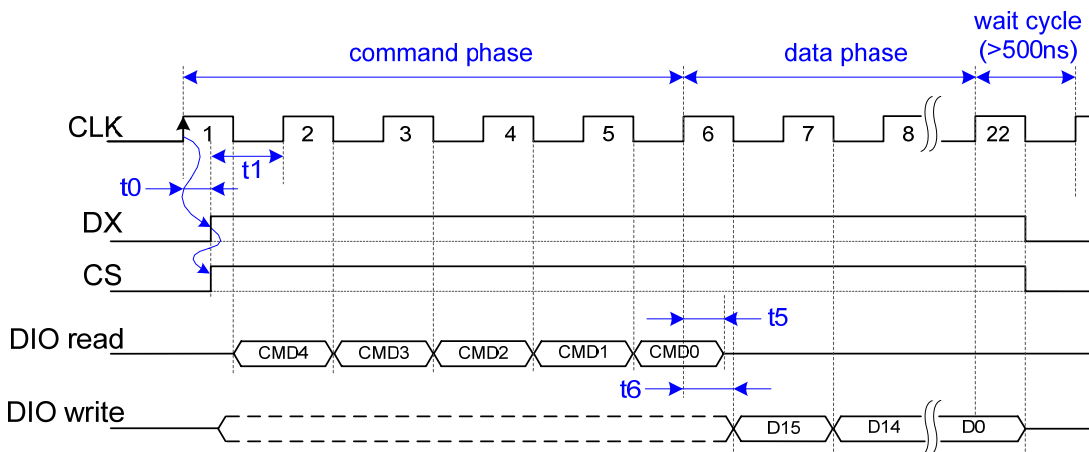
Figure 9: Timing diagram in 2-wire SSI mode

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4.16   Serial 2-wire Continuous Readout

The termination of each readout sequence by a timeout of CLK after the 22nd clock pulse as described in 4.15 is the safest method to ensure synchronization, as each timeout of CLK resets the serial interface.
However, it is not mandatory to apply a timeout of CLK and consequently synchronization after each reading. It is also possible to read several consecutive angle values without synchronization by simply continuing the CLK pulses without timeout after the 22nd clock. The 23rd clock is equal to the 1st clock of the next measurement, etc...
This is the fastest way to read multiple angle values, as there is no timeout period between the readings. It is still possible to synchronize the serial data transmission by a timeout of CLK after a given number of readouts (e.g. synchronize after every 5th reading, etc...)
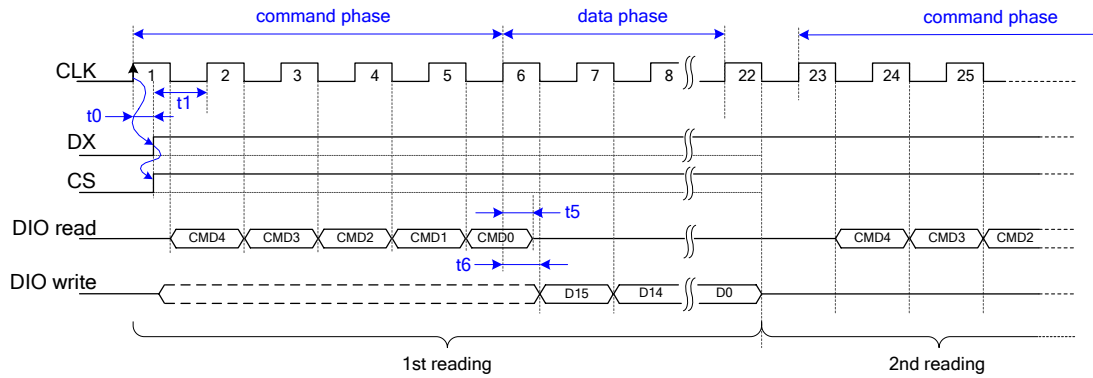
Figure 10: Timing diagram in 2-wire SSI continuous readout

4.17   Serial 2-Wire Differential SSI Connection
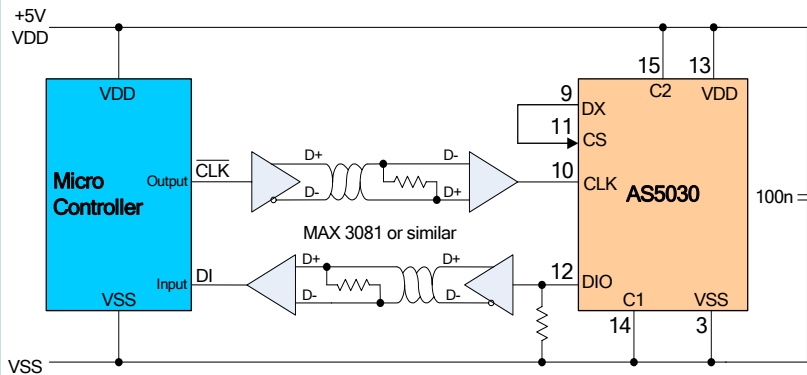
With the addition of a RS-422 / RS-485 transceiver, a fully differential data transmission, according to the 21-bit SSI interface standard is possible. To be compatible with this standard, the CLK signal must be inverted. This is done by reversing the Data+ and Data- lines of the transceivers.
Note: This type of transmission is read-only.

Figure 11: 2-wire SSI read-only mode
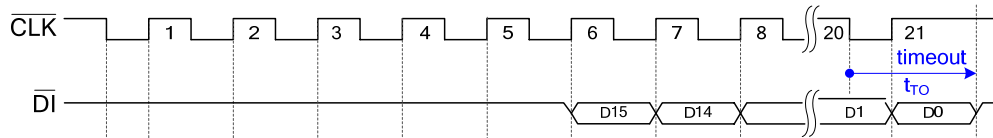
Figure 12: Timing diagram in 2-wire readonly mode (differential transmission)

SSI read-only serial bit sequence (21bit read):

Read																				
D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	C2	lock	AGC						Angle							
							D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

4.18   1-Wire PWM Connection
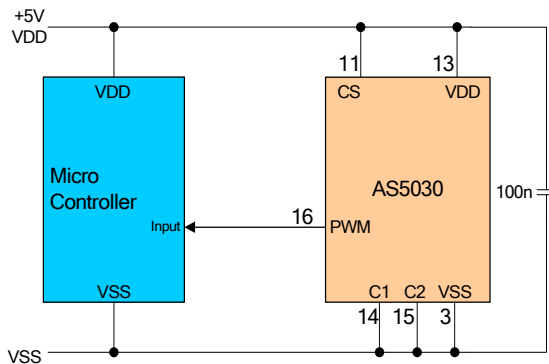
This configuration uses the least number of wires: only one line (PWM) is used for data, leaving the total number of connection to three, including the supply lines. This type of configuration is especially useful for remote sensors.
Ultra Low Power Mode is not possible in this configuration, as there is no bi-directional data transmission.

If the AS5030 angular data is invalid, the PWM output will remain at low state. Pins that are not shown may be left open. Note that the PWM output is invalid when the AGC is disabled (see 5.2.2).

Figure 13: Data transmission with pulse width modulated (PWM) output

The minimum PWM pulse width t_{ON} (PWM = high) is 1 LSB @ 0° (Angle reading = 00$_H$).
1LSB = nom. 2.26µs.
The PWM pulse width increases with 1LSB per step. At the maximum angle 358.6° (Angle reading = FF$_H$),
the pulse width t_{ON} (PWM = high) is 256 LSB and the pause width t_{OFF} (PWM = low) is 1 LSB.
This leads to a total period (t_{ON} + t_{OFF}) of 257LSB.
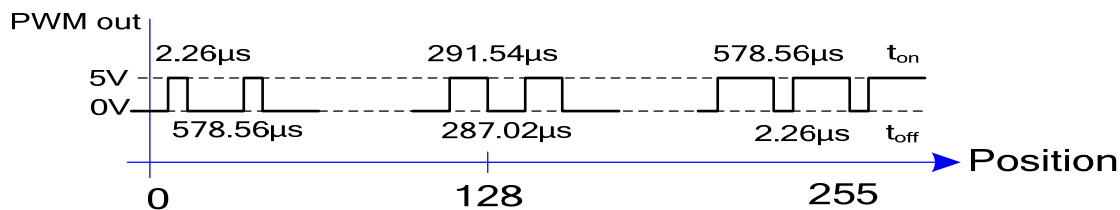
Position	Angle	High	t$_{\_high}$	Low	t$_{\_low}$	Duty-Cycle
0	0°	1	2.26µs	256	578.56µs	0.39%
127	178.59	128	287.02µs	129	291.54µs	49.4%
128	180°	129	291.54µs	128	287.02µs	50.2%
255	358.59°	256	578.56µs	1	2.26µs	99.6%

This means that the PWM pulse width is (position + 1) LSB, where position is 0....255.

The tolerance of the absolute pulse width and -frequency can be eliminated by calculating the angle with the duty cycle rather than with the absolute pulse width:

$$angle[8-bit] = \left(257 \frac{t_{ON}}{t_{ON} + t_{OFF}} \right) - 1$$

results in an 8-bit value from 00$_H$ to FF$_H$,

$$angle[°] = \frac{360}{256} \left[\left(257 \frac{t_{ON}}{t_{ON} + t_{OFF}} \right) - 1 \right]$$

results in a degree value from 0° ~ 358.6°

Note: the absolute frequency tolerance is eliminated by dividing t_{ON} by (t_{ON}+T_{OFF}), as the change of the absolute timing effects both T_{ON} and T_{OFF} in the same way.

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4.19   Analog Output
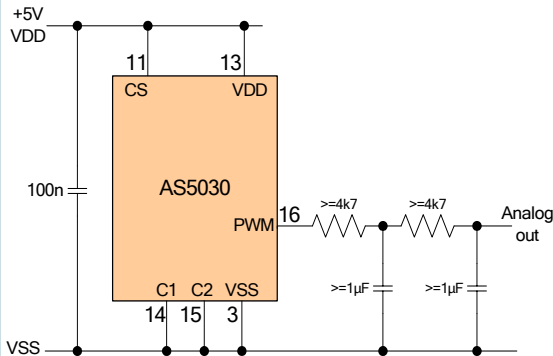
This configuration is similar to the PWM connection (only three lines including supply are required). With the addition of a lowpass filter at the PWM output, this configuration produces an analog voltage that is proportional to the angle.

This filter can be either passive (as shown) or active. The lower the bandwidth of the filter, the less ripple of the analog output can be achieved.

If the AS5030 angular data is invalid, the PWM output will remain at low state and thus the analog output will be 0V. Pins that are not shown may be left open.

Note that the PWM output is invalid when the AGC is disabled (see 5.2.2).

Figure 14: Data transmission with pulse width modulated (PWM) output
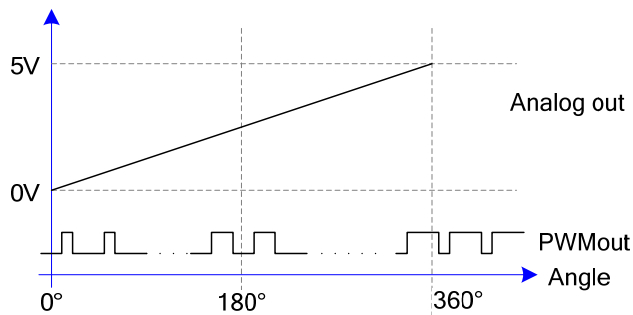
Figure 15: Relation of PWM/Analog output with angle

4.20   Analog Sin/Cos outputs with external interpolator
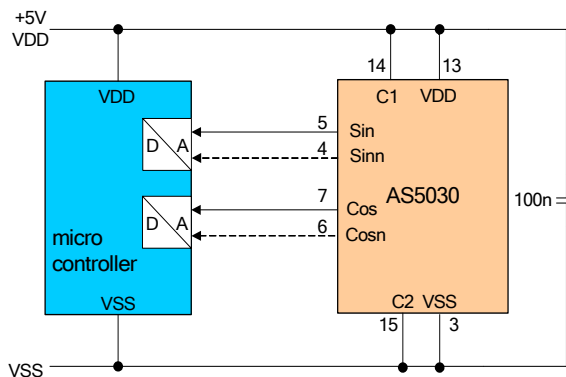
By connecting C1 to VDD, the AS5030 provides analog Sine and Cosine outputs (Sin, Cos) of the Hall array front-end for test purposes. These outputs allow the user to perform the angle calculation by an external ADC + µC, e.g. to compute the angle with a high resolution.
In addition, the inverted Sine and Cosine signals (Sinn, Cosn; see dotted lines) are available for differential signal transmission.

The input resistance of the receiving amplifier or ADC should be greater than 100kΩ. The signal lines should be kept as short as possible, longer lines should be shielded in order to achieve best noise performance.

Figure 16: Sine and Cosine outputs for external angle calculation

The SIN / COS / SINn / COSn signals are amplitude controlled to ~1.3Vp (differential) by the internal AGC controller. The DC bias voltage is 2.25 V.
If the SIN(n)- and COS(n)- outputs cannot be sampled simultaneously, it is recommended to disable the automatic gain control (see 5.2.2) as the signal amplitudes may be changing between two readings of the external ADC. This may lead to less accurate results.

4.21 3-Wire Daisy Chain Mode

The Daisy Chain mode allows connection of more than one AS5030 to the same controller interface. Independent of the number of connected devices, the interface to the controller remains the same with only three signals: CSn, CLK and DO. In Daisy Chain mode, the data from the second and subsequent devices is appended to the data of the first device.
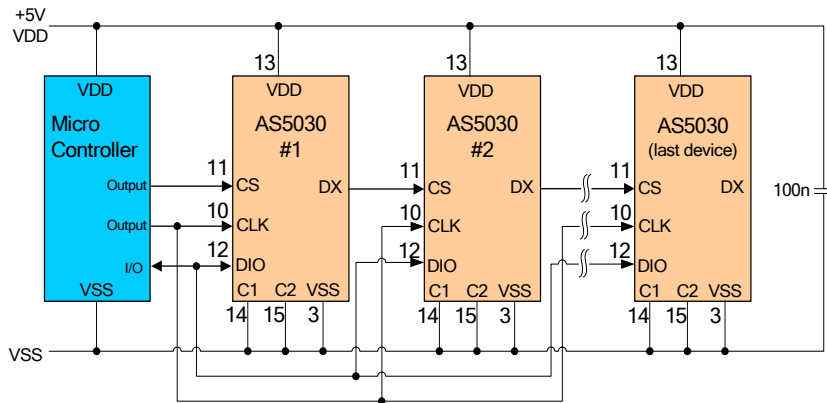
The 100nF buffer cap at the supply (shown only for the last device) is recommended for all devices.

The total number of serial bits is: n*21, where n is the number of connected devices:
e.g. for 2 devices, the serial bit stream is 42bits . For three devices it is 63 bits.

Figure 17: Connection of devices in 3-wire Daisy Chain mode
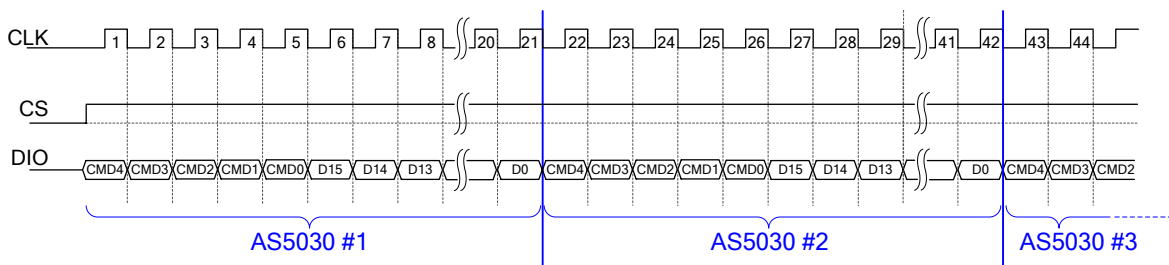
Figure 18: Timing diagram in 3-wire Daisy Chain mode

4.22 2-Wire Daisy Chain Mode
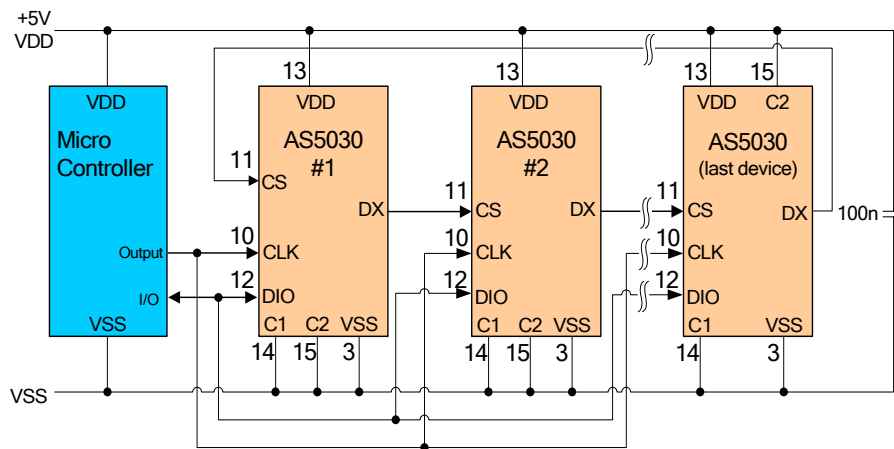
Figure 19: 2-wire Daisy Chain mode

The AS5030 can also be connected in 2-wire Daisy Chain mode, requiring only two signals (Clock and Data) for any given number of daisy-chained devices. Note that the connection of all devices except the last device is the same as for the 3-wire connection (see Figure 17). The last device must have pin C2 (#15) set to high and feeds the DX signal to CS of the first device.

Again, each device should be buffered with a 100nF cap (shown only for the last device).

The total number of serial bits is: n*21, where n is the number of connected devices. Note that this configuration requires one extra clock (#1) to initiate the generation of the CS signal for the first device. After reading the last device, the communication must be reset back to the first device by introducing a timeout of CLK (no rising edge for >24µs)
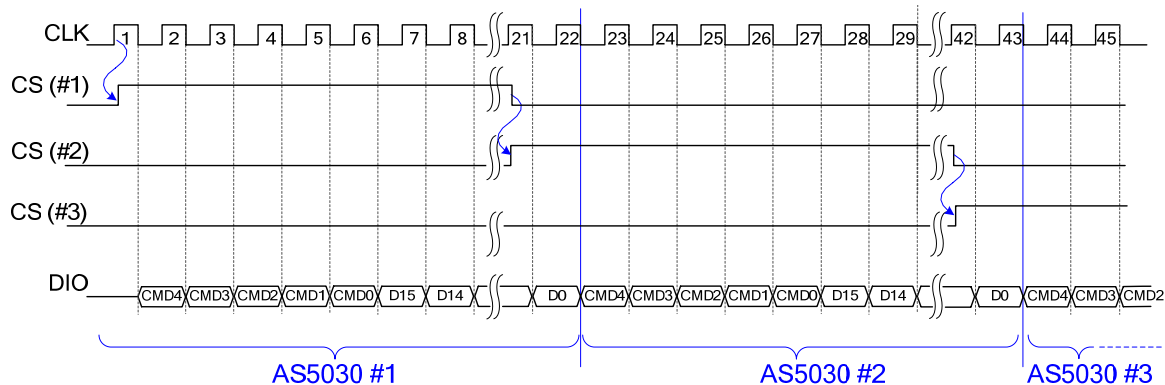

Figure 20: Timing diagram in 2-wire Daisy Chain mode

5   AS5030 Programming

5.1   Programming Options

The AS5030 has an integrated 18 Bit OTP ROM for configuration purposes.

5.1.1   OTP Programming options

The OTP programming options can be set permanently by programming or temporarily by overwriting. Both methods are carried out over the serial interface, but with different commands (WRITE OTP, PROG OTP, see 5.2.4).
Note: During the 18bit OTP programming, each bit needs 4 clock pulses to be validated.

- Zero Position Programming
  This programming option allows the user to program any rotation angle of the magnet as the new zero position. This useful feature simplifies the assembly process as the magnet does not need to be mechanically adjusted to the electrical zero position. It can be assembled in any rotation angle and later matched to the mechanical zero position by zero position programming.
  The 8-bit user programmable zero position can be applied both temporarily (command WRITE OTP, #1F$_H$) or permanently (command PROG OTP, #19$_H$)

- Magnetic Field Optimization
  This programming option allows the user to match the vertical distance of the magnet with the optimum magnetic field range of the AS5030 by setting the sensitivity level.
  The 2-bit user programmable sensitivity setting can be applied both temporarily (command WRITE OTP, #1F$_H$) or permanently (command PROG OTP, #19$_H$)

5.1.2   Reduced Power mode programming options

These temporary programming options are also carried out over the serial interface. See 5.2.2.

- Low Power Mode
  Low Power Mode is a power saving mode with fast start-up. In Low Power Mode, all internal digital registers are frozen and the power consumption is reduced to max. 1.5mA. The serial interface remains active. Start-up from this mode to normal operation can be accomplished within 150µs. This mode is recommended for applications, where low power, but fast start-up and short reading cycle intervals are required.

- Ultra Low Power Mode
  Ultra Low Power Mode is a power saving mode with even reduced power-down current consumption. In this mode, all chip functions are frozen and the power consumption is reduced to max. 50µA. The serial interface remains active. Start-up from this mode to normal operation can be accomplished within 500µs. This mode is recommended for applications, where very low average power consumption is required, e.g. for battery operated equipment. For example, in a cycled operation with 10 readings per second, the average power consumption of the AS5030 can be reduced to only 120µA.

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5.2   AS5030 Read / Write Commands

Data transmission with the AS5030 is handled over the 2-wire or 3-wire interface. The transmission protocol begins with sending a 5-bit command to the AS5030, followed by reading or writing 16 or 18 bits of data:

5.2.1   16-bit Read Command

Command	Bin	Hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RD ANGLE	00000	00	C2	lock	AGC 5:0						Angle 7:0							

C2   displays status of hardware pin C2 (pin #15)
Lock   indicates that the AGC is locked. Data is invalid when this bit is 0
AGC   6-bit AGC register. Indicates the strength of the magnet (e.g. for pushbutton applications)
          000000_b indicates a strong magnetic field
          111111_b indicates a weak magnetic field
          ideally, the vertical distance of the magnet should be chosen such that the AGC value is in the middle (around 100000b)
Angle   8-bit Angle value; represents the rotation angle of the magnet. One step = 360°/256 = 1.4°

5.2.2   16-bit Write Command

These settings are temporary; they cannot be programmed permanently. The settings will be lost when the power supply is removed.

Command	Bin	Hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EN PROG	10000	10	1	0	0	0	1	1	0	0	1	0	1	0	1	1	1	0
SET PWR MODE	10001	11	ULP/LPn	PSM	0													
DIS HYST	10011	13	HYS	0														
DIS AGC	10101	15	0	0	0	0	0	rst	0	0	0	AGC 5:0						FA

EN PROG   this command must be sent with a fixed 16-bit code ($8CAE_H$) to enable subsequent OTP access.
ULP/LPn   selects the Ultra Low Power Mode, when bit PSM is set: 0 = Low Power Mode, 1 = Ultra Low Power Mode
PSM   enables power saving modes: 0 = normal operation, 1 = reduced power mode selected by bit ULP/LPn
HYS   disables the hysteresis of the digital serial and PWM outputs:
                0 (default) = 1-bit hysteresis, 1 = no hysteresis
DIS AGC   disables the automatic gain control. The AGC will be frozen to a gain setting written in bits AGC 5:0 (D6:D1), bit FA must be set.
rst   General Reset: 0 = normal operation, 1 = perform general reset (required after return from reduced power modes)
FA   Freeze AGC; 0 = normal operation, 1= freeze AGC with the values stored in bits AGC 5:0. The PWM output will be invalid when bit FA is set.

5.2.3   18-bit OTP Read Commands

Note: to prohibit unintentional access to the OTP register, OTP PROG/write access is only enabled after the EN PROG command (see 5.2.2) has been sent. OTP access is locked again by sending a RD ANGLE or SET PWR MODE command. EN PROG has not to be sent before a READ OTP.
During the 18bit OTP read/write transfer, each bit needs 4 clock pulses to be validated.

Command	Bin	Hex	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
READ OTP	01111	0F	reserved for factory settings								sens 1:0		zero position 7:0							
ANALOG OTP RD	01001	09	reserved for factory settings								sens 1:0		zero position 7:0							

READ OTP   reads the contents of the OTP register in digital form. The reserved area may contain any value
ANALOG OTP RD   reads the contents of the OTP register as an analog voltage at pin PROG (see 5.4)
sens   reads the sensitivity setting of the Hall elements : 00 = high sensitivity, 11 = low sensitivity
zero position   reads the programmed zero position; the actual angle of the magnet which is displayed as 000

5.2.4   18-bit OTP Write Commands

During the 18bit OTP read/write transfer, each bit needs 4 clock pulses to be validated.

Command	Bin	Hex	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WRITE OTP	11111	1F	copy factory settings obtained from READ OTP command								sens 1:0		zero position 7:0							
PROG OTP	11001	19	00000000 reserved for factory settings,								sens 1:0		zero position 7:0							

WRITE OTP: non-permanent ("soft write") modification of the OTP register. To set the reserved factory settings area properly, a preceding READ OTP command must be made to receive the correct setting for bits D17:D10. The WRITE OTP command must then set these bits in exactly the same way. Improper setting of the factory settings by a WRITE OTP command may cause malfunction of the chip. The OTP register, including the factory settings can be restored to default by a power-up cycle.
For non-permanent writing, a programming voltage at pin PROG (#2) is not required.

PROG OTP: permanent modification of the OTP register. An unprogrammed OTP bit contains a '0, programmed bits are 1's. It is possible to program the OTP in several sequences. However, only a 0 can be programmed to 1. Once programmed, an OTP bit cannot be set back to 0. For subsequent programming, bits that are already programmed should be set to 0 to avoid double programming.
During permanent programming, the factory settings D17:D10 should always be set to zero to avoid modification of the factory settings.
Modifying the factory settings may cause irreversible malfunction of the chip.
For permanent programming, a static programming voltage of 8.0-8.5V must be applied at pin PROG (#2)

sens   sets the sensitivity setting of the Hall elements :
00: gain factor = 1.65 (low sensitivity)
01: gain factor = 1.75
10: gain factor = 1.86
11: gain factor = 2.00 (high sensitivity)

zero position   sets the user programmable zero position; the actual angle of the magnet which is displayed as 000
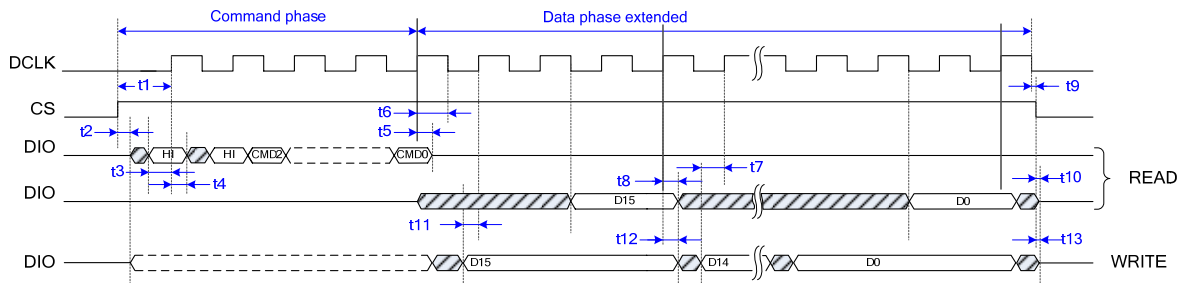
Figure 21: Timing diagram in OTP 18bit read/write mode

5.3   OTP Programming Connection
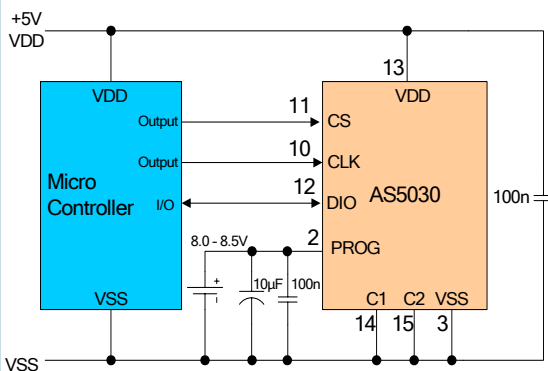
Figure 22: OTP programming connection

Programming of the AS5030 OTP memory does not require a dedicated programming hardware. The programming can be simply accomplished over the serial 3-wire interface (shown in Figure 22) or the optional 2-wire interface (shown in Figure 8).

For permanent programming (command PROG OTP, #19$_H$), a constant DC voltage of 8.0V ~ 8.5V (≥100mA) must be connected to pin #2 (PROG).
For temporary OTP write ("soft write"; command WRITE OTP, #1F$_H$), the programming voltage is not required.

To secure unintentional programming, any modification of the OTP memory is only enabled after a special password (command #10$_H$) has been sent to the AS5030.

Programming in Daisy Chain mode

Programming in Daisy chain mode is possible for both 3-wire and 2-wire mode (see Figure 17 and Figure 19). For temporary programming (soft write), no additional connections are required. Programming is executed with the respective programming commands (see 5.2). For permanent programming, the programming voltage must be applied on pin#2 (PROG) of the device to be programmed. It is also possible to apply the programming voltage simultaneously to all devices, as the actual programming is only executed by a software command.

A parallel connection of all PROG-pins allows digital programming verification but does not allow analog programming verification (see 5.4).

If analog programming verification is required, each PROG pin must be selected individually for verification.

5.4   Programming Verification
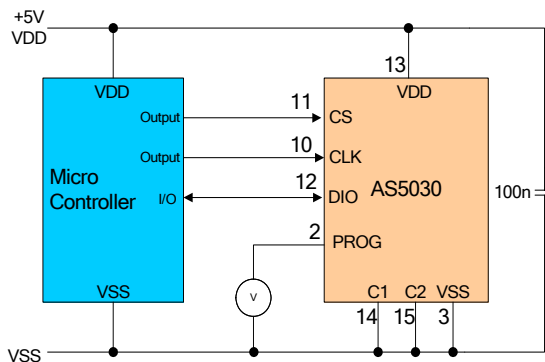
Figure 23: Analog OTP verification

After programming, the programmed OTP bits may be verified in two ways:

- **By digital verification:**
this is simply done by sending a READ OTP command (#0F$_H$ see 5.2.3). The structure of this register is the same as for the OTP PROG or OTP WRITE commands.

- **By analog verification:**
By sending an ANALOG OTP READ command (#09$_H$), pin PROG becomes an output, sending an analog voltage with each clock, representing a sequence of the bits in the OTP register. A voltage of <500mV indicates a correctly programmed bit ("1") while a voltage level between 2.2V and 3.5V indicates a correctly unprogrammed bit ("0"). Any voltage level in between indicates improper programming.

6   AS5030 Status Indicators

Refer to 5.2.1

6.1   C2 Status Bit

This bit represents the hardware connection of the C2 configuration pin (#15) to determine, which hardware configuration is selected for the AS5030 in question.

C2 = low : pin C2 is low, indicating that the AS5030 is in 3-wire mode or a member of a 2-wire daisy chain connection (except the last; see 4.21)

C2 = high: pin C2 is high, indicating that the AS5030 is in 2-wire mode and/or the last member of a 2-wire daisy chain connection (see 4.22)

6.2   Lock Status Bit

The Lock signal indicates the ADC lock status. If Lock = low (ADC unlocked), the angle information is invalid.

To determine a valid angular signal at best performance, the following indicators should be set:
Lock = 1
AGC > 00$_H$ and < 2F$_H$

Note that the angle signal may also be valid (Lock = 1), when the AGC is out of range (00$_H$ or 2F$_H$), but the accuracy of the AS5030 may be reduced due to the out of range condition of the magnetic field strength.

6.3   Magnetic Field Strength Indicators

The AS5030 is not only able to sense the angle of a rotating magnet, it can also measure the magnetic field strength (and hence the vertical distance) of the magnet.

This extra feature can be used for several purposes:
- as a safety feature by constantly monitoring the presence and proper vertical distance of the magnet
- as a state-of-health indicator, e.g. for a power-up self test
- as a pushbutton feature for rotate-and-push types of manual input devices

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The magnetic field strength information is available in two forms:

6.3.1   Magnetic Field Strength Hardware Indicator:

Pin MagRngn (#1) will be low, when the magnetic field is too weak. The switching limit is determined by the value of the AGC. If the AGC value is <$3F_H$, the MagRngn output will be high (green range), If the AGC is at its upper limit ($3F_H$), the MagRngn output will be low (red range).

6.3.2   Magnetic Field Strength Software Indicator:

D13:D7 in the serial data that is obtained by command READ ANGLE (5.2.1) contains the 6-bit AGC information (see 5.2.1). The AGC is an automatic gain control that adjusts the internal signal amplitude obtained from the Hall elements to a constant level. If the magnetic field is weak, e.g. with a large vertical gap between magnet and IC, with a weak magnet or at elevated temperatures of the magnet, the AGC value will be high. Likewise, the AGC value will be lower when the magnet is closer to the IC, when strong magnets are used and at low temperatures.
The best performance of the AS5030 will be achieved when operating within the AGC range. It will still be operational outside the AGC range, but with reduced performance especially with a weak magnetic field due to increased noise.

6.3.3   Factors Influencing the AGC Value

In practical use, the AGC value will depend on several factors:
- the initial strength of the magnet. Aging magnets may show a reducing magnetic field over time which results in an increase of the AGC value. The effect of this phenomenon is relatively small and can easily be compensated by the AGC.
- the vertical distance of the magnet. Depending on the mechanical setup and assembly tolerances, there will always be some variation of the vertical distance between magnet and IC over the lifetime of the application using the AS5030. Again, vertical distance variations can be compensated by the AGC
- the temperature and material of the magnet. The recommended magnet for the AS5030 is a diametrically magnetized, 5-6mm diameter NdFeB (Neodymium-Iron-Boron) magnet. Other magnets may also be used as long as they can maintain to operate the AS5030 within the AGC range.
  Every magnet has a temperature dependence of the magnetic field strength. The temperature coefficient of a magnet depends on the used material. At elevated temperatures, the magnetic field strength of a magnet is reduced, resulting in an increase of the AGC value. At low temperatures, the magnetic field strength is increased, resulting in a decrease of the AGC value.
  The variation of magnetic field strength over temperature is automatically compensated by the AGC.

6.3.4   OTP Sensitivity Adjustment

To obtain best performance and tolerance against temperature or vertical distance fluctuations, the AGC value at normal operating temperature should be in the middle between minimum and maximum, hence it should be around 100000 (20_H)

To facilitate the "vertical centering" of the magnet+IC assembly, the sensitivity of the AS5030 can be adjusted in the OTP register in 4 steps. A sensitivity adjustment is recommended, when the AGC value at normal operation is close to its lower limit (around 00_H). The default sensitivity setting is 00_H = high sensitivity. Any value >00H will reduce the sensitivity (see 5.2.4).

6.4   "Pushbutton" Feature
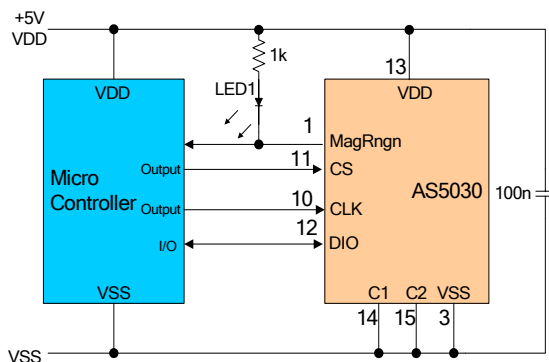
Using the magnetic field strength software and hardware indicators described above, the AS5030 provides a useful method of detecting both rotation and vertical distance simultaneously. This is especially useful in applications implementing a rotate-and-push type of human interface (e.g. in panel knobs and switches).
The MagRngn output is low, when the magnetic field is below the low limit (weak or no magnet) and high when the magnetic field is above the low limit (in-range or strong magnet).
A finer detection of a vertical distance change, for example when only short vertical strokes are made by the pushbutton, is achieved by memorizing the AGC value in normal operation and triggering on a change from that nominal the AGC value to detect a vertical movement.

Figure 24: Magnetic field strength indicator

7   High Speed Operation

The AS5030 is using a fast tracking ADC (TADC) to determine the angle of the magnet. The TADC has a tracking rate of 1.15µs (typ).

Once the TADC is synchronized with the angle, it sets the LOCK bit in the status register (see 5.2.1). In worst case, usually at start-up, the TADC requires a maximum of 127 steps (127 * 1.15µS = 146.05µs) to lock. Once it is locked, it requires only one cycle (1.15µs) to track the moving magnet.

The AS5030 can operate in locked mode at rotational speeds up to 30,000 rpm.

In Low Power Mode or Ultra Low Power Mode, the position of the TADC is frozen. It will continue from the frozen position once it is powered up again. If the magnet has moved during the power down phase, several cycles will be required before the TADC is locked again. The tracking time to lock in with the new magnet angle can be roughly calculated as:

$$t_{LOCK} = 1.15\mu s * |NewPos - OldPos|$$

t_{LOCK} =   time required to acquire the new angle after power up from one of the reduced power modes [µs]
OldPos =   Angle position when one of the reduced power modes is activated [°]
NewPos =   Angle position after resuming from reduced power mode [°]

7.1   Propagation Delay

The Propagation delay is the time required from reading the magnetic field by the Hall sensors to calculating the angle and making it available on the serial or PWM interface. While the propagation delay is usually negligible on low speeds it is an important parameter at high speeds.

The longer the propagation delay, the larger becomes the angle error for a rotating magnet as the magnet is moving while the angle is calculated. The position error increases linearly with speed.

The main factors contributing to the propagation delay are:

7.1.1   ADC Sampling Rate

For high speed applications, fast ADC's are essential. The ADC sampling rate directly influences the propagation delay. The fast tracking ADC used in the AS5030 with a tracking rate of only 1.15µs (typ.) is a perfect fit for both high speed and high performance.

7.1.2   Chip internal lowpass filtering

A commonplace practice for systems using analog-to-digital converters is to filter the input signal by an anti-aliasing filter. The filter characteristic must be chosen carefully to balance propagation delay and noise.

The lowpass filter in the AS5030 has a cut-off frequency of typ. 23.8kHz and the overall propagation delay in the analog signal path is typ. 15.6µs.

7.1.3   Digital readout rate

Aside from the chip-internal propagation delay, the time required to read and process the angle data must also be considered. Due to its nature, a PWM signal is not very usable at high speeds, as you get only one reading per PWM period. Increasing the PWM frequency may improve the situation but causes problems for the receiving controller to resolve the PWM steps. The frequency on the AS5030 PWM output is typ. 1.95kHz with a resolution of 2µs/step.

A more suitable approach for high speed absolute angle measurement is using the serial interface. With a clock rate of up to 6MHz, a complete set of data (21bits) can be read in >3.5µs

7.2   Total propagation delay of the AS5030

The total propagation delay of the AS5030 is the delay in the analog signal path and the tracking rate of the ADC:
15.6µs + 1.15µs = 16.75µs.
If only the SIN-/COS-outputs are used, the propagation delay is the analog signal path delay only (typ. 15.6µs).

Position Error over speed

The angle error over speed caused by the propagation delay is calculated as:

$\Delta\varphi_{pd}$ = rpm * 6 * 16.75E^{-6} in degrees.

In addition, the anti-aliasing filter causes an angle error calculated as:

$\Delta\varphi_{lpf}$ = ArcTan [rpm / (60*f$_0$)]

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Examples of the overall position error caused by speed, including both propagation delay and filter delay:

Speed (rpm)	Total Position error ($\Delta\varphi_{pd} + \Delta\varphi_{lpf}$)
100	0.0175°
1000	0.175°
10000	1.75°

8 Reduced Power Modes

The AS5030 can be operated in 3 reduced power modes. All 3 modes have in common that they switch off or freeze parts of the chip during intervals between measurements. In Low Power Mode or Ultra Low Power Mode, the AS5030 is not operational, but due to the fast start-up, an angle measurement can be accomplished very quickly and the chip can be switched to reduced power immediately after a valid measurement has been taken. Depending on the intervals between measurements, very low average power consumption can be achieved using such a strobed measurement mode.

- Low Power Mode: reduced current consumption, very fast start-up. Ideal for short sampling intervals (<3ms)
- Ultra Low Power Mode: further reduced current consumption, but slower start-up than Low Power Mode. Ideal for sampling intervals from 3....200ms
- Power Cycle mode: zero power consumption (externally switched off) during sampling intervals, but slower start-up than Ultra Low Power Mode. Ideal for sampling intervals 200ms

8.1 Low Power Mode and Ultra Low Power Mode
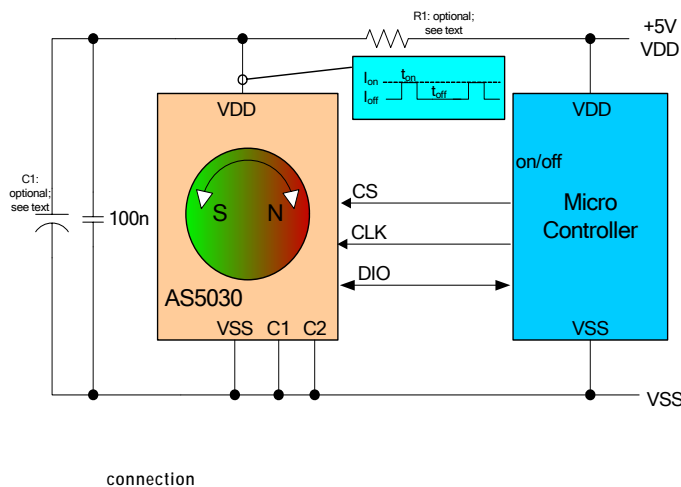
connection

The AS5030 can be put in Low Power Mode or Ultra Low Power Mode by simple serial commands, using the regular connection for 2-wire or 3-wire serial data transmission (Figure 4 , Figure 8)

The required serial command is SET PWR MODE (11H, see 5.2.3):

ULP/LPn	PSM	Mode
0	0	Normal operation
0	1	Low Power Mode
1	0	Normal operation
1	1	Ultra Low Power Mode

Figure 25: Low Power Mode and Ultra Low Power Mode

Note that after returning from Low Power Mode or Ultra Low Power mode to normal operation (PSM = 0), if the Hysteresis is enabled (Hys=0), a general reset must be performed: set bit RST and then clear bit RST using command 15H (see 5.2.2).
The two following cases describe the typical loop programmed in the software:

- Hys = 0 (1 LSB hysteresis):
  1. Wait for CPU interrupt or delay for next angle read (typ. <3ms in LP mode, typ>3ms in ULP mode)
  2. Wake up (PSM = 0)
  3. Set Reset (rst = 1)
  4. Clear Reset (rst = 0)
  5. Wait 0.15ms (Low Power Mode) or 0.5ms (Ultra Low Power Mode)
  6. Check if Lock = 1 then read angle
  7. Enable Low Power Mode or Ultra Low Power Mode (PSM=1)
  8. Return to 1

- Hys = 1 (No hysteresis)
  1. Wait for CPU interrupt or delay for next angle read (typ. <3ms in LP mode, typ>3ms in ULP mode)
  2. Wake up (PSM = 0)
  3. Wait 0.15ms (Low Power Mode) or 0.5ms (Ultra Low Power Mode)
  4. Check if Lock = 1 then read angle
  5. Enable Low Power Mode or Ultra Low Power Mode (PSM=1)
  6. Return to 1.

The differentiator between Low Power Mode and Ultra Low Power Mode is the current consumption and the wake-up time to switch back to active operation.

Mode	Current Consumption (typ.)	Wake-up Time to Active Operation
Active operation	14 mA	1.0 ms (without AGC) 3.8 ms(with locked AGC)
Low Power Mode	1.4 mA	0.15 ms
Ultra Low Power Mode	30 µA	0.5 ms

In both Reduced Power Modes, the AS5030 is inactive. The last state, e.g. the angle, AGC value, etc. is frozen and the chip starts from this frozen state when it resumes active operation. This method provides much faster start-up than a "cold start" from zero. If the AS5030 is cycled between active and reduced current mode, a substantial reduction of the average supply current can be achieved. The minimum dwelling time in active mode is the wake-up time. The actual active time depends on how much the magnet has moved while the AS5030 was in reduced power mode. The angle data is valid, when the status bit LOCK has been set (see 5.2.1). Once a valid angle has been measured, the AS5030 can be put back to reduced power mode. The average power consumption can be calculated as:

$$I_{avg} = \frac{I_{active} * t_{on} + I_{power\_down} * t_{off}}{t_{on} + t_{off}}$$ sampling interval = t_{on} + t_{off}

where:

I_{avg} average current consumption
I_{active}:   current consumption in active mode
I_{power_down}:   current consumption in reduced power mode
t_{on}:   time period during which the chip is operated in active mode
t_{off}:   time period during which the chip is in reduced power mode

Example: Ultra Low Power Mode; sampling period = one measurement every 10ms.
System constants = I_{active} = 14mA, I_{power_down} = 30µA, ton(min) = 500µs (startup from Ultra Low Power Mode):

$$I_{avg} = \frac{14mA * 500\mu s + 30\mu A * 9,5ms}{500\mu s + 9,5ms} = 729\mu A$$

see Figure 27 for an overview table of the average current consumption in the various reduced power modes.

Reducing Power Supply Peak Currents

An optional RC-filter (R1/C1) may be added to avoid peak currents in the power supply line when the AS5030 is toggled between active and reduced power mode. R1 must be chosen such that it can maintain a VDD voltage of 4.5V ~ 5.5V under all conditions, especially during long active periods when the charge on C1 has expired. C1 should be chosen such that it can support peak currents during the active operation period. For long active periods, C1 should be large and R1 should be small.

8.2   Power Cycling Mode
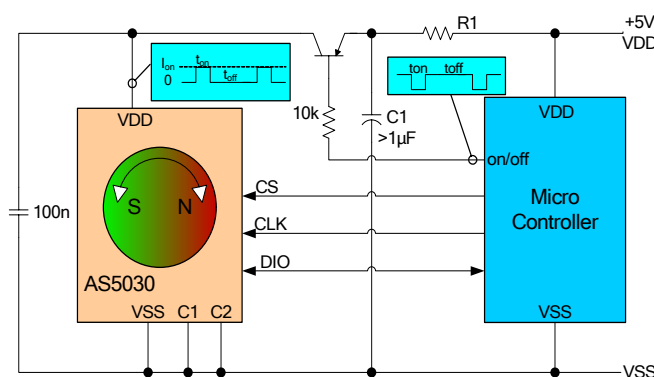
The power cycling method shown in Figure 26 cycles the AS5030 by switching it on and off, using an external PNP transistor high side switch.
This mode provides the least power consumption of all three modes; when the sampling interval is more than 400ms, as the current consumption in off-mode is zero.
It also has the longest start-up time of all modes, as the chip must always perform a "cold start" from zero, which takes about 1.9 ms (see 8.1).

The optional filter R1/C1 may again be added to reduce peak currents in the 5V power supply line.

Figure 26: Application example III: ultra-low power encoder

Figure 27 shows an overview of the average supply currents in the three reduced power modes, depending on the sampling interval. The graphs shows that the Low Power Mode is the best option for sampling intervals <4ms, while the Ultra Low Power Mode is the best option for sampling intervals between

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4~400ms. At sampling intervals >400ms, the power cycling mode is the best method to minimize the average current consumption.
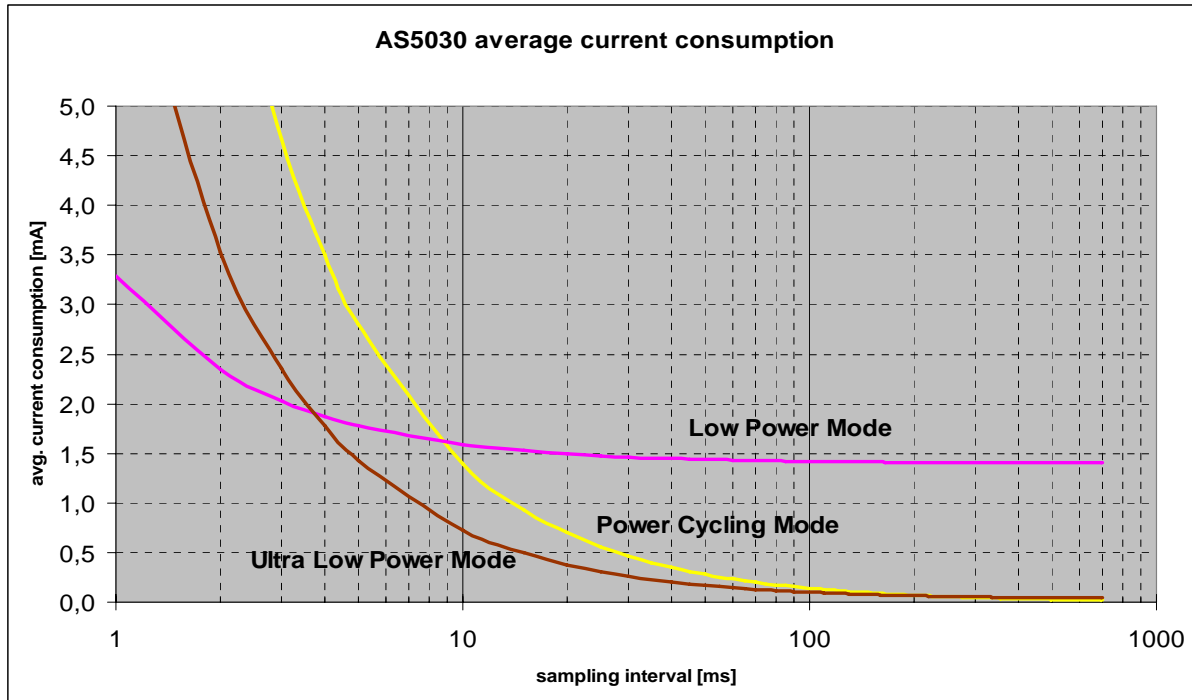The curves are based on the figures given in 8.1.

Figure 27: Average current consumption of reduced power modes

9   Accuracy of the Encoder system

This chapter describes which individual factors influence the accuracy of the encoder system and how to improve them.

Accuracy is defined as the difference between measured angle and actual angle. This is not to be confused with resolution, which is the smallest step that the system can resolve.
The two parameters are not necessarily linked together. A high resolution encoder may not necessarily be highly accurate as well.

9.1   Quantization error

There is however a direct link between resolution and accuracy, which is the quantization error:
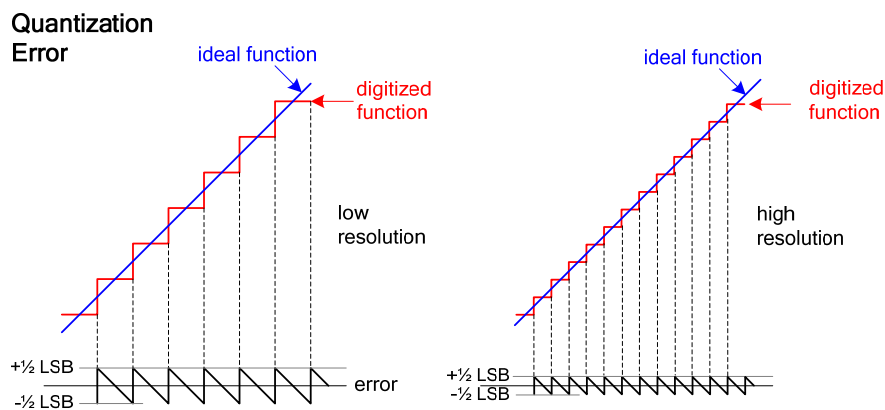
Figure 28: Quantization error of a low resolution and a high resolution system

The resolution of the encoder determines the smallest step size. The angle error caused by quantization cannot get better than ± ½ LSB. As shown in Figure 28, a higher resolution system (right picture) has a smaller quantization error, as the step size is smaller.
For the AS5030, the quantization error is ± ½ LSB = ± 0.7°
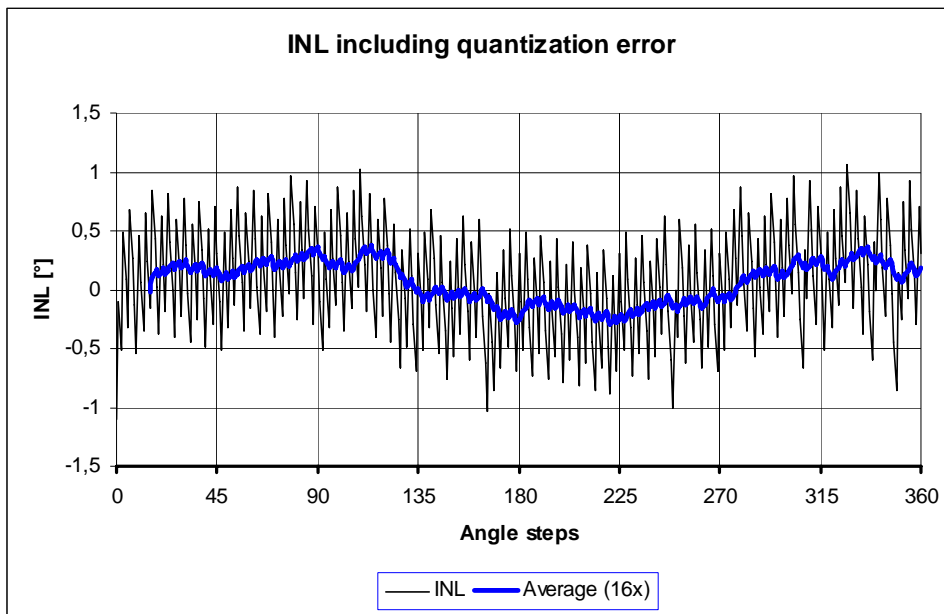
Figure 29: Typical INL error over 360°

Figure 29 shows a typical example of an error curve over a full turn of 360° at a given X-Y displacement. The curve includes the quantization error, transition noise and the system error. The total error is ~2.2° peak/peak (± 1.1°).

The sawtooth-like quantization error (see also Figure 28) can be reduced by averaging, provided that the magnet is in constant motion and there are an adequate number of samples available. The solid bold line in Figure 29 shows the moving average of 16 samples. The INL (intrinsic non-linearity) is reduced to from ~± 1.1° down to ~± 0.3°. The averaging however, also increases the total propagation delay, therefore it may be considered for low speeds only or adaptive; depending on speed (see also: 0, Position Error over speed).

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9.2   Vertical distance of the magnet

The chip-internal automatic gain control (AGC) regulates the input signal amplitude for the tracking-ADC to a constant value. This improves the accuracy of the encoder and enhances the tolerance for the vertical distance of the magnet.

Linearity and AGC vs Airgap
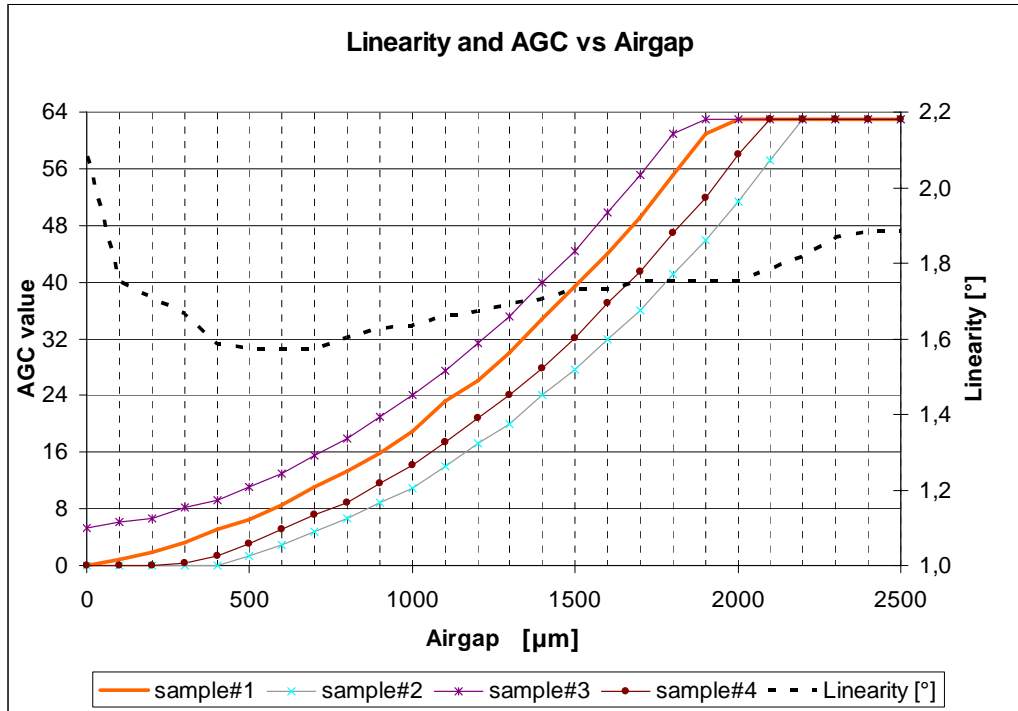
Figure 30: Typical curves for vertical distance versus ACG value on several untrimmed samples

As shown in Figure 30, the AGC value (left Y-axis) increases with vertical distance of the magnet.
Consequently, it is a good indicator for determining the vertical position of the magnet, for example as a pushbutton feature, as an indicator for a defective magnet or as a preventive warning (e.g. for wear on a ball bearing etc.) when the nominal AGC value drifts away.

If the magnet is too close or the magnetic field is too strong, the AGC will be reading 0,
If the magnet is too far away (or missing) or if the magnetic field is too weak, the AGC will be reading 63 ($3F_H$).
The AS5030 will still operate outside the AGC range, but the accuracy may be reduced as the signal amplitude can no longer be kept at a constant level.
The linearity curve in Figure 30 (right Y-axis) shows that the accuracy of theAS5030 is best within the AGC range, even slightly better at small airgaps (0.4mm ~ 0.8mm).
At very short distances (0mm ~ 0.1mm) the accuracy is reduced, mainly due to nonlinearities in the magnetic field.
At larger distances, outside the AGC range (~2.0mm ~ 2.5mm and more) the accuracy is still very good, only slightly decreased from the nominal accuracy.

Since the field strength of a magnet changes with temperature, the AGC will also change when the temperature of the magnet changes. At low temperatures, the magnetic field will be stronger and the AGC value will decrease. At elevated temperatures, the magnetic field will be weaker and the AGC value will increase.

Sensitivity trimming

As the curves for the 4 samples in Figure 30 show, the AGC value will not show exactly the same value at a given airgap on each part. For example, at 1mm vertical distance, the AGC may read a value between ~11 ~ 24. This is because for normal operation an exact trimming is not required since the AGC is part of a closed loop system.

However, the AS5030 offers an optional user trimming in the OTP (see 5.2.4) to allow an even tighter AGC tolerance for applications where the information about magnetic field strength is also utilized, e.g. for rotate-and-push types of knobs, etc...

10 Choosing the proper magnet

typ. 6mm diameter

N   S

Magnet axis

R1

Vertical field
component

R1 concentric circle;
radius 1.0 mm

Vertical field
component

Bz

(20...80mT)

0   360
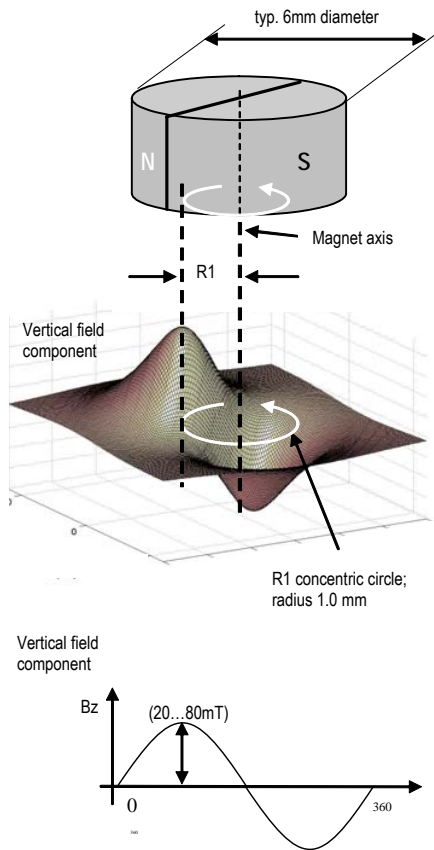
There is no strict requirement on the type or shape of the magnet to be used with the AS5030. It can be cylindrical as well as square in shape. The key parameter is that the vertical magnetic field B_z, measured at a radius of 1mm from the rotation axis is sinusoidal with a peak amplitude of 20 ~ 80mT (see Figure 31).

10.1   Magnet Placement:

Ideally, the center of the magnet, the diagonal center of the IC and the rotation axis of the magnet should be in one vertical line.
The lateral displacement of the magnet should be within   ± 0.25mm from the IC package center or ± 0.5mm from the IC center, including the placement of the chip within the IC package.
The vertical distance should be chosen such that the magnetic field on the die surface is within the specified limits. The typical
distance "z" between the magnet and the package surface is 0.5mm to 1.8mm with the recommended magnet (6mm x 2.5mm). Larger gaps are possible, as long as the required magnetic field strength stays within the defined limits.
A magnetic field outside the specified range may still produce acceptable results, but with reduced accuracy. The out-of-range condition will be indicated, when the AGC is at the limits (AGC= 0 : field too strong;
AGC=63=($3F_H$): field too weak or missing magnet.

Figure 31: Vertical magnetic fields of a rotating magnet

Bz; 6mm magnet @y=0; z=1mm

N   S

100

50

0

50

100

Hall elements (side view)

150

3,5   2,5   1,5   0,5   -0,5   -1,5   -2,5   -3,5

X-displacement [mm]
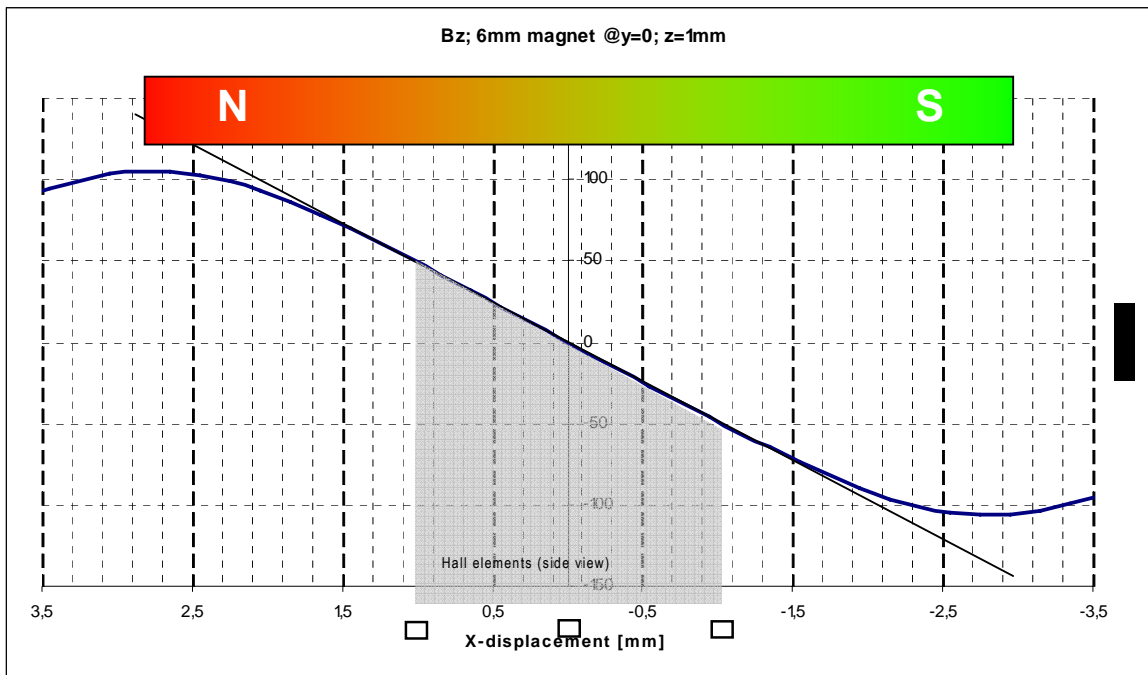
Figure 32: B_z field distribution along the x-axis of a 6mmØ diametric magnetized magnet

Figure 32 shows a cross sectional view of the vertical magnetic field component Bz between the north and south pole of a 6mm diameter magnet, measured at a vertical distance of 1mm. The poles of the magnet (maximum level) are about 2.8mm from the magnet center, which is almost at the outer magnet edges. The magnetic field reaches a peak amplitude of ~± 106mT at the poles.

The Hall elements are located at a radius of 1mm (indicated as squares at the bottom of the graph). Due to the side view, the two Hall elements at the Y-axis are overlapping at X = 0mm, therefore only 3 Hall elements are shown.

At 1mm radius, the peak amplitude is ~± 46mT, respectively a differential amplitude of 92mT.

The vertical magnetic field B_z follows a fairly linear pattern up to about 1.5mm radius. Consequently, even if the magnet is not perfectly centered, the differential amplitude will be the same as for a centered magnet.

For example, if the magnet is misaligned in X-axis by -0.5mm, the two X-Hall sensors will measure 70mT (@x = -1.5mm) and -22mt (@x = -0.5mm). Again, the differential amplitude is 92mT.

At larger displacements however, the B_z amplitude becomes nonlinear, which results in larger errors that mainly affect the accuracy of the system (see also Figure 34)
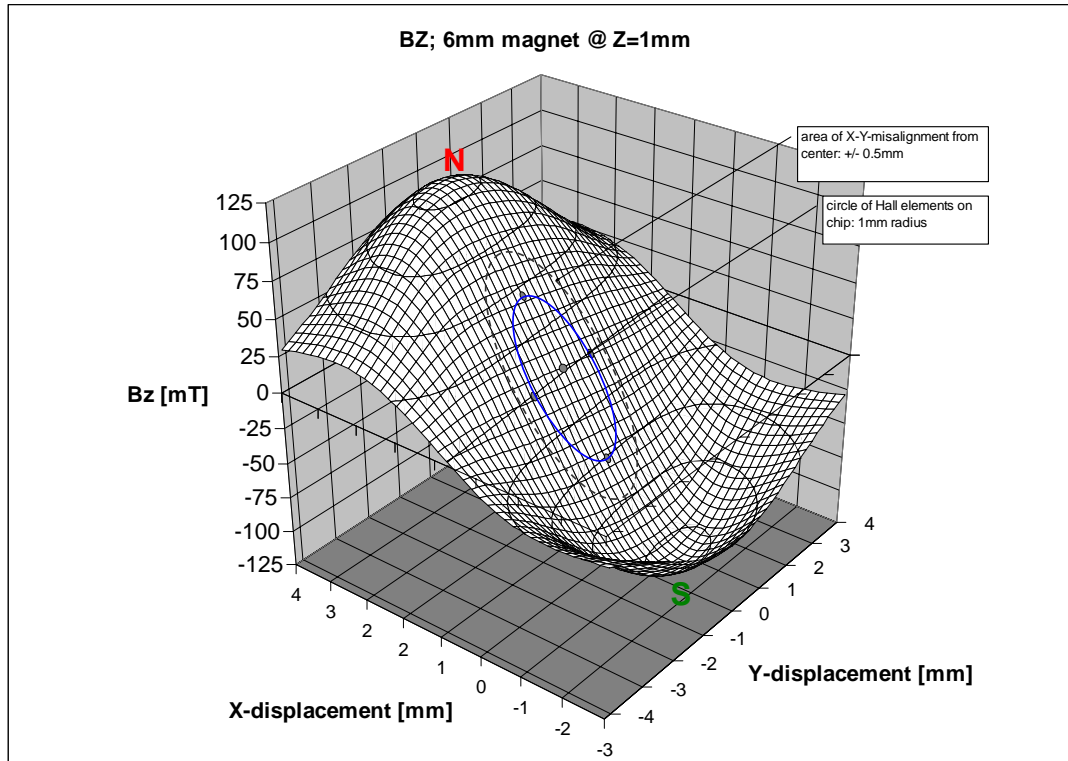
Figure 33: Vertical magnetic field distribution of a cylindrical 6mm Ø diametric magnetized magnet at 1mm gap

Figure 33 shows the same vertical field component as Figure 32, but in a 3-dimensional view over an area of ± 4mm from the rotational axis.

10.2 Lateral displacement of the magnet

As shown in the magnet specifications (4.4), the recommended horizontal position of the magnet axis with respect to the IC package center is within a circle of 0.25mm radius. This includes the placement tolerance of the IC within the package.

Figure 34 shows a typical error curve at a medium vertical distance of the magnet around 1.2mm (AGC = 24).

The X- and Y- axis of the graph indicate the lateral displacement of the magnet center with respect to the IC center.

At X = Y = 0, the magnet is perfectly centered over the IC. The total displacement plotted on the graph is for ± 1mm in both directions.

The Z-axis displays the worst case INL error over a full turn at each given X-and Y- displacement. The error includes the quantization error of ± 0.7° (see 0). For example, the accuracy for a centered magnet is between 1.0 ~ 1.5° (spec = 2° over full temperature range). Within a radius of 0.5mm, the accuracy is better than 2.0° (spec = 3° over temperature).

INL vs. Displacement: AS5030 for AGC24

Legend:
- 4,500-5,000
- 4,000-4,500
- 3,500-4,000
- 3,000-3,500
- 2,500-3,000
- 2,000-2,500
- 1,500-2,000
- 1,000-1,500
- 0,500-1,000
- 0,000-0,500

INL [°]: 5,000 / 4,500 / 4,000 / 3,500 / 3,000 / 2,500 / 2,000 / 1,500 / 1,000 / 0,500 / 0,000

X Displacement [µm]: -1000 / -750 / -500 / -250 / 0 / 250 / 500 / 750 / 1000

Y Displacement [µm]: 1000 / 750 / 500 / 250 / 0 / -250 / -500 / -750 / -1000
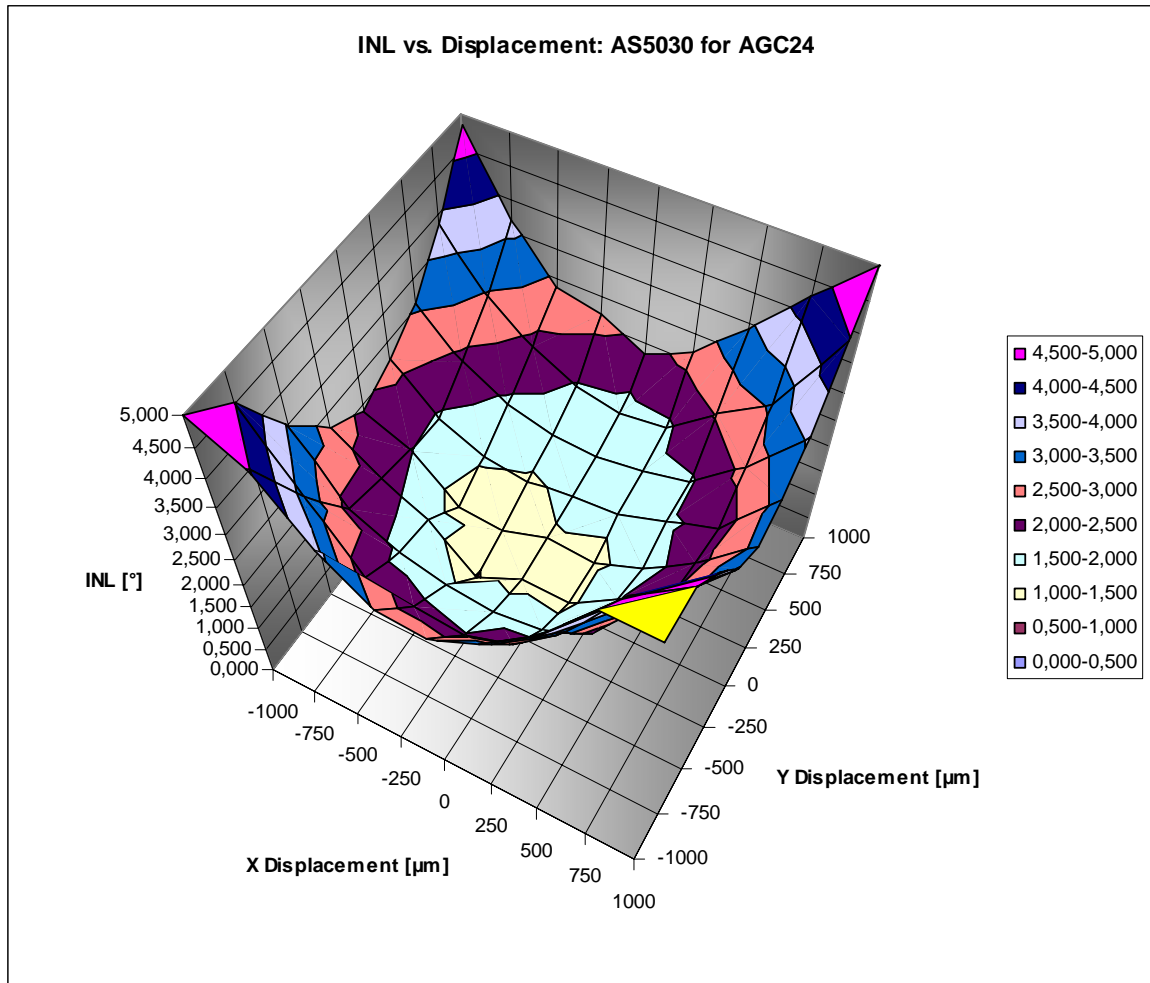
Figure 34: Typical error curve of INL error over lateral displacement (including quantization error)

10.3 Magnet size

Figure 32 to Figure 34 in this chapter describe a cylindrical magnet with a diameter of 6mm. Smaller magnets may also be used, but since the poles are closer together, the linear range will also be smaller and consequently the tolerance for lateral misalignment will also be smaller.
If the ± 0.25mm lateral misalignment radius (rotation axis to IC package center) is too tight, a larger magnet can be used.
Larger magnets have a larger linear range and allow more misalignment. However at the same time the slope of the magnet is more flat which results in a lower differential amplitude.
This requires either a stronger magnet or a smaller gap between IC and magnet in order to operate in the amplitude-controlled area (AGC > 0 and AGC < 63).
In any case, if a magnet other than the recommended 6mm diameter magnet is used, two parameters should be verified:

- Verify that the magnetic field produces a sinusoidal wave, when the magnet is rotated.
  Note: this can be done with the SIN-/COS- outputs of the AS5030, e.g. rotate the magnet at constant speed and analyze the SIN- (or COS-) output with an FFT-analyzer.
  It is recommended to disable the AGC for this test (see 4.20).
- Verify that the B_z-Curve between the poles is as linear as possible (see Figure 32). This curve may be available from the magnet supplier(s).
  Alternatively, the SIN- or COS- output of the AS5030 may also be used together with an X-Y- table to get a B_z-scan of the magnet (as in Figure 32 or Figure 33)
  Furthermore; the sinewave tests described above may be re-run at defined X-and Y- misplacements of the magnet to determine the maximum acceptable lateral displacement range.
  It is recommended to disable the AGC for both these tests (see 4.20).

Note: for preferred magnet suppliers, please refer to the austriamicrosystems website (Rotary Encoder section).

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11 Package Drawings and Markings

16-Lead Thin Shrink Small Outline Package TSSOP-16
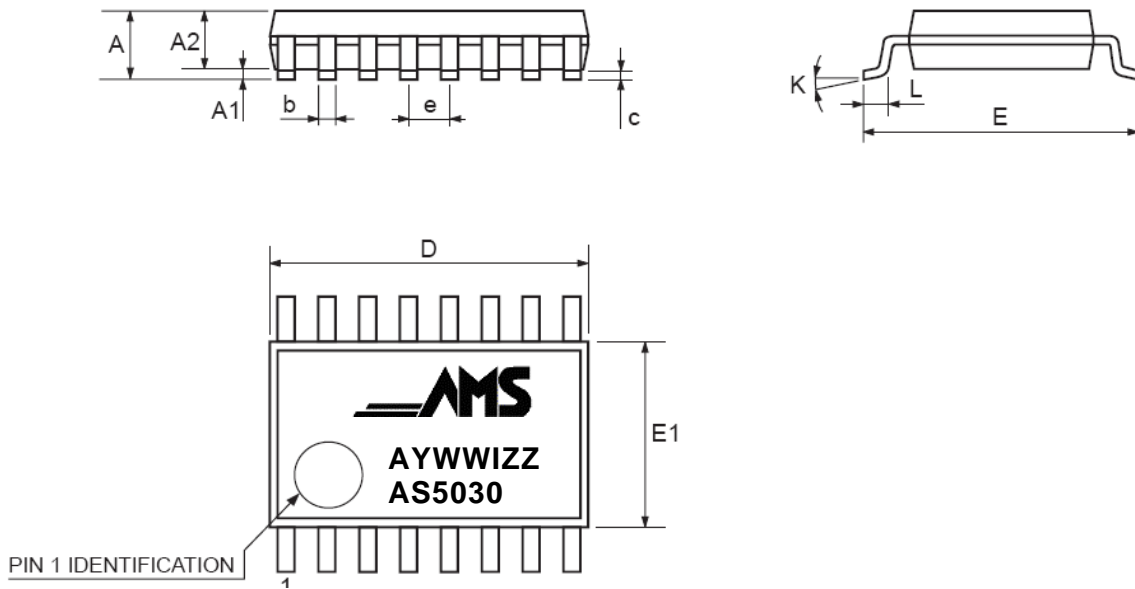
Dimensions						
Symbol	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.2			.047
A1	0.05	0.10	0.15	.002	.004	.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09	-	0.20	.004	-	.008
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e	0.65			.0256		
K	0°	-	8°	0°	-	8°
L	0.45	0.60	0.75	.018	.024	.030

Marking: AYWWIZZ

A: Pb-Free Identifier
Y: Last Digit of Manufacturing Year
WW: Manufacturing Week
I: Plant Identifier
ZZ: Traceability Code

JEDEC Package Outline Standard:
MO - 153

Thermal Resistance $R_{th(j-a)}$:
89 K/W in still air, soldered on PCB

IC's marked with a white dot or the
letters "ES" denote Engineering Samples

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12 Ordering Information

Delivery: Tape and Reel (1 reel = 4500 devices)
  Tubes (1 box = 100 tubes á 96 devices)

Order # AS5030ATSU for delivery in tubes
Order # AS5030ATST for delivery in tape and reel

13 Recommended PCB Footprint
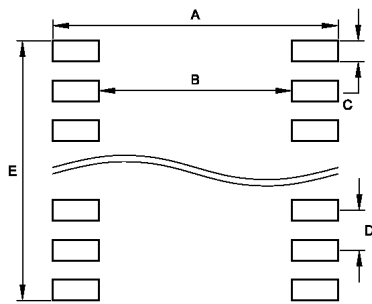
Recommended Footprint Data		
	mm	inch
A	7.26	0.286
B	4.93	0.194
C	0.36	0.014
D	0.65	0.0256
E	4.91	0.193

Table of contents

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