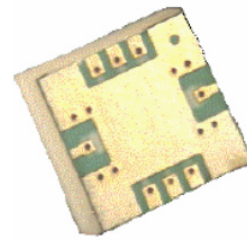


AMMP-6650

DC – 30 GHz Variable Attenuator



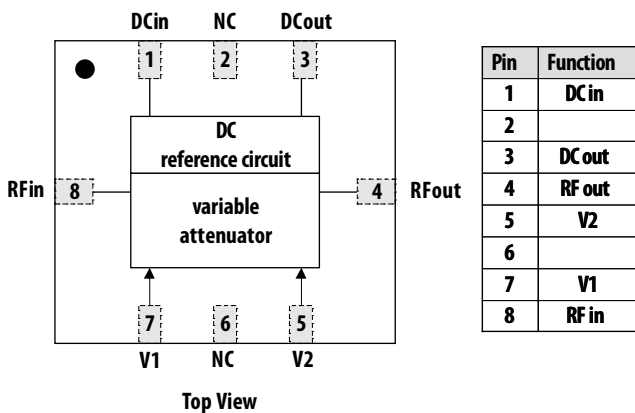
Data Sheet



Description

The AMMP-6650 is a voltage controlled variable attenuator in a surface mount package, designed to operate from DC to 30 GHz. It is fabricated using Avago Technologies enhancement mode pHEMT MMIC process and requires only positive voltage control. The distributed topology of the AMMP-6650 facilitates broadband operation by absorbing parasitic effects of its series and shunt FETs. An on-chip DC reference circuit may be used to maintain optimum VSWR for any attenuation setting or to provide more linear attenuation versus voltage response.

AMMP-6650 Pin Connections (Top View)



Note : Package base : GND

Features

- 5 x 5 mm Surface Mount Package
- Wide Frequency Range DC - 30 GHz
- Attenuation Range 20dB
- Single Positive Bias Supply
- Unconditionally Stable

Applications

- Microwave Radio Systems
- Satellite VSAT, DBS Up / Down Link
- LMDS & Pt – Pt mmW Long Haul
- Broadband Wireless Access (including 802.16 and 802.20 WiMax)
- WLL and MMDS loops



Attention: Observe precautions for handling electrostatic sensitive devices.

ESD Machine Model = 80 V
 ESD Human Body Model = 400 V
 Refer to Avago Application Note A004R:
 Electrostatic Discharge, Damage and Control.

Table 1. Absolute Maximum Ratings

Symbol	Parameters and Test Conditions	Unit	Minimum	Maximum
V ₁	Voltage to Control VSWR	V	0	1.6
V ₂	Voltage to Control Attenuation	V	0	1.6
P _{in}	RF Input Power	dBm	-	17
T _{ch}	Operating Channel Temperature	°C	-	+150
T _{stg}	Storage Temperature	°C	-65	+150
T _{max}	Maximum Assembly Temperature	°C		+300 for 60s

Notes:

Operation in excess of any one of these conditions may result in permanent damage to this device. The absolute maximum ratings for V₁, V₂ and P_{in} were determined at an ambient temperature of 25 C unless noted otherwise.

Table 2. DC Specifications

Symbol	Parameters	Test Conditions	Unit	Min	Typical	Max
I _{c_V1_ref}	V ₁ Control Current (Min Attenuation)	V1=1.5 V, V2=0 V	mA		1.93	2.0
I _{c_V2_ref}	V ₂ Control Current (Min Attenuation)	V1=1.5 V, V2=0 V	μA		0.8	2.5
I _{c_V1_max}	V ₁ Control Current (Max Attenuation)	V1=0 V, V2=1.25 V	μA		1.1	2.5
I _{c_V2_max}	V ₂ Control Current (Max Attenuation)	V1=0 V, V2=1.25 V	mA		1.41	1.5

Notes:

Ambient operation temperature T_A = 25°C.

Table 3. RF Specifications^[1,2] (T_A = 25°C, Z₀ = 50 Ω)

Symbol	Parameters and Test Conditions	Units	Freq. [GHz]	Minimum	Typical	Maximum
Minimum Attenuation (Reference State)	S ₂₁ V1 = 1.5 V V2 = 0.0 V	dB	2		0.9	1.5
			10		2.0	2.5
			20		0.9	2.5
			30		2.1	3.0
Maximum Attenuation	S ₂₁ V1 = 0.0 V V2 = 1.25 V	dB	2	23	26.6	
			10	23	28.0	
			20	23	30.0	
			30	23	35.6	
Return Loss (In/Out) at Reference State	V1=1.5 V, V2=0.0 V	dB	<30		10	
Return Loss (In/Out) at Max. Attenuation	V1=0.0 V, V2=1.25 V	dB	<30		10	

Notes:

- Fully de-embedded data obtained from in-fixture measurements
- All tested parameters guaranteed with measurement accuracy ±0.2 for Min Attenuation of 2&10GHz, ±0.5 for Min Attenuation of 20GHz&30GHz and Max Attenuation of 2GHz, ±1 for Max Attenuation of 10GHz&20GHz and ±1.2 for Max Attenuation of 30GHz.

Typical Distribution Charts^[1]

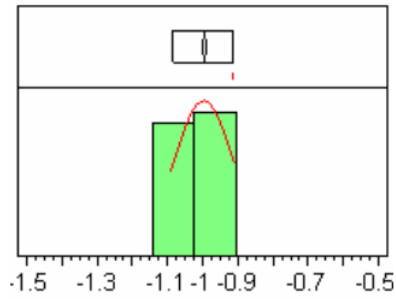


Figure 1d. Min Attenuation @ 2GHz, nominal=-0.9, LSL=-1.5

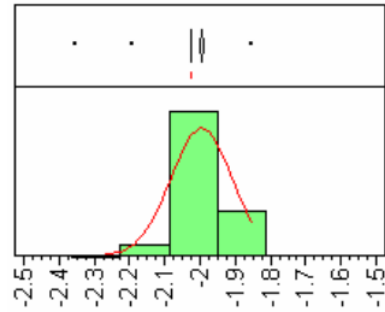


Figure 2d. Min Attenuation @ 10GHz, nominal=-2.0, LSL=-2.5

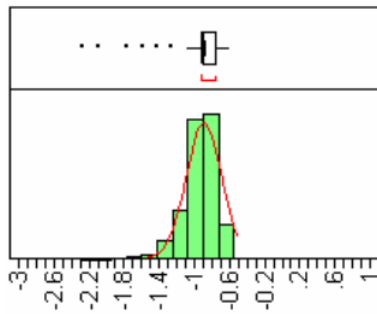


Figure 3d. Min Attenuation @ 20GHz, nominal=-0.9, LSL=-2.5

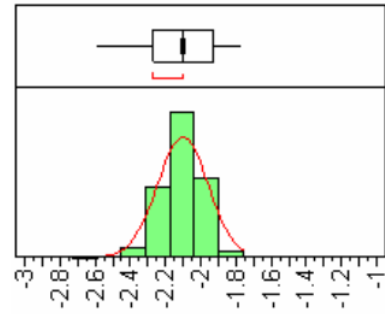


Figure 4d. Min Attenuation @ 30GHz, nominal=-2.1, LSL=-3.0

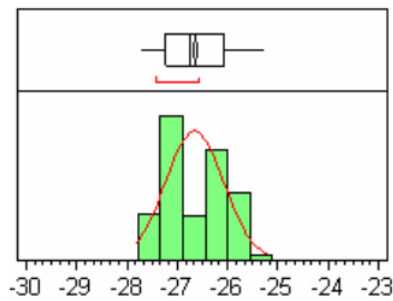


Figure 5d. Max Attenuation @ 2GHz, nominal=-26.6, USL=-23

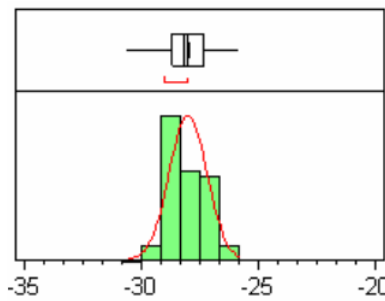


Figure 6d. Max Attenuation @ 10GHz, nominal=-28, USL=-23

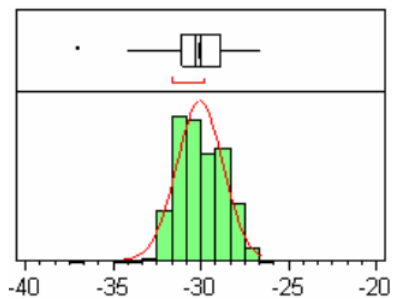


Figure 7d. Max Attenuation @ 33GHz, Nominal=-32.7, USL=-23.0

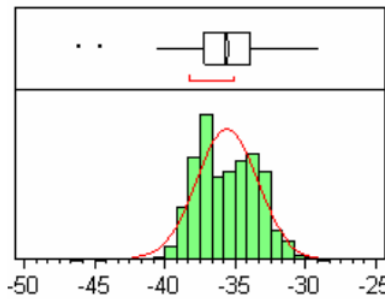


Figure 8d. Max Attenuation @ 40GHz, Nominal=-35.7, USL=-23.0

Notes:

1. Distribution data based on 5000 part sample from two wafer lots tested during initial characterization. Future wafers may have nominal values anywhere between upper and lower limit.

Typical Performance ($T_A = 25^\circ\text{C}$, $Z_{in} = Z_{out} = 50 \Omega$)

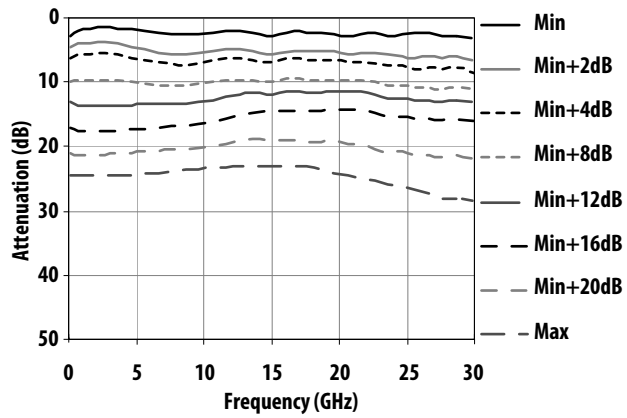


Figure 1. Attenuation vs Frequency

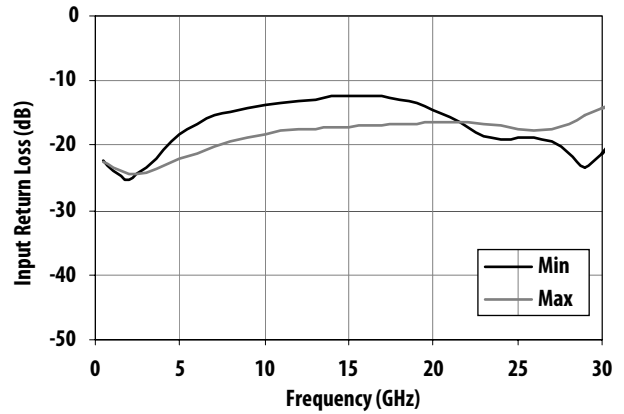


Figure 2. Input Return Loss vs Frequency

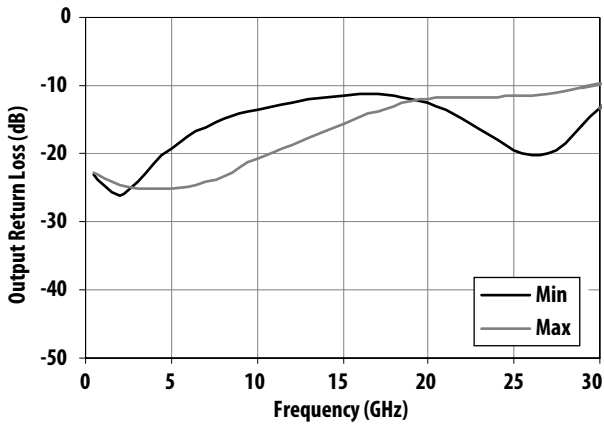


Figure 3. Output Return Loss vs Frequency

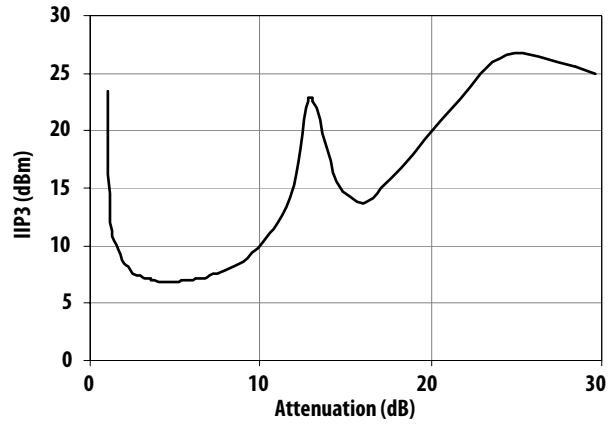


Figure 4. IIP3 vs Attenuation at 2 GHz (note 2)

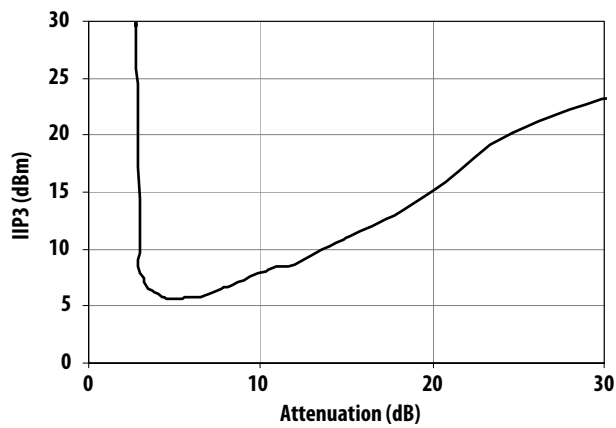


Figure 5. IIP3 vs Attenuation at 12 GHz (note 2)

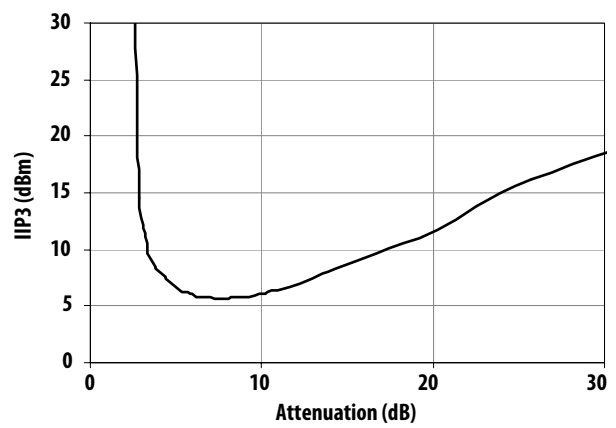


Figure 6. IIP3 vs Attenuation at 22 GHz (note 2)

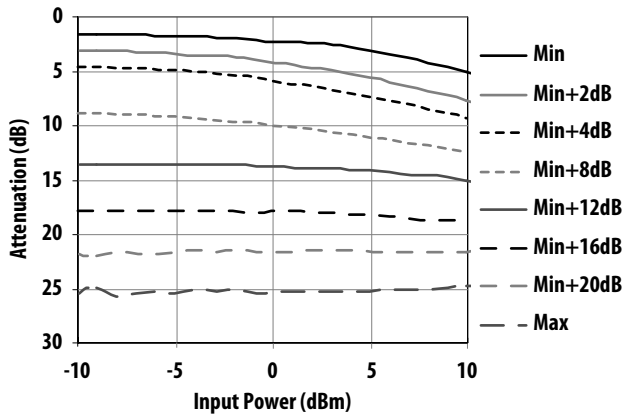


Figure 7. Attenuation vs Input Power at 2 GHz

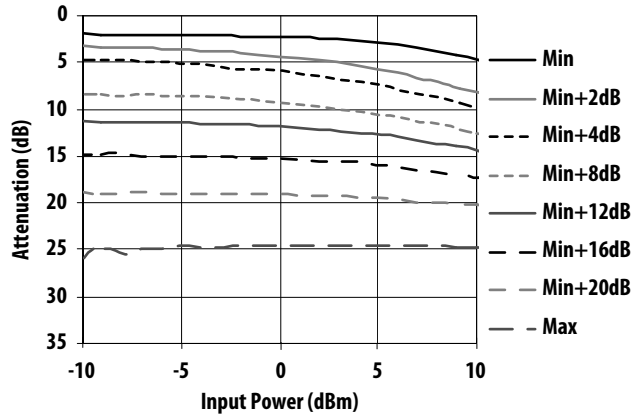


Figure 8. Attenuation vs Input Power at 12 GHz

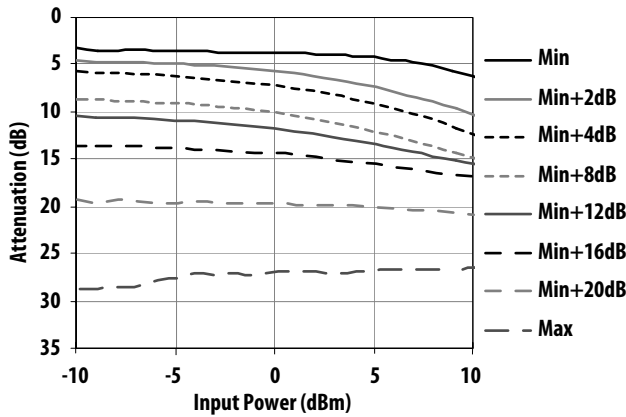


Figure 9. Attenuation vs Input Power at 22 GHz

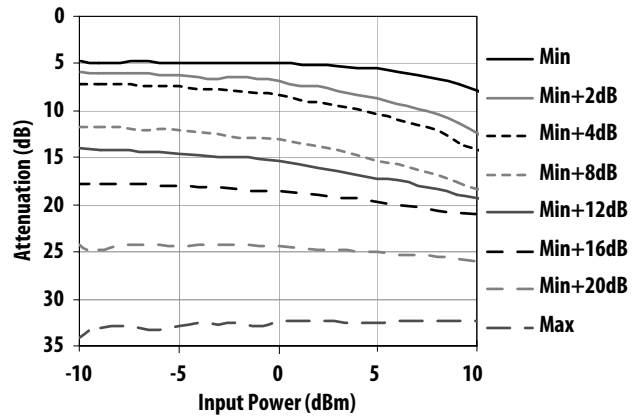


Figure 10. Attenuation vs Input Power at 32 GHz

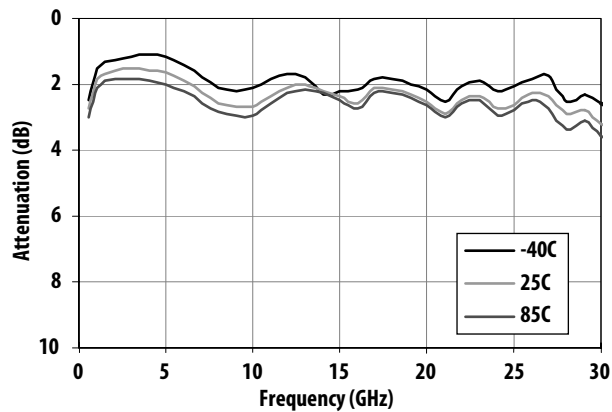


Figure 11. Attenuation vs Frequency (Min Attenuation)

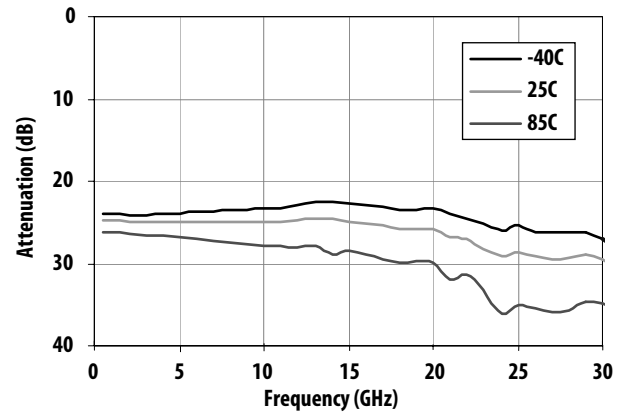


Figure 12. Attenuation vs Frequency (Max Attenuation)

Notes:

1. All tests done on an AMMP-6650 mounted on a PCB equipped with RF connectors and an op-amp driver shown in Figure 14.
2. IIP3 measured with two input signals with frequency difference of 10 MHz, each input signal at -10 dBm
3. All attenuation settings were done at 2GHz utilizing the AMMP-6650 DC Reference circuit. V_{REF} was set to 0.1 volt.

AMMP-6650 Typical Scattering Parameters at Minimum Attenuation

(Tc = 25°C, Zo = 50ohm, V1 = 1.5V, V2 = 0V)

Freq GHz	S11			S21			S12			S22		
	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase
0.5	-26.02	0.05	-39.1	-1.13	0.88	-5.8	-1.15	0.88	-5.8	-26.2	0.05	-39.2
1	-26.02	0.05	-66.7	-1.1	0.88	-10.3	-1.18	0.87	-10.3	-25.51	0.05	-60.2
2	-22.73	0.07	-93.5	-1.13	0.88	-19.2	-1.23	0.87	-19.2	-22.62	0.07	-85.5
3	-20.09	0.1	-108	-1.24	0.87	-28.1	-1.34	0.86	-28.1	-20.18	0.1	-102.1
4	-18.34	0.12	-120.3	-1.31	0.86	-36.9	-1.43	0.85	-36.9	-18.56	0.12	-115.4
5	-16.95	0.14	-131.5	-1.36	0.86	-45.5	-1.47	0.84	-45.5	-17.33	0.14	-127.6
6	-16.03	0.16	-140.9	-1.42	0.85	-54.2	-1.55	0.84	-54	-16.36	0.15	-137.4
7	-15.34	0.17	-149.7	-1.46	0.85	-62.7	-1.6	0.83	-62.5	-15.76	0.16	-146.5
8	-14.8	0.18	-157.5	-1.52	0.84	-71.3	-1.65	0.83	-71	-15.24	0.17	-155
9	-14.7	0.18	-165.3	-1.55	0.84	-79.8	-1.7	0.82	-79.5	-15.04	0.18	-163.3
10	-14.47	0.19	-172.9	-1.62	0.83	-88.4	-1.74	0.82	-88	-14.94	0.18	-171.8
11	-14.75	0.18	-180	-1.64	0.83	-96.8	-1.79	0.81	-96.5	-14.99	0.18	179.9
12	-14.85	0.18	172.5	-1.68	0.82	-105.4	-1.82	0.81	-105.1	-15.34	0.17	172.3
13	-15.39	0.17	165.6	-1.7	0.82	-114.1	-1.84	0.81	-113.7	-15.81	0.16	164.3
14	-15.92	0.16	158.2	-1.73	0.82	-122.8	-1.85	0.81	-122.4	-16.42	0.15	156.6
15	-16.83	0.14	151	-1.76	0.82	-131.5	-1.87	0.81	-131.2	-17.33	0.14	148.6
16	-17.86	0.13	143.5	-1.78	0.82	-140.3	-1.88	0.81	-139.9	-18.64	0.12	141.1
17	-19.33	0.11	135.1	-1.8	0.81	-149.3	-1.89	0.8	-148.9	-20.18	0.1	134
18	-21.11	0.09	127.3	-1.81	0.81	-158.4	-1.92	0.8	-158	-22.16	0.08	125.4
19	-23.35	0.07	116.3	-1.83	0.81	-167.7	-1.94	0.8	-167.1	-24.88	0.06	118.4
20	-27.33	0.04	99.3	-1.86	0.81	-176.9	-1.96	0.8	-176.5	-28.64	0.04	107.6
21	-32.77	0.02	59.4	-1.92	0.8	173.5	-2.03	0.79	174	-35.39	0.02	81.1
22	-31.7	0.03	-19.1	-2	0.79	163.9	-2.09	0.79	164.4	-37.72	0.01	-23.8
23	-25.68	0.05	-54	-2.12	0.78	154.2	-2.21	0.78	154.7	-29.37	0.03	-61.8
24	-21.62	0.08	-71.5	-2.23	0.77	144.6	-2.35	0.76	145.2	-24.44	0.06	-73.2
25	-18.34	0.12	-85.7	-2.35	0.76	135.4	-2.45	0.75	136	-20.92	0.09	-85.7
26	-16.48	0.15	-100.6	-2.38	0.76	126.8	-2.5	0.75	127.3	-18.49	0.12	-98.5
27	-14.99	0.18	-114.3	-2.45	0.75	118.8	-2.56	0.75	119.2	-16.77	0.15	-111
28	-14.33	0.19	-127.7	-2.5	0.75	110.1	-2.59	0.74	110.6	-15.86	0.16	-123.6
29	-14.24	0.19	-137.9	-2.58	0.74	101.1	-2.64	0.74	101.6	-15.49	0.17	-134.6
30	-14.47	0.19	-147.1	-2.65	0.74	91.5	-2.69	0.73	91.9	-15.65	0.17	-144.9
31	-14.52	0.19	-155.5	-2.7	0.73	82.3	-2.72	0.73	82.8	-15.76	0.16	-151.7
32	-14.99	0.18	-164.2	-2.73	0.73	73.2	-2.77	0.73	73.8	-16.14	0.16	-160.2
33	-16.03	0.16	-171.7	-2.78	0.73	63.3	-2.83	0.72	63.9	-17.2	0.14	-168.8
34	-17.72	0.13	-177.3	-2.83	0.72	53.1	-2.88	0.72	53.7	-18.86	0.11	-174.7
35	-20.09	0.1	-178	-2.83	0.72	42.8	-2.93	0.71	43.3	-20.92	0.09	-173.1
36	-22.5	0.08	-166.3	-2.95	0.71	32	-2.96	0.71	32.7	-23.48	0.07	-162.3
37	-23.48	0.07	-143.6	-2.96	0.71	21	-3.01	0.71	21.8	-24.01	0.06	-137.3
38	-21.41	0.09	-122.9	-3.01	0.71	9.9	-3.09	0.7	10.6	-21.62	0.08	-117.7
39	-18.56	0.12	-116.9	-3.12	0.7	-1.5	-3.2	0.69	-0.7	-18.56	0.12	-113.5
40	-16.36	0.15	-118.7	-3.25	0.69	-13	-3.31	0.68	-12.2	-16.31	0.15	-115.9
41	-14.56	0.19	-123.8	-3.43	0.67	-24.9	-3.49	0.67	-24.1	-14.33	0.19	-122
42	-13.11	0.22	-130.9	-3.69	0.65	-36.8	-3.76	0.65	-36.1	-12.69	0.23	-130.4
43	-12.01	0.25	-139.4	-4.01	0.63	-48.7	-4.08	0.63	-48.2	-11.5	0.27	-139.5
44	-11.28	0.27	-148.9	-4.34	0.61	-60.5	-4.42	0.6	-59.7	-10.66	0.29	-149.8
45	-10.81	0.29	-158.8	-4.78	0.58	-72.7	-4.82	0.57	-71.9	-9.95	0.32	-160.7
46	-10.57	0.3	-169.5	-5.26	0.55	-84.2	-5.29	0.54	-83.5	-9.47	0.34	-171.9
47	-10.6	0.3	-179.7	-5.66	0.52	-95.7	-5.71	0.52	-95.1	-9.22	0.35	176.6
48	-10.78	0.29	170.4	-6.14	0.49	-107.7	-6.23	0.49	-107	-9.14	0.35	165
49	-11.28	0.27	162.1	-6.76	0.46	-119.1	-6.8	0.46	-118.5	-9	0.36	152.8

Notes:

AMMP-6650 mounted on a PCB equipped with RF connectors and an op-amp driver shown in Figure 14.

AMMP-6650 Typical Scattering Parameters at Maximum Attenuation

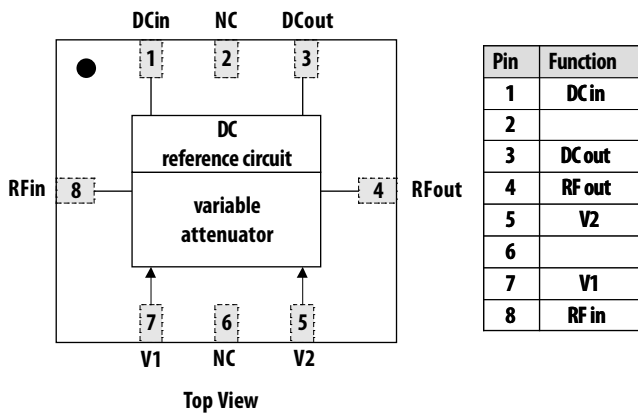
(Measured on-wafer, $T_c = 25^\circ\text{C}$, $Z_o = 50\text{ohm}$, $V_1 = 0\text{V}$, $V_2 = 1.25\text{V}$)

Freq GHz	S11			S21			S12			S22		
	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase
0.5	-22.85	0.07	-12.3	-24.44	0.06	-3.8	-24.58	0.06	-3.7	-22.62	0.07	-12.7
1	-22.5	0.08	-21.6	-24.44	0.06	-6.7	-24.58	0.06	-6.7	-22.5	0.08	-21.4
2	-21.94	0.08	-38.5	-24.58	0.06	-12.6	-24.58	0.06	-12.7	-21.94	0.08	-38
3	-20.82	0.09	-53.4	-24.44	0.06	-18.5	-24.44	0.06	-18.5	-21.01	0.09	-53.6
4	-19.83	0.1	-67	-24.44	0.06	-24.6	-24.44	0.06	-24.7	-20.18	0.1	-66.8
5	-19.02	0.11	-78.6	-24.29	0.06	-30.8	-24.29	0.06	-30.8	-19.25	0.11	-78.9
6	-18.2	0.12	-89	-24.15	0.06	-37.1	-24.15	0.06	-37.2	-18.42	0.12	-89.1
7	-17.46	0.13	-98.9	-24.01	0.06	-44	-24.01	0.06	-43.8	-17.65	0.13	-98.2
8	-16.77	0.15	-107	-23.88	0.06	-51.1	-23.88	0.06	-50.9	-17.02	0.14	-107
9	-16.36	0.15	-114.6	-23.74	0.07	-58.5	-23.61	0.07	-58.5	-16.48	0.15	-115
10	-15.86	0.16	-121.5	-23.48	0.07	-66.2	-23.48	0.07	-66.1	-16.08	0.16	-122.5
11	-15.49	0.17	-127.9	-23.35	0.07	-74.1	-23.35	0.07	-74.1	-15.76	0.16	-129.7
12	-15.29	0.17	-134.6	-23.22	0.07	-82.4	-23.22	0.07	-82.3	-15.49	0.17	-136.5
13	-15.19	0.17	-140.7	-23.1	0.07	-91	-23.1	0.07	-90.9	-15.34	0.17	-142.7
14	-14.99	0.18	-146.6	-23.1	0.07	-100	-22.97	0.07	-100	-15.29	0.17	-149.2
15	-15.04	0.18	-151.7	-22.97	0.07	-109.5	-22.97	0.07	-109.6	-15.24	0.17	-154.9
16	-15.19	0.17	-156.8	-22.85	0.07	-119.4	-22.85	0.07	-119.4	-15.39	0.17	-160.4
17	-15.34	0.17	-162	-22.97	0.07	-130.1	-22.85	0.07	-130.1	-15.55	0.17	-165.3
18	-15.44	0.17	-166.1	-23.1	0.07	-141.6	-23.1	0.07	-141.7	-15.76	0.16	-169.3
19	-15.7	0.16	-170.4	-23.48	0.07	-153.4	-23.48	0.07	-153.2	-15.92	0.16	-172.9
20	-15.97	0.16	-174.7	-24.01	0.06	-164.8	-23.88	0.06	-164.8	-15.86	0.16	-176.5
21	-16.14	0.16	-178.9	-24.44	0.06	-174.2	-24.44	0.06	-174.2	-15.92	0.16	178.7
22	-16.48	0.15	176.4	-24.88	0.06	178.2	-24.88	0.06	178.2	-16.03	0.16	173.4
23	-16.95	0.14	170.7	-25.35	0.05	172.3	-25.19	0.06	172.3	-16.14	0.16	167.4
24	-17.52	0.13	166.5	-25.85	0.05	167.1	-25.68	0.05	167	-16.48	0.15	161.9
25	-18.06	0.13	164.2	-26.2	0.05	164.2	-26.2	0.05	163.9	-16.83	0.14	156.1
26	-18.64	0.12	159.6	-26.74	0.05	159.2	-27.13	0.04	159	-17.14	0.14	149.9
27	-19.33	0.11	154.9	-27.33	0.04	154	-27.54	0.04	153.4	-17.59	0.13	143.3
28	-19.66	0.1	149.9	-27.96	0.04	146.1	-27.74	0.04	145.7	-17.92	0.13	136.2
29	-20.54	0.09	144.5	-28.18	0.04	137.2	-28.18	0.04	137.1	-18.56	0.12	128.3
30	-21.62	0.08	135.2	-28.4	0.04	127.3	-28.4	0.04	126.5	-19.17	0.11	118.7
31	-22.73	0.07	126.4	-28.87	0.04	120.3	-28.87	0.04	120.3	-20	0.1	109.2
32	-24.01	0.06	118.1	-28.87	0.04	112.8	-28.87	0.04	112.6	-20.63	0.09	99.5
33	-25.51	0.05	103.6	-29.12	0.04	104	-29.12	0.04	103.2	-21.31	0.09	86.3
34	-26.94	0.05	81.6	-29.63	0.03	95.5	-29.37	0.03	95.1	-21.62	0.08	71.8
35	-27.54	0.04	58	-29.9	0.03	86.6	-29.9	0.03	86.3	-21.83	0.08	57.5
36	-27.13	0.04	33.7	-30.17	0.03	77.8	-30.17	0.03	77	-21.94	0.08	41.4
37	-25.85	0.05	12.4	-30.75	0.03	69.3	-30.75	0.03	70.4	-21.62	0.08	26.2
38	-23.88	0.06	-1.6	-31.06	0.03	61.3	-31.37	0.03	59.1	-21.01	0.09	12.2
39	-22.16	0.08	-16	-31.7	0.03	53.2	-31.7	0.03	53.8	-20.45	0.1	0.4
40	-20.35	0.1	-25.2	-32.04	0.03	45.6	-32.04	0.03	43.4	-19.66	0.1	-11.7
41	-19.25	0.11	-32.1	-32.4	0.02	36.2	-32.77	0.02	34.8	-18.79	0.12	-21.6
42	-17.92	0.13	-40.3	-33.15	0.02	27.5	-33.15	0.02	27.4	-18.2	0.12	-29.8
43	-17.14	0.14	-46.9	-33.98	0.02	18.7	-33.56	0.02	17.2	-17.86	0.13	-38
44	-16.42	0.15	-52.7	-34.42	0.02	10.3	-34.42	0.02	11.9	-17.27	0.14	-44.2
45	-15.76	0.16	-57	-34.89	0.02	-0.1	-35.39	0.02	-2.9	-16.89	0.14	-47.7
46	-15.04	0.18	-58	-35.92	0.02	-10	-35.92	0.02	-7.6	-16.65	0.15	-49
47	-14.29	0.19	-58.8	-36.48	0.02	-19.6	-36.48	0.02	-18.6	-15.92	0.16	-49.9
48	-13.47	0.21	-62.3	-37.72	0.01	-29.1	-37.72	0.01	-28.8	-14.7	0.18	-51
49	-12.04	0.25	-67.5	-38.42	0.01	-41.4	-37.72	0.01	-37.8	-13.56	0.21	-54.4

Notes:

AMMP-6650 mounted on a PCB equipped with RF connectors and an op-amp driver shown in Figure 14.

Biasing considerations



Note : Package base : GND

Figure 13. Bias voltage connections

Attenuation is controlled by applying voltage to pin V1 (Pin 7) and pin V2 (Pin5), as shown in Figure 13.

For the minimum attenuation, V1 is set to 1.5 V and V2 is set to 0 V. The 1.5 V applied to the V1 pin biases the series FETs to a full “on” state, while the 0 V applied to the V2 pin keeps the shunt FETs in an “off” or “open” state; thus creating the lumped element 50 Ω transmission line effect. The V2 voltage swing from 0 V to 1.25 V increases the level of attenuation. The V1 voltage swing from 1.5 V to 0 V effectively optimizes the input and output match at higher attenuation levels. The AMMP-6650 can be driven by two complementary voltage ramps placed on V1 and V2. Careful adjustments of the two control lines over a relatively small voltage ranges are required to set the attenuation and optimize VSWR.

The on-chip DC reference circuit can be used to optimize VSWR for any attenuation setting, improve voltage versus attenuation linearity and range, and provide temperature compensation.

The on-chip DC reference circuit is a non-distributed “T” attenuator designed to operate in a 50 Ω system and track the control voltage versus attenuation characteristics of the RF attenuator. A simplified schematic of the AMMP-6650 together with an op-amp driver that utilizes the DC reference circuit is shown in Figure 14.

OP AMP 1 insures that the attenuator maintains a good input and output match to 50 Ω , while **OP AMP 2** increases the usable control voltage range versus using only direct voltage ramps for V1 and V2 and improves over temperature operation.

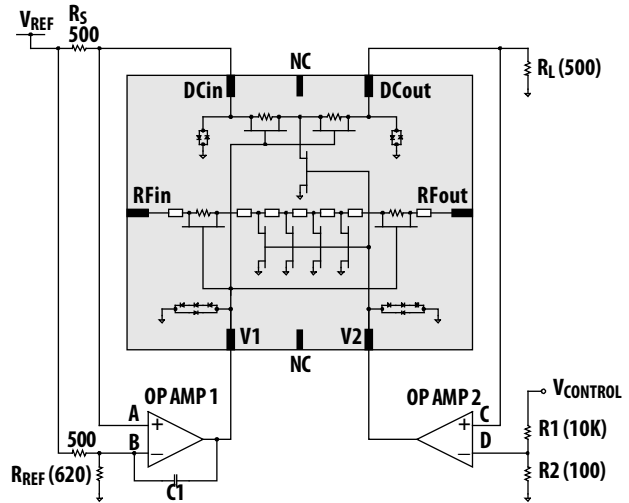


Figure 14. AMMP-6650 and the op-amp driver circuit

If optimum VSWR is all that is required, **OP AMP 2** may be eliminated however, R_L must remain connected to the DCout pad of the AMMP-6650 and the control voltage can be applied directly to V2.

CAUTION: Low voltage op-amps must be used so as not to exceed the maximum limit of V1 and V2 control voltages.

As shown, a voltage reference (V_{REF}) is fed to the reference circuit DCin pad via a 500 Ω resistor, creating a 500 Ω source. The reference circuit termination R_L , is connected to the DCout pad and ideally is also equal to 500 Ω . This voltage is controlled in parallel with the RF attenuator. The chosen value of V_{REF} must be low enough to avoid modifying the FET biasing and lower than the turn-on voltage of the ESD protection diode but high enough such that the attenuated voltage at **OP AMP 2** is usable compared to input offsets etc. The optimum value for the positive reference voltage is approximately 0.1 to 0.4 V.

At equilibrium, the voltages at nodes A and B of the **OP AMP 1** must be equal which implies that the input impedance to the DC reference circuit is equal to R_{REF} . When V2 is changed to a lower value, the voltage at node A becomes greater than that of node B. This voltage difference causes the output voltage of op **OP AMP 1** to move toward its positive rail until equilibrium is once again established. When V2 is changed to a higher value the voltage at node A becomes less than that of node B and the output voltage of **OP AMP 1** will swing toward its negative rail until equilibrium is reached. If the reference circuit precisely tracks the RF circuit, the voltage output of **OP AMP 1** at equilibrium insures that the RF circuit is matched to 50 Ω .

If attenuation linearity is required, **OP AMP 2** is included as shown in Figure 14 and a positive control voltage is applied to V_{CONTROL} . At equilibrium, voltages at nodes C and D are equal. When V_{CONTROL} is changed, the output of **OP AMP 2** adjusts to a value that forces the voltage at node C to equal the voltage at node D. Therefore, the output voltage of the DC reference circuit is proportional to V_{CONTROL} . The input voltage to the reference circuit is being held constant and the $\log(V_{\text{CONTROL}})$ is proportional to the reference circuit attenuation $20\log(\text{DCout}/\text{DCin})$.

If the FET parameters of the DC reference circuit track the FET parameters of the RF circuit, the voltage output of the RF circuit is also proportional to the control voltage. This translates to a linear relationship between the attenuation (in dB) and the $\log(V_{\text{CONTROL}})$.

Two RF attenuation vs voltage curves corresponding to different values of V_{REF} are shown in Figure 15. These curves were obtained by using the driver circuit shown in Figure 14 and the V_{REF} values 0.1 V and 0.4 V. Values for R_L , R_1 and R_2 were $500\ \Omega$, $10\ \text{k}\Omega$ and $100\ \Omega$ respectively. Control voltage ranged from 4.5 V to 0 V.

Because the FETs in the DC circuit are not identical to those in the RF circuit, the DC circuit does not exactly track the RF circuit. This results in attenuation vs. voltage curves that are not exactly linear.

OP AMP 2 provides temperature compensation by adjusting V_2 in such a way as to keep voltage at point C equal to that point D. If the attenuation changes over temperature, voltage at point C tries to change, but is corrected by **OP AMP 2**.

Another way to improve performance of the attenuator driver circuit is to adjust R_L and R_{REF} . If the reference circuit precisely tracked the RF circuit and the ON resistance of the FETs was zero ohms, then R_L and R_{REF} would be exactly $500\ \Omega$.

Due to the difference in layout structures, the reference circuit does not track the RF circuit precisely. R_L and R_{REF} can be adjusted in order to compensate for these differences. Optimum values of R_L and R_{REF} have been found to be between $500\ \Omega$ and $650\ \Omega$.

For maximum dynamic range on the attenuation control circuit, R_L should be less than R_{REF} by an amount equal to the "ON resistance" of the reference circuit series FETs. The "ON resistance" of the series FETs is about $95\ \Omega$ total. Therefore, the relationship between R_L and R_{REF} is as follows:

$$R_{\text{REF}} = R_L + 95\ \Omega$$

The voltage divider formed by R_1 and R_2 can be used to adjust the sensitivity of the attenuator versus control voltage. For the driver circuit shown in Figure 14, maximum attenuation is always achieved by setting V_{CONTROL} equal to 0 V. Minimum attenuation is achieved when

$$V_{\text{control}} \approx \left(\frac{R_1 + R_2}{R_2} \right) \times \left(\frac{R_L}{500\ \Omega + R_L} \right) \times V_{\text{ref}}$$

or

$$V_{\text{control}} \approx \left(1 + \frac{R_1}{R_2} \right) \times \text{DC}_{\text{out}}$$

Therefore, an increase in the resistor ratio R_1/R_2 increases the value of the control voltage required to produce minimum attenuation.

LMV932 (National Semiconductor) was used in the control circuit that produced the results shown in Figure 15; however, any low noise, low offset voltage op amp should produce similar results. LMV932's low supply voltage of 1.8 volts, limits the possibility of exceeding the 1.5 volt absolute maximum of the AMMC-6650 V1 and V2 control line inputs.

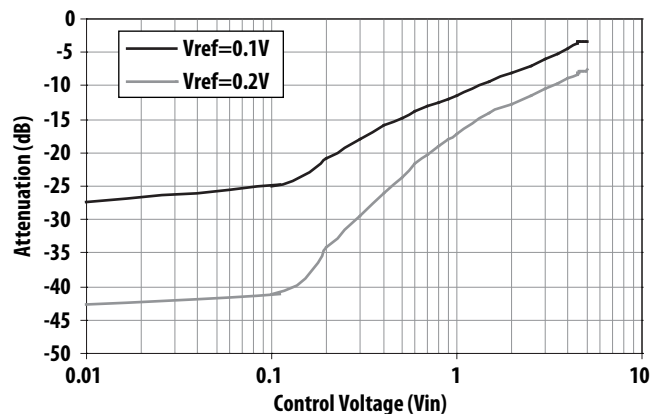


Figure 15. Attenuation vs. Control Voltage @ 15 GHz

Recommended SMT Attachment

The AMMP Packaged Devices are compatible with high volume surface mount PCB assembly processes.

The PCB material and mounting pattern, as defined in Figure 19, optimizes RF performance and is strongly recommended. An electronic drawing of the land pattern is available upon request from Avago Sales & Application Engineering.

Manual Assembly

1. Follow ESD precautions while handling packages.
2. Handling should be along the edges with tweezers.
3. Recommended attachment is conductive solder paste. Please see recommended solder reflow profile. Conductive epoxy is not recommended. Hand soldering is not recommended.
4. Apply solder paste using a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance.
5. Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temperature to avoid damage due to thermal shock.
6. Packages have been qualified to withstand a peak temperature of 260°C for 20 seconds. Verify that the profile will not expose device beyond this limit.

Solder Reflow Profile

A commonly used solder reflow method is accomplished in a belt furnace using convection heat. The suggested reflow profile Figure 16. This profile will vary among different solder pastes from different manufacturers and is shown here for reference only.

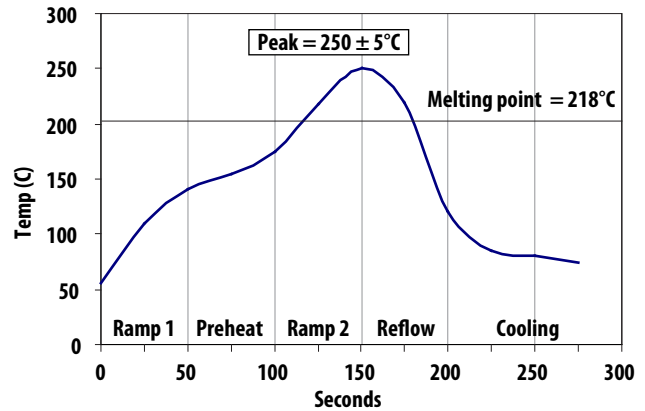
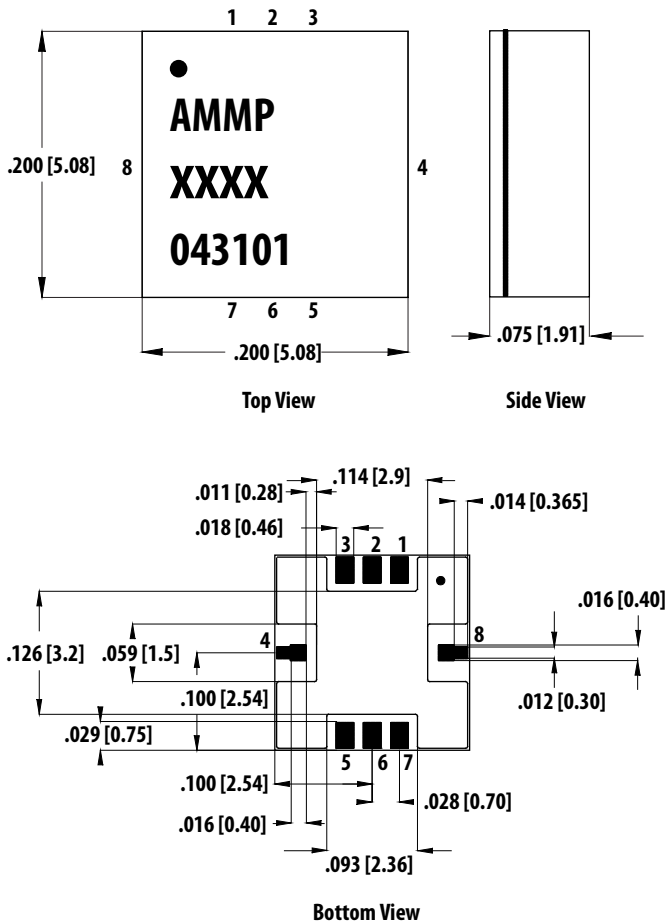


Figure 16. Suggested lead free reflow profile for SnAgCu Solder paste

Package Outline Drawing



Notes:

1. Indicates Pin 1 (Backside of the Package)
2. Dimensions are in inches [millimeters]
3. All grounds must be soldered to PCB RF ground

Dimensional Tolerances: 0.002" [0.05mm]

Stencil Design Guidelines

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads. The recommended stencil layout is shown in Fig 17. The stencil has a solder paste deposition opening approximately 70% to 90% of the PCB pad. Reducing stencil opening can potentially generate more voids underneath. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use a laser cut stencil composed of 0.127 mm (5 mils) thick stainless steel which is capable of producing the required fine stencil outline.

Recommended PCB Land Pattern for Rogers R04350 is shown in Fig 18.

The combined PCB and stencil layout is shown in Fig 19.

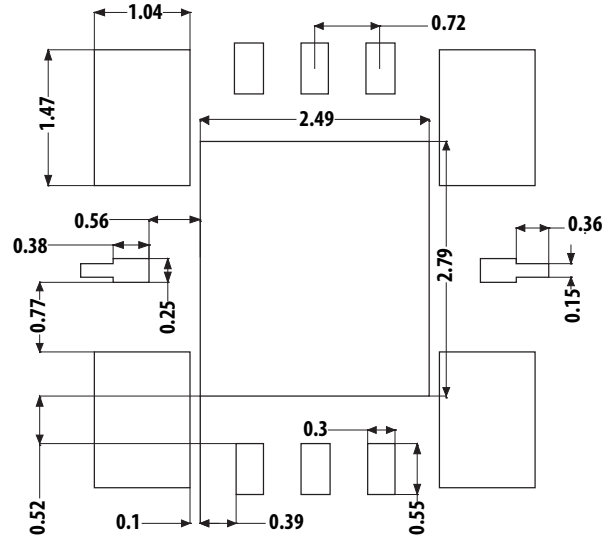


Figure 17. Stencil Outline Drawing (mm).

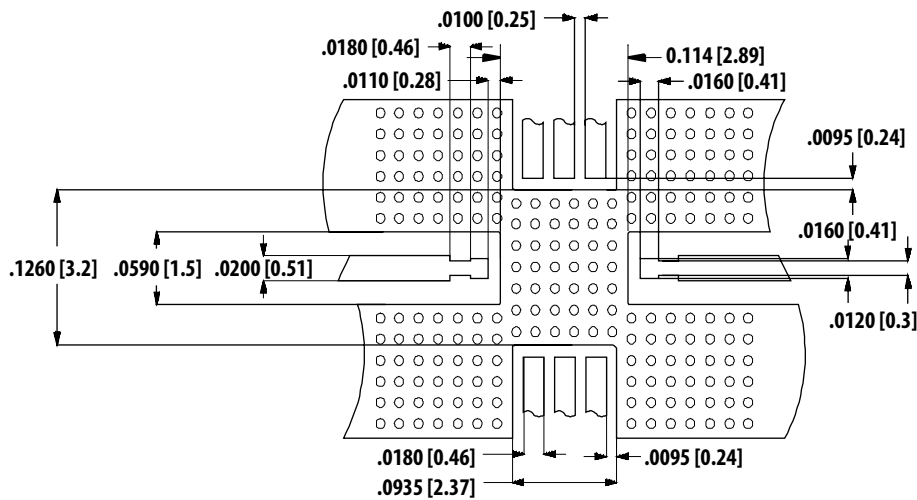


Figure 18. Recommended PCB Land Pattern for Rogers R04350, 0.010" thick.

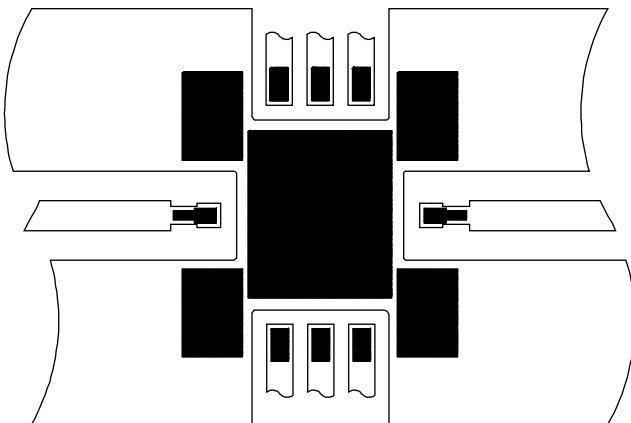
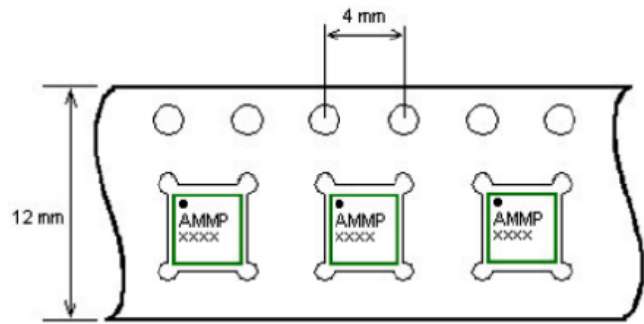


Figure 19. Combined PCB and Stencil Layouts

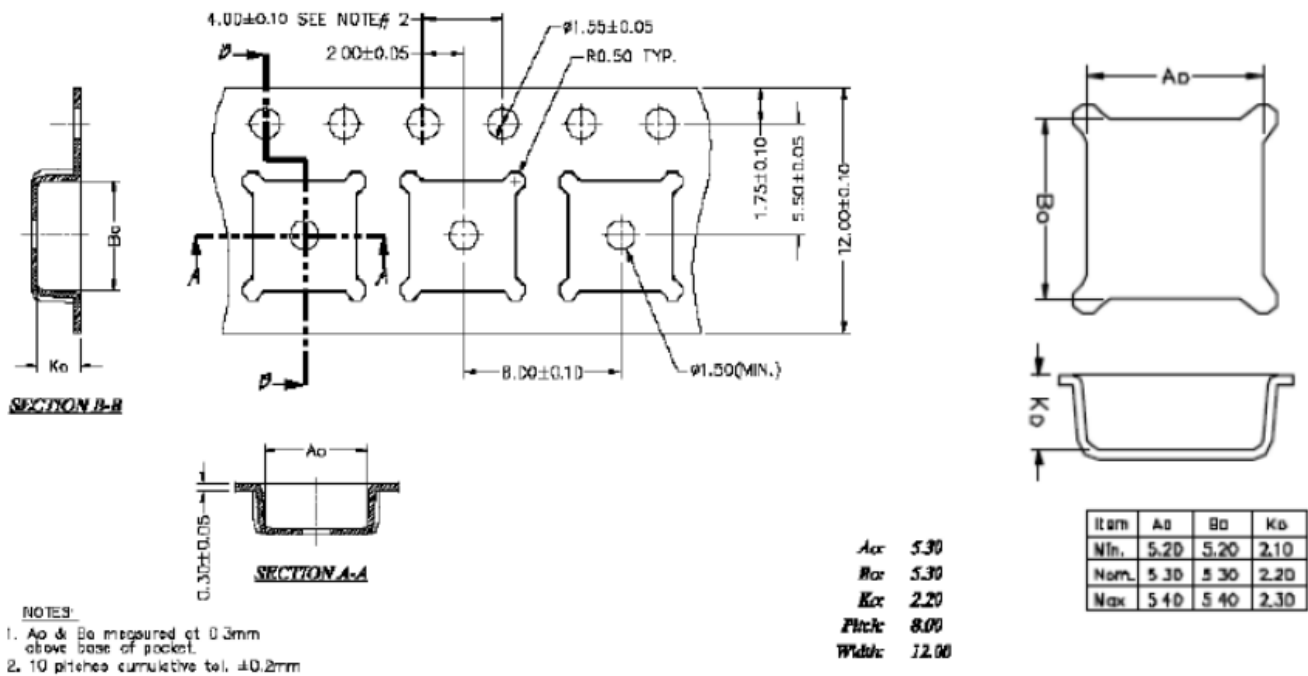
Ordering Information

Part Number	Devices Per Container	Container
AMMP-6650-BLKG	10	Antistatic bag
AMMP-6650-TR1G	100	7" Reel
AMMP-6650-TR2G	500	7" Reel

Device Orientation (Top View)



Carrier Tape and Pocket Dimensions



For product information and a complete list of distributors, please go to our web site: www.avagotech.com

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