

FEATURES

Divide-by-4 prescaler

High frequency operation: 4 GHz to 18 GHz

Integrated RF decoupling capacitors

Low power consumption

Active mode: 26 mA

Power-down mode: 7 mA

Low phase noise: -150 dBc/Hz

Single dc supply: 3.3 V compatible with ADF4xxx PLLs

Temperature range: -40°C to $+105^{\circ}\text{C}$

Small package: 3 mm \times 3 mm LFCSP

APPLICATIONS

Point-to-point radios

VSAT radios

Communications test equipment

GENERAL DESCRIPTION

The ADF5001 prescaler is a low noise, low power, fixed RF divider block that can be used to divide down frequencies as high as 18 GHz to a lower frequency suitable for input into a PLL IC, such as the [ADF4156](#) or [ADF4106](#). The ADF5001 provides a divide-by-4 function. The ADF5001 operates off a 3.3 V supply and has differential 100 Ω RF outputs to allow direct interface to the differential RF inputs of PLLs such as the ADF4156 and ADF4106.

FUNCTIONAL BLOCK DIAGRAM

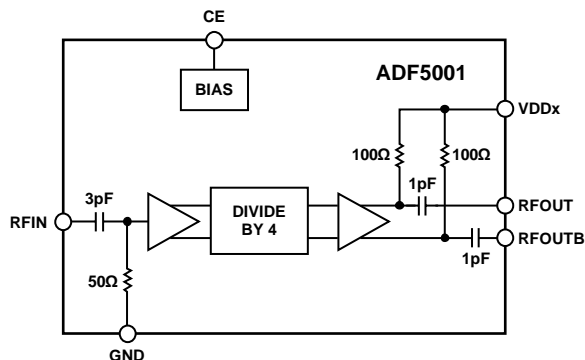


Figure 1.

08402-001

Rev. 0

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.

Tel: 781.329.4700

Fax: 781.461.3113

www.analog.com

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REVISION HISTORY

10/09—Revision 0: Initial Version

SPECIFICATIONS

VDD1 = VDD2 = 3.3 V \pm 10%, GND = 0 V; dBm referred to 50 Ω ; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Operating temperature range for the B version is –40°C to +105°C.

Table 1.

| Parameter | B Version ¹ | | | Unit | Test Conditions/Comments |
|--------------------------------------|------------------------|------|------|--------|---|
| | Min | Typ | Max | | |
| RF CHARACTERISTICS | | | | | |
| Maximum Input Frequency | | | 18 | GHz | 4 GHz to 18 GHz. Single-ended output connected into 50 Ω load. Differential outputs connected into 50 Ω load. Differential outputs connected into 100 Ω load. Input frequency (F _{IN}) = 12 GHz, offset = 100 kHz. RF input power (P _{IN}) = 0 dBm, RFOUT = 4 GHz. |
| Minimum Input Frequency | 4 | | | GHz | |
| RF Input Sensitivity | −10 | | +10 | dBm | |
| Output Power | −15 | −11 | | dBm | |
| | −12 | −8 | | dBm | |
| | | −5 | | dBm | |
| Phase Noise | | −150 | | dBc/Hz | |
| Reverse Leakage | | −60 | | dBm | |
| Second Harmonic Content | | −38 | | dBc | |
| Third Harmonic Content | | −12 | | dBc | |
| Fourth Harmonic Content | | −20 | | dBc | |
| Fifth Harmonic Content | | −19 | | dBc | |
| CE INPUT | | | | | |
| V _{IH} , Input High Voltage | 2.2 | | | V | |
| V _{IL} , Input Low Voltage | | | 0.3 | V | |
| POWER SUPPLIES | | | | | |
| Voltage Supply | 3.0 | 3.3 | 3.6 | V | CE is high. CE is low. |
| IDD (IDD1 + IDD2) | | | | | |
| Active | | 26 | 42 | mA | |
| Power-Down | | 7 | 12.5 | mA | |

¹ Operating temperature range for the B version is –40°C to +105°C.

ABSOLUTE MAXIMUM RATINGS


Table 2.

| Parameter | Rating |
|---------------------------------------|------------------|
| VDDx to GND | −0.3 V to +3.9 V |
| RFIN | 10 dBm |
| Operating Temperature Range | |
| Industrial (B Version) | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Maximum Junction Temperature | 150°C |
| LFCSP θ_{JA} Thermal Impedance | 27.3°C/W |
| Peak Temperature | 260°C |
| Time at Peak Temperature | 40 sec |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

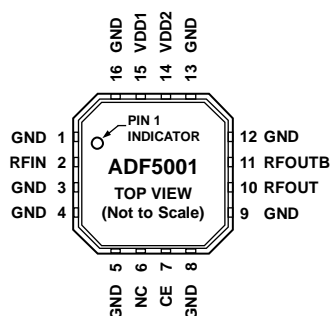
This device is a high performance RF integrated circuit with an ESD rating of 2 kV, human body model (HBM) and is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. NC = NO CONNECT.
2. THE EXPOSED PADDLE MUST BE CONNECTED TO GND.

08402-002

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|------------------------------|----------|---|
| 1, 3, 4, 5, 8, 9, 12, 13, 16 | GND | RF Ground. All ground pins should be tied together. |
| 2 | RFIN | Single-Ended 50 Ω Input to the RF Prescaler. This pin is ac-coupled internally via a 3 pF capacitor. |
| 6 | NC | No Connect. This pin can be left unconnected. |
| 7 | CE | Chip Enable. This pin is active high. When CE is brought low, the part enters into power-down mode. If this functionality is not required, the pin can be left unconnected because it will be pulled up internally through a weak pull-up resistor. |
| 10 | RFOUT | Divided Down Output of the Prescaler. This pin has an internal 100 Ω load resistor tied to VDD2 and an ac-coupling capacitor of 1 pF. |
| 11 | RFOUTB | Complementary Divided Down Output of the Prescaler. This pin has an internal 100 Ω load resistor tied to VDD2 and an ac-coupling capacitor of 1 pF. |
| 14 | VDD2 | Voltage Supply for the Output Stage. This pin should be decoupled to ground with a 1 nF capacitor and can be tied directly to VDD1. |
| 15 | VDD1 | Voltage Supply for the Input Stage and Divider Block. This pin should be decoupled to ground with a 1 nF capacitor. |
| | EPAD | The LFCSP package has an exposed paddle that must be connected to GND. |

TYPICAL PERFORMANCE CHARACTERISTICS

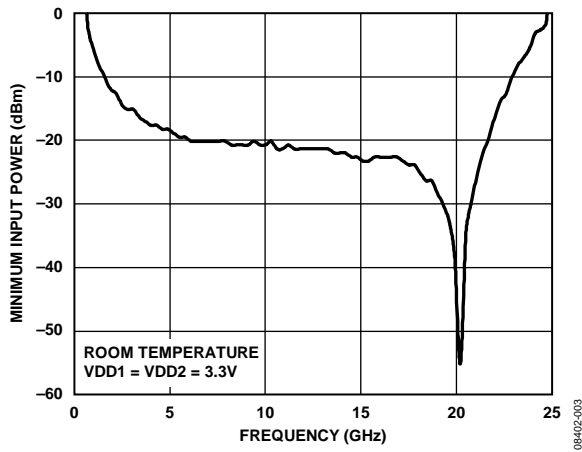


Figure 3. RF Input Sensitivity

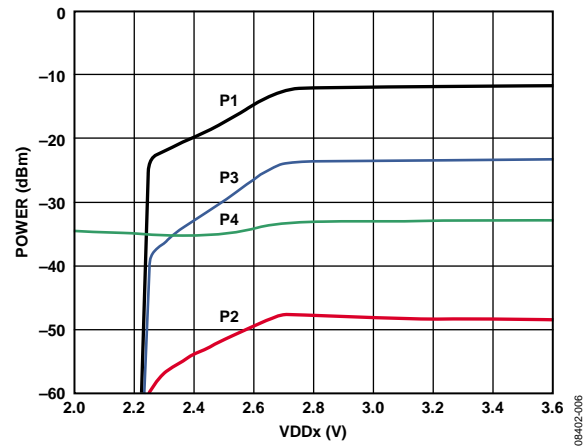


Figure 6. RF Output Harmonic Content

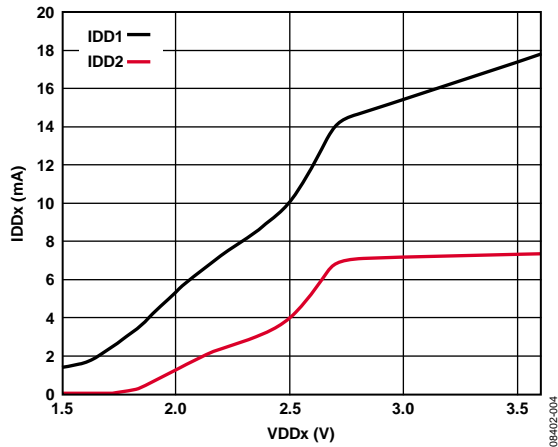


Figure 4. $IDD1$ and $IDD2$ vs. $VDDx$

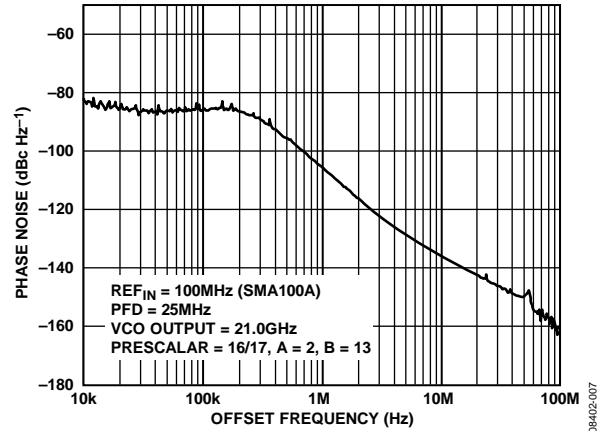


Figure 7. Phase Noise Plot of 20 GHz PLL Output Using the ADF5001 Prescaler and ADF4106 Synthesizer ICs

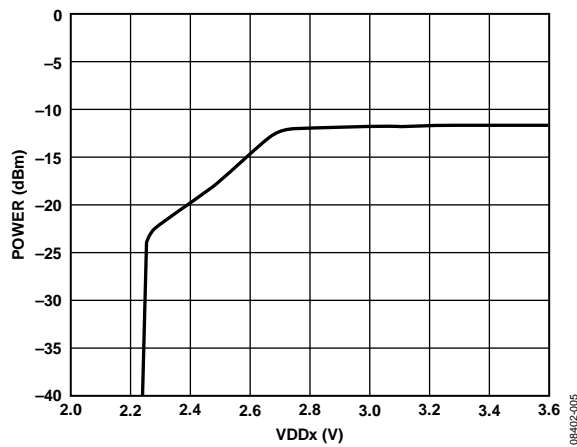


Figure 5. RF Output Power (Single-Ended) vs. $VDDx$

EVALUATION BOARD PCB

The evaluation board has four connectors as shown in Figure 8. The RF input connector (J4) is a 2.92 mm precision connector from Rosenberger. This connector is mechanically compatible with SMA/3.5 mm cables, although it is recommended to use a 2.92 mm cable when connecting the board to measurement equipment or to another RF evaluation board to avoid accidental damage to the connector.

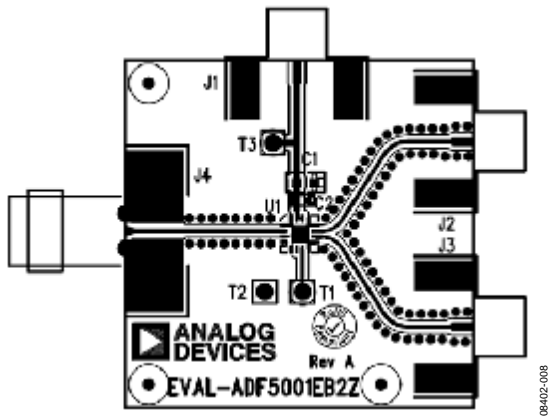


Figure 8. Evaluation Board Silkscreen—Top View

The evaluation board is powered from a single 3.0 V to 3.6 V supply, which should be connected to the J1 SMA connector. The power supply can also be connected using the T3 (VDDx) and T2 (GND) test points.

The differential RF outputs are brought out on the J2 and J3 SMA connectors. If only one of the outputs is being used, the unused output should be correctly terminated using a 50 Ω SMA termination.

The chip enable (CE) pin can be controlled using the T1 test point. If this function is not required, the test point can be left unconnected.

PCB MATERIAL STACK-UP

The evaluation board is built using Rogers 4003C material (0.008 in.). RF track widths are 0.015 in. to achieve a controlled 50 Ω characteristic impedance. The complete PCB stack-up is shown in Figure 9.

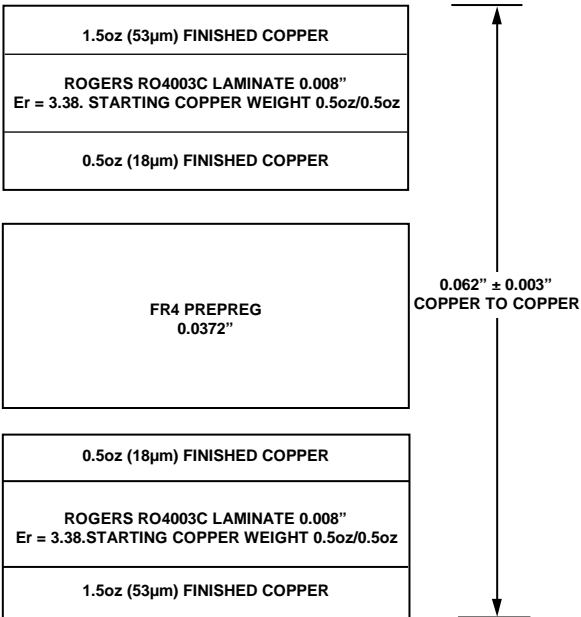


Figure 9. Evaluation Board PCB Layer Stack-Up

BILL OF MATERIALS

Table 4.

| Qty | Reference Designator | Description | Supplier/Part Number |
|-----|----------------------|-------------------------|-----------------------------------|
| 1 | C1 | 0.1 µF, 0603 capacitor | Murata GRM188R71H104KA93D |
| 1 | C2 | 10 pF, 0402 capacitor | Murata GRM1555C1H100JZ01D |
| 1 | J1 | 2.92 mm RF connector | Rosenberger 02K243-40ME3 |
| 3 | J2, J3, J4 | 3.5 mm RF SMA connector | Johnson Components 142-0701-851 |
| 3 | T1, T2, T3 | Testpoints | Vero 20-2137 |
| 1 | U1 | ADF5001 RF prescaler | Analog Devices, Inc., ADF5001BCPZ |

APPLICATION CIRCUIT

The ADF5001 can be connected either single-ended or differentially to any of the Analog Devices PLL family of ICs. It is recommended to use a differential connection for best performance and to achieve maximum power transfer. The application circuit shown in Figure 10 shows the ADF5001 used as the RF prescaler in a microwave 16 GHz PLL loop. The ADF5001 divides down the 16 GHz RF signal to 4 GHz, which is input differentially into the ADF4156 PLL. An active filter topology, using the OP184 op amp, is used to provide the wide tuning ranges

typically required by microwave VCOs. The positive input pin of the OP184 is biased at half the ADF4156 charge pump supply (VP). This can be easily achieved using a simple resistor divider, ensuring sufficient decoupling close to the +IN A pin of the OP184. This then allows the use of a single positive supply for the op amp. Alternatively, to optimize performance by ensuring a clean bias voltage, a low noise regulator like the ADP150 can be used to power the resistor divider network or the +IN A pin directly.

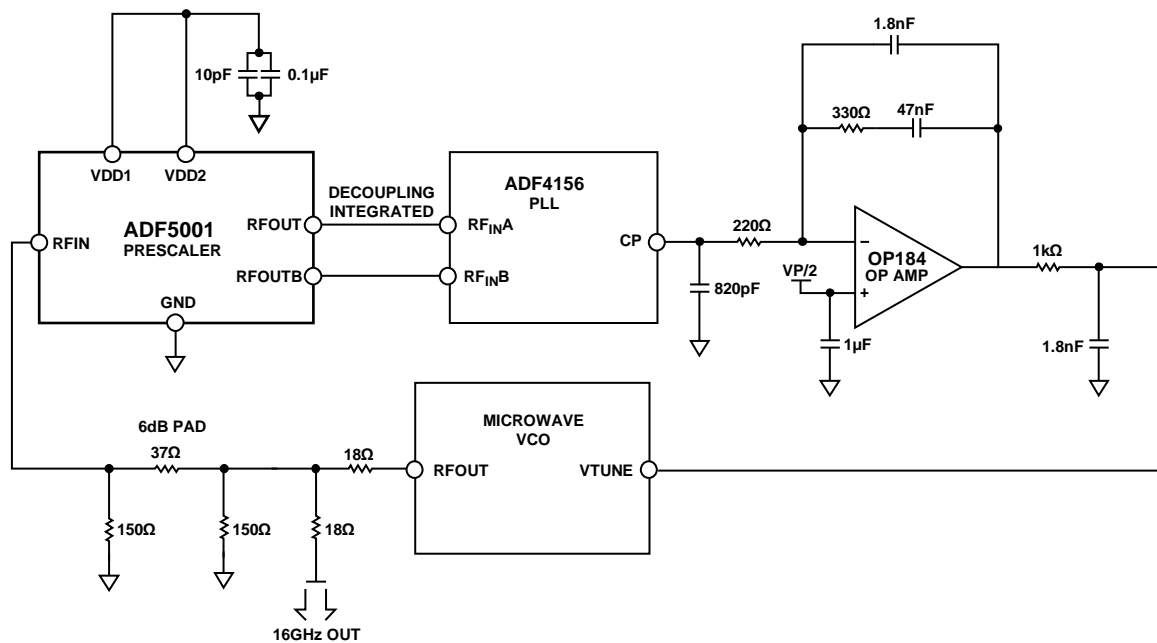
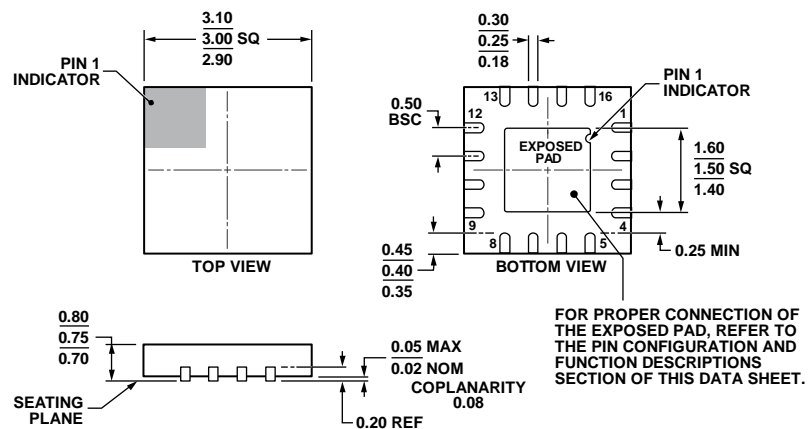


Figure 10. ADF5001 Used as the RF Prescaler in a Microwave 16 GHz PLL Loop

09402-010

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 11. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
(CP-16-18)

Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|-------------------------------|-------------------|--|----------------|
| ADF5001BCPZ ¹ | −40°C to +105°C | 16-Lead Lead Frame Chip Scale Package (LFCSP_WQ) | CP-16-18 |
| ADF5001BCPZ-RL7 ¹ | −40°C to +105°C | 16-Lead Lead Frame Chip Scale Package (LFCSP_WQ), 7" Tape & Reel | CP-16-18 |
| EVAL-ADF5001EB2Z ¹ | | Evaluation Board | |

¹ Z = RoHS Compliant Part.

ADF5001

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ADF5001

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