Ordering number: EN 4945

Monolithic Digital IC

SANYO No. 4945

LB1893

3-Phase Brushless Motor Driver for CD-ROM Spindle Motors

Overview

The LB1893 is a 3-phase brushless motor driver for use in CD-ROM spindle motors.

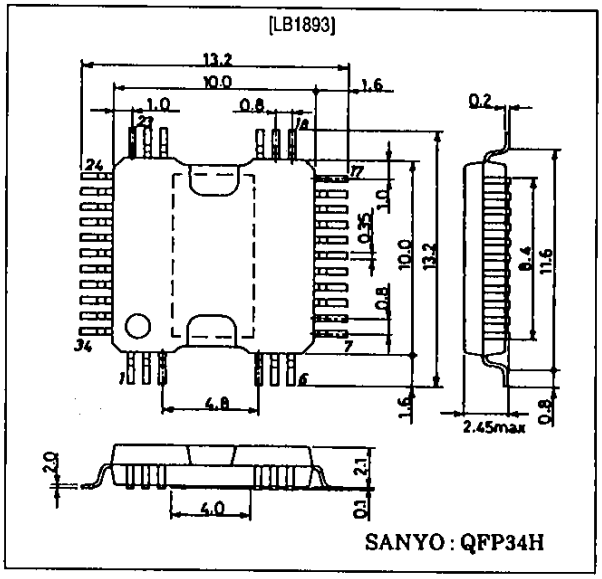
Functions and Features

- 120° voltage linear type
- V-type control voltage
- Switchable control gain
- Control, non-feedback, and speed increment/decrement control pin built-in
- Start/Stop pin built-in
- Hall device bias built-in

Package Dimensions

Unit: mm

3206-QFP34H



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}1$ max		20	V
	$V_{CC}2$ max		7.0	V
Output transistor blocking voltage	$V_{O(sus)}$	I_{OUT} = 20mA, design value	20	V
Output supply voltage	$V_{OU, V, W}$		20	V
Output current	I_{OUT}		1.2	A
Allowable power dissipation	Pd max	Unmounted IC	0.77	W
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}1$		5 to 18	V
	$V_{CC}2$	$V_{CC}1 \geq V_{CC}2$	4.3 to 6.5	V
V_{Cref} pin input voltage	V_{Cref}		$V_{CC}2/2 \pm 1.0$	V
V_{NS} pin input voltage	V_{NS}		0 to $V_{CC}2/2 - 1.0$	V

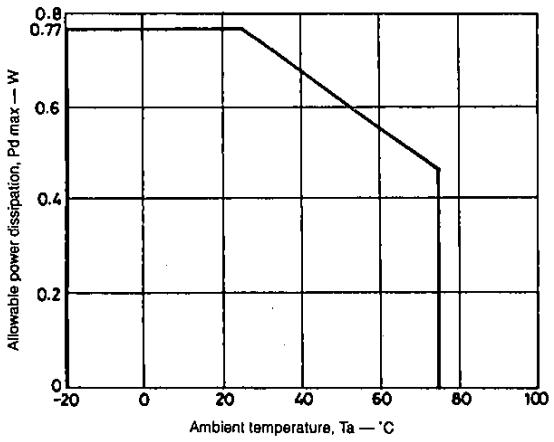
Electrical Characteristics at Ta = 25°C, $V_{CC}1$ = 12V, $V_{CC}2$ = 5V, specified test circuit

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 1	$I_{CC}1$	V_C = open, V_{Cref} = open, R_L = ∞, $V_{S/S}$ = 5V	–	17	30	mA
Supply current 2	$I_{CC}2$	V_C = open, V_{Cref} = open	–	7.5	10.5	mA
Supply current 3	$I_{CC}3$	V_C = open, V_{Cref} = open, R_L = ∞, $V_{S/S}$ = 0V	–	0.9	3	mA
Output saturation voltage	$V_{O(sat)}1$	I_{OUT} = 0.4A, sink + source	–	1.6	2.2	V
	$V_{O(sat)}2$	I_{OUT} = 0.8A, sink + source	–	2.0	3.0	V
Output center voltage	V_{OQ}	V_C = 2.5V, V_{Cref} = 2.5V	5.7	6.0	6.3	V
Hall amplifier input offset voltage	$V_{H\ offset}$		–5	–	+5	mV
Hall amplifier input bias current	$I_{H\ bias}$		–	1	5	μA
Hall amplifier common-mode input voltage range	V_{Hch}		1.3	–	2.2	V
Hall amplifier input-output voltage gain	G_{VHO}		40	43	46	dB
Control-output drive gain 1	$G_{VCO}1$	RZ1 = RZ2, GC1 = LOW, GC2 = LOW	26	29	–	dB
Control-output channel difference 1	$\Delta G_{VCO}1$	RZ1 = RZ2, GC1 = LOW, GC2 = LOW	–1.5	–	+1.5	dB
Control-output drive gain 2	$G_{VCO}2$	RZ1 = RZ2, GC1 = LOW, GC2 = HIGH	32	35	–	dB
Control-output channel difference 2	$\Delta G_{VCO}2$	RZ1 = RZ2, GC1 = LOW, GC2 = HIGH	–1.9	–	+1.9	dB
Input dead-zone voltage	V_{DZ}	RZ1 = RZ2, GC1 = LOW, GC2 = LOW	±13	±38	±55	mV
Input bias current 1	$I_{B\ SERVO}$	V_C = 1.0V	–	–	500	nA
Input bias current 2	$I_{B\ NS}$	V_{NS} = 1.0V	–	–	500	nA

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
S/S pin HIGH-level voltage	$V_{S/S\,H}$	CMOS-level input. S/S pin threshold Vth = V_{CC}2/2	4.0	–	–	V
S/S pin LOW-level voltage	$V_{S/S\,L}$		–	–	1.0	V
Gain control 1 HIGH-level voltage	$V_{GC1\,H}$	CMOS-level input. GC1 pin threshold Vth = 2.0V	4.0	–	–	V
Gain control 1 LOW-level voltage	$V_{GC1\,L}$		–	–	1.0	V
Gain control 2 HIGH-level voltage	$V_{GC2\,H}$	CMOS-level input. GC2 pin threshold Vth = 2.0V	4.0	–	–	V
Gain control 2 LOW-level voltage	$V_{GC2\,L}$		–	–	1.0	V
S/S pin input current	$I_{S/S}$	5V input voltage	–	50	100	μA
Gain controls 1 and 2 current	I_{GC}	5V input voltage	–	53	110	μA
Motor output saturation voltage	$V_{(sat)HFG}$	I_O = –5mA	–	0.24	0.5	V
Motor output saturation blocking voltage	$V_{(sus)HFG}$	Design value	–	–	7	V
Hall bias voltage	$V_{H\pm}$	I_O = 5mA, R_H = 200Ω	0.7	0.97	1.2	V
CTRL pin HIGH-level voltage	$V_{CTRL\,H}$	CTRLϕ and CTRL1 common, CMOS-level input. CTRL pin threshold Vth = 2.5V	4.0	–	–	V
CTRL pin LOW-level voltage	$V_{CTRL\,L}$		–	–	1.0	V
CTRL input current	I_{CTRL}	5V input voltage	–	53	110	μA
Thermal shutdown operating temperature	TSD	Design value	150	180	210	°C
TSD hysteresis	ΔTSD	Design value	–	15	–	°C

Performance Characteristics

Pd max — Ta



Mode Switching Truth Table

CTRLϕ[1]	CTRL1[1]	Mode
LOW	LOW	Control
LOW	HIGH	Non-feedback
HIGH	LOW	Increment
HIGH	HIGH	Decrement

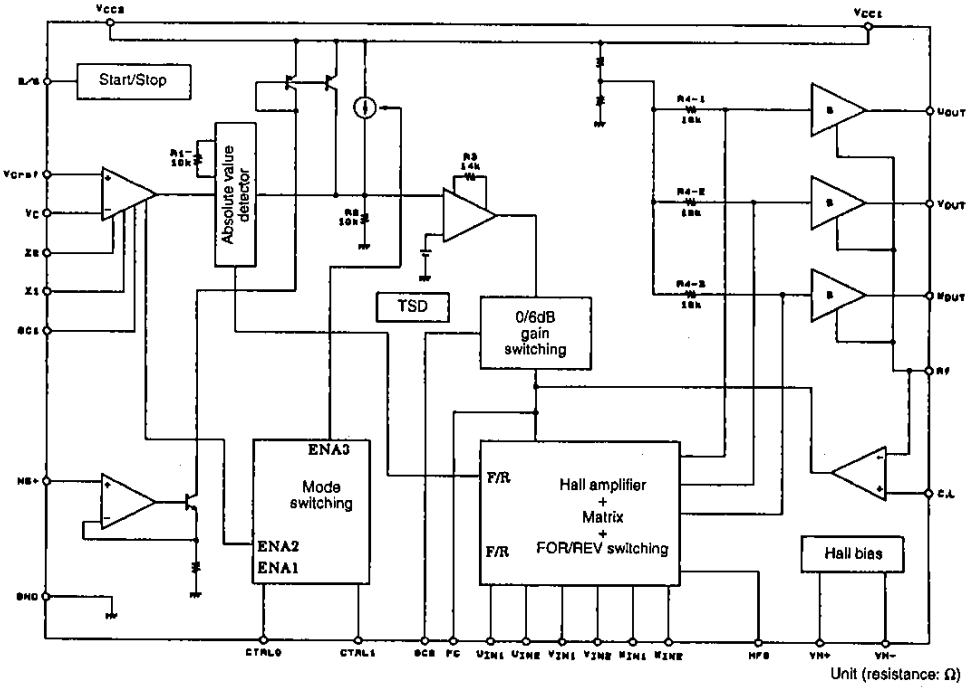
1. LOW = 0 to 1.0V, and HIGH ≥ 4.0V.

Hall Element Logic Truth Table

	Source → sink	Hall Input[1]			Forward/Reverse control[2]
		U_{IN}	V_{IN}	W_{IN}	
1	W phase → V phase	HIGH	HIGH	LOW	Forward
	V phase → W phase				Reverse
2	W phase → U phase	HIGH	LOW	LOW	Forward
	U phase → W phase				Reverse
3	V phase → W phase	LOW	LOW	HIGH	Forward
	W phase → V phase				Reverse
4	U phase → V phase	LOW	HIGH	LOW	Forward
	V phase → U phase				Reverse
5	V phase → U phase	HIGH	LOW	HIGH	Forward
	U phase → V phase				Reverse
6	U phase → W phase	LOW	HIGH	HIGH	Forward
	W phase → U phase				Reverse

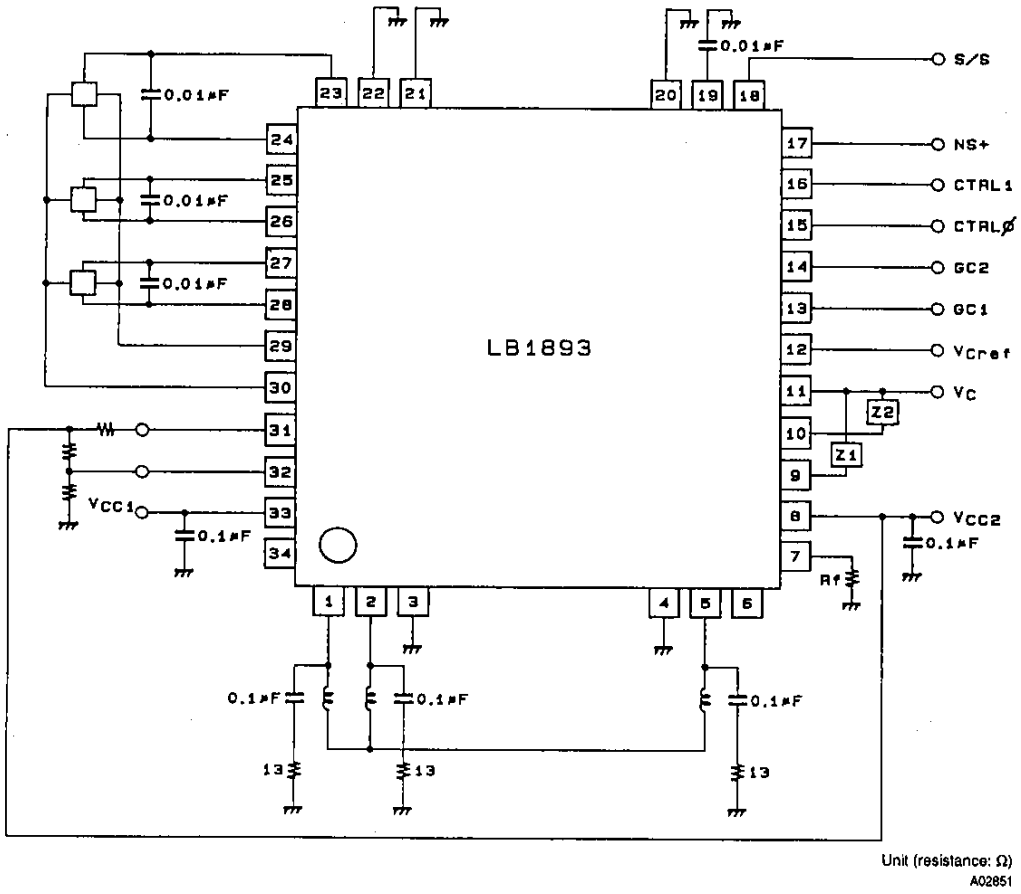
1. An input is considered to be HIGH when $U_{IN}1 > U_{IN}2$, $V_{IN}1 > V_{IN}2$, and $W_{IN}1 > W_{IN}2$ by 0.2V or more.
2. Forward is selected when $V_C > V_{Cref}$. Reverse is selected when $V_C < V_{Cref}$.

Block Diagram

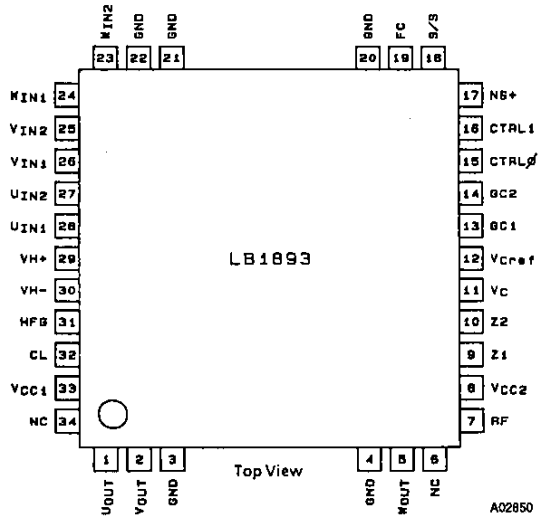


Unit (resistance: Ω)
A02849

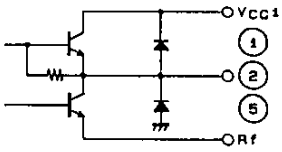
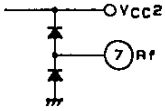
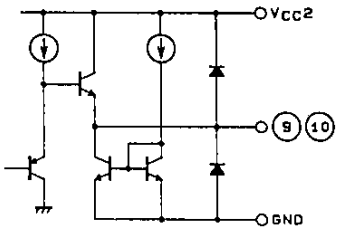
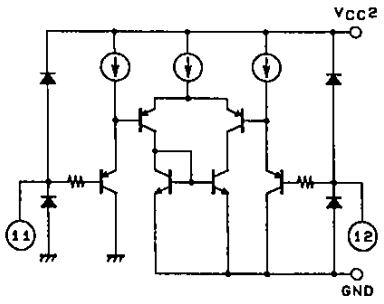
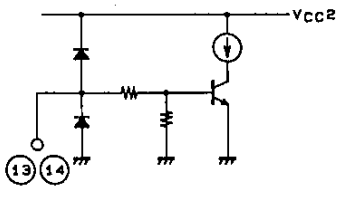
Sample Peripheral Circuit

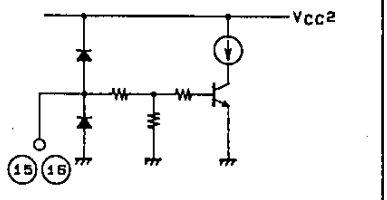
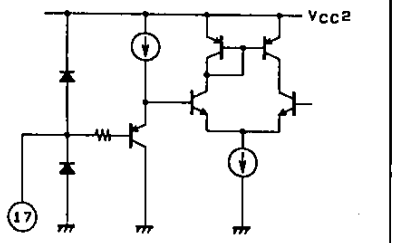
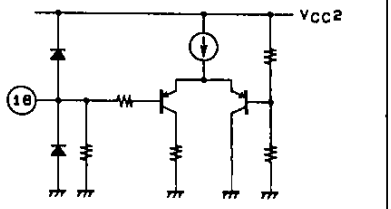
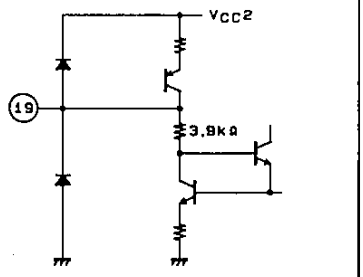
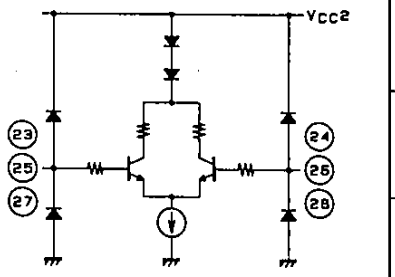
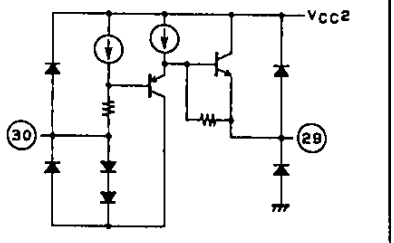


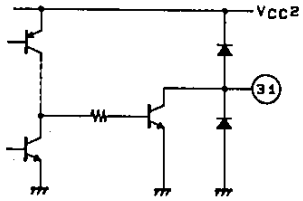
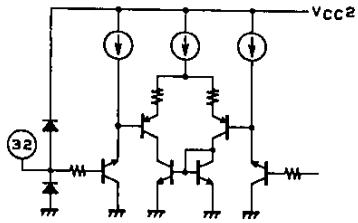
Pin Assignment



Pin Functions

Number	Name	Pin voltage	Equivalent circuit	Function
3, 4, 20, 21	Frame GND			Frame ground. Connected to the common ground.
22	GND			Ground pin
1 2 5	U_{OUT} V_{OUT} W_{OUT}		 A02852	Output pins. Connected to the motor.
7	Rf		 A02853	Output transistor ground. A resistor can be connected between this pin and GND to sense the output current as a voltage drop to provide for overcurrent protection.
6, 34	NC			No connection
8	$V_{CC}2$	4.3 to 6.5V		Supply for all circuits except the output stage. This supply should be kept stable to prevent noise from entering this pin.
9 10	Z1 Z2		 A02854	First-stage amplifier gain setting impedance connection. Z1 and Z2 should be in the order of 30kΩ to several hundred kΩ. The gain should be in the order of 6dB.
11 12	V_C V_{Cref}	$V_{CC}2/2 \pm 1.0$	 A02855	V_C is the speed control pin; forward when $V_C > V_{Cref}$ and reverse when $V_C < V_{Cref}$. The output voltage is controlled by the V_C voltage. V_{Cref} determines the motor control stop voltage, and is normally set to $V_{CC}2/2$.
13 14	GC1 GC2	0 to $V_{CC}2$	 A02856	Input gain control switching pin. GC1 switches the first-stage amplifier impedances Z1 and Z2. Z1 is selected when GC1 is LOW, and Z2 is selected when GC1 is HIGH. GC2 is the second-stage amplifier switching pin.

Number	Name	Pin voltage	Equivalent circuit	Function
15 16	CTRLϕ CTRL1	0 to $V_{CC}2$		Operating mode switch pin. The mode switching truth table shows how to select control, non-feedback, and speed increment/decrement modes.
17	NS+	0 to $V_{CC}2 - 1V$		Non-feedback mode input pin. Input-output gain is approximately 14dB (GC2 = LOW) Motor stops when V_{NS} = 0V.
18	S/S	0 to $V_{CC}2$		Start/Stop pin. Start when HIGH, and stop when LOW. The threshold is $V_{CC}2/2$.
19	FC			Connect a capacitor between this pin and ground to reduce the input-output gain frequency response and to prevent abnormal oscillation.
23 24	$W_{IN}2$ $W_{IN}1$	1.3 to 2.2V		W-phase Hall device input pins. Logic HIGH is represented by $W_{IN}1 > W_{IN}2$.
25 26	$V_{IN}2$ $V_{IN}1$			V-phase Hall device input pins. Logic HIGH is represented by $V_{IN}1 > V_{IN}2$.
27 28	$U_{IN}2$ $U_{IN}1$			U-phase Hall device input pins. Logic HIGH is represented by $U_{IN}1 > U_{IN}2$.
29 30	VH+ VH–	2.4V 1.4V		Hall device supply pins. The potential difference between VH+ and VH– is 1.0V.

Number	Name	Pin voltage	Equivalent circuit	Function
31	HFG	0 to $V_{CC}2$		Hall device FG pin. The Hall device waveform is converted to a pulse and used as the FG pulse.
32	CL	0 to $V_{CC}2$		When the voltage on Rf pin becomes equal to the voltage on CL, the current limiter operates. The CL voltage is determined externally.
33	$V_{CC}1$	5 to 18V		Output-stage supply pin. This supply should be kept stable to prevent noise from entering this pin.