Ordering number : EN7948

SANYO Semiconductors
DATA SHEET

Monolithic Digital IC

LB11695M — Direct PWM Drive Brushless Motor Predriver IC for Hot Water Heaters and Air Conditioners

Overview

The LB11695M is a direct PWM drive predriver IC designed for three-phase power brushless motors. A motor driver circuit with the desired output power (voltage and current) can be implemented by adding discrete transistors in the output circuits. This device is optimal for driving all types of large-scale motors such as those used in air conditioners and on-demand water heaters.

Functions and features

- Three-phase bipolar drive
- Direct PWM drive
- Built-in forward/reverse switching circuit
- Many protection circuits including current limiter circuit, undervoltage protection circuit, constraint protection circuit, and thermal protection circuit
- Supports control by command voltage or PWM duty input.
- Four types of Hall signal pulse outputs

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	$V_{CC}1$ max	$V_{CC}1$ pin	14.5	V
Maximum supply voltage 2	V15 max	V15 pin	20	V
Maximum output current	I_O max	UL, VL, WL, UH, VH, and WH pins	40	mA
RF pin applied voltage	VRF max		4	V
LVS pin applied voltage	VLVS max		20	V
TOC pin applied voltage	VTOC max		VREG	V
VCTL pin applied voltage	VCTL max		14.5	V
Allowable power dissipation	Pd max	Independent IC	0.9	W
Operating temperature	Topr		-20 to +100	°C
Storage temperature	Tstg		-55 to +150	°C

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D1306 SY IM B8-7320 No.7948-1/17

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1-1	$V_{CC}1$-1	$V_{CC}1$ pin	8 to 13.5	V
Supply voltage range 1-2	$V_{CC}1$-2	$V_{CC}1$ pin, when V_{CC} and VREG are shorted	4.5 to 5.5	V
Supply voltage range 2	V15	V15 pin	13.5 to 19	V
Output current	I_O	UL, VL, WL, UH, VH, and WH pins	30	mA
12 V constant voltage output current	I12REG		-50	mA
5 V constant voltage output current	IREG		-20	mA
HP pin applied voltage	VHP		0 to 13.5	V
HP pin output current	IHP		0 to 10	mA

Electrical Characteristics at Ta = 25°C, $V_{CC}1$ = 12 V, $V_{CC}2$ = VREG

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain 1	$I_{CC}1$			15	20	mA
Current drain 2	$I_{CC}2$	Stop mode		2.5	4	mA
[Output Block]						
Output voltage 1-1	V_{OUT}1-1	Low level, I_O = 400 µA		0.1	0.3	V
Output voltage 1-2	V_{OUT}1-2	Low level, I_O = 10 mA		0.8	1.1	V
Output voltage 2	$V_{OUT}2$	High level, I_O = -20 mA	V_{CC}1-1.1	V_{CC}1-0.9		V
Temperature coefficient 1-1	ΔV_{OUT}1-1	Design target value* Low level, I_O = 400 µA		0.2		mV/°C
Temperature coefficient 1-2	ΔV_{OUT}1-2	Design target value* Low level, I_O = 10 mA		-1.5		mV/°C
Temperature coefficient 2	$\Delta V_{OUT}2$	Design target value* High level, I_O = -20 mA		1.5		mV/°C
[12V Constant Voltage Output (12REG pin)]						
Output voltage	V12REG	V15=15V, I_O=-30mA	11.7	12.1	12.6	V
Line regulation	ΔV12REG1	V15=13.5 to 19V, I_O=-30mA		150	300	mV
Load regulation	ΔV12REG2	I_O=-5 to -45mA, V15=15V		100	200	mV
Temperature coefficient	ΔV12REG3	Design target value*		2		mV/°C
[5V Constant Voltage Output (VREG pin)]						
Output voltage	VREG		4.7	5.0	5.3	V
Line regulation	ΔVREG1	V_{CC}=8 to 13.5V		40	100	mV
Load regulation	ΔVREG2	I_O=-5 to -20mA		5	30	mV
Temperature coefficient	ΔVREG3	Design target value*		0		mV/°C
[Hall Amplifier Block]						
Input bias current	IHB(HA)		-2	-0.5		µA
Common-mode input voltage range 1	VICM1	When a Hall effect device is used	0.5		V_{CC}1-2.0	V
Common-mode input voltage range 2	VICM2	Single-sided input bias mode (when a Hall IC is used)	0		V_{CC}1	V
Hall Input Sensitivity			50			mVp-p
Hysteresis	ΔV_{IN}(HA)		20	30	50	mV
Input voltage low→high	VSLH(HA)		5	15	25	mV
Input voltage high→low	VSHL(HA)		-25	-15	-5	mV
[VCTL Pin]						
Input voltage 1	VCTL1	Output duty: 0%	1.60	2.10	2.55	V
Input voltage 2	VCTL2	Output duty: 80%	4.05	4.75	5.60	V
Maximum output duty	HDUTY	VCTL=6.5V,fPWM=15kHz to 50kHz	85		96	%
Input bias current 1	IB1(CTL)	VCTL=0V	-95	-70		µA
Input bias current 2	IB2(CTL)	VCTL=6.5V		100	135	µA

*: Design target value and no measurement was made.

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[PWM Oscillator (PWM pin)]						
High-level output voltage	V_{OH}(PWM)		2.75	3.0	3.25	V
Low-level output voltage	V_{OL}(PWM)		1.0	1.2	1.3	V
External capacitor charge current	ICHG	VPWM=2.1V	-60	-45	-30	μA
Oscillator frequency	f(PWM)	C=1000pF	17.6	22	26.8	kHz
Amplitude	V(PWM)		1.6	1.8	2.1	Vp-p
[TOC pin]						
Clamp voltage	VCL(TOC)	VCTL=6.5V	1.09	1.24	1.39	V
[HP pin]						
Output saturation voltage	VHPL	I_O=7mA		0.15	0.5	V
Output leakage current	IHPleak	V_O=13.5V			10	μA
[CSD Oscillator (CSD pin)]						
High-level output voltage	V_{OH}(CSD)		3.2	3.6	4.0	V
Low-level output voltage	V_{OL}(CSD)		0.9	1.1	1.3	V
External capacitor charge current	ICHG1		-14	-10	-6	μA
External capacitor discharge current	ICHG2		7	11	15	μA
Oscillator frequency	f(CSD)	C=0.01μF		200		Hz
Amplitude	V(CSD)		2.2	2.5	2.75	Vp-p
[Current Limiter Circuit (RF pin)]						
Limiter voltage	VRF		0.45	0.5	0.55	V
[Undervoltage Protection Circuit (LVS pin)]						
Operating voltage	VSDL		3.6	3.8	4.0	V
Release voltage	VSDH		4.1	4.3	4.5	V
Hysteresis	ΔVSD		0.35	0.5	0.65	V
[Thermal Shutdown Operation (Thermal Protection Circuit)]						
Thermal shutdown operation temperature	TTSD	Design target value* (junction temperature)	125	145	165	°C
Hysteresis	ΔTSD	Design target value* (junction temperature)	20	25	30	°C
[PWMIN Pin]						
Input frequency	f(PI)				50	kHz
High-level input voltage	V_{IH}(PI)		2.0		VREG	V
Low-level input voltage	V_{IL}(PI)		0		1.0	V
Input open voltage	VIO(PI)		VREG-0.5		VREG	V
Hysteresis	VIS(PI)		0.2	0.3	0.4	V
High-level input current	I_{IH}(PI)	VPWMIN=VREG	-10	0	10	μA
Low-level input current	I_{IL}(PI)	VPWMIN=0V	-130	-96		μA
[S/S Pin]						
High-level input voltage	V_{IH}(SS)		2.0		VREG	V
Low-level input voltage	V_{IL}(SS)		0		1.0	V
Input open voltage	VIO(SS)		VREG-0.5		VREG	V
Hysteresis	VIS(SS)		0.2	0.3	0.4	V
High-level input current	I_{IH}(SS)	VS/S=VREG	-10	0	10	μA
Low-level input current	I_{IL}(SS)	VS/S=0V	-130	-96		μA

*: Design target value and no measurement was made.

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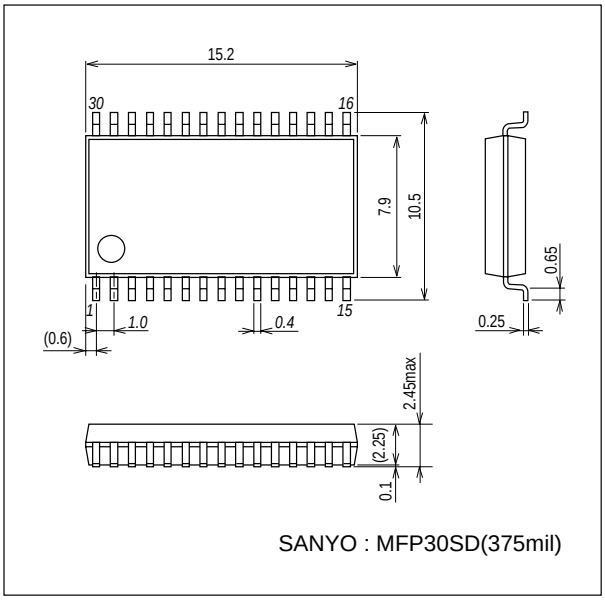
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[F/R Pin]						
High-level input voltage	V_{IH}(FR)		2.0		VREG	V
Low-level input voltage	V_{IL}(FR)		0		1.0	V
Input open voltage	VIO(FR)		VREG-0.5		VREG	V
Hysteresis	VIS(FR)		0.2	0.3	0.4	V
High-level input current	I_{IH}(FR)	VF/R=VREG	-10	0	10	μA
Low-level input current	I_{IL}(FR)	VF/R=0V	-130	-96		μA
[N1 Pin]						
High-level input voltage	V_{IH}(N1)		2.0		VREG	V
Low-level input voltage	V_{IL}(N1)		0		1.0	V
Input open voltage	VIO(N1)		VREG-0.5		VREG	V
High-level input current	I_{IH}(N1)	VN1=VREG	-10	0	10	μA
Low-level input current	I_{IL}(N1)	VN1=0V	-130	-96		μA
[N2 Pin]						
High-level input voltage	V_{IH}(N2)		2.0		VREG	V
Low-level input voltage	V_{IL}(N2)		0		1.0	V
Input open voltage	VIO(N2)		VREG-0.5		VREG	V
High-level input current	I_{IH}(N2)	VN2=VREG	-10	0	10	μA
Low-level input current	I_{IL}(N2)	VN2=0V	-130	-96		μA

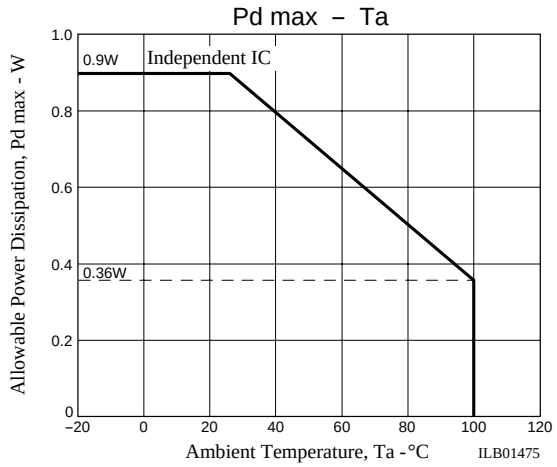
Package Dimensions

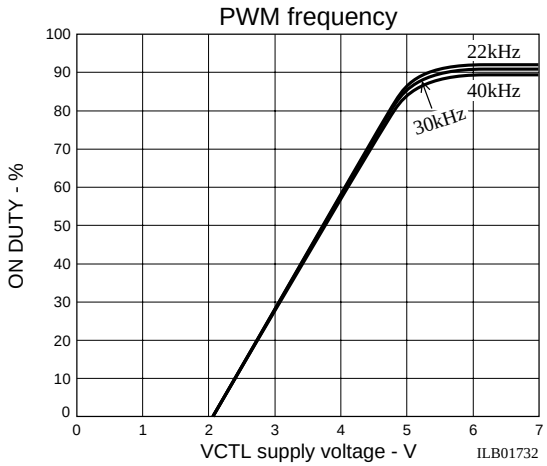
unit : mm (typ)

3073C



SANYO : MFP30SD(375mil)





Three-Phase Logic Truth Table ("IN = 'H'" indicates the state where IN+ > IN-.)

	F/R="L"			F/R="H"			Output	
	IN1	IN2	IN3	IN1	IN2	IN3	PWM	-
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

S/S Pin

Input state	State
H or open	Stop
L	Start

PWMIN Pin

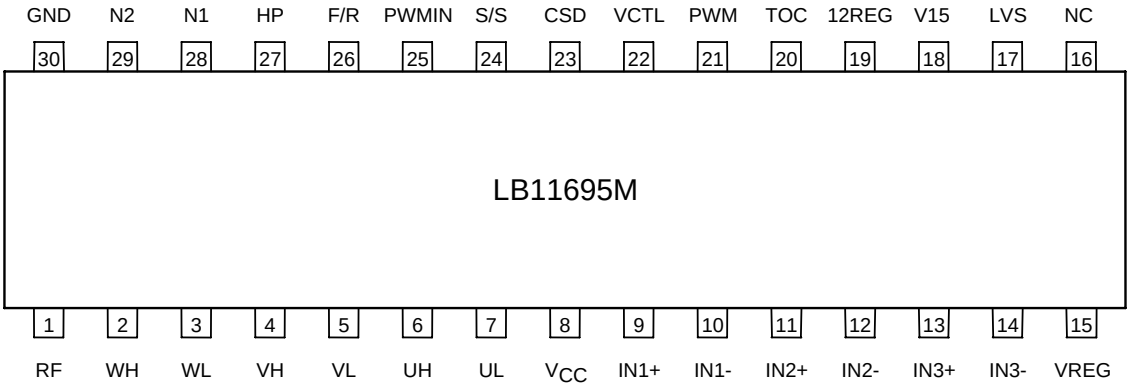
Input state	State
H or open	Output off
L	Output on

N1 and N2 Pins

Input state		HP output
N1 pin	N2 pin	
L	L	Single Hall sensor period divided by 2
L	High or open	Single Hall sensor period
High or open	L	Three Hall sensor synthesized period divided by 2
High or open	High or open	Three Hall sensor synthesized period

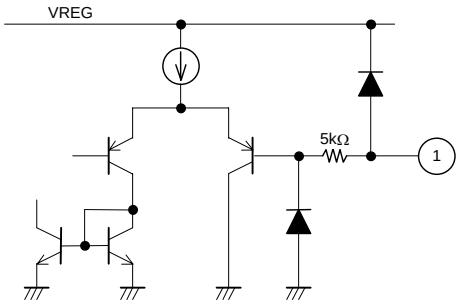
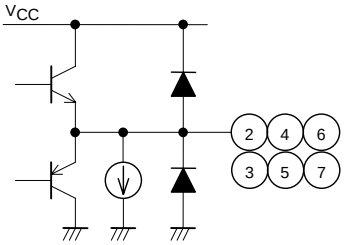
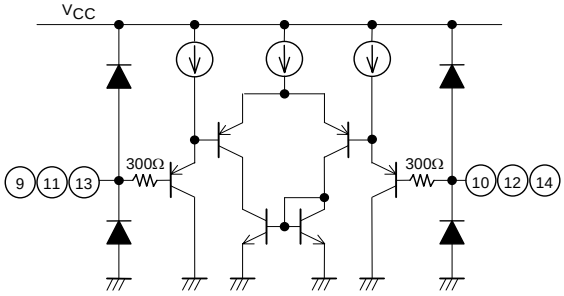
If either the S/S or PWMIN pins are not to be used, the unused pin input must be set to the low-level voltage.
The HP output can be selected (by the N1 and N2 settings) to be one of the following four functions: the IN1 Hall input converted to a pulse output (one-Hall output), the one-Hall output divided by two or the three-phase output synthesized from the Hall inputs (three-Hall synthesized output).

Pin Assignment



Top view

Pin Functions

Pin No.	Symbol	Equivalent Circuit	Pin Description
1	RF		Output current detection Connect a resistor with a small value between this pin and ground. Maximum output current must be set such that I_{OUT} = 0.5/Rf.
2 4 6 3 5 7	WH VH UH WL VL UL		Outputs (external transistor drive outputs) The duty control applies to the UH, VH, and WH pins.
8	V_{CC}		Power supply (for output, Hall input, and other blocks). Normally used as 12V power source. Must be connected to VREG for 5V single-source applications. Connect a capacitor between this pin and ground for stabilization.
9 10 11 12 13 14	IN1+ IN1- IN2+ IN2- IN3+ IN3-		Hall sensor inputs A high-level state is recognized when IN+ > IN-, and a low-level state is recognized under the reverse condition. If noise on the Hall sensor signals becomes a problem, insert capacitors between the IN+ and IN- inputs.

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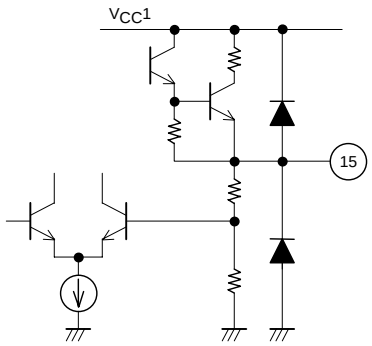
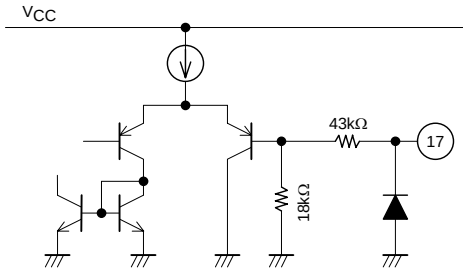
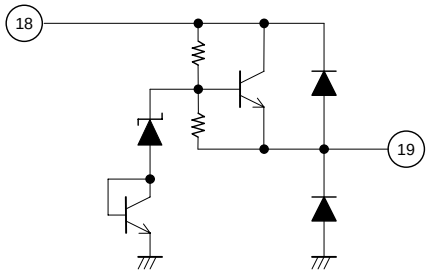
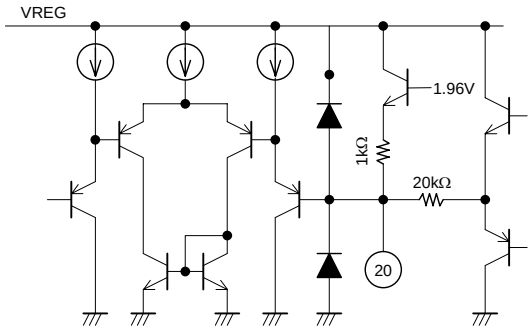
Pin No.	Symbol	Equivalent Circuit	Pin Description
15	VREG		Stabilized power supply output (5V output) Insert a capacitor (about 0.1µF) between this pin and ground for stabilization.
16	NC		NC pin. Available for wiring convenience.
17	LVS		Undervoltage protection voltage detection If a 5V or higher supply voltage is to be detected, set the detection voltage by inserting an appropriate zener diode in series.
18 19	V15 12REG		Power pin (V15) used for applications requiring 12V or higher voltages. 12V appears at the 12REG pin. Connect this pin to VCC when the 12REG pin is to be used. When the 12REG pin is not to be used, both V15 and 12REG pins must be held open or connected to ground for stabilization.
20	TOC		PWM waveform comparison Normally held open.

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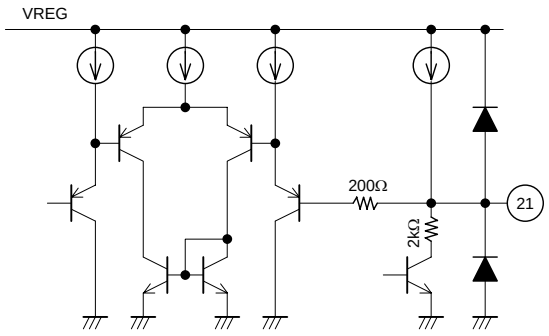
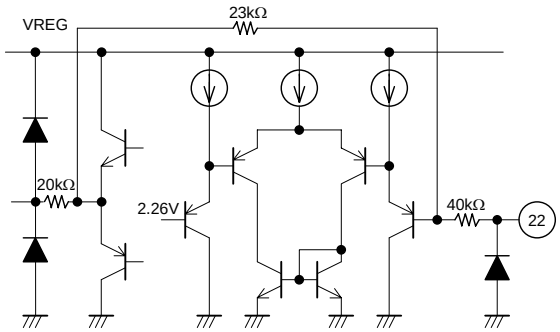
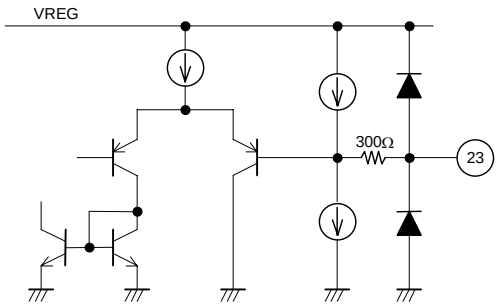
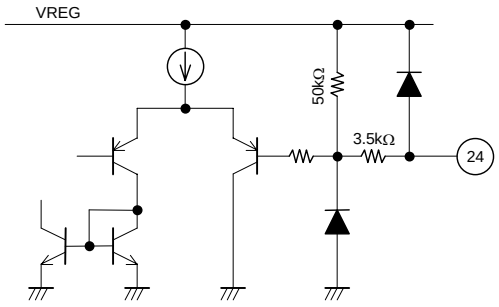
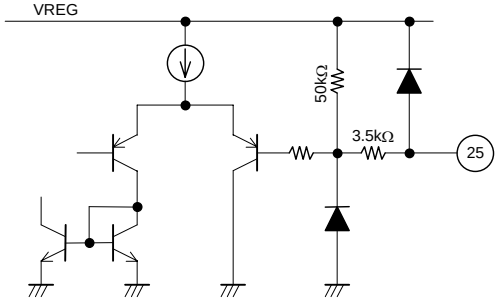
Pin No.	Symbol	Equivalent Circuit	Pin Description
21	PWM		PWM oscillator frequency setting Insert a capacitor between this pin and ground.
22	VCTL		Control voltage input. The PWMIN pin must be set low when this pin is to be used for voltage control.
23	CSD		Shared function pin: Constraint protection circuit operating time setting and initial reset pulse setting. Insert a capacitor between this pin and ground. When the protection circuit is not to be used, connect a resistor (150kΩ) and a capacitor (4700pF) in parallel between this pin and ground.
24	S/S		Start/Stop control A low-level input sets the IC to start mode, and a high level input sets it to stop mode.
25	PWM IN		PWM pulse input A low-level input specifies the output drive state, and a high-level or open input specifies the output off state. When using this pin for output control, connect the VCTL pin to the VREG pin and insert a 2kΩ resistor between the TOC pin and ground.

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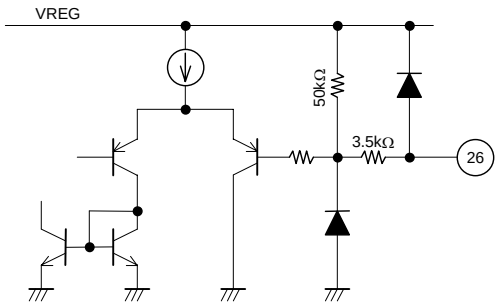
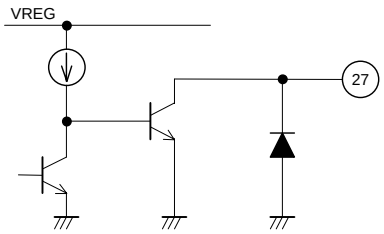
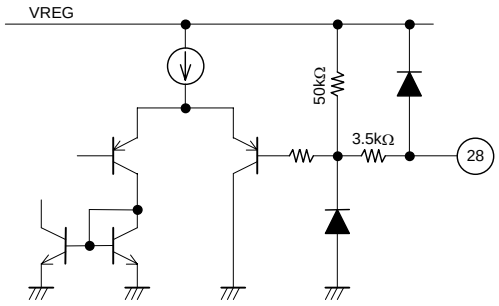
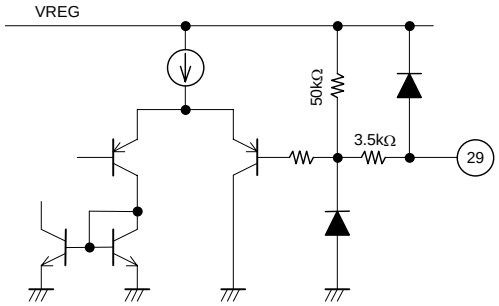
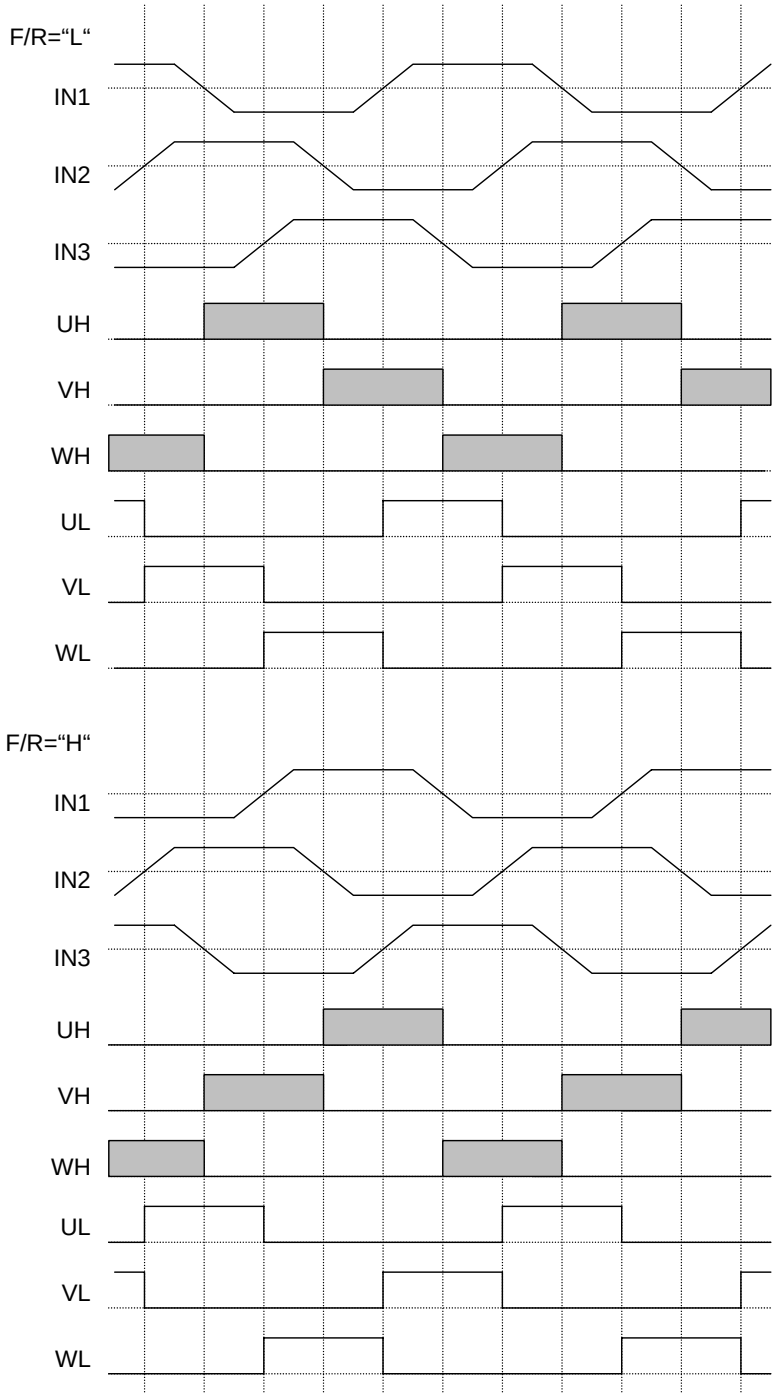
Pin No.	Symbol	Equivalent Circuit	Pin Description
26	F/R		Forward/Reverse direction input
27	HP		Hall signal output
28	N1		Hall signal output (HP signal) selector
29	N2		Hall signal output (HP signal) selector
30	GND		Ground pin.

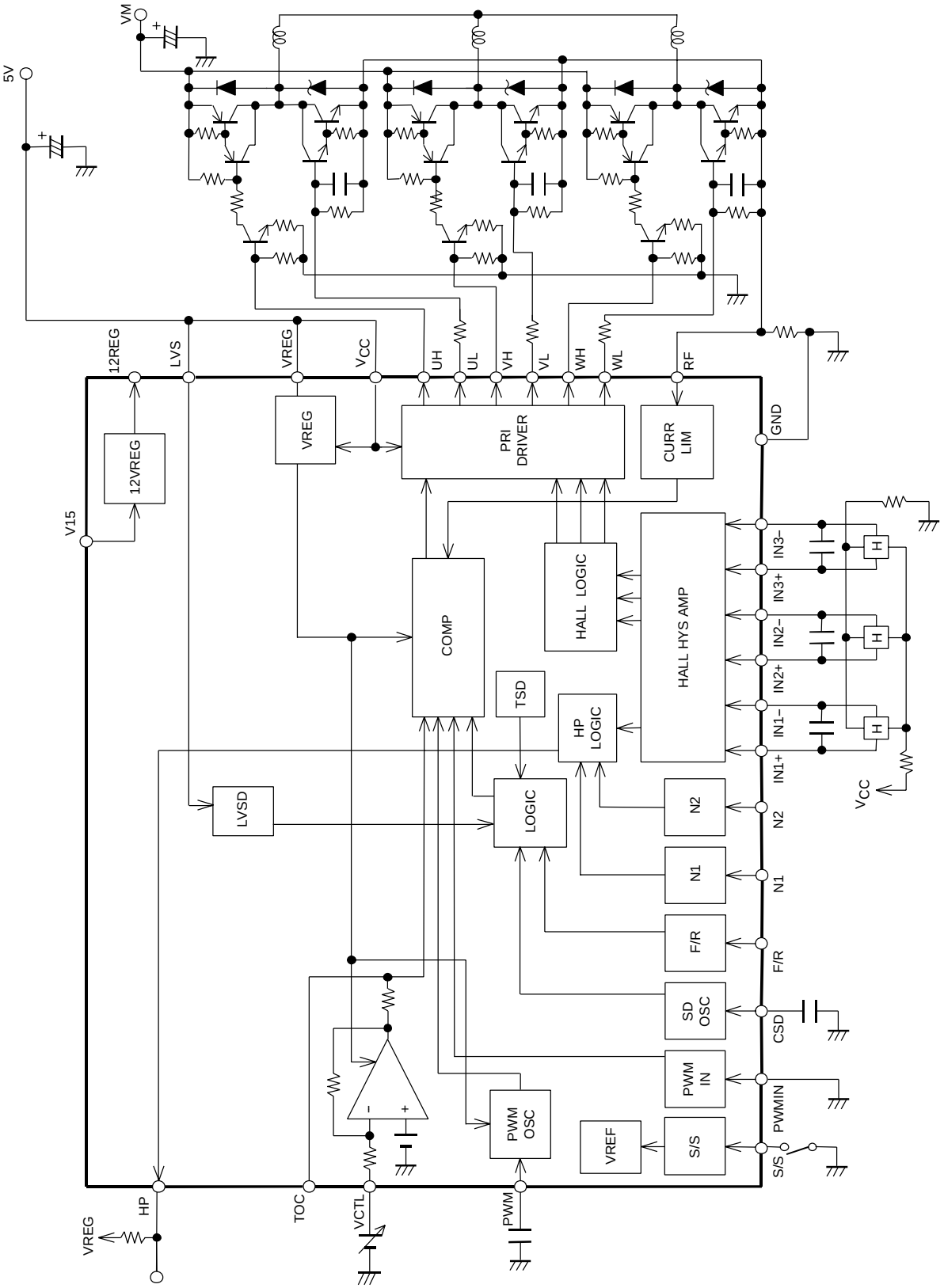
Hall Sensor Signal Input/Output Timing Chart



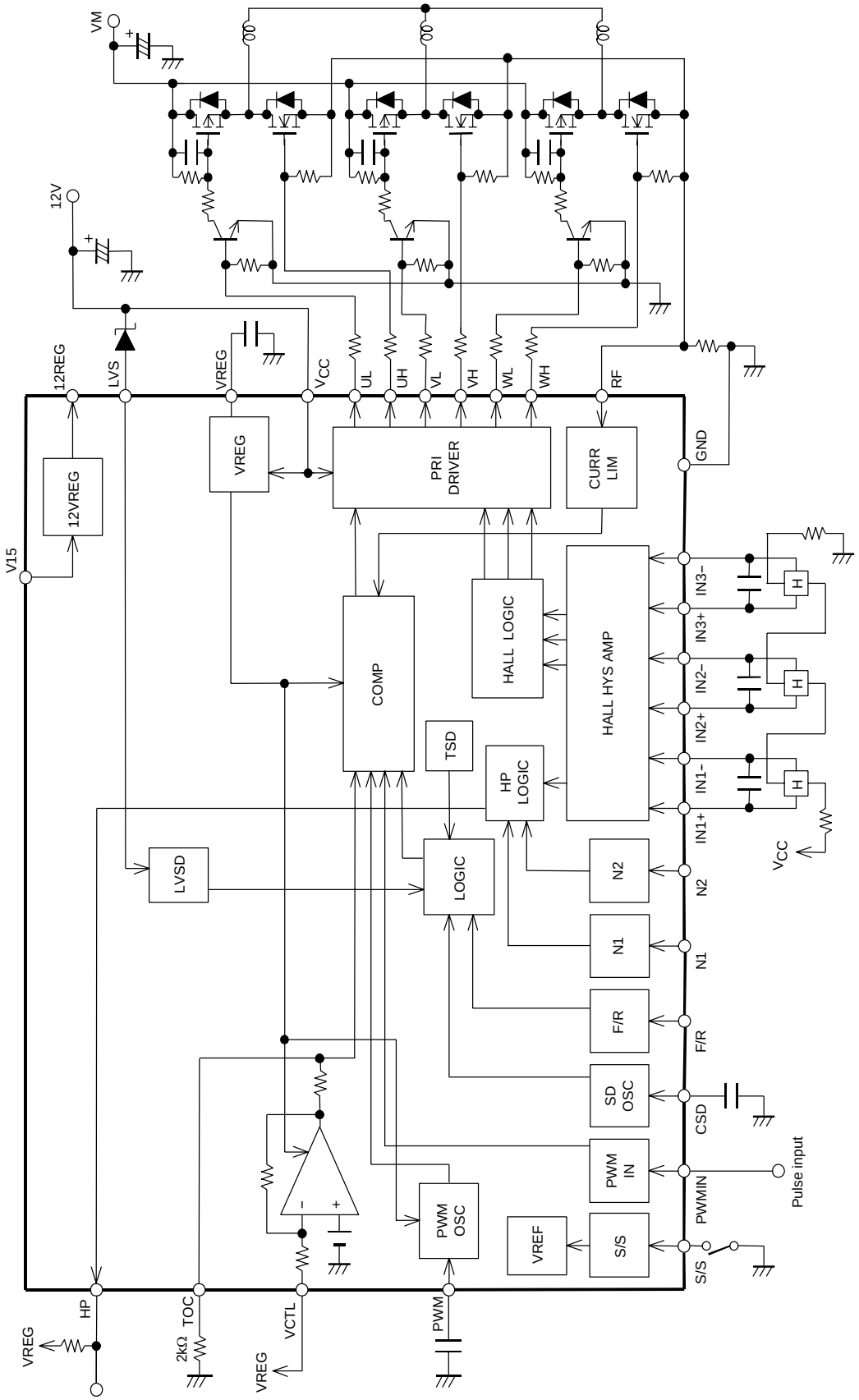
Areas shown in grey ( ) indicates PWM output.

Application Circuit Examples

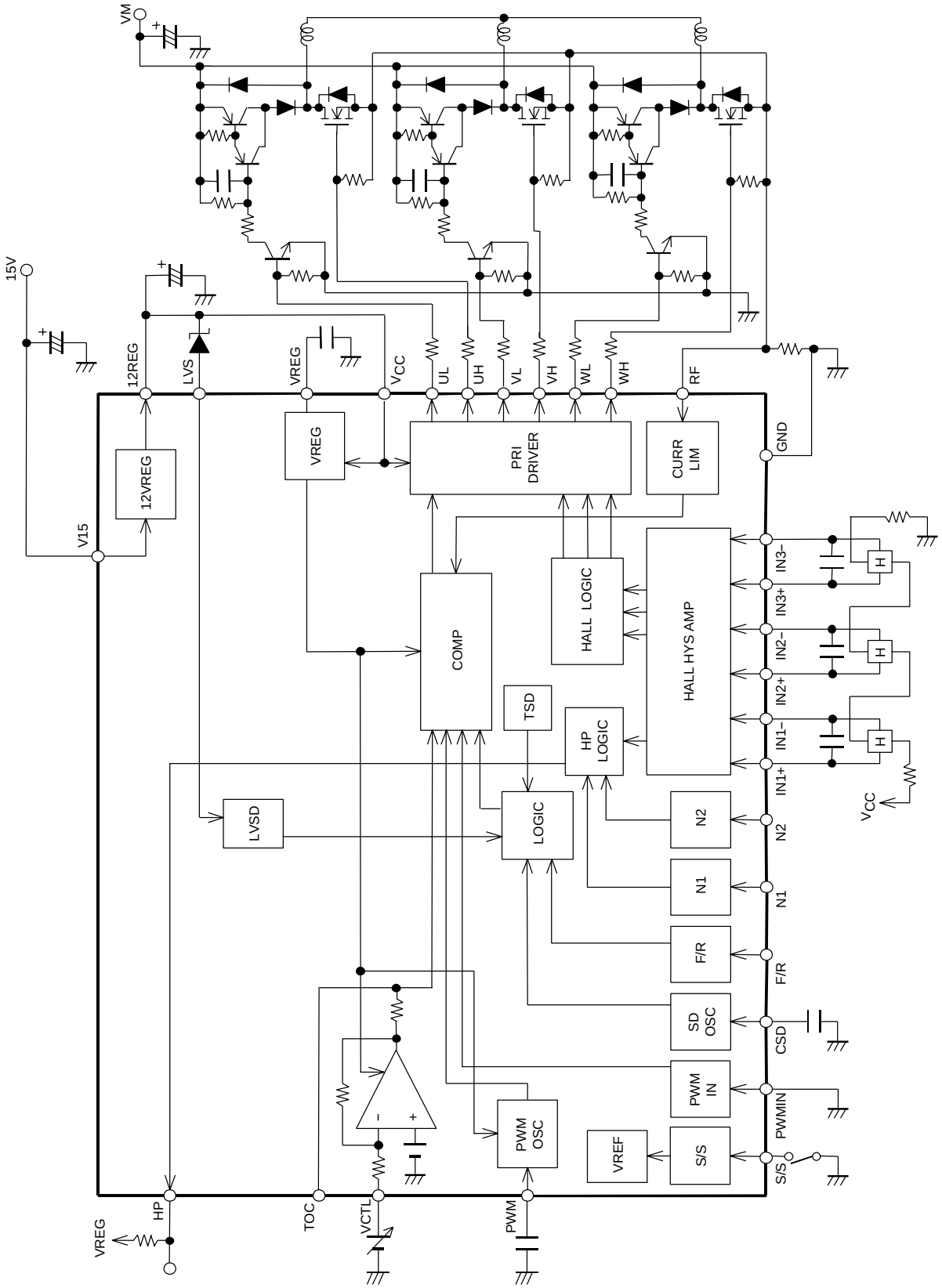
(1) Bipolar transistor drive (high side PWM) using a 5V power supply



(2) MOS transistor drive (low side PWM) using a 12V power supply



(3) NMOS transistor+PNP Transistor drive (low side PWM) using a 15V power supply



LB11695M Functional Description

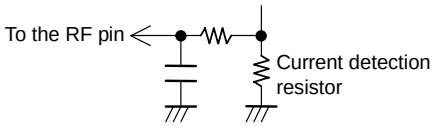
1. Output Drive Circuit

The LB11695M adopts direct PWM drive to minimize power loss in the outputs. The output transistors are always saturated when on, and the motor drive power is adjusted by changing the on duty of the output. The output PWM switching is performed on the UH, VH, and WH outputs. Since the UL to WL and UH to WH outputs have the same output form, applications can select either low side PWM or high side PWM drive by changing the way the external output transistors are connected. Since the reverse recovery time of the diodes connected to the non-PWM side of the outputs is a problem, these devices must be selected with care. (This is because through currents will flow at the instant the PWM side transistors turn on if diodes with a short reverse recovery time are not used.)

The outputs UL through WL and UH through WH are held in the high-impedance state when the IC is stopped or the supply voltage is too low (below the allowable operating voltage level). Consequently, it is necessary to take necessary measures (e.g., adding a pull-down resistor) to prevent the external circuit from malfunctioning due to leak current.

2. Current Limiter Circuit

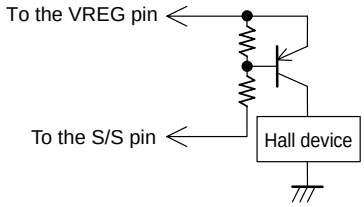
The current limiter circuit limits the output current peak value to a level determined by the equation $I = V_{RF}/Rf$ (V_{RF} = 0.25V typical, Rf: current detection resistor). This circuit suppresses the output current by reducing the output on duty.



The current limiter circuit includes an internal filter circuit to prevent incorrect current limiter circuit operation due to detecting the output diode reverse recovery current due to PWM operation. Although there should be no problems with the internal filter circuit in normal applications, applications should add an external filter circuit (such as an RC low-pass filter) if incorrect operation occurs (if the diode reverse recovery current flows for longer than 1μs).

3. Power Saving Circuit

This IC goes to a low-power mode (power saving state) when set to the stop state with the S/S pin. In the power saving state, the bias currents in most of the circuits are cut off. However, the 5V regulator output (V_{REG}) is still provided in the power saving state. If it is also necessary to cut the Hall device bias current, this function can be provided by an application that, for example, connects the Hall devices to 5V through PNP transistors.



4. Handling Different Power Supply Types

When this IC is operated from an externally supplied 5V power supply (4.5 to 5.5V), short the V_{CC} pin to the V_{REG} pin and connect them to the external power supply. When this IC is operated from an externally supplied 12V power supply (8 to 13.5V), connect the V_{CC} pin to the power supply. (The V_{REG} pin will generate a 5V to function as the power supply to the control circuit.)

When this IC is operated from on an externally supplied 15V power supply (13.5 to 19V), connect the V15 pin to the power supply and short between the 12REG and VCC pins. (The 12REG pin will generate a 12V to function as the V_{CC} power supply.)

5. Notes on the PWM Frequency

The PWM frequency is determined by the capacitor C (F) connected to the PWM pin.

$fPWM \approx 1/(45000 \times C)$

If a 1000pF capacitor is used, the circuit will oscillate at about 22kHz. If the PWM frequency is too low, switching noise will be audible from the motor, and if it is too high, the output power loss will increase. Thus a frequency in the range 15 to 50kHz must be used. The capacitor's ground side lead must be placed as close as possible to the IC's ground pin to minimize the influence of output noise and other noise sources.

6. Control Methods

The output duty can be controlled by either of the following methods.

- Using the voltage at the V_{CTL} pin

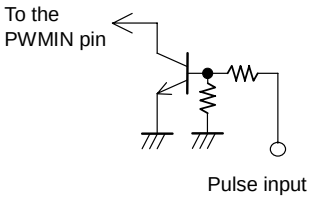
Refer to the section entitled "Electrical Characteristics" for legitimate control voltages. Set the PWMIN pin to the low level when controlling the output duty using the V_{CTL} pin.

The IC is designed so that the 100% output duty cannot be achieved with the input through the V_{CTL} pin in consideration of possible application during bootstrap (the output duty is limited by the maximum output duty specified in "Electrical Characteristics"). Consequently the motor speed must be controlled while adjusting the output duty within the range of 0 to 80%.

- Pulse Control Using the PWMIN Pin

A pulse signal can be input to the PWMIN pin, and the output can be controlled based on the duty of that signal. Note that the output is on when a low level is input to the PWMIN pin, and off when a high level is input. When the PWMIN pin is open, it goes to the high level and the output is turned off. If inverted input logic is required, this can be implemented with an external transistor (npn).

When controlling motor operation using the PWMIN pin, the VCTL pin must be connected to the VREG pin and a 2kΩ resistor must be inserted between the TOC pin and ground. The use of this IC while controlling the drive mode using the PWMIN pin during bootstrap is not taken into consideration.



7. Hall Input Signals

A signal input with an amplitude in excess of the hysteresis (50mV maximum) is required for the Hall inputs. Considering the possibility of noise and phase displacement, an amplitude of 120mV or higher is desirable.

If disruptions to the output waveforms (during phase switching) or to the HP output (Hall signal output) occur due to noise, this must be prevented by inserting capacitors between the inputs. The constraint protection circuit uses the Hall inputs to identify the motor constraint state. Although the circuit is designed to tolerate a certain amount of noise, care is required when using the constraint protection circuit.

If all three phases of the Hall input signal system go to the same input state, the outputs are all set to the off state (the UL, VL, WL, UH, VH, and WH outputs all turn off).

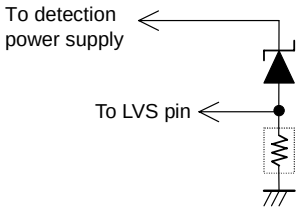
If the outputs from a Hall IC are used, fixing one side of the inputs (either the + or - side) at a voltage within the common-mode input voltage range allows the other input side to be used as an input over the 0 V to VCC1 range.

8. Undervoltage Protection Circuit

The undervoltage protection circuit turns one side of the outputs (UH, VH, and WH) off when the LVS pin voltage falls below the minimum operation voltage (see the Electrical Characteristics). To prevent this circuit from repeatedly turning the outputs on and off in the vicinity of the protection operating voltage, this circuit is designed with hysteresis. Thus the output detected will not recover until the operating voltage rises by 0.5V (typical) with respect to the operating voltage.

The protection operating voltage detection level is set up for the 5V system. The detected voltage level can be increased by shifting the voltage by inserting a zener diode in series with the LVS pin. The LVS sink current during detection is about 65µA. To increase the diode current to stabilize the zener diode voltage rise, insert a resistor between the LVS pin and ground.

When the protection circuit is not to be used, do not keep the LVS pin open (output is off when put in the open state); instead, a voltage of the level that will not activate the circuit to the LVS pin.



9. Constraint Protection Circuit

The LB11695M is provided with a constraint protection circuit that protects the IC itself and the motor in case the motor is physically constrained (held stopped). The protection circuit turns off the outputs on one side (UH, VH, and WH) when the Hall input signals remain unchanged for a certain time in the motor drive mode. The time the Hall input signals remain unchanged (protection time) is determined by the capacitance of the capacitor connected to the CSD pin.

Setup time (s) ≈ 154×C (μF)

A 0.01μF capacitor provides a protection time of approximately 1.54 seconds. The drive mode is turned off when one period of the Hall input signals become longer than this time). This time should be configured with an adequate margin of safety so that the protection circuit will not get activated in the normal motor startup time. More specifically, the capacitance of the capacitor to be used for this purpose must be 4700pF or larger. One of the following actions must be taken to restore the IC from the constraint protection state:

- Keeping the IC in the stopped state (10μs or longer)
- Keeping the 0% output duty state of the IC, which is placed by the VCTL input or PWMIN input, for a period of tCSD×2 or longer. (The 0% output duty state must be maintained for approximately 10ms or longer if a capacitor with a capacitance of tCSD (s) ≈ 0.5×C (μF) or 0.01μF is used.)
- Turning off and on the power

  Since the CSD pin is also used to generate the initial reset pulse, any attempt to connect this pin to ground causes the logic circuit to be reset, disabling the motor to be driven. Accordingly, when the constraint protection function is not to be used, connect a resistor of approximately 150kΩ and a capacitor of approximately 4700pF in parallel between this pin and ground. The thermal protection circuit is also disabled when the constraint protection circuit is disabled.

10. Thermal protection circuit

The thermal protection circuit turns off the outputs on one side (UH, VH, and WH) when the temperature at the junction (Tj) goes beyond the predetermined temperature (TSD). Since the minimum value of the variations of TSD values is 125°C, thermal design must be carried out so that the junction temperature can never exceed 125°C except under abnormal conditions. Consequently, the value of Pd max is calculated as 0.72W (Ta = 25°C) for a Tj (max) value of 125°C.

The thermal protection circuit will be disabled if the constraint protection function is disabled by connecting a resistor of approximately 150kΩ and a capacitor of approximately 4700pF in parallel between the CSD pin and ground. In this case, Tj (max) = 150°C holds and Pd max = 0.9W (Ta = 25°C) is derived.

11. Forward/Reverse Direction Switching

This IC is designed so that through currents (due to the output transistor off delay time when switching) do not flow in the output when switching directions while the motor is turning. However, if the direction is switched when the motor is turning, currents in excess of the current limiter value may flow in the output transistors due to the motor coil resistance and the motor back EMF state when switching. Therefore, designers must consider selecting external output transistors that are not destroyed by those currents or only switching directions after the speed has fallen below a certain speed.

12. Power Supply Stabilization

Since this IC uses a switching drive technique, the power supply line level can be disturbed easily. Therefore capacitors with adequate capacitance to stabilize the power supply line must be inserted between V_{CC} and ground. If diodes are inserted in the power supply lines to prevent destruction if the power supply is connected with reverse polarity, the power supply lines are even more easily disrupted, and even larger capacitors are required.

If the power supply is turned on and off by a switch, and if there is a significant distance between that switch and the stabilization capacitor, the supply voltage can be disrupted significantly by the line inductance and surge current into the capacitor. As a result, the withstand voltage of the device may be exceeded. In application such as this, the surge current must be suppressed and the voltage rise prevented by not using ceramic capacitors with a low series impedance, and by using electrolytic capacitors instead.

13. VREG Stabilization

To stabilize the VREG voltage, which is the control circuit power supply voltage, a 0.1μF or larger capacitor must be inserted between the VREG pin and ground. The ground side of this capacitor must be connected to the IC ground pin with a line that is as short as possible.