Ordering number : EN8791

SANYO Semiconductors
DATA SHEET

LB11889M — Monolithic Digital IC For VCR Capstan Three-Phase Brushless Motor Driver

Overview

The LB11889M is three-phase brushless motor driver for VCR capstan motors.

Features

- 3-phase full-wave current linear drive.
- Torque ripple correction circuit (fixed correction ratio).
- Current limiter circuit with control characteristics gain switching.
- Output stage upper/lower oversaturation prevention circuit (No external capacitor required).
- FG amplifier built in.
- Thermal shutdown circuit built in.

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage	V_{CC} max		7	V
	VS max		24	V
Maximum output current	I_O max		1.3	A
Allowable power dissipation voltage	Pd max	Independent IC	950	mW
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-55 to +150	°C

Allowable Operating Range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	VS		5 to 22	V
	V_{CC}		4.5 to 5.5	V
Hall input amplitude	VHALL	Between hall inputs	±30 to ±80	mVo-p
GSENSE input range	VGSENSE	Relative to the control system GND	-0.20 to +0.20	V

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D2706 TI IM B8-4207 No.8791-1/11

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Electrical Characteristics at Ta = 25°C, V_{CC} = 5V, VS = 15V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
V_{CC} power supply current	I_{CC}	R_L = ∞, VCTL = 0V, VLIM = 0V (at static mode)		12	18	mA
Output						
Output saturation voltage	$V_O$sat1	I_O = 500mA, Rf = 0.5Ω, sink+source VCTL = VLIM = 5V (With saturation prevention)		2.1	2.6	V
	$V_O$sat2	I_O = 1.0A, Rf = 0.5Ω, sink+source VCTL = VLIM = 5V (With saturation prevention)		2.6	3.5	
Output leak current	$I_O$leak				1.0	mA
FR						
FR pin input threshold voltage	VFSR		2.25	2.50	2.75	V
FR pin input input bias current	Ib (FSR)		-5.0			μA
Control						
CTLREF pin voltage	VCREF		2.37	2.50	2.63	V
CTLREF pin input range	VCREF IN		1.70		3.50	V
CTL pin input bias current	Ib (CTL)	VCTL = 5V, CTLREF : OPEN			8.0	μA
CTL pin control start voltage	VCTL (ST)	Rf = 0.5Ω, VLIM = 5V, I_O≥10mA With hall input logic fixed (U, V, W = H, H, L)	2.20	2.35	2.50	V
CTL pin control switching voltage	VCTL (ST2)	Rf = 0.5Ω, VLIM = 5V	3.00	3.15	3.30	V
CTL pin control Gm1	Gm1 (CTL)	Rf = 0.5Ω, ΔI$_O$ = 200mA With hall input logic fixed (U, V, W = H, H, L)	0.52	0.65	0.78	A/V
CTL pin control Gm2	Gm2 (CTL)	Rf = 0.5Ω, ΔVCTL = 200mV With hall input logic fixed (U, V, W = H, H, L)	1.20	1.50	1.80	A/V
Current limiter						
LIM current limiter offset voltage	Voff (LIM)	Rf = 0.5Ω, VCTL = 5V, I_O≥10mA With hall input logic fixed (U, V, W = H, H, L)	140	200	260	mV
LIM pin input bias current	Ib (LIM)	VCTL = 5V, CTLREF : OPEN, VLIM = 0V	-2.5			μA
LIM pin current limiter level	Ilim	Rf = 0.5Ω, VCTL = 5V, VLIM = 2.06V With hall input logic fixed (U, V, W = H, H, L)	830	900	970	mA
Hall amplifier						
Hall amplifier input offset voltage	Voff (HALL)		-6		+6	mV
Hall amplifier input bias current	Ib (HALL)			1.0	3.0	μA
Hall amplifier common-mode	VCM (HALL)		1.3		3.3	V
TRC						
Torque ripple correction factor	TRC	At bottom and peak of Rf waveform at I_O = 200mA (RF = 0.5Ω, ADJ-OPEN) Note 2		9		%
ADJ pin voltage	VADJ		2.37	2.50	2.63	V
FG amplifier						
FG amplifier input offset voltage	Voff (FG)		-8		+8	mV
FG amplifier input bias current	Ib (FG)		-100			nA
FG amplifier output saturation voltage	$V_O$sat (FG)	At internal pull-up resistor on the sink side			0.5	V
FG amplifier common-mode input voltage	VCM (FG)		0.5		4.0	V
Saturation						
Saturation prevention circuit lower set voltage	$V_O$sat (DET)	Voltage between each OUT and Rf at I_O = 10mA, Rf = 0.5Ω, VCTL = VLIM = 5V	0.175	0.25	0.325	V
TSD						
TSD operating temperature	T-TSD	(Design target) Note.1		180		°C
TSD temperature hysteresis width	ΔTSD	(Design target) Note.1		20		°C

Note 1. No measurements are made on the parameters with Note (Design target).

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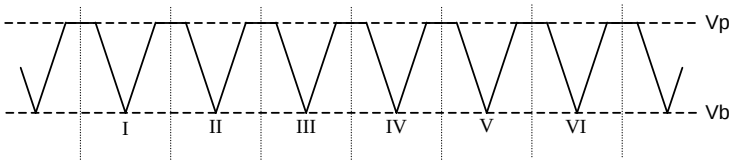
Note 2. The torque ripple correction factor is obtained based on the voltage waveform across Rf as shown below.



Each hall logic setting

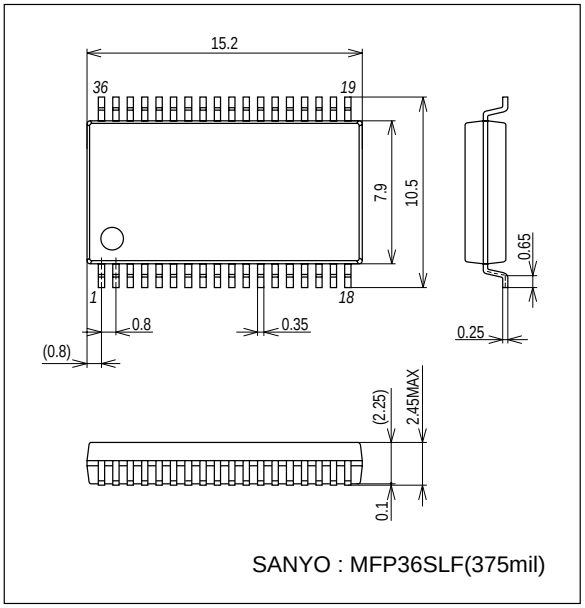
GND lebel

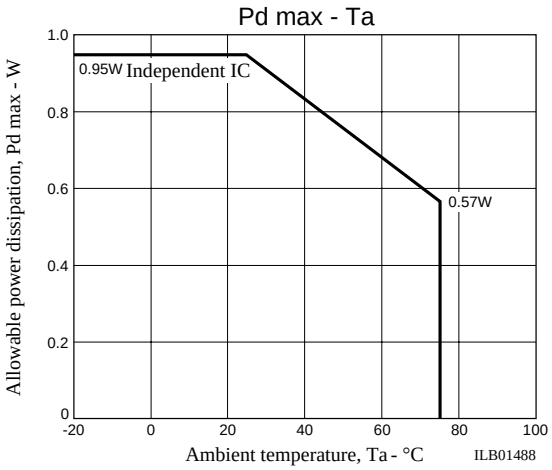
$$\text{Correnction factor} = \frac{2\times (Vp-Vb)}{Vp+Vb} \times 100\ (\%)$$

Package Dimensions

unit : mm (typ)

3280A





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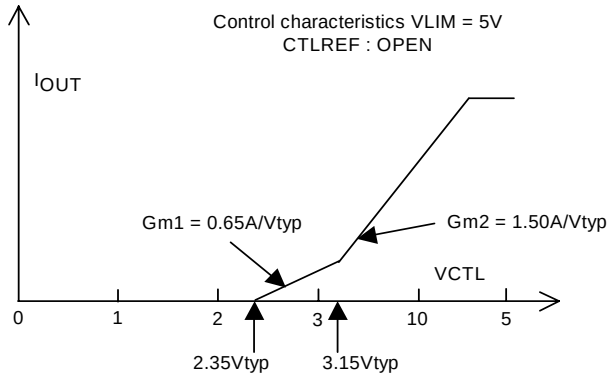
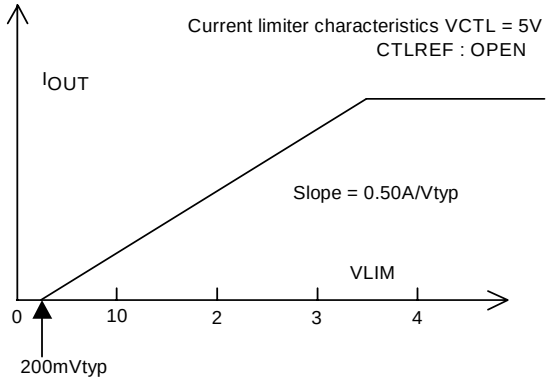
Truth Table and Control Function

	Source → Sink	Hall input			FR
		U	V	W	
1	V → W	H	H	L	H
	W → V				L
2	U → W	H	L	L	H
	W → U				L
3	U → V	H	L	H	H
	V → U				L
4	W → V	L	L	H	H
	V → W				L
5	W → U	L	H	H	H
	U → W				L
6	V → U	L	H	L	H
	U → V				L

Note) “H” for FR represents a voltage of 2.75V or greater ; “L” represents a voltage of 2.25V or lower (at V_{CC} = 5V).
Note) Input “H” for all input represents that (+) is higher than each phase input (-) by 0.01V or greater ; input “L” represents that (+) is lower than each phase input (-) by 0.01V or greatre.
Note) Since this drive scheme is the 180° energizing scheme, phases other than Sink, Source phases are not turned OFF.

Control Function & Current Limiter Function





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Pin Functions

Pin name	Pin no.	Functions
FGIN (-)	3	Input pin for the FG amplifier to be used with inverted input. A feedback resistor is connected between this pin and FG OUT.
FGIN (+)	4	Noninverting input pin for the FG amplifier to be used as differential input. No bias is applied internally.
FG-OUT	5	FG amplifier output pin with resistive load internally.
CTL	6	Speed control pin. Control is performed by means of constant current drive which is applied by current feedback from Rf. Gm = 0.65A/V & 1.50A/V TYP at Rf = 0.5Ω
CTLREF	7	Control reference voltage pin. The voltage is set at approximately V_{CC}/2 internally, but can be varied by applying a voltage through a low impedance. (The input impedance is approximately 2.5kΩ.)
LIM	8	Current limiter function control pin. This pin voltage is capable of varying the output current linealy. Slope = 0.5A/V TYP at Rf = 0.5Ω
FC	9	Speed control loop's frequency characteristics correction pin.
U_{IN}+, U_{IN}- V_{IN}+, V_{IN}- W_{IN}+, W_{IN}-	10, 11 12, 13 14, 15	U phase hall element input pin. "H" for logic represents IN+>IN-. V phase hall element input pin. "H" for logic represents IN+>IN-. W phase hall element input pin. "H" for logic represents IN+>IN-.
V_{CC}	16	Power supply pin used to supply to each circuit other than the output blocks inside the IC. This voltage must be stabilized to reject noise and ripple.
VS	21	Power supply pin for output blocks.
ADJ	22	Pin to be used to adjust the torque ripple correction factor externally. When adjusting the correction factor, apply voltage externally to the ADJ pin through a low impedance. Increasing the applied voltage decreases the correction factor ; lowering the applied voltage increases the correction factor. The rate of change, when left open, ranges approximately from 0 to 2 times. (Approximately V_{CC}/2 is set internally and the input impedance is approximately 5kΩ.)
Rf (PWR) Rf (SNS)	23 31	Output current detection pins. Current feedback is provided to the control blocks by connecting Rf between the pins and GND. The operation of the lower over-saturation prevention circuit and torque ripple correction circuit depends on the pin voltage. In particular, since the oversaturation prevention level is set by the pin voltage, decreasing the Rf value extremely may cause the lower over-saturation prevention to work less efficiently in the large current region. The PWR pin and SENSE pin must be connected.
U_{OUT} V_{OUT} W_{OUT}	26 27 28	U phase output pin V phase output pin W phase output pin (With spark killer diode built in)
GSENSE	32	GND sensing pin. By connecting this pin to GND in the vicinity of the Rf resistor side of the Rf included motor GND wiring, the influence that the GND common impedance exerts on Rf can be excluded. (Must not be left open.)
FR	33	Forward/reverse select pin. This pin voltage determines forward/reverse. (Vth = 2.5V typ. At V_{CC} = 5V)
GND	34	GND for other than output transistors. The lowest potential of output transistors is on the Rf pin.

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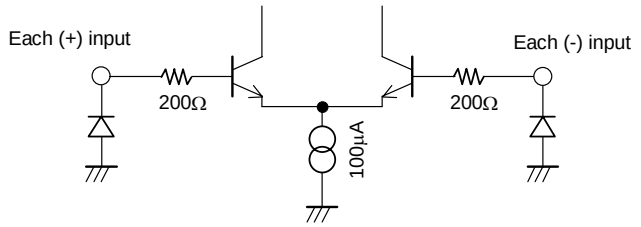
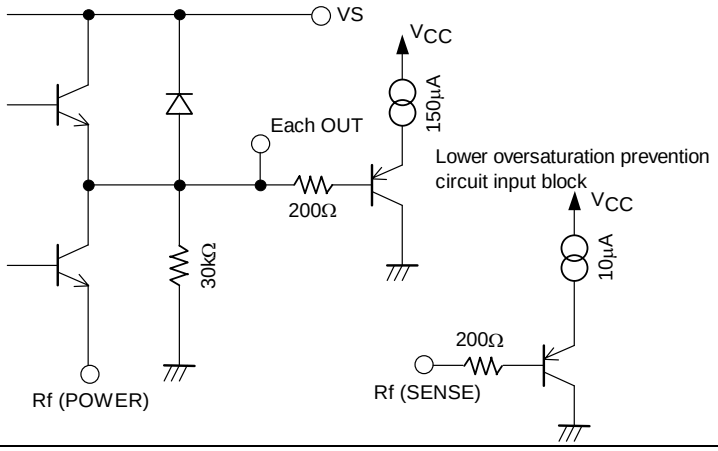
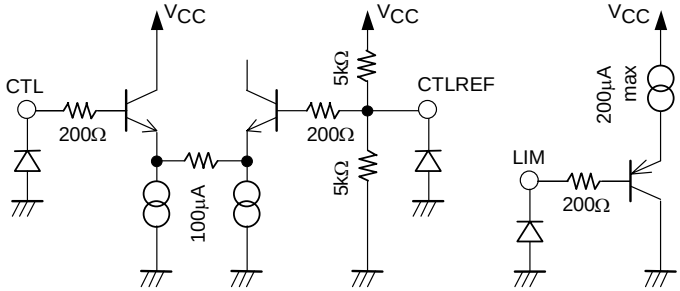
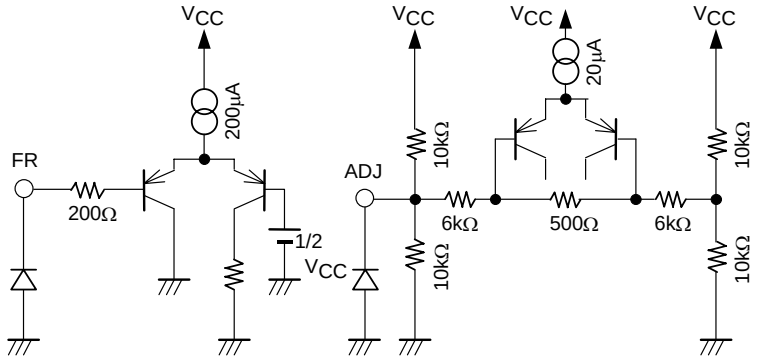
Each Input/Output Equivalent Circuit

Pin name	Input/Output equivalent circuit
U_{IN} (+) U_{IN} (-) V_{IN} (+) V_{IN} (-) W_{IN} (+) W_{IN} (-)	
U_{OUT} V_{OUT} W_{OUT} VS Rf (POWER) Rf (SENSE)	
CTL LIM CTLREF	
FR ADJ	

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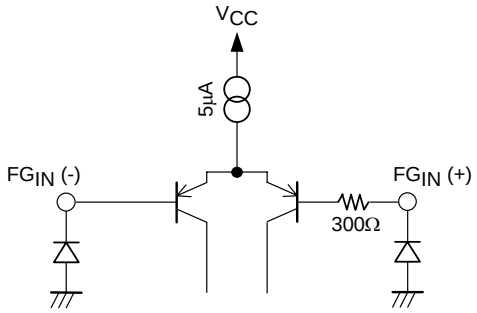
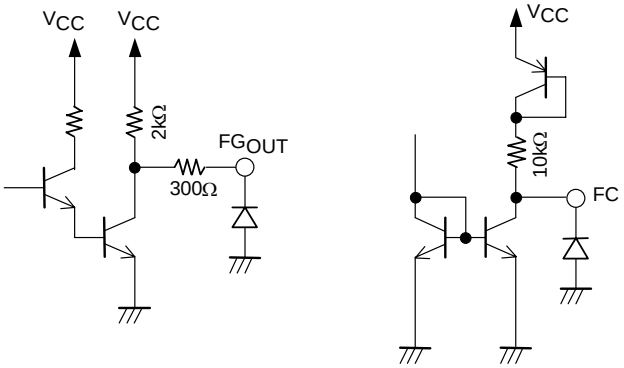
Pin name	Input/output equivalent circuit
FG_{IN} (-) FG_{IN} (+)	
FG_{OUT} FC	

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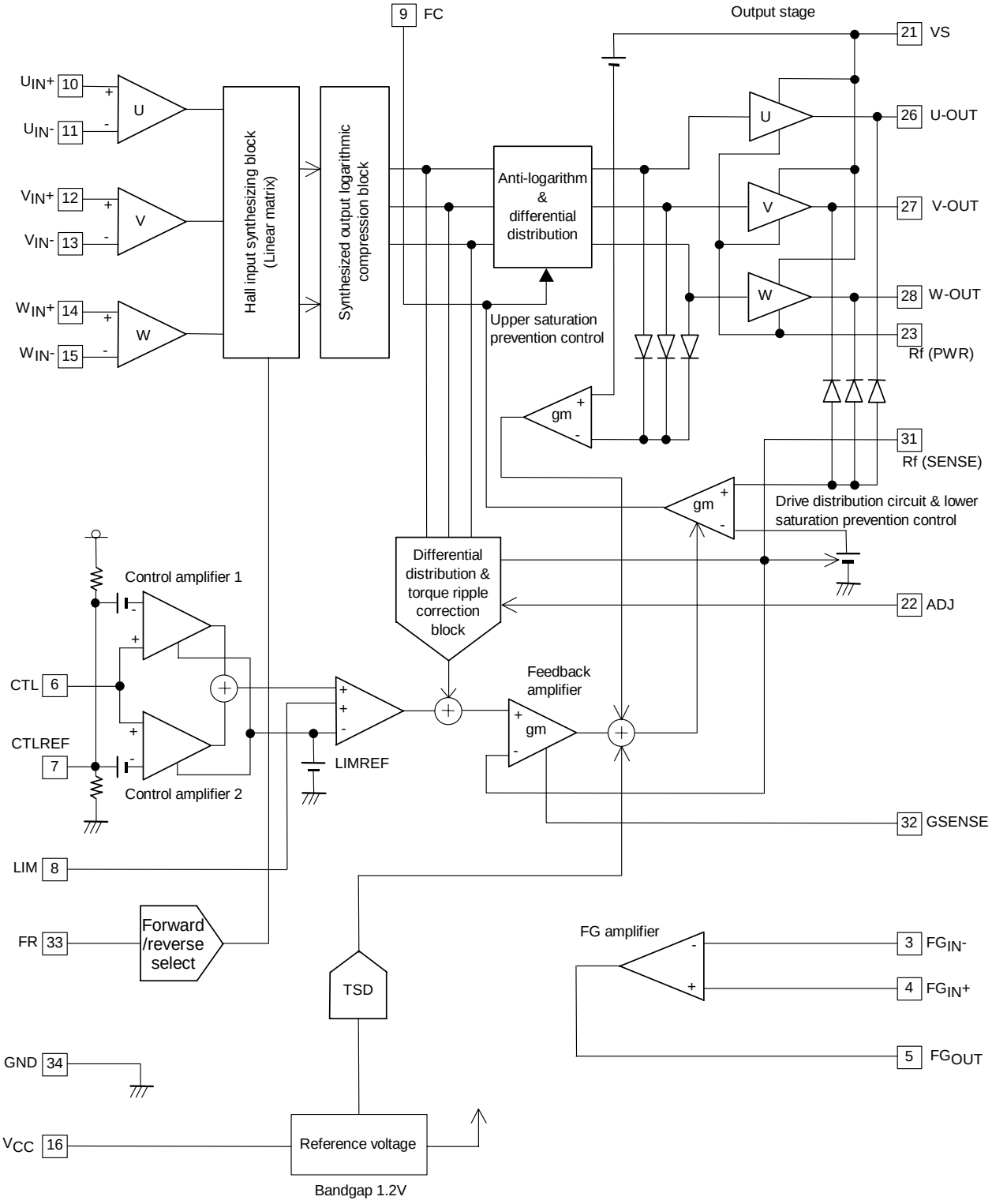
Block Diagram



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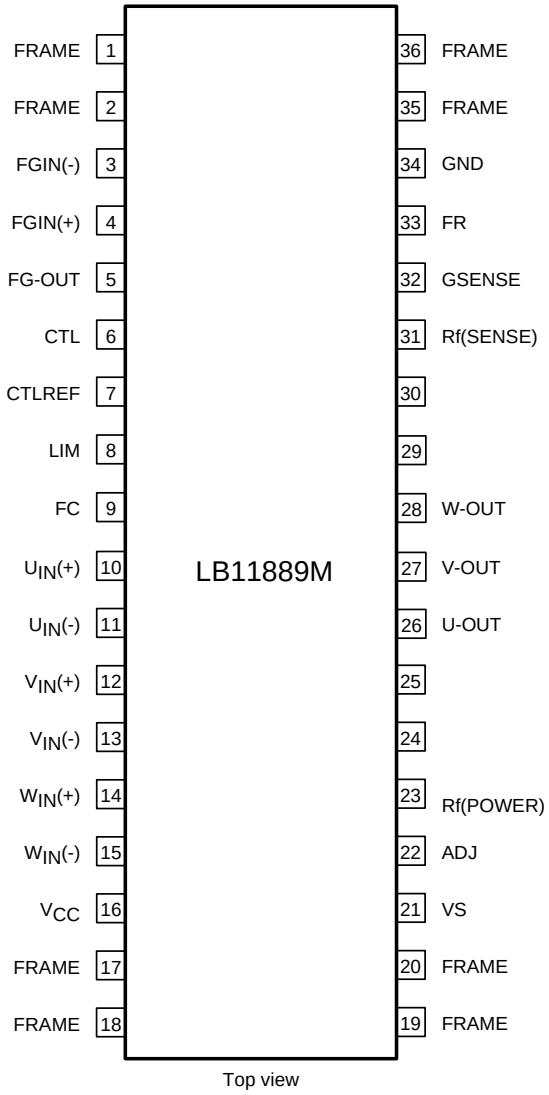
Pin Assignment



Top view

Note: Although the FRAME pins and the GND pin are not connected internally in the IC, the FRAME pins must be connected to the GND pin externally for ground potential stabilization.

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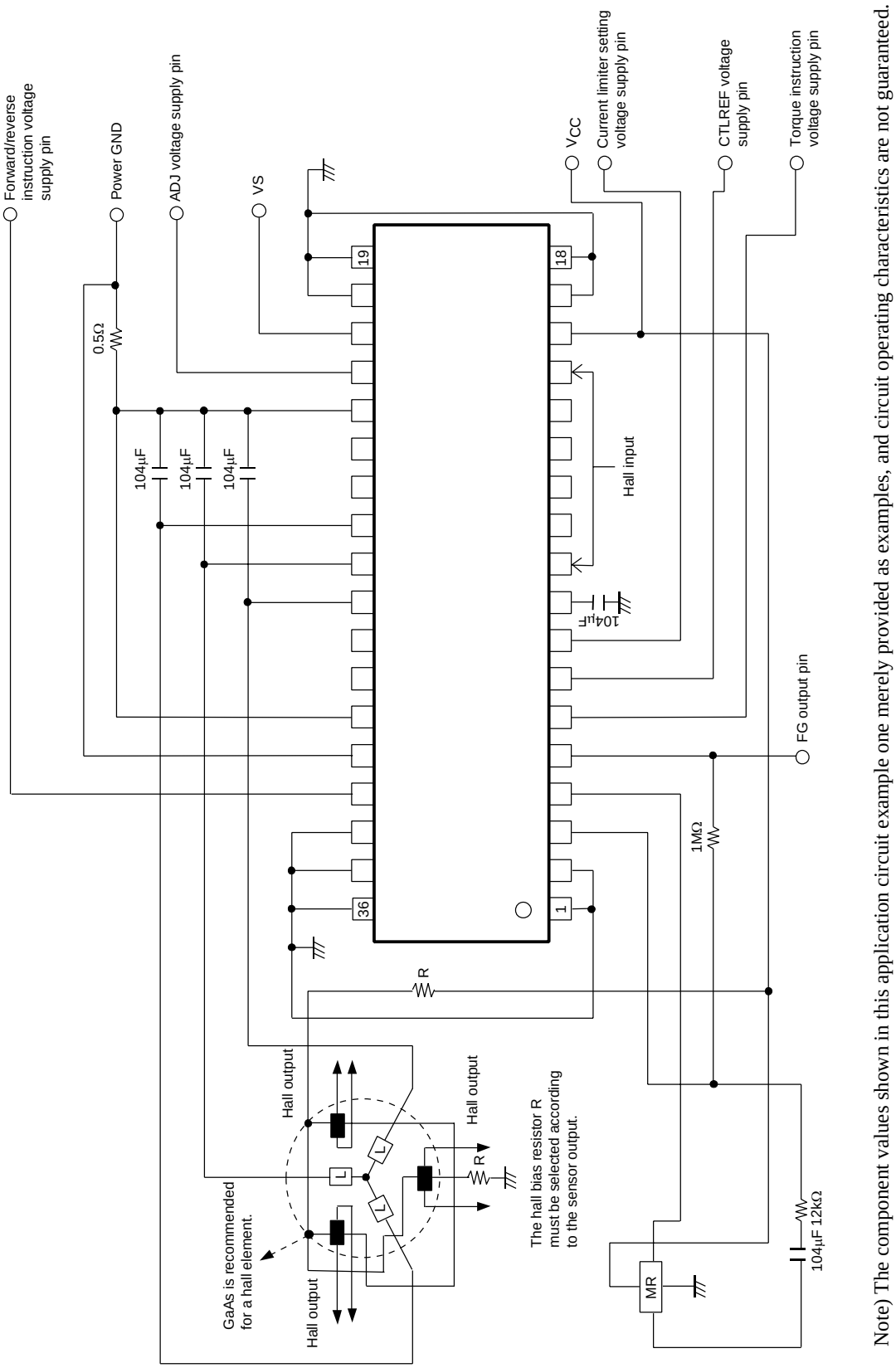
Sample Application Circuit



Note) The component values shown in this application circuit example one merely provided as examples, and circuit operating characteristics are not guaranteed.

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