Ordering number : ENA0919

SANYO Semiconductors
DATA SHEET

LV8095LQ — Bi-CMOS IC For VCMs Constant-current Driver IC

Overview

The LV8095LQ is a constant current driver IC for voice coil motors. It supports I²C control and integrates a digital/analog converter (DAC).
Its ultraminiature package makes the IC ideal for constant-current driving the voice coil motors (AF and ZM) used in a wide variety of portable equipment including camera cell-phones.

Features

- Constant current driver for voice coil motors.
- I²C bus control supported.
- No external capacitors needed (capacitor-less).
- Ultraminiature package (USLP8 : 2.0×1.3×0.56mm) for easy soldering.
- Built-in thermal protection circuit.
- Built-in voltage drop protection circuit.
- Constant current control enabled by DAC (8 bits).
- Wide operating voltage range (2.5 to 5.5V).

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		-0.3 to +5.5	V
Maximum VDD voltage	V_{DD} max		-0.3 to +5.5	V
Output voltage	V_{OUT} max	OUT1	-0.3 to +6.0	V
Input voltage	V_{IN} max	SCL, SDA, PD	-0.3 to +5.5	V
GND pin source current	I_{GND}		200	mA
Allowable power dissipation	Pd max	*Mounted on a specified board.	650	mW
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-40 to +150	°C

* Specified board : 50mm×40mm×0.8mm, 4-layer glass epoxy circuit board.

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Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		2.5 to 5.0	V
V_{DD} voltage	V_{DD}		1.3 to 5.0	V
Maximum preset output current	I_O		200	mA
High-level input voltage	V_{IH}	Applied to SCL, SDA, and PD pins	0.8×V_{DD} to V_{DD}	V
Low-level input voltage	V_{IL}		-0.3 to 0.2×V_{DD}	V

Electrical Characteristics Ta = 25°C, V_{CC} = 2.8V, V_{DD} = 2.8V

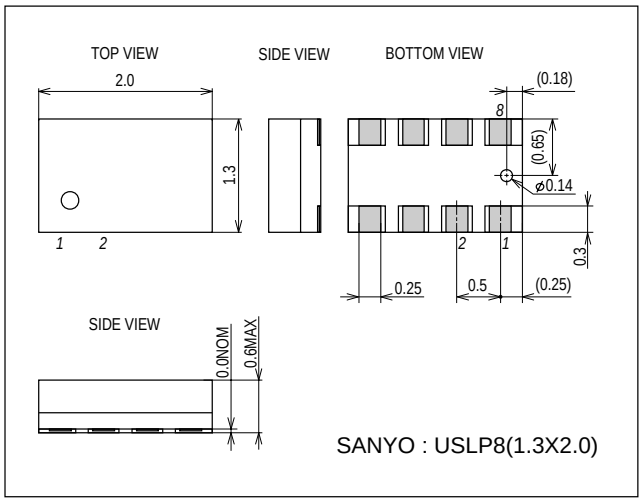
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current	I_{CCO}	PD = 0V		0.1	1	μA
	I_{CC}1	PD = 2.8V		0.5	3	mA
Input current	I_{IN}	V_{IN} = 2.8V, VENA = 2.8V	-1	0	1	μA
Output saturation voltage	Vsat1	SW : ON, SW : b, Full code setting, I_{OUT} = 50mA		0.10	0.18	V
	Vsat2	SW : ON, SW : b, Full code setting, I_{OUT} = 100mA		0.20	0.4	V
DAC block						
Resolution		RF = 1Ω, SW1 : OFF, SW2 : a		8		bits
Relative accuracy	INL	RF = 1Ω, SW1 : OFF, SW2 : a			±1	LSB
Differential linearity	DNL	RF = 1Ω, SW1 : OFF, SW2 : a			±1	LSB
Full code current	Ifull	RF = 1Ω, SW1 : OFF, SW2 : a	95	100	105	mA
Error code current 0	Izero	RF = 1Ω, SW1 : OFF, SW2 : a		1	4	mA
Spark killer diode						
Reverse current	IS (leak)				1	μA
Forward voltage	VSF	I_{OUT} = 200mA *			1.3	V

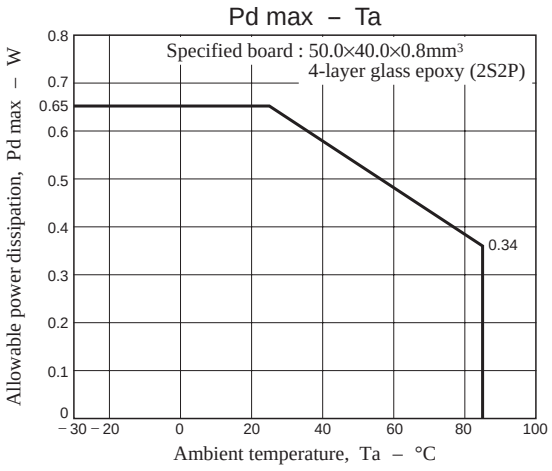
*1 : Design guaranteed value (no measurement is performed)

Package Dimensions

unit : mm (typ)

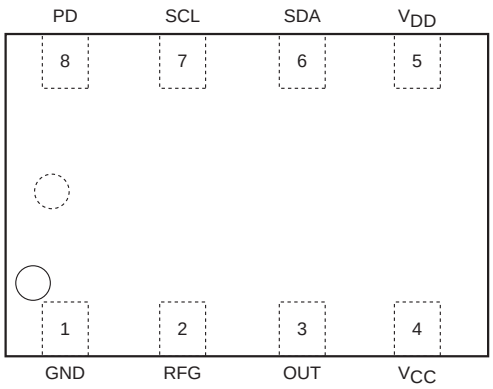
3348





Pin Assignment

USLP8
(Top View)

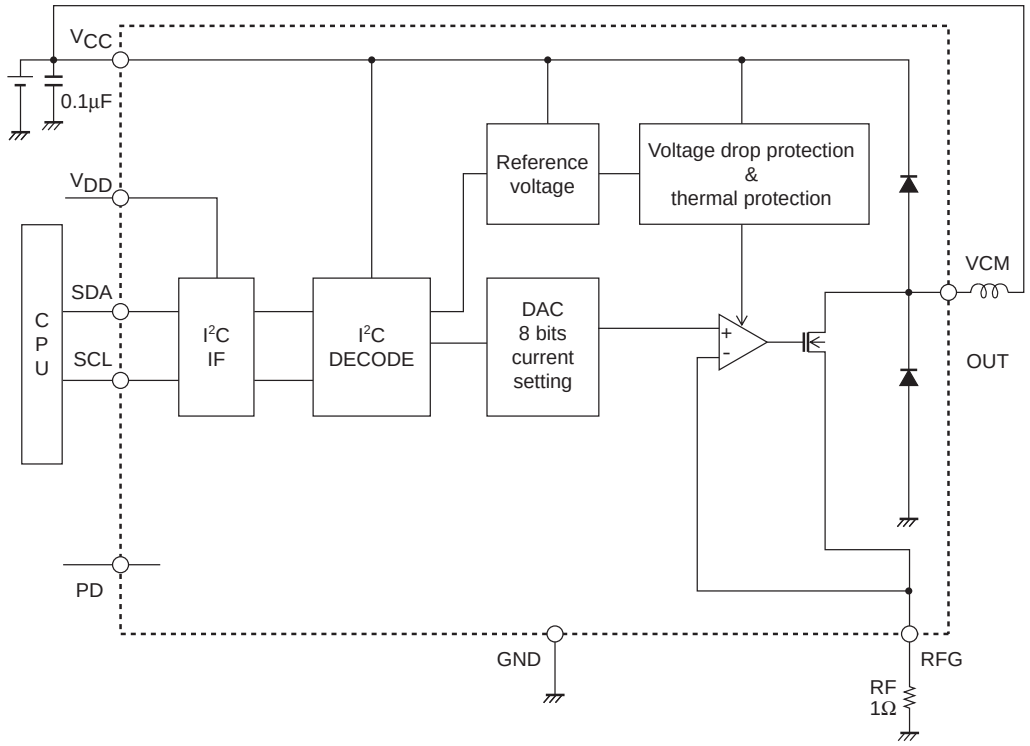


Pin No.	Pin Name	Pin Description
1	GND	Ground
2	RFG	Current sensing resistor connection
3	OUT	Output pin
4	V_{CC}	Analog system power supply
5	V_{DD}	Logic system power supply *1
6	SDA	I^2C SDA input
7	SCL	I^2C SCL input
8	PD	Power-down & reset *2

*1 : The voltage applied to the V_{DD} pin must be set to the same level as those of the SDA, SCL and PD input high-level voltages.

*2 : Setting the PD pin to low level powers down and resets the IC. Set this pin temporarily to low level, then to high level after power-on, and keep it to high level (same voltage level as V_{DD}) during normal operation.

Block Diagram



Wiring resistance (thick line) around the RF is added to the resistance of RF as an error. It must be kept as small as possible.

Formula for calculating constant current : $I_{OUT} = 0.1 \div RF$

If, for instance, I_{OUT} is to be set to 100mA max :

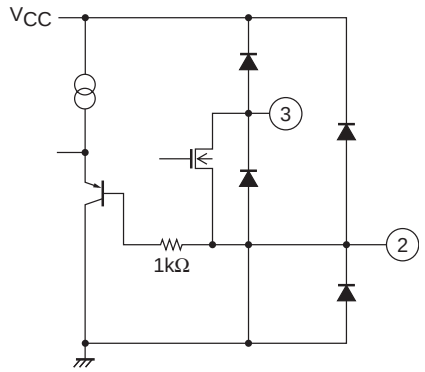
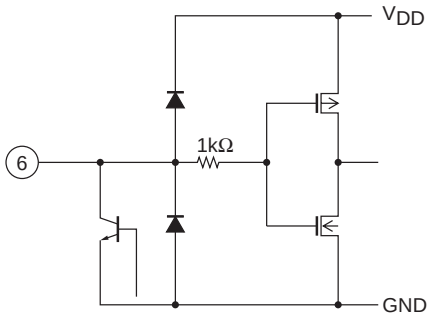
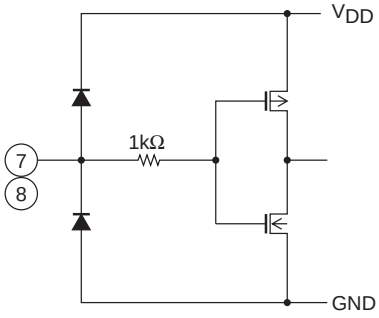
$RF = 0.1 \div (100mA)$

$RF = 1\Omega$

Notes on use

- Determine the preset current value using the resistor between RFG and GND according to the formula above.
- The recommended RF value is 1Ω.

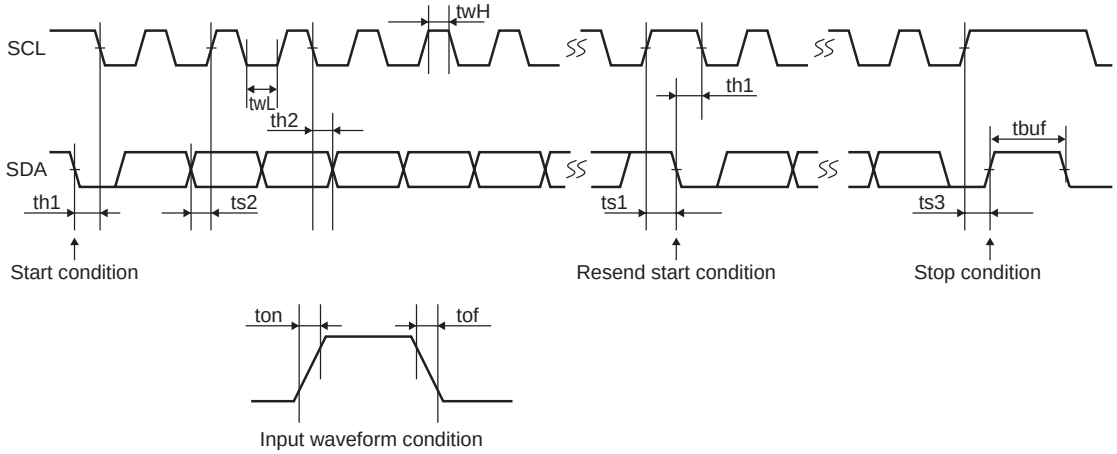
Pin Description

Pin No.	Pin Name	Description	Equivalent Circuit
1	GND	Ground pin	
2 3	RFG OUT	2 : RFG Current detection resistor connection pin The current detection resistor (1Ω) is connected between this pin and GND to detect the output current and perform constant current control. 3 : OUT Output pin This is an NMOS open drain output, and the voice coil motor is connected between this pin and the V_{CC} pin for use.	
4 5	V_{CC} V_{DD}	4 : V_{CC} Power supply input pin 5 : V_{DD} This is separate from the V_{CC} power supply pin for the SDA, SCL and PD logic input, and it is used while the same voltage as that for the high level of these logic input is applied to it.	
6	SDA	I^2C serial data input pin Input high level : 0.8 × V_{DD} or higher Input low level : 0.2 × V_{DD} or lower	
7 8	SCL PD	7 : SCL I^2C serial clock input pin 8 : PD Power down and reset When low, power-down and reset is performed at the same time. This pin is held high for normal use. In normal operation, however, this pin must be set low temporarily and an initial reset must be applied after V_{CC} starts up. Input high level : 0.8 × V_{DD} or higher Input low level : 0.2 × V_{DD} or lower	

Serial Bus Communication Specifications

I²C serial transfer timing conditions

Standard mode



Standard mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0		100	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	4.7			µs
	ts2	Setup time of SDA with respect to the rising edge of SCL	250			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	4.0			µs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	4.0			µs
	th2	Hold time of SDA with respect to the falling edge of SCL	0			µs
Pulse width	twL	SCL low period pulse width	4.7			µs
	twH	SCL high period pulse width	4.0			µs
Input waveform conditions	ton	SCL, SDA (input) rising time			1000	ns
	tof	SCL, SDA (input) falling time			300	ns
Bus free time	tbuf	Interval between stop condition and start condition	4.7			µs

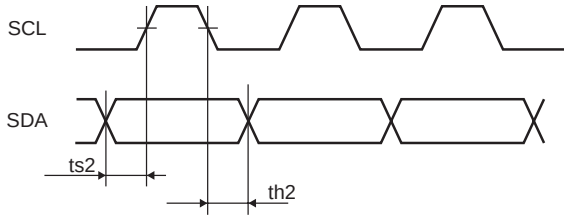
High-speed mode

Parameter	Symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0		400	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	0.6			µs
	ts2	Setup time of SDA with respect to the rising edge of SCL	100			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	0.6			µs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	0.6			µs
	th2	Hold time of SDA with respect to the falling edge of SCL	0			µs
Pulse width	twL	SCL low period pulse width	1.3			µs
	twH	SCL high period pulse width	0.6			µs
Input waveform conditions	ton	SCL, SDA (input) rising time			300	ns
	tof	SCL, SDA (input) falling time			300	ns
Bus free time	tbuf	Interval between stop condition and start condition	1.3			µs

I²C bus transmission method

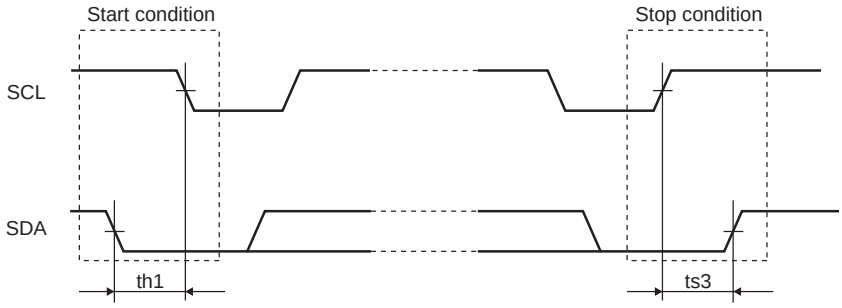
Start and stop conditions

The I²C bus requires that the state of SDA be preserved while SCL is high as shown in the timing diagram below during a data transfer operation.



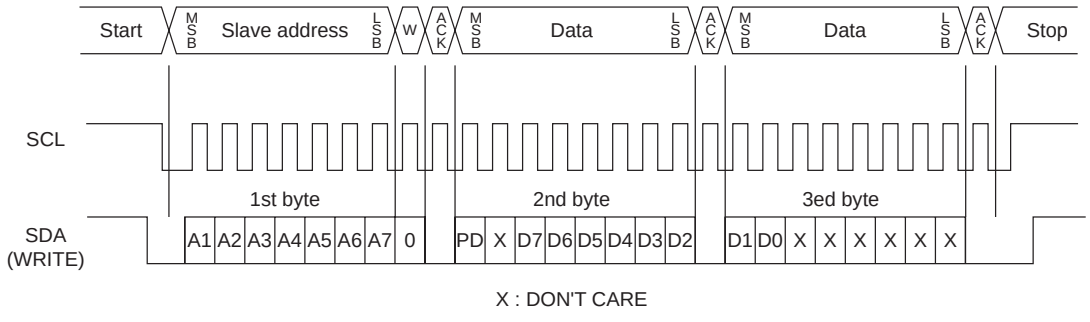
When data is not being transferred, both SCL and SDA are in the high state. The start condition is generated and access is started when SDA is changed from high to low while SCL and SDA are high.

Conversely, the stop condition is generated and access is ended when SDA is changed from low to high while SCL is high.



Data transfer and acknowledgement response

After the start condition has been generated, the data is transferred one byte (8 bits) at a time. Generally, in an I²C bus, a unique 7-bit slave address is assigned to each device, and the first byte of the transfer data is allocated to the 7-bit slave address and to the command (R/W) indicating the transfer direction of the subsequent data. However, this IC is provided with only a write mode for receiving the data. Every time 8 bits of data for each byte are transferred, the ACK signal is sent from the receiving end to the sending end. Immediately after the clock pulse of SCL bit 8 in the data transferred has fallen to low, SDA at the sending end is released, and SDA is set to low at the receiving end, causing the ACK signal to be sent. When, after the receiving end has sent the ACK signal, the transfer of the next byte remains in the receiving status, the receiving end releases SDA at the falling edge of the ninth SCL clock.



X : DON'T CARE

The standard data transfer to this device consists of three bytes : the slave address of the first byte and the data of the second and third bytes.
The table below shows the format of the second and third bytes.

	2nd byte								3rd byte							
Serial data bits	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Function	PD	×	D7	D6	D5	D4	D3	D2	D1	D0	×	×	×	×	×	×

Slave address : 0110011(0)
PD : Power-down
D1-D7 : 8-bit data used to set output constant current ; MIN = 00000000, MAX = 11111111

D0-D7 setting method (output current design values assume an RF of 1Ω)

Current setting code	D7	D6	D5	D4	D3	D2	D1	Output setting (LSB)	Output current (mA) (design value)
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	1	0.392
2	0	0	0	0	0	1	0	2	0.784
254	1	1	1	1	1	1	0	254	99.608
255	1	1	1	1	1	1	1	255	100

Specified Test Circuit