

# Dropper Type Regulator with Reset Function SI-3011S

## Features

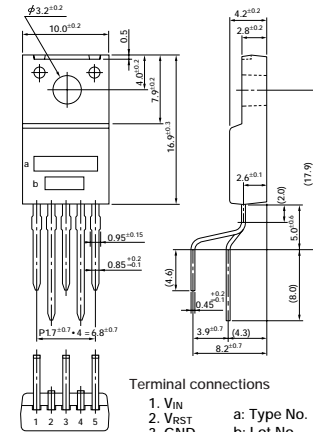
- 5-terminal IC regulator with reset function; 0.7A output current
- Voltage accuracy of  $\pm 2\%$
- Low Dropout voltage  $\leq 0.5V$  at  $I_O \leq 0.3A$
- Built-in constant current type overcurrent, overvoltage and thermal protection circuits
- TO-220 equivalent full-mold miniature package

## Absolute Maximum Ratings

( $T_a = 25^\circ C$ )

Parameter	Symbol	Ratings	Unit	Conditions
DC input voltage	$V_{IN}$	35	V	
Output current	$I_O$	0.7 *1	A	
Power Dissipation	$P_{D1}$	22	W	With infinite heatsink
	$P_{D2}$	1.8	W	Stand-alone without heatsink
Junction temperature	$T_J$	-40 to +150	$^\circ C$	
Operating temperature	$T_{OP}$	-40 to +105	$^\circ C$	
Storage temperature	$T_{stg}$	-40 to +150	$^\circ C$	
Junction to case thermal resistance	$\theta_{j-c}$	5.5	$^\circ C/W$	
Junction to ambient-air thermal resistance	$\theta_{j-a}$	66.7	$^\circ C/W$	Stand-alone without heatsink

## External Dimensions (unit: mm)



Terminal connections

1.  $V_{IN}$
  2.  $V_{RST}$
  3. GND
  4. DLY
  5.  $V_{OUT}$
- a: Type No.  
b: Lot No.
- (Forming No. 1101)

## Electrical Characteristics

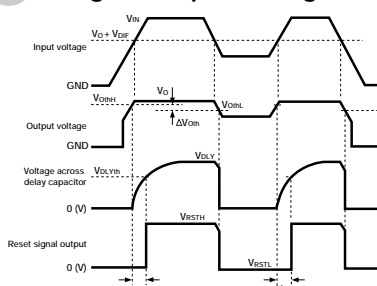
( $T_J = 25^\circ C$ ,  $V_{IN} = 14V$ ,  $I_O = 0.3A$  unless otherwise specified)

Parameter	Symbol	Ratings			Unit	Conditions		
		min	typ	max				
Input voltage	$V_{IN}$	6 *2		30 *1	V			
Output voltage	$V_O$	4.90	5.00	5.10	V			
Dropout voltage	$V_{DIF}$			0.5	V			
Ripple rejection	$R_{REJ}$		54		dB	$f = 100$ to $120Hz$		
Quiescent circuit current	$I_q$		8.5	12	mA	$I_O = 0A$		
Overcurrent protection starting current	$I_S$	0.71 *3			A			
DLY terminal	Threshold voltage	$V_{DLYth}$	2.7	2.9	3.1	V	DLY terminal open	
	Source current	$I_{DLY}$	25	35	45	$\mu A$		
Reset threshold voltage level	$V_{OthL}$ *4	$V_O \cdot 0.90$	$V_O \cdot 0.92$	$V_O \cdot 0.94$	V	$V_O = 5.0V$ (typ)		
		Reset threshold voltage hysteresis	$\Delta V_{Oth}$	50	100	150	mV	$\Delta V_{Oth} = V_{OthH} - V_{OthL}$
		$V_{RST}$ terminal	H-level output voltage	$V_{RSTH}$	$V_O - 0.1$		V	$V_O = 5.0V$ (typ), $R_L = 510\Omega$
L-level output voltage	$V_{RSTL}$			0.5	V	$V_O = 5.0V$ (typ), $R_L = 510\Omega$		
Source current when H-level	$I_{RSTH}$		1.3		mA	$V_O = 5.0V$ (typ), shorted across $V_{RST}$ and GND		
Sink current when L-level	$I_{RSTL}$			-10	mA	$V_{RST} = 0.5V$		

### Notes:

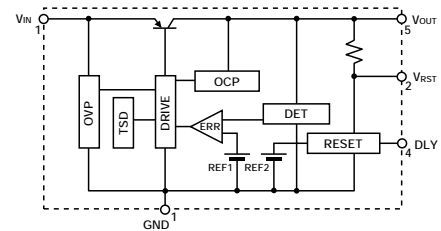
- \*1. Since  $P_{D(max)} = (V_{IN} - V_O) \cdot I_O = 22(W)$ ,  $V_{IN(max)}$  and  $I_O(max)$  may be limited depending on operating conditions. Refer to the  $T_a - P_D$  curve to compute the corresponding values.
- \*2. Refer to the dropout voltage.
- \*3.  $I_S$  rating shall be the point at which the output voltage  $V_O$  ( $V_{IN} = 14V$ ,  $I_O = 0.3A$ ) drops to -5%.
- \*4.  $V_{OthL}$  is the  $V_O$  threshold voltage at which the  $V_{RST}$  terminal turns from high to low.
- \*5.  $V_{OthH}$  is the  $V_O$  threshold voltage at which the  $V_{RST}$  terminal turns from low to high.  $V_{OthH}$  may be given by  $V_{OthL}$  plus  $\Delta V_{Oth}$ .
- \*6. Reset signal output terminal  $V_{RST}$  is pulled up in the IC [pull-up resistance 3k $\Omega$  (typ)], allowing direct connection with a logic circuit.

## Reset Signal Output Timing Chart

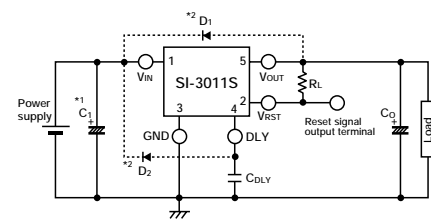


[Calculating  $t_{DLY}$ ]  
Reset signal delay time  $t_{DLY}$  is calculated from the following formula:  
$$t_{DLY} = \frac{V_{DLYth} + 0.2}{I_{DLY}} \cdot C_{DLY}$$
  
\*  $I_{DLY}$  is the current flowing from DLY terminal shown in the Standard Circuit Diagram.

## Equivalent Circuit Diagram

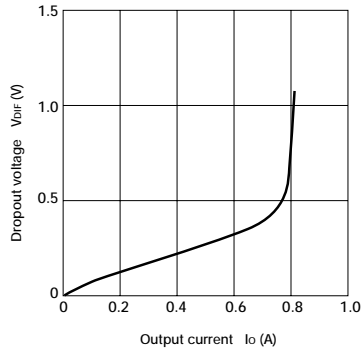


## Standard Circuit Diagram

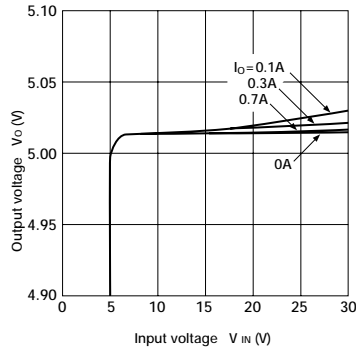


- $C_O$ : Output capacitor (47 to 100 $\mu F$ , 50V)  
 \*1  $C_1$ : Anti-oscillation capacitors ( $C_1$ : approx. 47 $\mu F$ ). This must be connected to terminals 1 ( $V_{IN}$ ) and 3 (GND) via the shortest possible routing. An approximately 0.33 $\mu F$  capacitor with good high frequency characteristics must be connected in parallel in case of inductive input lines or long-distance wiring. Tantalum capacitors are recommended for  $C_1$  and  $C_O$ , especially at low temperatures.  
 \*2  $D_1, D_2$ : Protection diode. Required as protection against reverse biasing between input and output. (Recommended diode: Sanken EU2Z.)

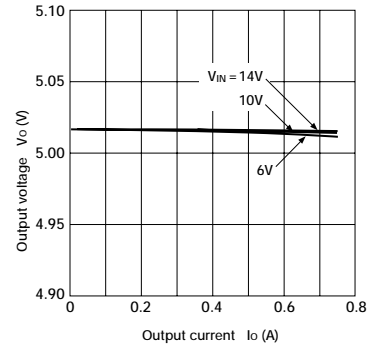
■  $I_o$  vs  $V_{DIF}$  Characteristics



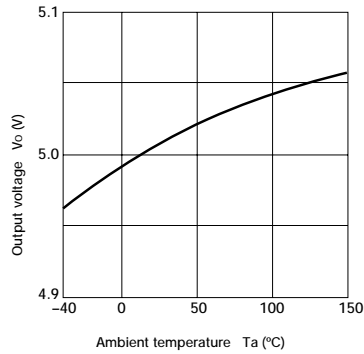
■ Line Regulation



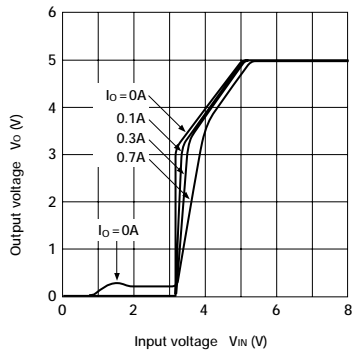
■ Load Regulation



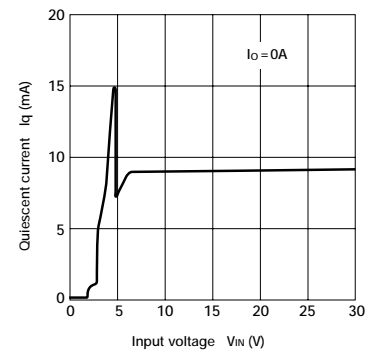
■ Output Voltage Temperature Characteristics



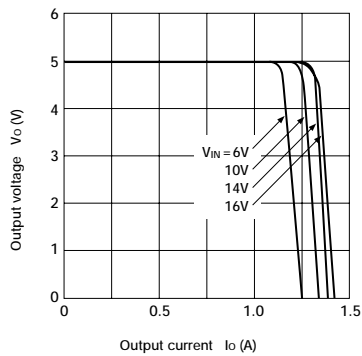
■ Rise Characteristics



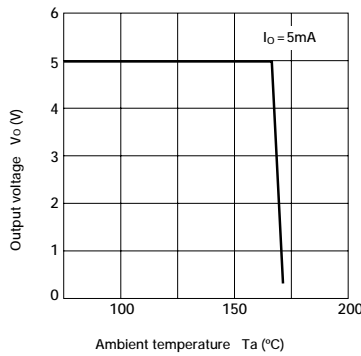
■ Quiescent Circuit Current



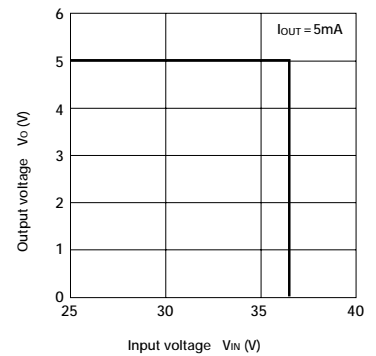
■ Overcurrent Protection Characteristics



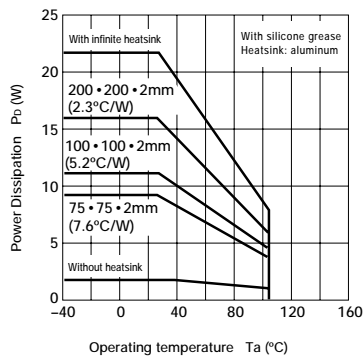
■ Thermal Protection Characteristics



■ Overvoltage Protection Characteristics



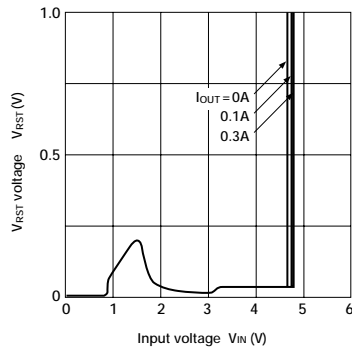
■  $T_a$ — $P_D$  Characteristics



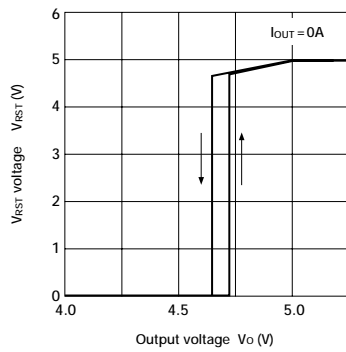
Note on Thermal Protection Characteristics:  
The thermal protection circuit is intended for protection against heat during instantaneous short-circuiting. Its operation, including reliability, is not guaranteed for short-circuiting over an extended period of time.

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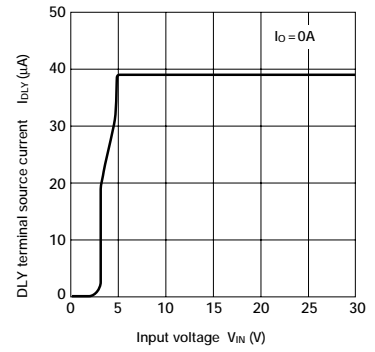
■  $V_{RST}$  Terminal L-level Output Characteristics



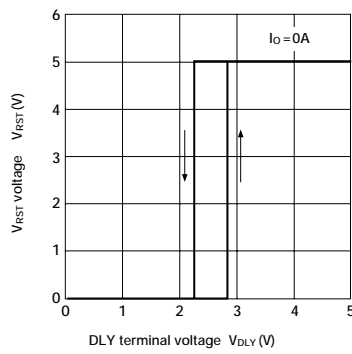
■ Reset Threshold Voltage Characteristics



■ DLY Terminal Source Current Characteristics



■ DLY Terminal Output Voltage Characteristics



■ Reset Signal Delay Characteristics

