# MGA-31289

High-Gain, High-Linearity Driver Amplifier

# Application Note 5488

## Introduction

The MGA-31289 is a highly linear enhancement-mode pseudomorphic high electron mobility transistor (E-pHEMT) amplifier with a frequency range extending from 1.5GHz to 3GHz. The MGA-31289 is a complement of the Avago high-gain and high-linearity driver amplifier series as shown in Table 1. MGA-31289 is a 0.25 W monolithic microwave integrated circuit (MMIC) housed in a standard SOT-89 package – the preferred industrial package for low-power driver amplifiers due to its exceptional thermal dissipation. This device features an excellent Input Return Loss (IRL) and good Output Return Loss (ORL) achieved through the use of internal input match and output pre-match circuits. This reduces the number of external components and the complexity of the manufacturing process.

MGA-31289 operates with a +5 V power supply and draws a nominal current of 120 mA at room temperature. The device delivers an excellent third-order Output Intercept Point (OIP3) of 42 dBm, Small Signal Gain (SSGain) of 19 dB and an Output 1 dB Gain Compression (OP1dB) of 23 dBm. These exceptional performance specifications are achieved through Avago Technologies' proprietary 0.25 µm GaAs E-pHEMT process, making MGA-31289 a good candidate for high-gain and high-linearity applications such as Time Division Long Term Evolution (TD-LTE) and Base Transceiver Station (BTS) repeater modules. The enhancement mode technology provides superior high-linearity performance that allows direct DC grounding at the source pin and the use of an easy-to-build single polarity supply [1].

Besides providing typical application guidelines for issues such as DC bias and impedance matching, this application note focuses on the effect of improving the output return loss towards linearity performance, especially the third-order intercept point (IP3). The method will be systematically discussed with the aid of a 1.6 GHz design example.

**Table 1. Avago high-gain, high-linearity driver amplifier series**

| Part Number | Frequency Band | Gain | OIP3 |
|---|---|---|---|
| MGA-31189 | 0.25 GHz to 1.5 GHz | 21 dB | 42 dBm |
| MGA-31289 | 1.5 GHz to 3 GHz | 19 dB | 42 dBm |

## PCB Material and Layer Stack Design

Figures 1 and 2 show the top and bottom view respectively of the MGA-31289 demonstration circuit board and reveal the component placement. The demo board is a three-layer board containing a Coplanar Waveguide with Ground (CPWG) on the topside serving as RF traces and a solid metal ground plane on the backside. The copper thickness for each layer is 0.5 oz or 0.7 mils. Every copper layer is separated with a dielectric material; the board cross-sectional diagram is shown in Figure 3. The first dielectric material is 10 mils Rogers, RO4350 with a dielectric constant ($\varepsilon_r$) of 3.48. The second dielectric material is for mechanical strength and stability and utilizes FR4 with $\varepsilon_r$ of 4.3. Alternatively, FR-4 or G-10 type material are a good choice for low-cost wireless applications. For noise-figure-critical or high-frequency applications, the additional cost of PTFE/glass dielectric materials may be necessary to minimize transmission line loss at the amplifier's input.

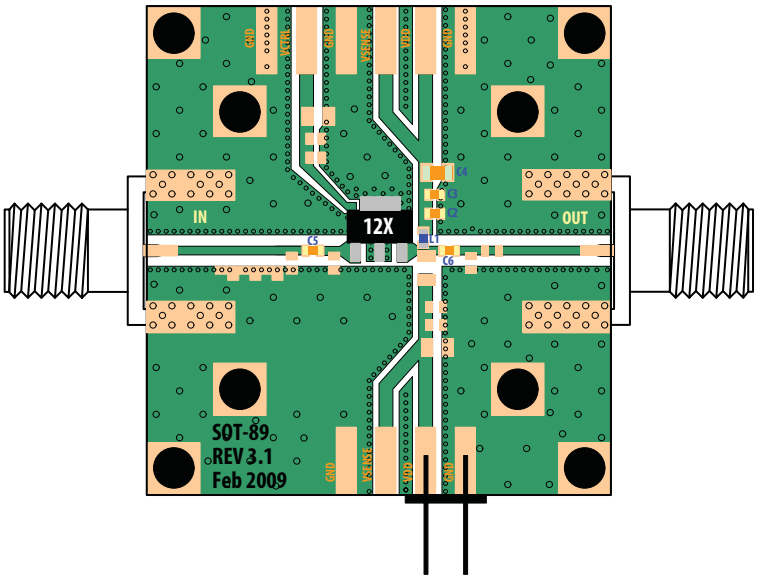


**Figure 1. Demonstration board – top view**

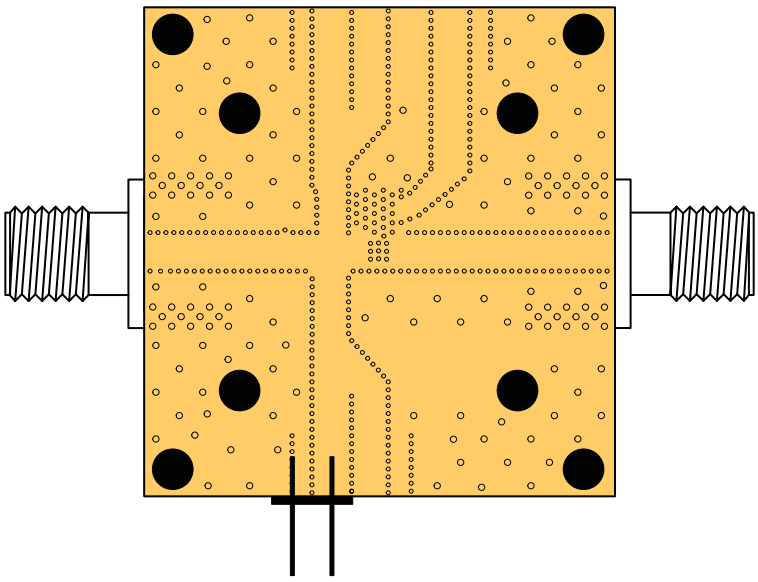

**Figure 2. Demonstration board – bottom view**

## CPWG Design

One can easily determine the dimension of the CPWG lines using AppCAD, the free and handy RF simulation software from Avago Technologies, as shown in Figure 4. An overall board thickness of 62 mil allows the use of SMA connectors from EF Johnson (142-0701-851) at both board edges. The SMA connector's center pin diameter is 20 mil, thus requiring the demo board transmission line width to be slightly wider. Since MMICs are designed for a 50 Ω environment, it is important to ensure that the RF traces have a characteristic impedance ($Z_o$) of 50 Ω, thereby eliminating any possible signal reflection and/or RF performance degradation during operation. This demonstration board utilizes a 22 mil transmission line with a $Z_o$ of 50.1 Ω at 1600 MHz. Some degree of freedom is afforded to the designer to determine the appropriate transmission line width, as long the resultant $Z_o$ is close to 50 Ω and there remains sufficient space for the design.

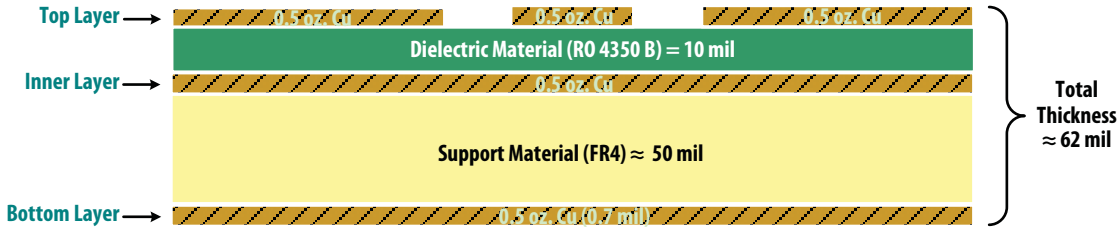


**Figure 3. Demonstration board cross sectional view**

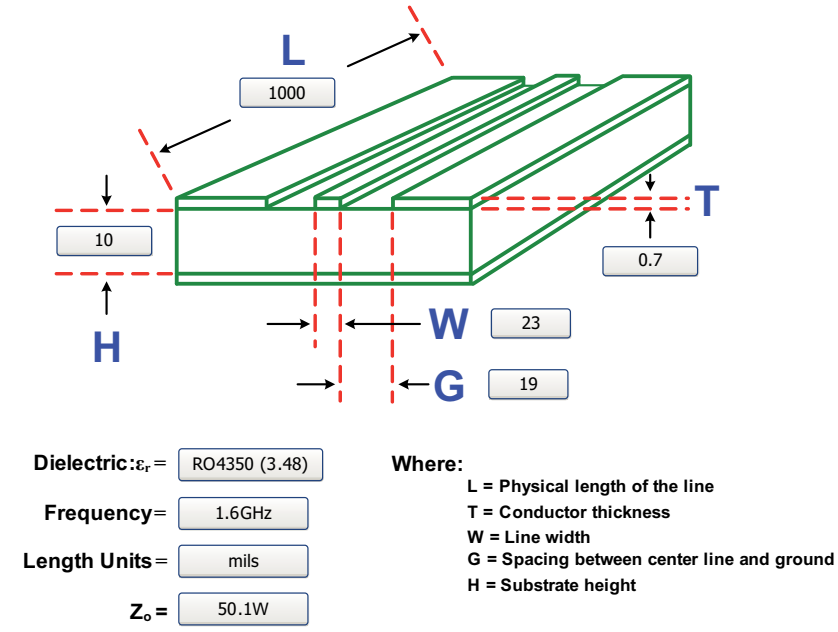


**Figure 4. CPWG Design using AppCAD**

## Application Example – 1.6 GHz

In microwave amplifier design it is desirable to minimize reflected power to ensure most of the power is transferred to the load. Typically, designers aim for at least a 10 dB return loss or 2:1 VSWR. However, the 10dB return loss "rule of thumb" may sometimes be circumvented to achieve better Noise Figure (NF), linearity or gain in a system, as will be discussed in the following section with the aid of the 1.6 GHz design example intended for a Second Stage (Q2) BTS LNA application. MGA-31289 is tuned to meet the following specifications:

1. SSGain of 17-20 dB
2. IIP3 (input third-order intercept point) should be better than +19 dBm
3. Noise Figure (NF) should be less than 3 dB
4. ORL should be better than 20 dB

## Impedance Matching

For most applications, operation of the MGA-31289 only requires the application of a DC bias of +5 V and proper matching of the RF input and output impedances. Modifying the impedance for the input and the output of MGA-31289 enables the designer to effectively introduce trade-offs between linearity, gain, NF and return loss performance. Table 2 briefly lists the input and output parameters required for different types of impedance matching. This application example will reveal the effect on the Output Reflection Coefficient ($\Gamma_L$) as the ORL is improved.

**Table 2. Required impedance matching for NF, IP3, IRL, ORL and Gain**

| Matching Purposes | Input Tuning | Output Tuning |
|---|---|---|
| IP3 | $\Gamma_S$ | $\Gamma_L$ |
| NF | $\Gamma_{opt}$ | none |
| IRL | S11* | none |
| ORL | none | S22* |
| SSGain | S11* | S22* |

The 1.6 GHz amplifier was tuned in accordance with the datasheet's 1.9 GHz circuit configuration as shown in Figure 5. In addition to the 1.9 GHz design reference, the datasheet also provides a recommendation circuit for 2.5 GHz. In order to improve the ORL, the value of capacitor (C6) was reduced while the RF choke (L1) value was gradually increased to observe the effect on IP3 performance. These changes moved the MGA-31289's output impedance closer to the 50 W point while simultaneously time-shifting the $\Gamma_L$ location for the best OIP3.

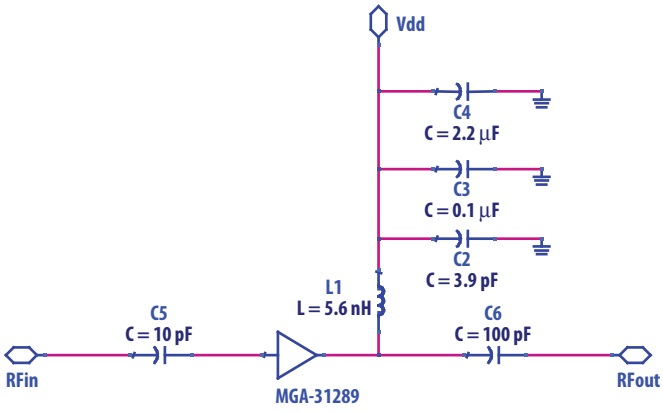


**Figure 5. 1.9 GHz schematic diagram**

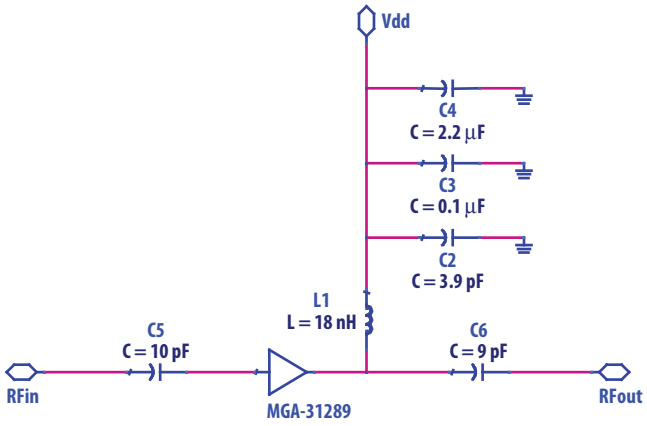


**Figure 6. Suggested 1.6 GHz schematic diagram**

Figure 6 shows the suggested 1.6 GHz circuit (configuration number 6) with the component parts listed in Table 4. This configuration is recommended to provide the desired performance trade-off for IP3 and ORL while minimizing the material parts list. This was done by combining circuit functions, i.e., combining the DC feed, output DC blocking and output matching functions.

Inductor L1 is set at 18 nH and simultaneously serves both as an RF Choke and as part of the output matching network that helps steer the $\Gamma_L$ towards the center of the Smith Chart. The 181 kΩ reactance exhibited by L1 is an exceptional figure to isolate the DC supply from in-band signals [2]. Using a higher Q inductor, (i.e., a wire-wound inductor) will minimize loss and improve IP3 performance. The 0.1 μF (C3) and 2.2 μF (C4) capacitors serve as a DC bypass to short any unwanted low-frequency signals to ground, especially signals from the Voltage supply rail. If any high-frequency signals are created by or enter the DC supply, a 3.9 pF (C2) capacitor will short them to ground as well. Since a coupling capacitor or DC block is best selected so that its impedance at the frequency of interest is as low as possible, values of 10 pF for C5 and 9 pF for C6 were chosen to provide a mere 6 μ of impedance.

**Table 3. Component parts list for 1.6 GHz design**

| Reference Designator | Value | Size | Part Number | Description |
|---|---|---|---|---|
| C2 | 3.9 pF | 0402 | MURATA, GRM1555C1H3R9CZ01 | RF Bypass |
| C3 | 0.1 μF | 0402 | MURATA, GRM155R71C104KA88D | DC Bypass |
| C4 | 2.2 μF | 0805 | MURATA, GRM21BR61E225KA12L | DC Bypass |
| C5 | 10 pF | 0402 | MURATA, GRM1555C1H100JZ01 | DC Blocking |
| C6 | 9 pF | 0402 | MURATA, GRM1555C1H9R0DZ01 | DC Blocking |
| L1 | 18 nH | 0402 | TOKO, LL1005-FHL18NJ | RF Choke |

## Performance of MGA-31289 at 1.6 GHz

Clearly, an improvement of ORL is possible at the expense of IP3 performance, as shown in Table 4 which lists the effect of improving the ORL towards the IIP3 and SSGain performance. Referring to the specification, circuit configuration 6 simultaneously produces an ORL greater than 20 dB and an IIP3 greater than 19 dBm. Figure 7 shows the $\Gamma_L$ for each circuit configuration which were obtained using ADS Momentum from Agilent Technologies [3].

Biased with +5V of Vdd and a nominal current of 120 mA, circuit configuration 6 delivers an SSGain of 19.5 dB as shown in Figure 9. Figure 8 shows the return loss curves for MGA-31289 when tuned for 1.6 GHz. The narrowband impedance matching approach allows MGA-31289 to produce an exceptionally good IRL (about -21.9dB) while ORL is about -20.5 dB at 1.6 GHz. Figure 10 exemplifies the 1.6 GHz reverse isolation for MGA-31289 which is about -26.9 dB. As for linearity performance, the MGA-31289 produces 19.1 dBm of IIP3 and 22.7 dBm of OP1dB at 1.6 GHz. The NF for the device is about 2.1 dB at 1.6 GHz. Table 5 lists the MGA-31289's performance at 1.6 GHz.

**Table 4. MGA-31289 Tuning & Performance Trade-off**

| | Configuration | Gain | ORL | OIP3 | IIP3 |
|---|---|---|---|---|---|
| 1 | 1.9 GHz BOM | 18.6 | -8.0 | 42.35 | 23.75 |
| 2 | C6 = 10 pF | 18.9 | -10.0 | 41.52 | 22.62 |
| 3 | C6 = 3.3 pF | 19.0 | -12.0 | 40.11 | 21.11 |
| 4 | L1 = 18 nH and C6 = 11 pF | 19.4 | -19.3 | 38.70 | 19.30 |
| 5 | L1 = 18 nH and C6 = 10 pF | 19.4 | -19.9 | 38.60 | 19.20 |
| 6 | L1 = 18 nH and C6 = 9 pF | 19.5 | -20.5 | 38.60 | 19.10 |

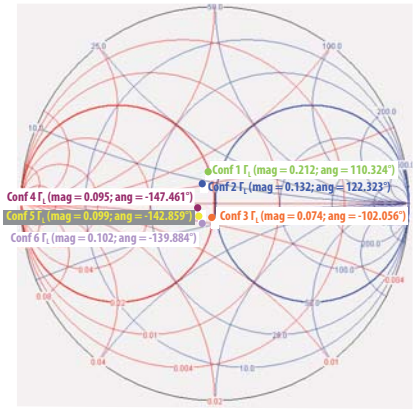


**Figure 7. $\Gamma_L$ location for each circuit configuration**

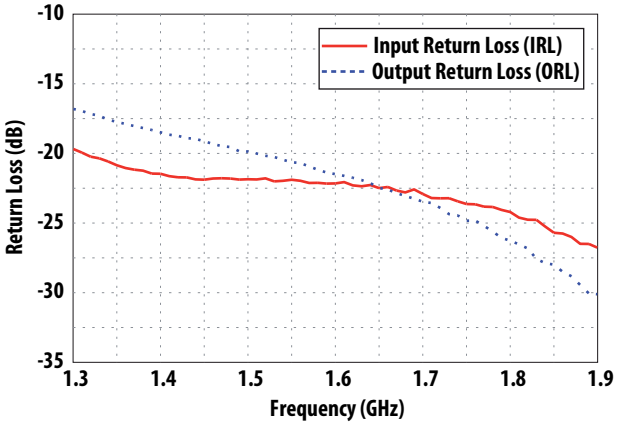


Figure 8. Input and Output Return Loss

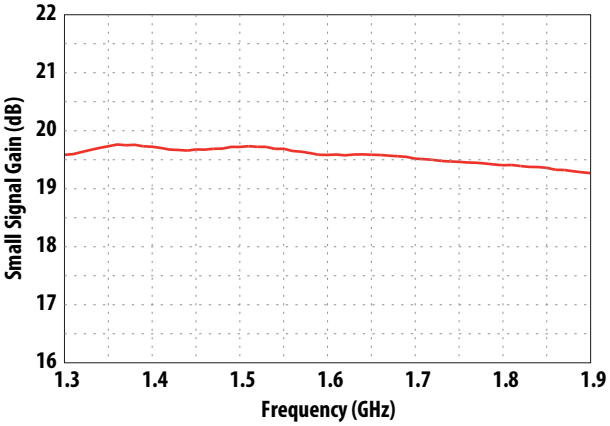


Figure 9. Small Signal Gain

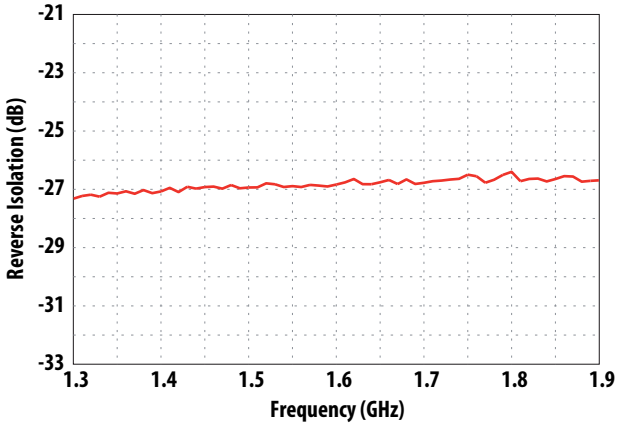


Figure 10. Reverse Isolation

**Table 5. MGA-31289 performance summary at 1.6 GHz**

| Parameter | Performances | Unit |
|---|---|---|
| Frequency | 1.6 | GHz |
| Input Return Loss (IRL) | -21.9 | dB |
| Small Signal Gain (SSGain) | 19.5 | dB |
| Reverse Isolation (ISO) | -26.9 | dB |
| Output Return Loss (ORL) | -20.5 | dB |
| Noise Figure (NF) | 2.1 | dB |
| Input Third-Order Intercept Point (IIP3) | 19.1 | dBm |
| Output Third-Order Intercept Point (OIP3) | 38.6 | dBm |
| Output 1 dB Gain Compression Point (OP1dB) | 22.7 | dBm |

## Phase Reference Plane

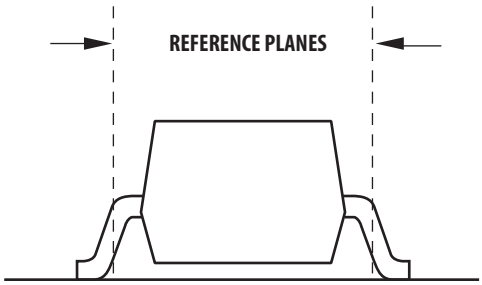


**Figure 11. MGA-31289 phase reference plane**

The positions of the reference planes used to specify the S-Parameters and Noise Parameters for MGA-31289 are shown in Figure 11. As seen in the illustration, the reference planes are located at the point where the package leads contact the TRL board (10 mil Rogers RO4350).

## PCB Design and Layout Guidelines

The details of recommended PCB land pattern, stencil design and reflow profile for Avago SOT89 device can be found in Application Note 5051 [4] from Avago website.

## Conclusion

This application note demonstrates the versatility of the MGA-31289 by showing how the device can be tuned for an application that requires either high linearity or good output return loss with a small amount of acceptable trade-offs. With proper input and output impedance matching of the MGA-31289, it is possible to produce an exceptionally good input return loss and at the same time, good linearity is guaranteed.

## References

[1] "Characteristics of E-pHEMT vs. HBTs for PA Applications, White Paper, Avago Technologies, March 2010.

[2] "MGA-53543", Datasheet, Avago Technologies.

[3] "70 to 500 MHz Amplifier for IF Applications using the Avago Technologies MGA-31189 Amplifier", Application Notes, Avago Technologies.

[4] "SOT89 Package", Application Note 5051, Avago Technologies.

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