National Semiconductor

LM604 4 Channel Mux-Amp

General Description

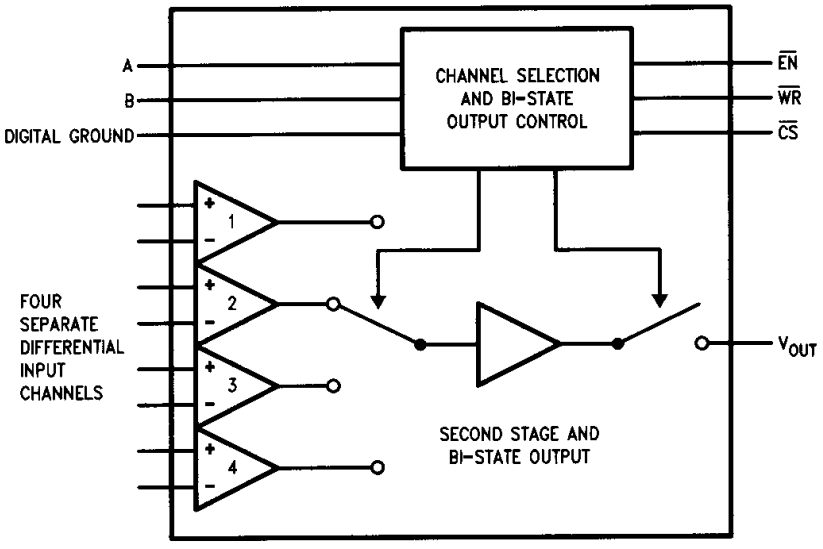
The LM604 Mux-Amp is an op-amp with four selectable differential inputs, combining the functions of a multiplexer with an op-amp. The LM604 can select, buffer, and amplify one of four different input signals, providing a complete system for multiplexing analog signals. It also has the unique Bi-State output which allows two or more Mux-Amps to be connected together at their outputs to increase the number of multiplexed channels. Channel selection and the Bi-State output are controlled by internal logic that interfaces directly to a microprocessor. Besides these unique features, the LM604 has excellent AC and DC op-amp specifications and is internally compensated.

Applications include signal multiplexing and linear circuits that are controlled by digital signals (i.e., programmable gain blocks, filters, and other op-amp circuits).

Features

- Multiplexes four differential input channels to a single op-amp
- Easy to interface to microprocessor, or operates "stand alone"
- Bi-State output: Operates in two states, Active and Disabled. When disabled, it becomes a high impedance.
- Wide operating voltage range
  - single supply: 4V to 32V
  - split supply: ±2V to ±16V
- Wide input common mode range: V^- to $V^+ - 1V$
- Fast channel to channel switching time: 5 μs
- Output will drive a 600Ω load

Block Diagram



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Channel Selection

A	B	WR	CS	Channel
0	0	0	0	1
0	1	0	0	2
1	0	0	0	3
1	1	0	0	4
X	X	X	1	Unchanged
X	X	1	X	Unchanged

Bi-State Output Control

EN	WR	CS	Output State
0	0	0	Enabled
1	0	0	Disabled, High Z
X	X	1	Unchanged
X	1	X	Unchanged

Order Number LM604AMJ, LM604IJ, LM604IN, LM604ACN, LM604CN, LM604ACM, or LM604CM
See NS Package Number J18A, N18A or M20B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36V or ±18V
Differential Input Voltage	±Supply Voltage
Input Voltage Range	±Supply Voltage
Output Short Circuit to Gnd	Continuous (Note 1)
ESD Tolerance (C_{ZAP} = 120 pF, R_{ZAP} = 1500Ω)	2,000V
Lead Temperature (Soldering, 5 sec.)	300°C
Storage Temperature Range	−65°C to 150°C

Operating Ambient Temperature Range

LM604AM	$-55°C \le T_A \le 125°C$
LM604I	$-40°C \le T_A \le 85°C$
LM604AC, LM604C	$0°C \le T_A \le 70°C$

	J Pkg.	M Pkg.	N Pkg.
Power Dissipation (Note 2)	1,600 mW	1,500 mW	1,900 mW
T_{JMAX}	150°C	150°C	150°C
θ_{JA} (Typical, Board Mounted)	75°C/W	83°C/W	65°C/W

DC Electrical Characteristics V_{SUPPLY} = ±15V (Note 3)

Parameter	Conditions		Typical	LM604AM		LM604I		LM604AC LM604C		Units (Limit)
				Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage (V_{OS})	R_S = 10 kΩ	LM604	1.0			3.0	**5.0**	3.0	**5.0**	mV (Max)
		LM604A	0.5	1.0 **3.0**				1.0	**3.0**	
V_{OS} Temperature Drift			5.5							µV/°C
Input Offset Current (I_{OS})			2	10 **12**		10	**12**	10	**12**	nA (Max)
I_{OS} Temperature Drift			10							pA/°C
Input Bias Current (I_B)		LM604	50			80	**100**	80	**100**	nA (Max)
		LM604A	30	50 **60**				50	**60**	
I_B Temperature Drift			55							pA/°C
Input Common Mode Voltage Range		Upper Limit	14.0	13.5 **13.0**		13.5	**13.0**	13.5	**13.0**	V (Min)
		Lower Limit	−15.0	−15.0 **−15.0**		−15.0	**−15.0**	−15.0	**−15.0**	V (Max)
Input Resistance			1.0							Meg Ω
Output Voltage Swing	R_L = 10 kΩ	Upper Limit	13.4	13.0 **12.5**		13.0	**12.5**	13.0	**12.5**	V (Min)
		Lower Limit	−14.2	−13.8 **−13.3**		−13.8	**−13.3**	−13.8	**−13.3**	V (Max)
	R_L = 600Ω	Upper Limit	12.7	12.3 **10.0**		12.3	**10.0**	12.3	**10.0**	V (Min)
		Lower Limit	−12.6	−12.2 **−11.7**		−12.2	**−11.7**	−12.2	**−11.7**	V (Max)
Large Signal Voltage Gain	V_{OUT} = ±10V	R_L = 2 kΩ	200	50 **25**		50	**25**	50	**25**	V/mV (Min)
		R_L = 600Ω	200	50 **25**		50	**25**	50	**25**	
Common Mode Rejection Ratio	V_{CM} = −15.0V to 13.5V		100	80 **70**		80	**70**	80	**70**	dB (Min)

DC Electrical Characteristics V_{SUPPLY} = ±15V (Note 3)

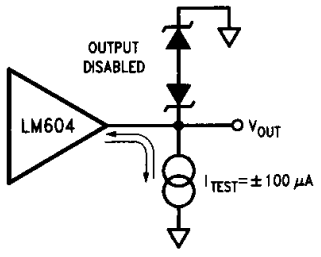
Parameter	Conditions	Typical	LM604AM		LM604I		LM604AC LM604C		Units (Limit)
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Power Supply Rejection Ratio	V_{SUPPLY} = ±5.0V to ±16.0V	100	80 **70**		80	**70**	80	**70**	dB (Min)
Output Short Circuit Current		±35	±50 **±60**		±50	**±60**	±50	**±60**	mA (Max)
Output Leakage Current	V_{OUT} = −13.5V to 13.0V Bi-State Output Disabled	4.0	10.0 **20.0**		10.0	**20.0**	10.0	**20.0**	µA (Max)
Output Capacitance	Bi-State Output Disabled See *Figure 1*	10							pF
Supply Current		7.0	9.0 **10.0**		9.0	**10.0**	9.0	**10.0**	mA (Max)

AC Electrical Characteristics V_{SUPPLY} = ±15V (Note 3)

Parameter	Conditions	Typical	LM604AM		LM604I		LM604AC LM604C		Units (Limit)
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Slew Rate	A_V = 1, R_L = 2 kΩ	3.0	2.0 **1.5**		2.0	**1.5**	2.0	**1.5**	V/µs (Min)
Gain Bandwidth Product	f = 100 kHz	7.0	6.0 **3.0**		6.0	**3.0**	6.0	**3.0**	MHz (Min)
Unity Gain Frequency		3.0		2.5		2.5		2.5	MHz (Min)
Phase Margin	R_L = 2 kΩ, C_L = 200 pF	50							Degrees
Settling Time to 0.1% of Final Value	A_V = −1, V_{OUT} = −5.0V to 5.0V R_L = 2 kΩ	4.0							µs
Channel Switching Time	See *Figure 2* t_{SW1} t_{SW2}	4.0 5.0	5.5 **6.5**	 6.5	5.5	**6.5** 6.5	5.5	**6.5** 6.5	µs (Max)
Channel to Channel Isolation	R_S = 10 kΩ, f = 10 kHz V_{IN} = 10.0V_{p-p}	100							dB
Input Noise Voltage	R_S = 100 Ω, f = 1 kHz	20							nV/√Hz
Input Noise Current	f = 1 kHz	0.3							pA/√Hz
Mux-Amp Enable Time	See *Figure 3* t_{EN1} t_{EN2}	3.0 4.0	4.0 **5.0**	 5.5	4.0	**5.0** 5.5	4.0	**5.0** 5.5	µs (Max)
Mux-Amp Disable Time (t_{DIS})	See *Figure 3*	1.0	2.0 **3.0**		2.0	**3.0**	2.0	**3.0**	µs (Max)

DC Electrical Characteristics V_{SUPPLY} = 5V (Note 3)

Parameter	Conditions		Typical	LM604AM		LM604I		LM604AC LM604C		Units (Limit)
				Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage	R_S = 10 kΩ V_{OUT} = 2.0V	LM604 LM604A	1.0 0.5	 1.0 **3.0**		3.0	**5.0**	3.0 1.0	**5.0** **3.0**	mV (Max)
Input Offset Current	V_{OUT} = 2.0V		3.0	10 **18**		10	**18**	10	**18**	nA (Max)
Input Bias Current	V_{OUT} = 2.0V	LM604 LM604A	70 50	 80 **110**		130	**150**	130 80	**150** **110**	nA (Max)
Input Common Mode Voltage Range	V_{OUT} = 2.0V	Upper Limit	4.0	3.5 **3.0**		3.5	**3.0**	3.5	**3.0**	V (Min)
		Lower Limit	0	0 **0**		0	**0**	0	**0**	
Output Voltage Swing	R_L = 10 kΩ	Upper Limit	3.5	3.2 **3.0**		3.2	**3.0**	3.2	**3.0**	V (Min)
		Lower Limit	0.5	0.7 **0.8**		0.7	**0.8**	0.7	**0.8**	V (Max)
	R_L = 600Ω	Upper Limit	3.3	3.0 **2.8**		3.0	**2.8**	3.0	**2.8**	V (Min)
		Lower Limit	0.4	0.6 **0.7**		0.6	**0.7**	0.6	**0.7**	V (Max)
Large Signal Voltage Gain	V_{OUT} = 0.8V to 2.8V	R_L = 2 kΩ	200		50 **25**		50 **25**		50 **25**	V/mV (Min)
		R_L 600Ω	200		50 **25**		50 **25**		50 **25**	
Common Mode Rejection Ratio	V_{CM} = 0V to 3.5V V_{OUT} = 2.0V		100	80 **70**		80	**70**	80	**70**	dB (Min)
Power Supply Rejection Ratio	V^+ = 4.0V to 5.0V V_{OUT} = 2.0V		100	80 **70**		80	**70**	80	**70**	dB (Min)



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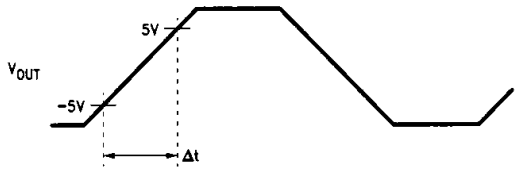

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$$C_{OUT} = \frac{\Delta t}{10V} \times 100\ \mu A$$

FIGURE 1. Output Capacitance Test

Digital Input Electrical Characteristics $V_{SUPPLY} = \pm 15V$ (Note 6)

Parameter	Conditions	Typical	LM604AM		LM604I		LM604AC LM604C		Units (Limit)
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
V_{INHI}			1.8 **2.0**		1.8	**2.0**	1.8	**2.0**	V (Min)
V_{INLO}			1.0 **0.8**		1.0	**0.8**	1.0	**0.8**	V (Max)
I_{INHI}			5.0 **10.0**		5.0	**10.0**	5.0	**10.0**	μA (Max)
I_{INLO}			5.0 **10.0**		5.0	**10.0**	5.0	**10.0**	μA (Max)
Minimum Pulse Width for WR & CS				**100**		**100**		**100**	ns (Min)
Minimum Set-Up Time (t_S)	See *Figures 3* and *5*			**100**		**100**		**100**	ns (Min)
Minimum Hold Time (t_H)	See *Figures 3* and *5*			**50**		**50**		**50**	ns (Min)
Input Capacitance		5							pF

Note 1: Applies to both single and split supply operation. Continuous short circuit operation can result in exceeding the maximum allowed junction temperature.

Note 2: When operating at $T_A > 25°C$, the maximum power dissipation must be derated based on θ_{JA}.

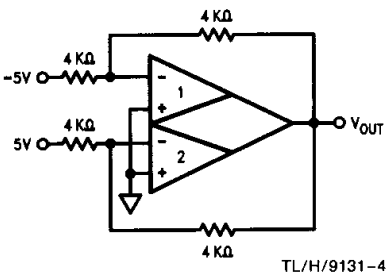
Note 3: Unless specified otherwise, all limits are guaranteed for $T_A = T_J = 25°C$, $V_{CM} = 0V$, $V_{OUT} = 0V$, and $R_L > 1Meg\Omega$. **Boldface** limits apply at $0°C \le T_J \le 70°C$ for LM604AC and LM604C, $-40°C \le T_J \le 85°C$ for LM604I, and $-55°C \le T_J$ 125°C for LM604AM.

Note 4: Guaranteed and 100% production tested.

Note 5: Guaranteed but not 100% production tested. These numbers are not used to calculate outgoing quality levels.

Note 6: Unless specified otherwise, all units are guaranteed at $T_A = T_J = 25°C$. **Boldface** limits apply at the junction temperature extremes specified in note 3. Input voltage levels are with respect to digital ground (pin 4) which must be at least 4.0V below V^+.

Switching from Channel 1 to 2 with Channel Select preset to $\overline{AB}$ before $\overline{WR}$ = 0. This test applies to all channels.



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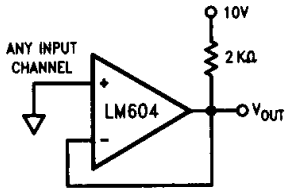

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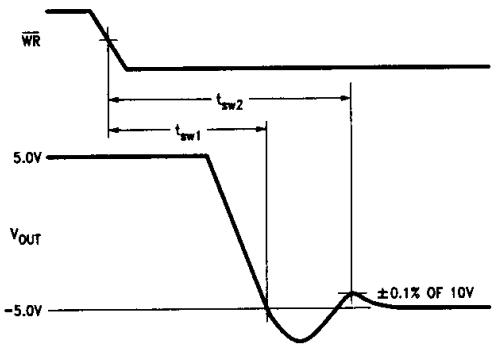

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FIGURE 2. Channel Switching Time Test

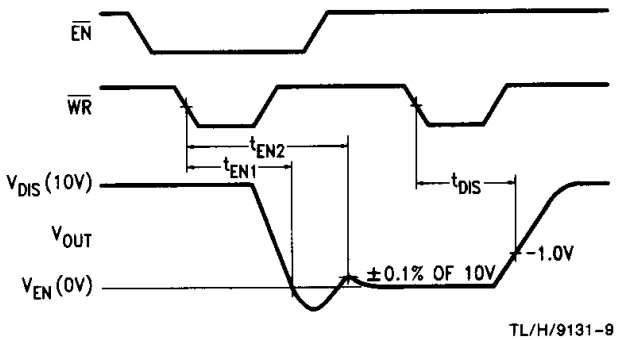

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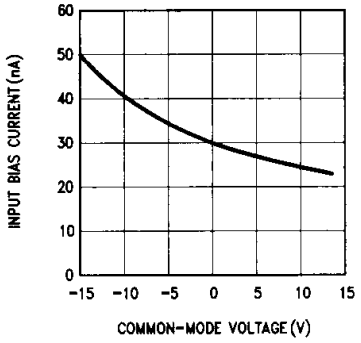
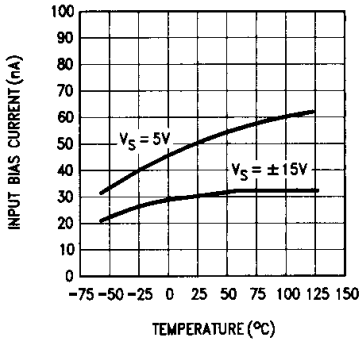
FIGURE 3. Bi-State Output Enable and Disable Time Test

Typical Performance Characteristics (Note 7)

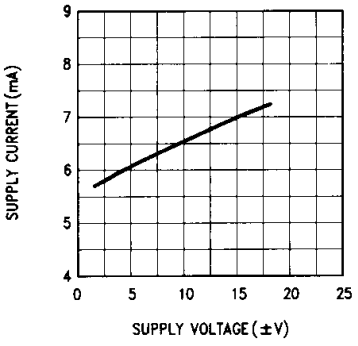
Input Bias Current vs Input Common-Mode Voltage



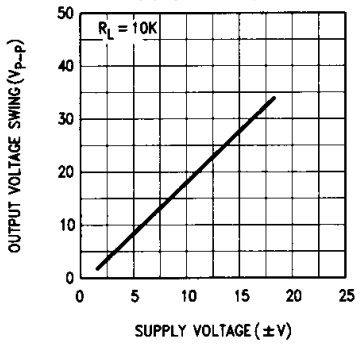
Input Bias Current vs Temperature



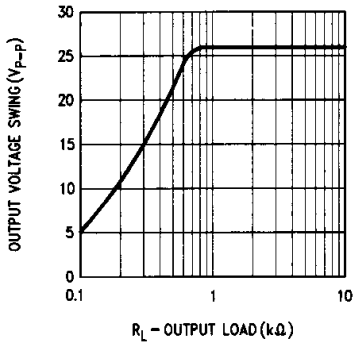
Supply Current vs Supply Voltage



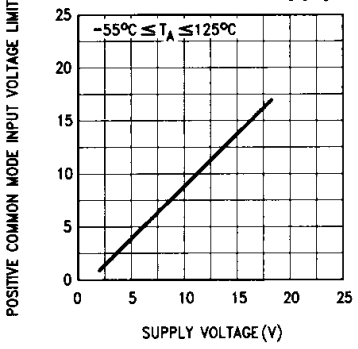
Output Voltage Swing vs Supply Voltage



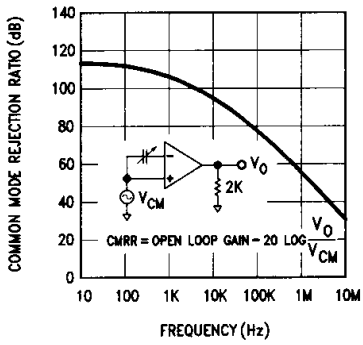
Output Voltage Swing vs Output Load Resistance



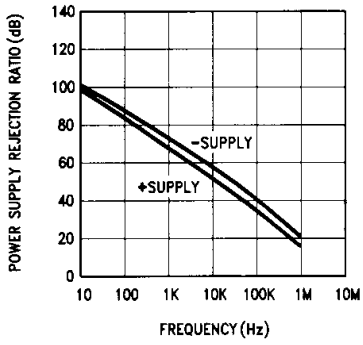
Upper Common-Mode Voltage Limit vs Positive Supply Voltage



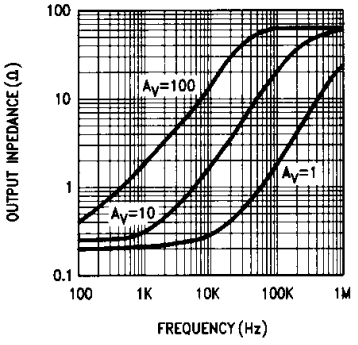
Common-Mode Rejection Ratio vs Frequency



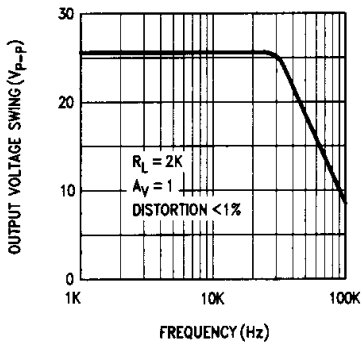
Power Supply Rejection Ratio vs Frequency



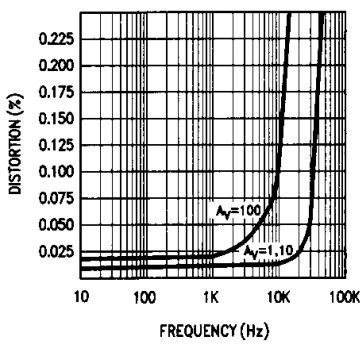
Output Impedance vs Frequency



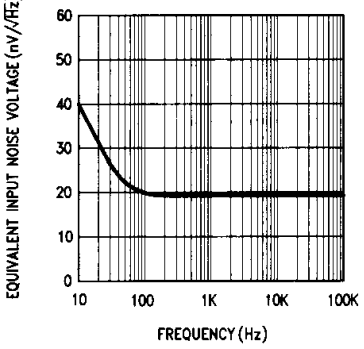
Undistorted Output Voltage Swing vs Frequency



Distortion vs Frequency



Equivalent Input Noise Voltage vs Frequency



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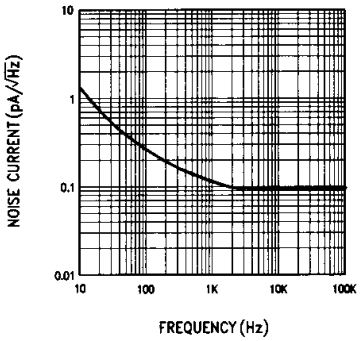
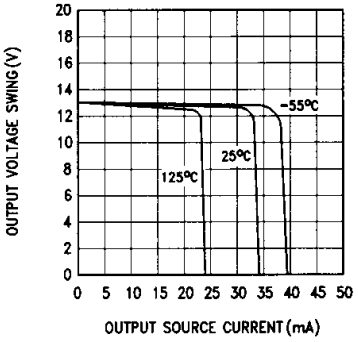
Typical Performance Characteristics (Note 7)

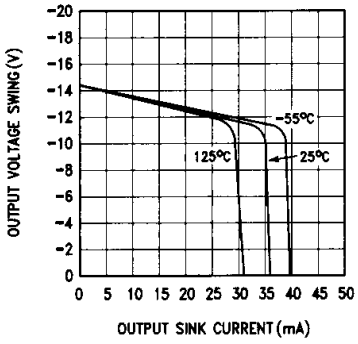
Equivalent Input Noise Current vs Frequency



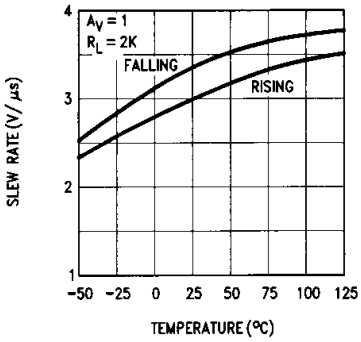
Positive Current Limit



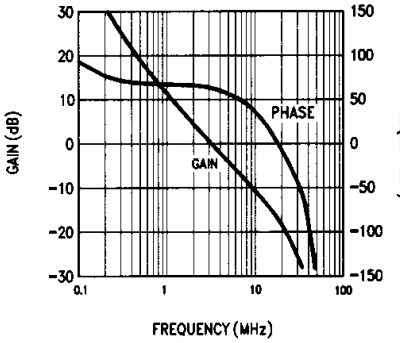
Negative Current Limit



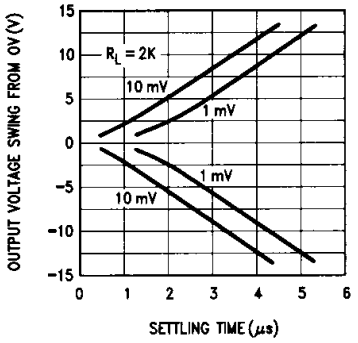
Slew Rate vs Temperature



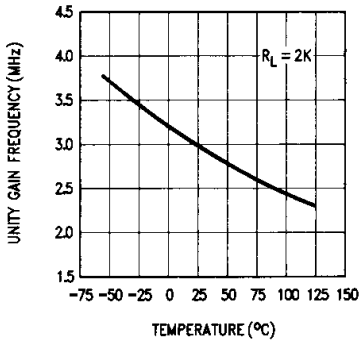
Bode Plot



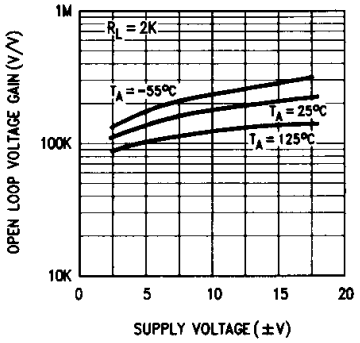
Inverter Settling Time vs Output Voltage Swing



Unity Gain Frequency vs Temperature



Open Loop Voltage Gain



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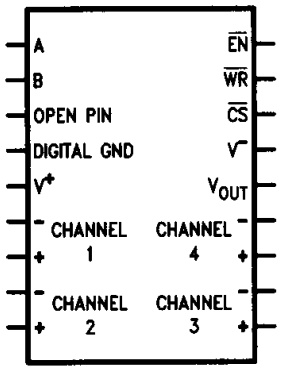
Note 7: Unless specified otherwise, $T_A = T_J = 25°C$, $V_S = \pm 15V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, and $R_L > 1$ Meg.

Connection Diagrams

18 Pin Dual-In-Line Package



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20 Pin Small Outline Package

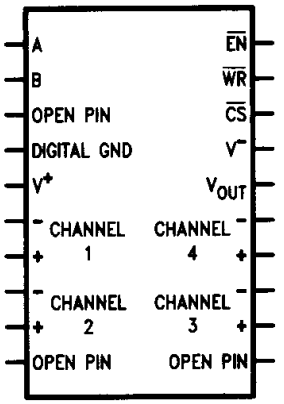

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FIGURE 4

Timing Diagrams

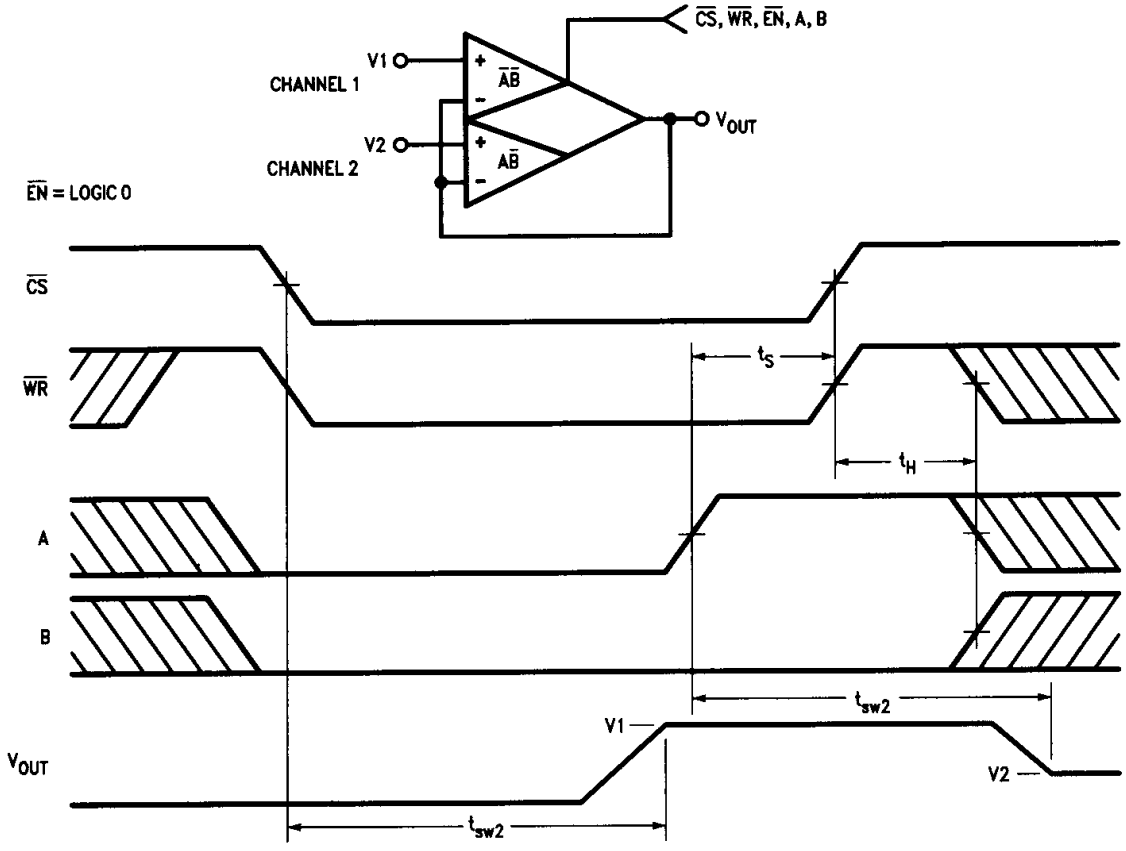

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FIGURE 5. Channel Switching Timing Diagram

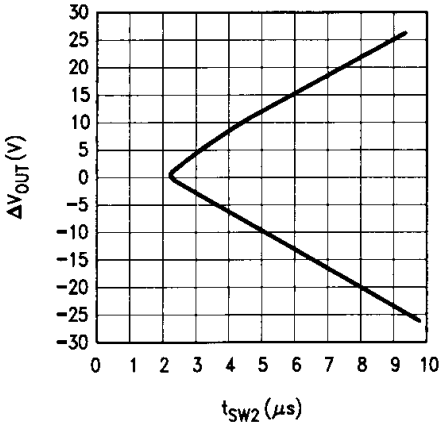
Functional Description

INPUT CHANNEL SELECTION

The LM604 contains four differential input channels that are selected one at a time. An input is selected by writing its binary code to pins A and B when $\overline{CS}$ and $\overline{WR}$ are a logic 0, see block diagram. The LM604 always has one of its inputs selected. In order to isolate all four channels from the output, the Bi-State output can be disabled.

Figure 5 illustrates how the LM604 switches from one channel to another. The switching begins on the falling edge of $\overline{WR}$ if A and B are valid before $\overline{WR}$ is a logic 0, or when A and B become valid while $\overline{WR}$ is a logic 0. In either case, the channel switching time (t_{SW2}) remains the same. If a channel is to remain selected, its binary code must be valid during the rising edge of $\overline{WR}$ as specified by t_S and t_H.

Channel switching time is specified by t_{SW1} and t_{SW2} as shown in *Figure 2*. t_{SW1} is the time it takes the output to first reach its new value, and t_{SW2} is the time it takes the output to settle to within 0.1% of its new value. Clearly, t_{SW2} is a more useful parameter for specifying switching time, but it is difficult to test on a production basis. Therefore, t_{SW1} is tested and this allows t_{SW2} to be guaranteed. Channel switching time will vary as a function of how far the output swings to reach its new value. This is shown in *Figure 6* where t_{SW2} is plotted as a function of output voltage swing (ΔV_{OUT}).



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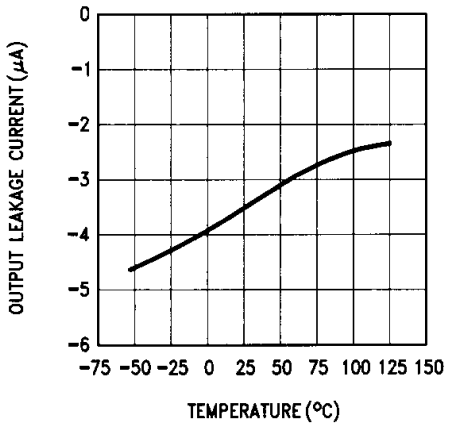
$\Delta V_{OUT} = V_{OUT}$ (Selected Channel) − V_{OUT} (Previous Channel)

FIGURE 6. t_{SW2} vs ΔV_{OUT}

BI-STATE OUTPUT

The Bi-State output can be either enabled (on) or disabled (off). When disabled, the output becomes a high impedance load that can be driven by another output stage. This allows several Mux-Amps to be connected together at their outputs by having only one output enabled at one time. Thus, several Mux-Amps can be in parallel to the same output to increase the number of multiplexed channels. The Bi-State output is controlled by $\overline{EN}$ when $\overline{CS}$ and $\overline{WR}$ are a logic 0, see block diagram.

When the output is disabled and driven by another output, it behaves like a small capacitive load with a few microamps of leakage current. The data sheet specifies this with the parameters "Output Capacitance" and "Output Leakage Current". Both parameters vary with temperature, as shown in *Figure 7*.



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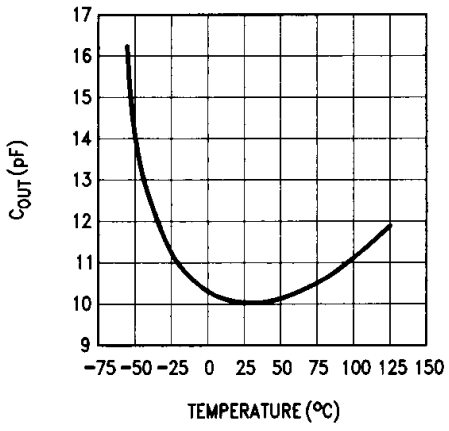

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FIGURE 7. $I_{LEAKAGE}$ and C_{OUT} vs Temperature

Figure 8 illustrates switching between two Mux-Amps that are connected in parallel to the same output. Switching begins on the falling edge of $\overline{WR}$ if the $\overline{EN}$ signals are correctly set before $\overline{WR}$ is a logic 0, or when the $\overline{EN}$ signals become valid while $\overline{WR}$ is a logic 0. The Bi-State output takes less time to become disabled than it does to become enabled, and this insures the outputs are switched in a "break before make" method. If an in output is to remain enabled or disabled after $\overline{WR}$ becomes a logic 1, $\overline{EN}$ must be valid during the rising edge of $\overline{WR}$ as specified by t_S and t_H. Note that when a Mux-Amp has its output enabled, the binary code for the selected input channel must also be written.

Bi-State output enable time (t_{EN1} and t_{EN2}) and disable time (t_{DIS}) are defined in *Figure 3*. t_{EN1} is the time it takes the output to first reach its enabled value (V_{EN}), and t_{EN2} is the time it takes the output to settle to within 0.1% of V_{EN}. As with channel switching time, t_{EN1} is a tested parameter that allows t_{EN2} to be guaranteed. t_{DIS} is the time it takes the output to become a high impedance. Output enable time will vary according to how far the output swings from V_{DIS} to V_{EN}, and this is plotted in *Figure 9*.

Functional Description (Continued)

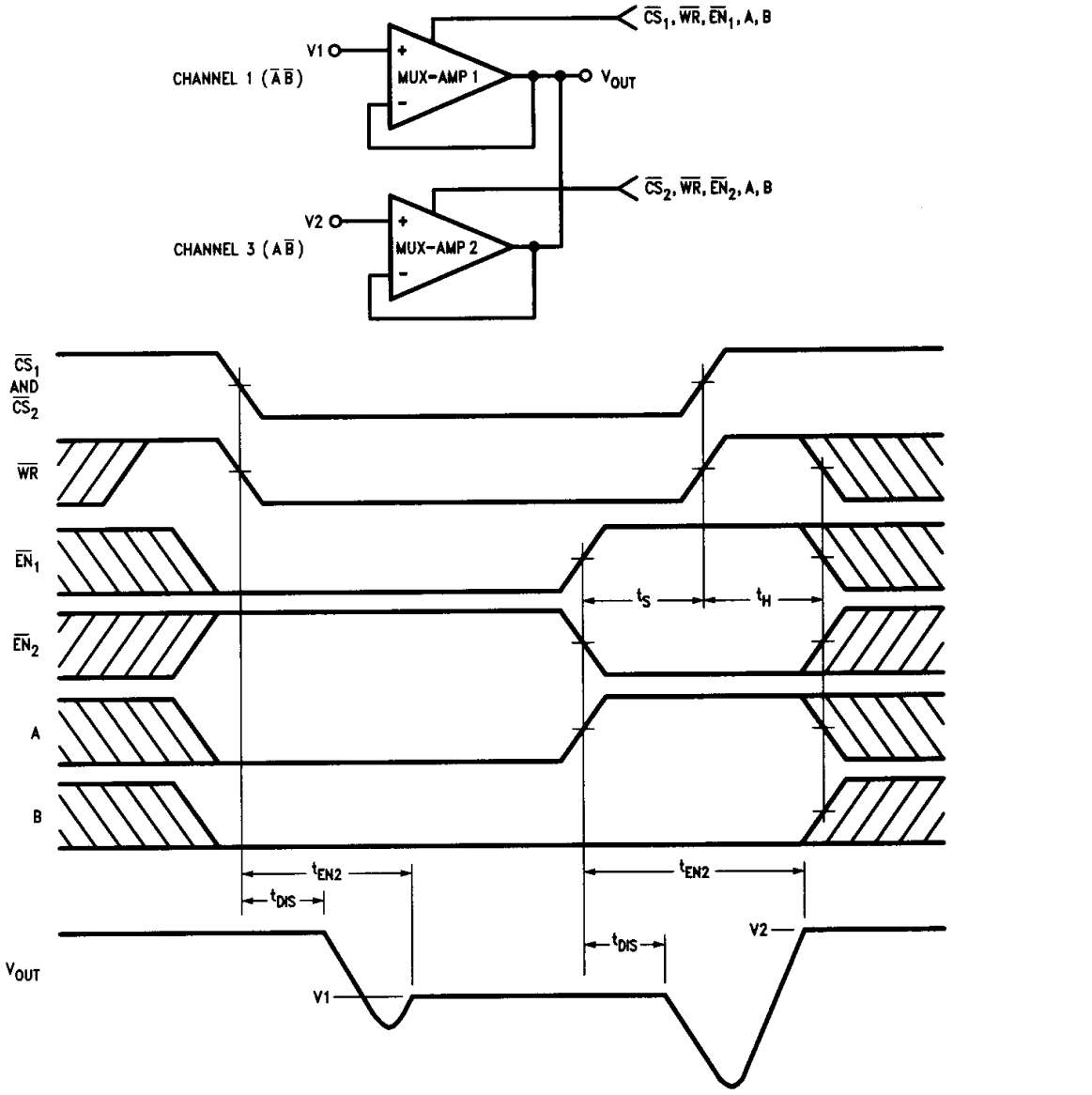

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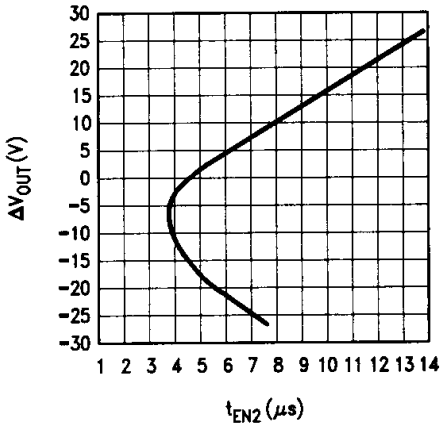
FIGURE 8. Timing Diagram for Switching Bi-State Outputs



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$\Delta V_{OUT} = V_{EN} - V_{DIS}$

FIGURE 9. t_{EN2} vs ΔV_{OUT}

DIGITAL CONTROL

As mentioned in the previous sections, the input channels and Bi-State output are controlled by logic levels on pins A, B, and $\overline{EN}$. There are two ways to apply logic levels to these pins. 1) Hardwire $\overline{WR}$ and $\overline{CS}$ directly to digital ground so that the LM604 operates in a "stand alone" mode. This allows input logic levels to directly control the LM604. 2) Write digital signals to A, B, and $\overline{EN}$ as shown in the timing diagrams of *Figures 5* and *8*. This method is used when the LM604 interfaces to a microprocessor. Note that $\overline{CS}$ and $\overline{WR}$ can occur simultaneously, so set-up and hold times are not required for $\overline{CS}$. Also, notice that $\overline{WR}$ must remain a logic 1 during the hold time period.

Input logic levels are referenced to a 1.4V threshold voltage, making the LM604 compatible with TTL and CMOS logic. This threshold voltage is referenced to digital ground. The voltage level of digital ground can be as low as V^- (pin 15) and as high as 4V below V^+ (pin 5).

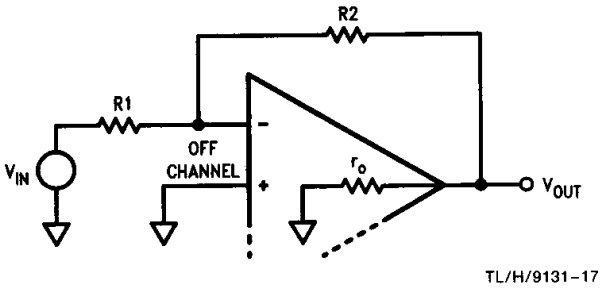
Application Hints

USING MULTIPLE FEEDBACK LOOPS

Each input channel of the LM604 is used as a single op-amp with its own feedback loop. Two examples of this are circuits with multiple inverting gain channels and non-inverting gain channels (*Figure 10*). These circuits have multiple feedback loops connected to the same output with one feedback loop connected to a selected channel and the others connected to "off" channels. The feedback loop of the selected channel determines the gain of these circuits. The off channel feedback loops affect these circuits in two ways. 1) They create an additional load at the output. 2) Feedback loops for inverting gain channels provide feedthrough paths from the inputs of the off channels to the output.

In *Figure 10*, the loading affect of multiple feedback loops is given in terms of current flowing through the feedback loops (I_F). In circuits with non-inverting gain channels, I_F is a function of V_{OUT} and the resistance of the feedback loops. In circuits with inverting gain channels, I_F is different for each channel selected because it is also a function of the off channel input voltages. This additional loading must be accounted for when designing Mux-Amp circuits. Otherwise, the output load resistance will be less than anticipated.

Figure 11 illustrates feedthrough in an off inverting gain channel. Feedthrough occurs because the feedback resistors and the Mux-Amp output impedance (r_o) form a voltage divider. This divider allows a portion of the off channel's input signal to appear at the output. The amount of signal that feeds through depends on the ratio of output impedance to feedback loop resistance. Output impedance varies according to Mux-Amp gain (gain of the selected channel) and the frequency of the feedthrough signal. This variation must be considered when calculating feedthrough, and it is plotted in the "Typical Device Characteristics" section.



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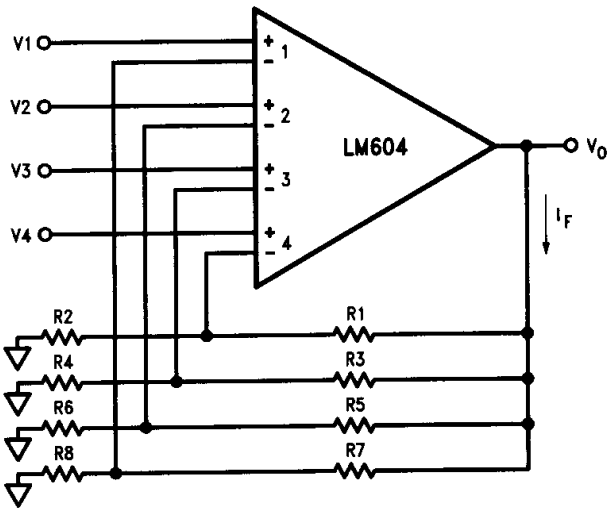
$$V_{OUT} = V_{IN}\left(\frac{r_o}{R1 + R2 + r_o}\right)$$

FIGURE 11. Inverting Gain Channel Feedthrough



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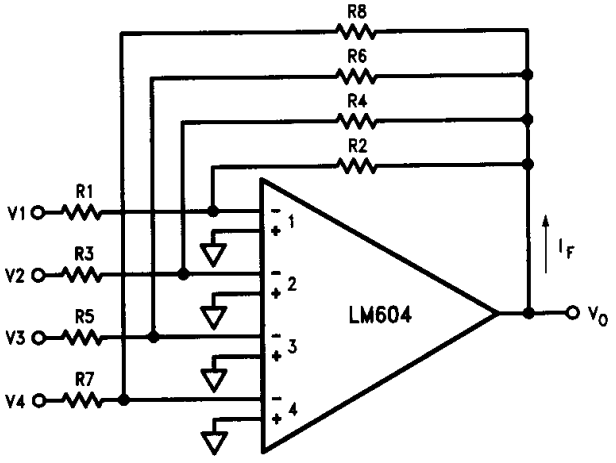
Channel	V_O
1	$V1\left(1 + \frac{R7}{R8}\right)$
2	$V2\left(1 + \frac{R5}{R6}\right)$
3	$V3\left(1 + \frac{R3}{R4}\right)$
4	$V4\left(1 + \frac{R1}{R2}\right)$

$$I_F = V_O\left(\frac{1}{R1 + R2} + \frac{1}{R3 + R4} + \frac{1}{R5 + R6} + \frac{1}{R7 + R8}\right)$$

Multiple Non-Inverting Gain Channels



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Channel	V_O	I_F
1	$-V1\left(\frac{R2}{R1}\right)$	$\frac{V_O}{R2} + \frac{V_O - V2}{R3 + R4} + \frac{V_O - V3}{R5 + R6} + \frac{V_O - V4}{R7 + R8}$
2	$-V2\left(\frac{R4}{R3}\right)$	$\frac{V_O}{R4} + \frac{V_O - V1}{R1 + R2} + \frac{V_O - V3}{R5 + R6} + \frac{V_O - V4}{R7 + R8}$
3	$-V3\left(\frac{R6}{R5}\right)$	$\frac{V_O}{R6} + \frac{V_O - V1}{R1 + R2} + \frac{V_O - V2}{R3 + R4} + \frac{V_O - V4}{R7 + R8}$
4	$-V4\left(\frac{R8}{R7}\right)$	$\frac{V_O}{R8} + \frac{V_O - V1}{R1 + R2} + \frac{V_O - V2}{R3 + R4} + \frac{V_O - V3}{R5 + R6}$

Multiple Inverting Gain Channels

FIGURE 10. Circuits Using Multiple Inverting and Non-Inverting Gain Channels

Application Hints (Continued)

INPUT CHARGE INJECTION

When the Mux-Amp switches channels, charge is injected from the inputs of the selected and previous channels, see *Figure 12*. This causes a positive error voltage at the input of the selected channel and a negative voltage at the previous channel. The amplitude of this error voltage equals Q_{INJ}/C_{IN}, where C_{IN} is the total capacitance at the input and Q_{INJ} is the charge injected. As plotted in *Figure 13*, Q_{INJ} increases proportionally with the difference in voltage between a channel's input common mode voltage and the negative supply. The RC time constant of C_{IN} times resistance seen from the input will determine how long the error voltage remains at the input.

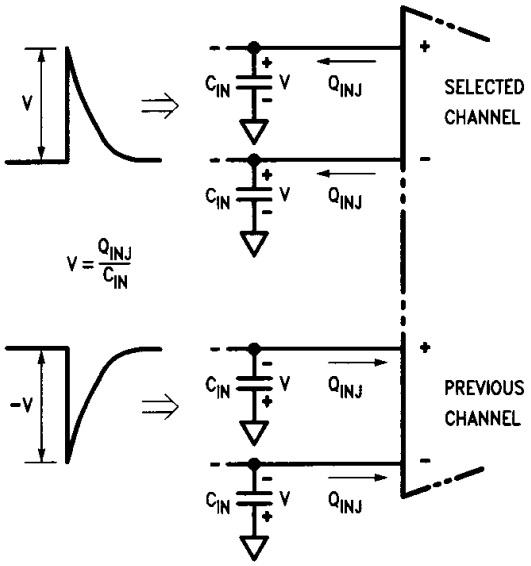

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FIGURE 12. Error Voltage From Input Charge Injection

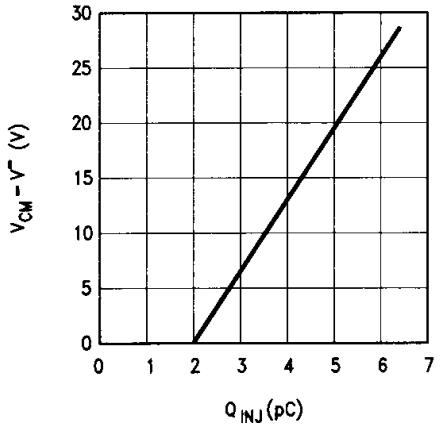

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FIGURE 13. Q_{INJ} vs $V_{CM} - V^-$

MAXIMUM OUTPUT LOAD CONDITIONS

The Mux-Amp is guaranteed to drive a 600Ω load as specified over its entire operating range. Reducing the load resistance below this value may cause the output to current limit. It may also cause the junction temperature limit to be exceeded when operating the part near its maximum ambient temperature.

The Mux-Amp is unconditionally stable with as much as 500 pF connected from the output to ground. If the output is required to drive a larger capacitive load, the Mux-Amp may need to operate with at least a gain of 10. Otherwise, it may become unstable when sinking current.

DIGITAL FEEDTHROUGH

When interfacing the Mux-Amp to a microprocessor, pins A, B, $\overline{EN}$, and $\overline{WR}$ are connected to an address bus where high frequency digital signals are present. The fast edges of these signals can propagate into the Mux-Amp's analog signal path, causing fast transients to appear at the output. To avoid this problem, the following precautions should be taken.

1) Analog and digital ground must be kept separate. They can only be connected together back at the power supply or supply bus.

2) Bypass capacitors should have low inductance to prevent noise spikes on the voltage supply pins. A ceramic disc capacitor of 0.1 μF is usually sufficient.

3) All lead lengths should be kept short to prevent them from picking up digital signals.

By using these rules, digital signals can be attenuated at the input channels by typically 100 dB.

Lab measurements have shown a minimum digital feedthrough signal of 2 mV occurs at the output even when the best layout precautions are taken. This is fine for many applications, but to completely eliminate digital feedthrough, any signals coming directly from the bus must be sent to the Mux-Amp via a Tri-State buffer, see *Figure 14*. This isolates the Mux-Amp's digital pins from the address bus to prevent pin to pin feedthrough. CS can be used to enable the Tri-State buffers when signals are sent to the Mux-Amp from the address bus.

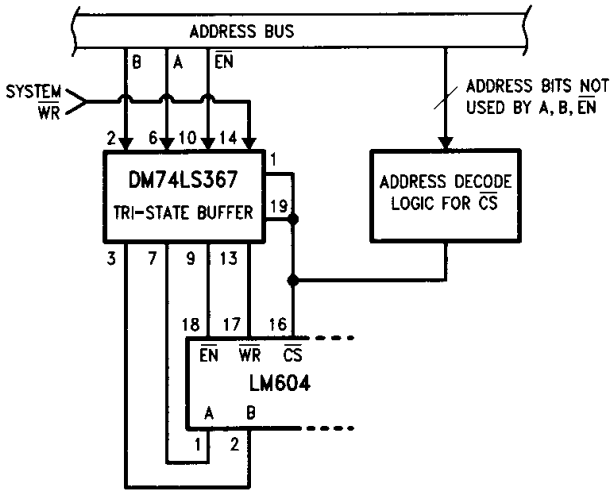

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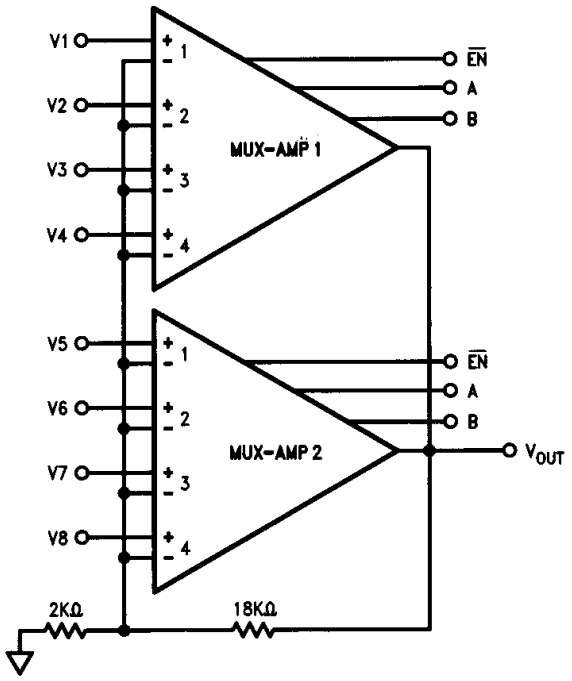
FIGURE 14. Isolating Mux-Amp from Address Bus by Using a Tri-State Buffer

Typical Applications



Mux-Amp 1			Mux-Amp 2			Input
A	B	$\overline{EN}$	A	B	$\overline{EN}$	
0	0	0	X	X	1	V1
0	1	0	X	X	1	V2
1	0	0	X	X	1	V3
1	1	0	X	X	1	V4
X	X	1	0	0	0	V5
X	X	1	0	1	0	V6
X	X	1	1	0	0	V7
X	X	1	1	1	0	V8

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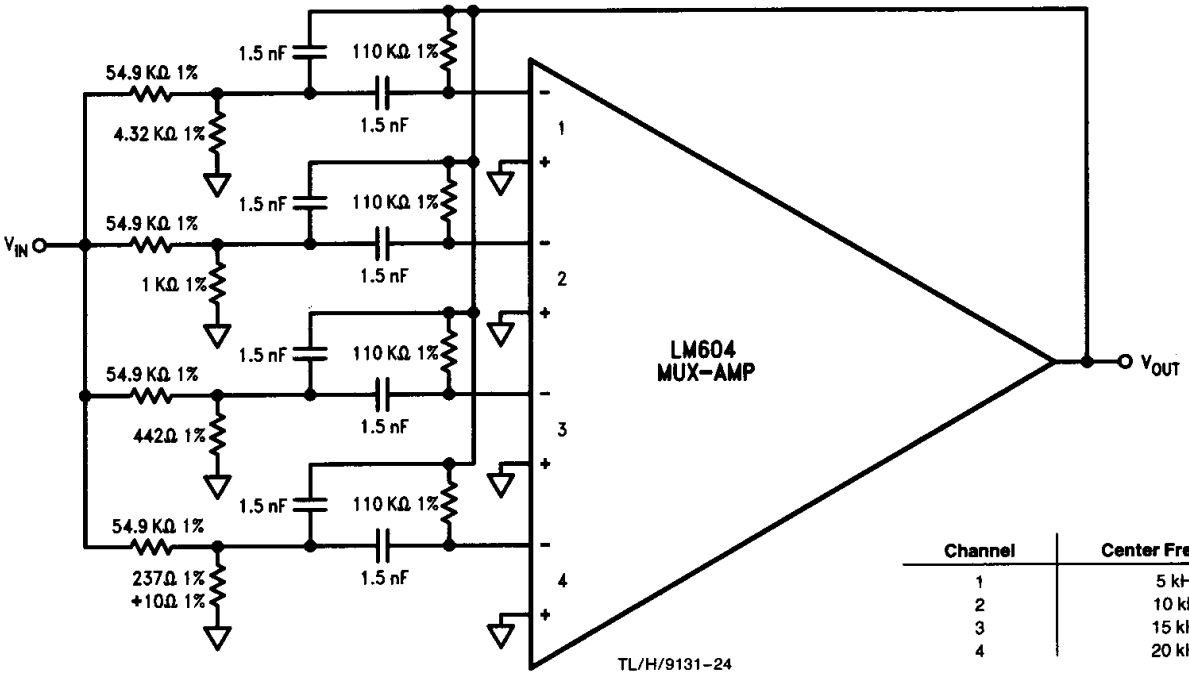
Eight Channel Multiplexer and Amplifier with a Gain of 10



Channel	Center Frequency
1	5 kHz
2	10 khz
3	15 kHz
4	20 kHz

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Programmable Bandpass Filter: Each channel has a 2 kHz bandwidth and a gain of 1 at the center frequency