P89LPC932

8-bit microcontroller with accelerated two-clock 80C51 core
8 kB Flash with 512-byte data EEPROM and 768-byte RAM

Rev. 04 — 06 January 2004 **Product data**

1. General description

The P89LPC932 is a single-chip microcontroller, available in low cost packages, based on a high performance processor architecture that executes instructions in two to four clocks, six times the rate of standard 80C51 devices. Many system-level functions have been incorporated into the P89LPC932 in order to reduce component count, board space, and system cost.

2. Features

- A high performance 80C51 CPU provides instruction cycle times of 167-333 ns for all instructions except multiply and divide when executing at 12 MHz. This is 6 times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- 2.4 V to 3.6 V V_{DD} operating range. I/O pins are 5 V tolerant (may be pulled up or driven to 5.5 V).
- 8 kB Flash code memory with 1 kB erasable sectors, 64-byte erasable page size.
- 256-byte RAM data memory. 512-byte auxiliary on-chip RAM.
- 512-byte customer Data EEPROM on chip allows serialization of devices, storage of set-up parameters, etc.
- Two 16-bit counter/timers. Each timer may be configured to toggle a port output upon timer overflow or to become a PWM output.
- Real-Time clock that can also be used as a system timer.
- Capture/Compare Unit (CCU) provides PWM, input capture, and output compare functions.
- Two analog comparators with selectable inputs and reference source.
- Enhanced UART with fractional baud rate generator, break detect, framing error detection, automatic address detection and versatile interrupt capabilities.
- 400 kHz byte-wide I^2C-bus communication port.
- SPI communication port.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Four interrupt priority levels.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from 8 values.
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Low voltage reset (Brownout detect) allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.

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- Oscillator Fail Detect. The Watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Configurable on-chip oscillator with frequency range and RC oscillator options (selected by user programmed Flash configuration bits). The RC oscillator option allows operation without external oscillator components. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 12 MHz. The RC oscillator option is selectable and fine tunable.
- Programmable port output configuration options:
  - quasi-bidirectional,
  - open drain,
  - push-pull,
  - input-only.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- Second data pointer.
- Schmitt trigger port inputs.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- 23 I/O pins minimum (28-pin package). Up to 26 I/O pins while using on-chip oscillator and reset options.
- Only power and ground connections are required to operate the P89LPC932 when on-chip oscillator and reset options are selected.
- Serial Flash programming allows simple in-circuit production coding. Flash security bits prevent reading of sensitive application programs.
- In-Application Programming of the Flash code memory. This allows changing the code in a running application.
- Idle and two different Power-down reduced power modes. Improved wake-up from Power-down mode (a low interrupt input starts execution). Typical Power-down current is 1 μA (total Power-down with voltage comparators disabled).
- 28-pin PLCC, TSSOP, and HVQFN packages.
- Emulation support.

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3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
P89LPC932BA	PLCC28	plastic leaded chip carrier; 28 leads	SOT261-2
P89LPC932BDH	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1
P89LPC932FDH	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1
P89LPC932FHN	HVQFN28	plastic thermal enhanced very thin quad flat package; no leads; 28 terminals; body 6 × 6 × 0.85 mm	SOT788-1

3.1 Ordering options

Table 2: Part options

Type number	Flash memory	Temperature range	Frequency
P89LPC932BA	8 kB	0 °C to +70 °C	0 to 12 MHz
P89LPC932BDH	8 kB	0 °C to +70 °C	0 to 12 MHz
P89LPC932FDH	8 kB	–40 °C to +85 °C	0 to 12 MHz
P89LPC932FHN	8 kB	–40 °C to +85 °C	0 to 12 MHz

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4. Block diagram

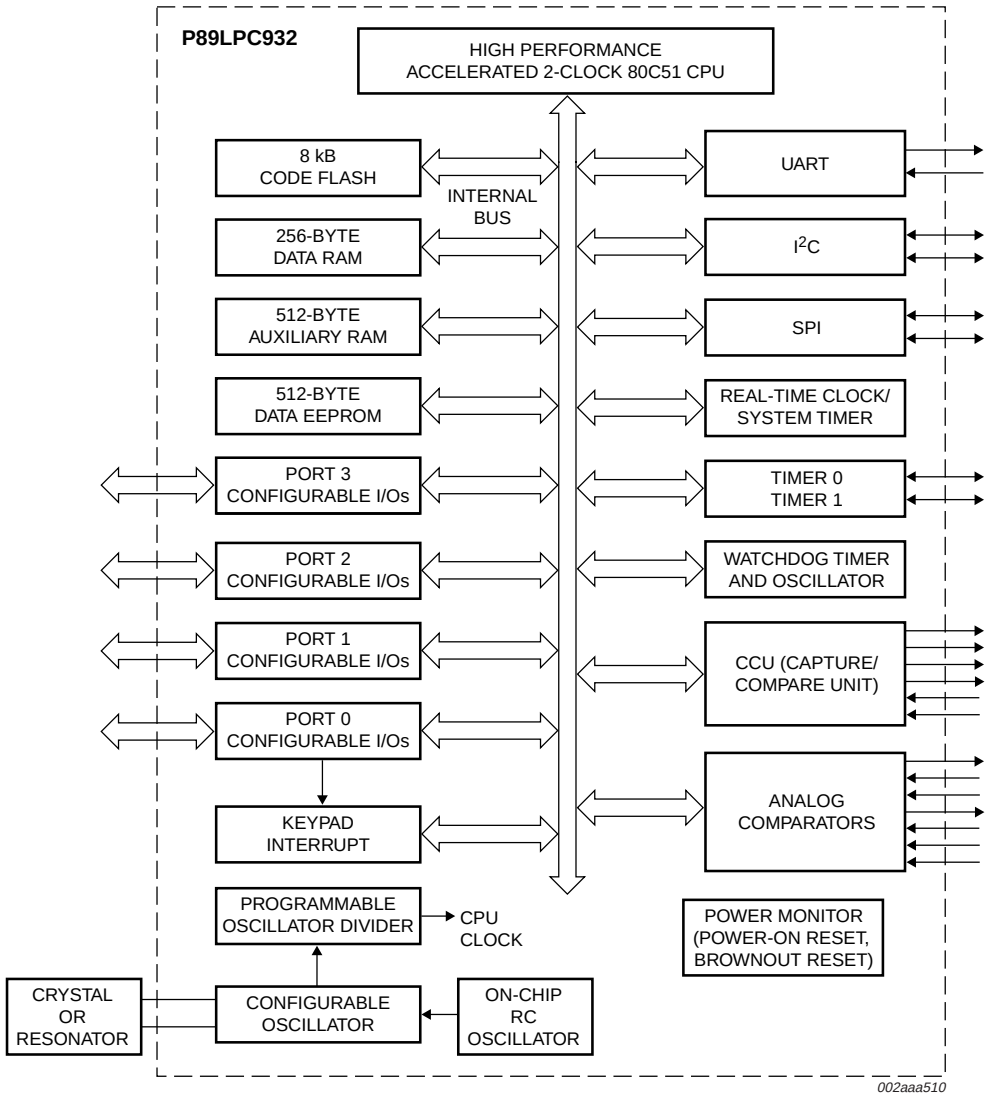

Fig 1. Block diagram.

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5. Pinning information

5.1 Pinning

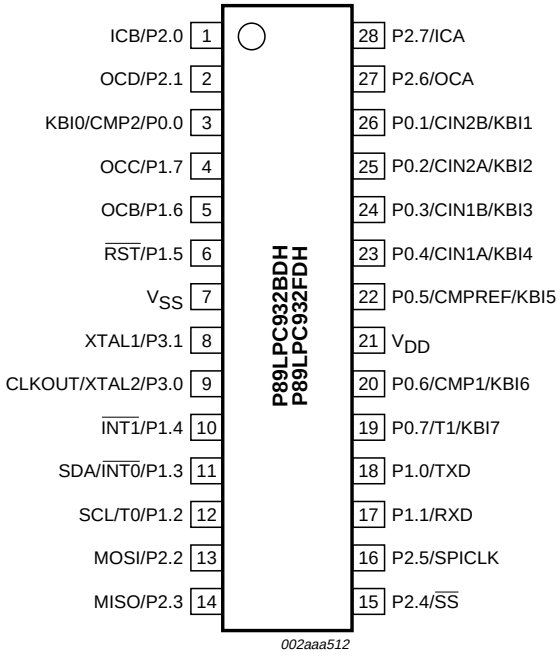

Fig 2. TSSOP28 pin configuration.

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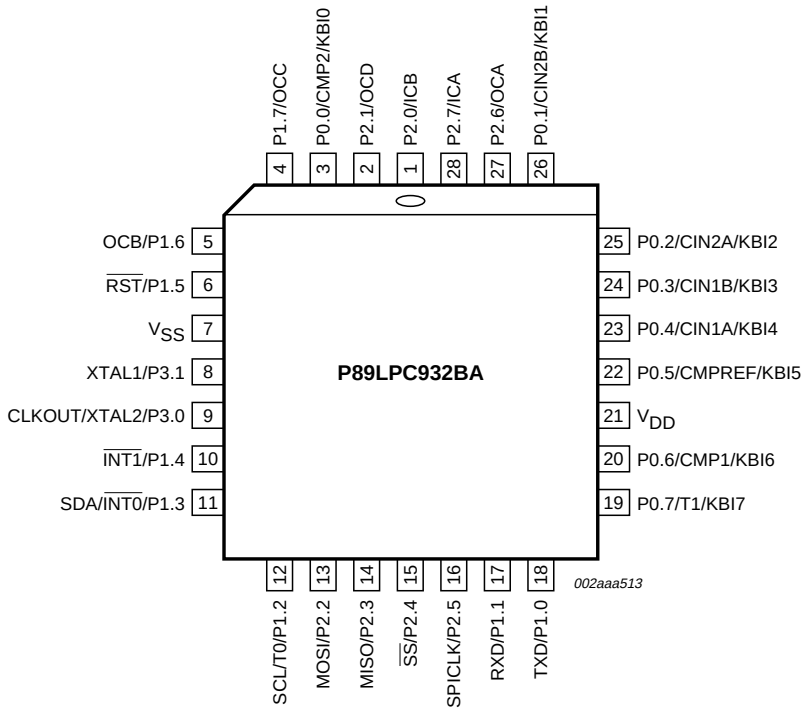

Fig 3. PLCC28 pin configuration.

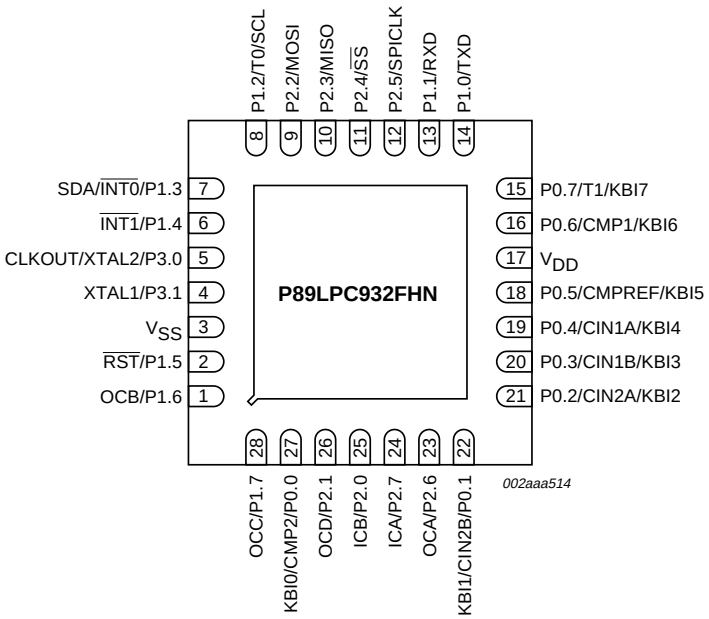

Fig 4. HVQFN28 pin configuration.

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5.2 Pin description

Table 3: Pin description

Symbol	Pin		Type	Description
	TSSOP, PLCC	HVQFN		
P0.0 - P0.7	3, 26, 25, 24, 23, 22, 20, 19	27, 22, 21, 20, 19, 18, 16, 15	I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 “Port configurations” and Table 8 “DC electrical characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
	3	27	I/O	**P0.0 —** Port 0 bit 0.
			O	**CMP2 —** Comparator 2 output.
			I	**KBI0 —** Keyboard input 0.
	26	22	I/O	**P0.1 —** Port 0 bit 1.
			I	**CIN2B —** Comparator 2 positive input B.
			I	**KBI1 —** Keyboard input 1.
	25	21	I/O	**P0.2 —** Port 0 bit 2.
			I	**CIN2A —** Comparator 2 positive input A.
			I	**KBI2 —** Keyboard input 2.
	24	20	I/O	**P0.3 —** Port 0 bit 3.
			I	**CIN1B —** Comparator 1 positive input B.
			I	**KBI3 —** Keyboard input 3.
	23	19	I/O	**P0.4 —** Port 0 bit 4.
			I	**CIN1A —** Comparator 1 positive input A.
			I	**KBI4 —** Keyboard input 4.
	22	18	I/O	**P0.5 —** Port 0 bit 5.
			I	**CMPREF —** Comparator reference (negative) input.
			I	**KBI5 —** Keyboard input 5.
	20	16	I/O	**P0.6 —** Port 0 bit 6.
			O	**CMP1 —** Comparator 1 output.
			I	**KBI6 —** Keyboard input 6.
	19	15	I/O	**P0.7 —** Port 0 bit 7.
			I/O	**T1 —** Timer/counter 1 external count input or overflow output.
			I	**KBI7 —** Keyboard input 7.

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Table 3: Pin description...*continued*

Symbol	Pin		Type	Description
	TSSOP, PLCC	HVQFN		
P1.0 - P1.7	18, 17, 12, 11, 10, 6, 5, 4	14, 13, 8, 7, 6, 2, 1, 28	I/O, I [1]	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 "Port configurations" and Table 8 "DC electrical characteristics" for details. P1.2 - P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
	18	14	I/O	**P1.0 —** Port 1 bit 0.
			O	**TXD —** Transmitter output for the serial port.
	17	13	I/O	**P1.1 —** Port 1 bit 1.
			I	**RXD —** Receiver input for the serial port.
	12	8	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
			I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
			I/O	**SCL —** I^2C serial clock input/output.
	11	7	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
			I	**$\overline{INT0}$ —** External interrupt 0 input.
			I/O	**SDA —** I^2C serial data input/output.
	10	6	I	**P1.4 —** Port 1 bit 4.
			I	**$\overline{INT1}$ —** External interrupt 1 input.
	6	2	I	**P1.5 —** Port 1 bit 5 (input only).
			I	**$\overline{RST}$ —** External Reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force In-System Programming mode.
	5	1	I/O	**P1.6 —** Port 1 bit 6.
			O	**OCB —** Output Compare B.
	4	28	I/O	**P1.7 —** Port 1 bit 7.
			O	**OCC —** Output Compare C.

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Table 3: Pin description...*continued*

Symbol	Pin		Type	Description
	TSSOP, PLCC	HVQFN		
P2.0 - P2.7	1, 2, 13, 14, 15, 16, 27, 28	25, 26, 9, 10, 11, 12, 23, 24	I/O	**Port 2:** Port 2 is an 8-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 8 "DC electrical characteristics" for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
	1	25	I/O	**P2.0 —** Port 2 bit 0.
			I	**ICB —** Input Capture B.
	2	26	I/O	**P2.1 —** Port 2 bit 1.
			O	**OCD —** Output Compare D.
	13	9	I/O	**P2.2 —** Port 2 bit 2.
			I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input.
	14	10	I/O	**P2.3 —** Port 2 bit 3.
			I/O	**MISO —** When configured as master, this pin is input, when configured as slave, this pin is output.
	15	11	I/O	**P2.4 —** Port 2 bit 4.
			I	$\overline{\textbf{SS}}$ **—** SPI Slave select.
	16	12	I/O	**P2.5 —** Port 2 bit 5.
			I/O	**SPICLK —** SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input.
	27	23	I/O	**P2.6 —** Port 2 bit 6.
			O	**OCA —** Output Compare A.
	28	24	I/O	**P2.7 —** Port 2 bit 7.
			I	**ICA —** Input Capture A.

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Table 3: Pin description...*continued*

Symbol	Pin		Type	Description
	TSSOP, PLCC	HVQFN		
P3.0 - P3.1	9, 8	5, 4	I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 8 "DC electrical characteristics" for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
	9	5	I/O	**P3.0 —** Port 3 bit 0.
			O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the FLASH configuration.
			O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the Real-Time clock/system timer.
	8	4	I/O	**P3.1 —** Port 3 bit 1.
			I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the FLASH configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the Real-Time clock/system timer.
V_{SS}	7	3	I	**Ground:** 0 V reference.
V_{DD}	21	17	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-Down modes.

[1] Input/Output for P1.0-P1.4, P1.6, P1.7. Input for P1.5.

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6. Logic symbol

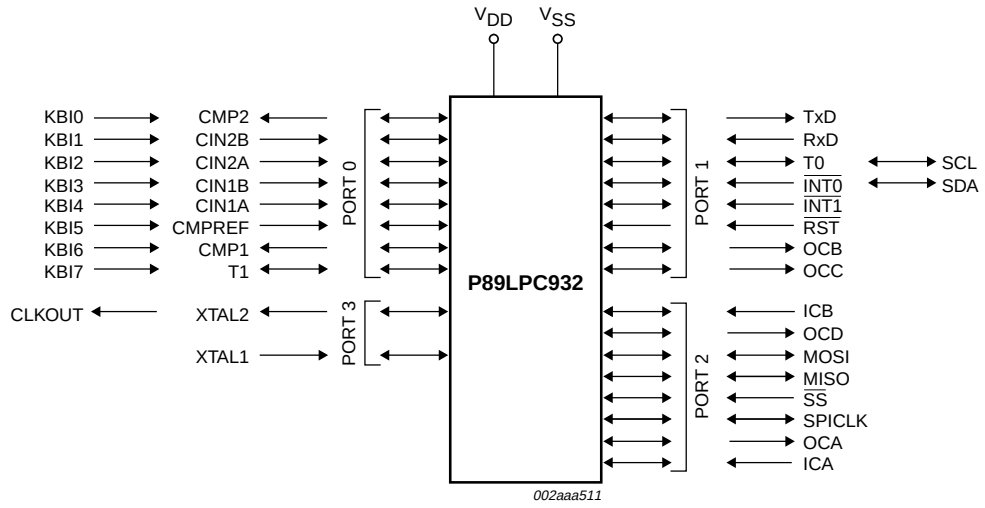

Fig 5. Logic symbol.

7. Special function registers

Remark: Special Function Registers (SFRs) accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

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Table 4: Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	00000000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00	000000x0
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	00000000
BRGR0[2]	Baud rate generator rate LOW	BEH									00	00000000
BRGR1[2]	Baud rate generator rate HIGH	BFH									00	00000000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[2]	xxxxxx00
CCCRA	Capture compare A control register	EAH	ICECA2	ICECA1	ICECA0	ICESA	ICNFA	FCOA	OCMA1	OCMA0	00	00000000
CCCRB	Capture compare B control register	EBH	ICECB2	ICECB1	ICECB0	ICESB	ICNFB	FCOB	OCMB1	OCMB0	00	00000000
CCCRC	Capture compare C control register	ECH	-	-	-	-	-	FCOC	OCMC1	OCMC0	00	xxxxx000
CCCRD	Capture compare D control register	EDH	-	-	-	-	-	FCOD	OCMD1	OCMD0	00	xxxxx000
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00[1]	xx000000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00[1]	xx000000
DEECON	Data EEPROM control register	F1H	EEIF	HVERR	ECTL1	ECTL0	-	-	-	EADR8	0E	00001110
DEEDAT	Data EEPROM data register	F2H									00	00000000
DEEADR	Data EEPROM address register	F3H									00	00000000
DIVM	CPU clock divide-by-M control	95H									00	00000000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer HIGH	83H									00	00000000
DPL	Data pointer LOW	82H									00	00000000

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Table 4: Special function registers...*continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
I2ADR	I²C slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	00000000
	Bit address		**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**	**D8**		
I2CON*	I²C control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x00000x0
I2DAT	I²C data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register HIGH	DDH									00	00000000
I2SCLL	Serial clock generator/SCL duty cycle register LOW	DCH									00	00000000
I2STAT	I²C status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	11111000
ICRAH	Input capture A register HIGH	ABH									00	00000000
ICRAL	Input capture A register LOW	AAH									00	00000000
ICRBH	Input capture B register HIGH	AFH									00	00000000
ICRBL	Input capture B register LOW	AEH									00	00000000
	Bit address		**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	00000000
	Bit address		**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1*	Interrupt enable 1	E8H	EIEE	EST	-	ECCU	ESPI	EC	EKBI	EI2C	00[1]	00x00000
	Bit address		**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00[1]	x0000000
IP0H	Interrupt priority 0 HIGH	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	PX1H	PT0H	PX0H	00[1]	x0000000
	Bit address		**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**	**F8**		
IP1*	Interrupt priority 1	F8H	PIEE	PST	-	PCCU	PSPI	PC	PKBI	PI2C	00[1]	00x00000
IP1H	Interrupt priority 1 HIGH	F7H	PIEEH	PSTH	-	PCCUH	PSPIH	PCH	PKBIH	PI2CH	00[1]	00x00000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxxxx00
KBMASK	Keypad interrupt mask register	86H									00	00000000
KBPATN	Keypad pattern register	93H									FF	11111111

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Table 4: Special function registers...*continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
OCRAH	Output compare A register HIGH	EFH									00	00000000
OCRAL	Output compare A register LOW	EEH									00	00000000
OCRBH	Output compare B register HIGH	FBH									00	00000000
OCRBL	Output compare B register LOW	FAH									00	00000000
OCRCH	Output compare C register HIGH	FDH									00	00000000
OCRCL	Output compare C register LOW	FCH									00	00000000
OCRDH	Output compare D register HIGH	FFH									00	00000000
OCRDL	Output compare D register LOW	FEH									00	00000000
	Bit address		**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0*	Port 0	80H	T1/KB7	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1	CMP2 /KB0		[1]
	Bit address		**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1*	Port 1	90H	OCC	OCB	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/ SDA	T0/SCL	RXD	TXD		[1]
	Bit address		**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P2*	Port 2	A0H	ICA	OCA	SPICLK	$\overline{\text{SS}}$	MISO	MOSI	OCD	ICB		[1]
	Bit address		**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2		[1]
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[1]	11111111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[1]	00000000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[1]	11x1xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[1]	00x0xx00

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Table 4: Special function registers...*continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
P2M1	Port 2 output mode 1	A4H	(P2M1.7)	(P2M1.6)	(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	(P2M1.1)	(P2M1.0)	FF[1]	11111111
P2M2	Port 2 output mode 2	A5H	(P2M2.7)	(P2M2.6)	(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	(P2M2.1)	(P2M2.0)	00[1]	00000000
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[1]	xxxxxx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[1]	xxxxxx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	00000000
PCONA	Power control register A	B5H	RTCPD	DEEPD	VCPD	-	I2PD	SPPD	SPD	CCUPD	00[1]	00000000
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	00000000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX		[3]
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1][6]	011xxx00
RTCH	Real-time clock register HIGH	D2H									00[6]	00000000
RTCL	Real-time clock register LOW	D3H									00[6]	00000000
SADDR	Serial port address register	A9H									00	00000000
SADEN	Serial port address enable	B9H									00	00000000
SBUF	Serial Port data buffer register	99H									xx	xxxxxxxx
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	00000000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	00000000
SP	Stack pointer	81H									07	00000111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	00000100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xxxxxx
SPDAT	SPI data register	E3H									00	00000000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0xxx0
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	00000000
TCR20*	CCU control register 0	C8H	PLLEN	HLTRN	HLTEN	ALTCD	ALTAB	TDIR2	TMOD21	TMOD20	00	00000000
TCR21	CCU control register 1	F9H	TCOU2	-	-	-	PLLDV.3	PLLDV.2	PLLDV.1	PLLDV.0	00	0xxx0000

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Table 4: Special function registers...*continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
TH0	Timer 0 HIGH	8CH									00	00000000
TH1	Timer 1 HIGH	8DH									00	00000000
TH2	CCU timer HIGH	CDH									00	00000000
TICR2	CCU interrupt control register	C9H	TOIE2	TOCIE2D	TOCIE2C	TOCIE2B	TOCIE2A	-	TICIE2B	TICIE2A	00	00000x00
TIFR2	CCU interrupt flag register	E9H	TOIF2	TOCF2D	TOCF2C	TOCF2B	TOCF2A	-	TICF2B	TICF2A	00	00000x00
TISE2	CCU interrupt status encode register	DEH	-	-	-	-	-	ENCINT.2	ENCINT.1	ENCINT.0	00	xxxxx000
TL0	Timer 0 LOW	8AH									00	00000000
TL1	Timer 1 LOW	8BH									00	00000000
TL2	CCU timer LOW	CCH									00	00000000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	00000000
TOR2H	CCU reload register HIGH	CFH									00	00000000
TOR2L	CCU reload register LOW	CEH									00	00000000
TPCR2H	Prescaler control register HIGH	CBH	-	-	-	-	-	-	TPCR2H.1	TPCR2H.0	00	xxxxxx00
TPCR2L	Prescaler control register LOW	CAH	TPCR2L.7	TPCR2L.6	TPCR2L.5	TPCR2L.4	TPCR2L.3	TPCR2L.2	TPCR2L.1	TPCR2L.0	00	00000000
TRIM	Internal oscillator trim register	96H	-	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0		[5] [6]
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK		[4] [6]
WDL	Watchdog load	C1H									FF	11111111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is '0'. If any are written while BRGEN = 1, the result is unpredictable.

[3] The RSTSRC register reflects the cause of the P89LPC932 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx110000.

[4] After reset, the value is 111001x1, i.e., PRE2-PRE0 are all '1', WDRUN = 1 and WDCLK = 1. WDTOF bit is '1' after watchdog reset and is '0' after power-on reset. Other resets will not affect WDTOF.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] The only reset source that affects these SFRs is power-on reset.

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8. Functional description

Remark: Please refer to the *P89LPC932 User's Manual* for a more detailed functional description.

8.1 Enhanced CPU

The P89LPC932 uses an enhanced 80C51 CPU which runs at 6 times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

8.2 Clocks

8.2.1 Clock definitions

The P89LPC932 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 6) and can also be optionally divided to a slower frequency (see Section 8.7 "CPU Clock (CCLK) modification: DIVM register").

Note: f_{OSC} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output.

PCLK — Clock for the various peripheral devices and is $^{CCLK}/_{2}$.

8.2.2 CPU clock (OSCCLK)

The P89LPC932 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the FLASH is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 12 MHz.

8.2.3 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

8.2.4 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

8.2.5 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 12 MHz. Ceramic resonators are also supported in this configuration.

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8.2.6 Clock output

The P89LPC932 supports a user-selectable clock output function on the XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on X1) and if the Real-Time clock is not using the crystal oscillator as its clock source. This allows external devices to synchronize to the P89LPC932. This output is enabled by the ENCLK bit in the TRIM register.

The frequency of this clock output is ½ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

8.3 On-chip RC oscillator option

The P89LPC932 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory pre-programmed value to adjust the oscillator frequency to 7.373 MHz, ±2.5 %. End-user applications can write to the TRIM register to adjust the on-chip RC oscillator to other frequencies.

8.4 Watchdog oscillator option

The watchdog has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

8.5 External clock input option

In this configuration, the processor clock is derived from an external source driving the XTAL1/P3.1 pin. The rate may be from 0 Hz up to 12 MHz. The XTAL2/P3.0 pin may be used as a standard port pin or a clock output.

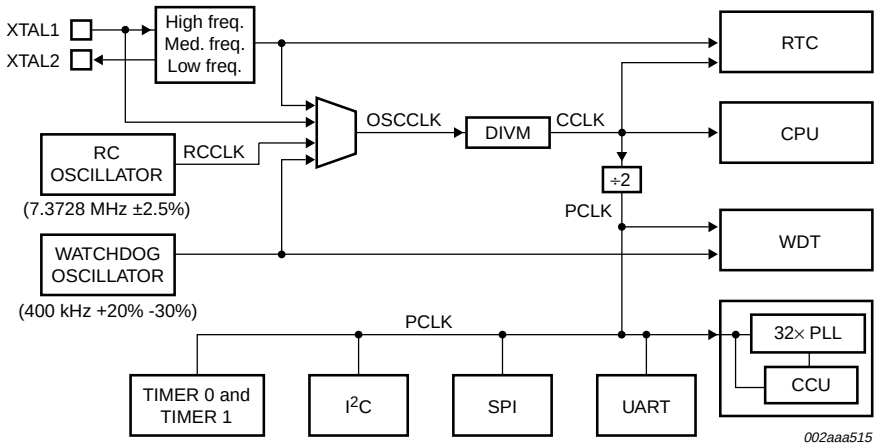

Fig 6. Block diagram of oscillator control.

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8.6 CPU Clock (CCLK) wake-up delay

The P89LPC932 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 992 OSCCLK cycles plus 60 to 100 μs. If the clock source is either the internal RC oscillator, watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60 to 100 μs.

8.7 CPU Clock (CCLK) modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.8 Low power select

The P89LPC932 is designed to run at 12 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to ‘1’ to lower the power consumption further. On any reset, CLKLP is ‘0’ allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

8.9 Memory organization

The various P89LPC932 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00h:7Fh) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00h:FFh) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- XDATA

  ‘External’ Data or Auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the SPTR, R0, or R1. All or part of this space could be implemented on-chip. The P89LPC932 has 512 bytes of on-chip XDATA memory.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC932 has 8 kB of on-chip Code memory.

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The P89LPC932 also has 512 bytes of on-chip Data EEPROM that is accessed via SFRs (see Section 8.26 “Data EEPROM”).

8.10 Data RAM arrangement

The 768 bytes of on-chip RAM are organized as shown in Table 5.

Table 5: On-chip data memory usages

Type	Data RAM	Size (bytes)
DATA	Memory that can be addressed directly and indirectly	128
IDATA	Memory that can be addressed indirectly	256
XDATA	Auxiliary (‘External Data’) on-chip memory that is accessed using the MOVX instructions	512

8.11 Interrupts

The P89LPC932 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC932 supports 15 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port Tx, serial port Rx, combined serial port Rx/Tx, brownout detect, watchdog/Real-Time clock, I^2C, keyboard, comparators 1 and 2, SPI, CCU, data EEPROM write completion.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

8.11.1 External interrupt inputs

The P89LPC932 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in Register TCON.

In edge-triggered mode, if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

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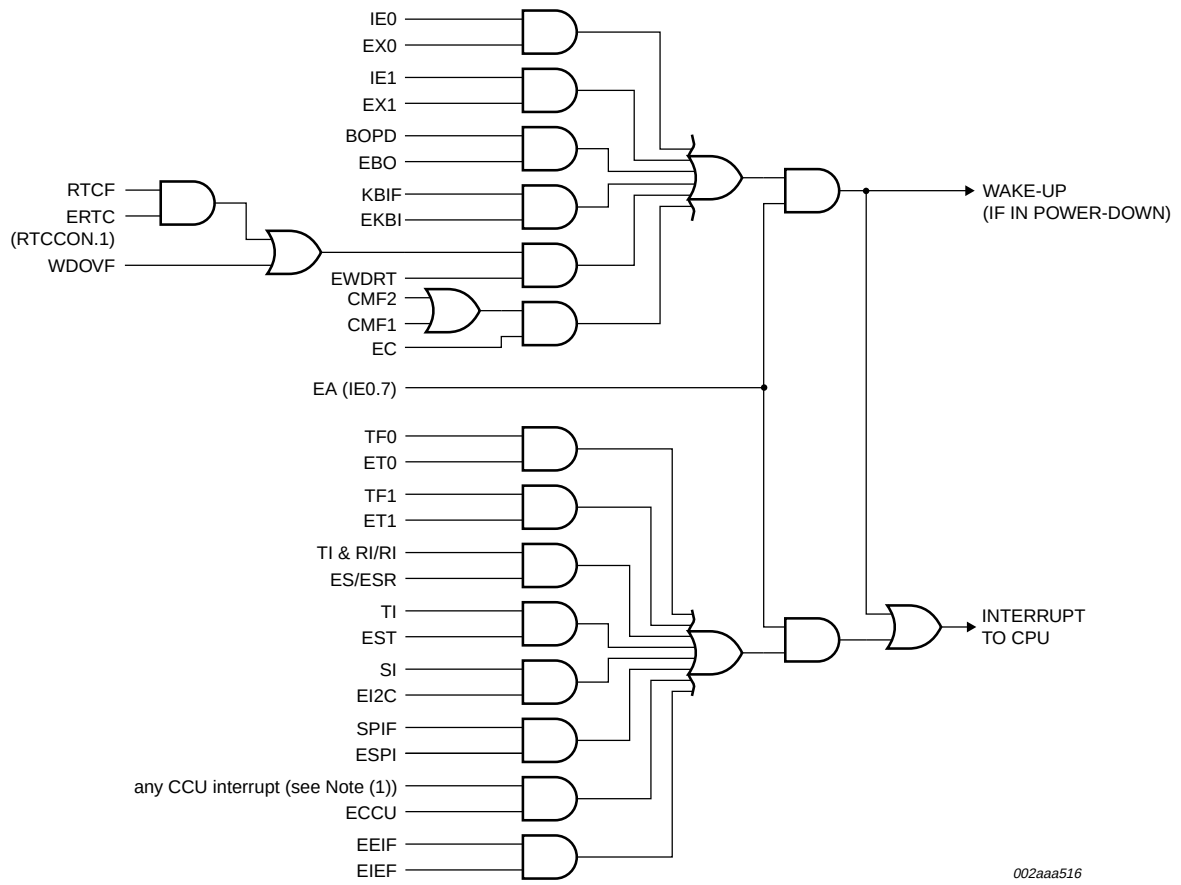
If an external interrupt is enabled when the P89LPC932 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 8.14 “Power reduction modes” for details.



(1) See Section 8.18 “Capture/Compare Unit (CCU)”

Fig 7. Interrupt sources, interrupt enables, and power-down wake-up sources.

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8.12 I/O ports

The P89LPC932 has four I/O ports: Port 0, Port 1, Port 2, and Port 3. Ports 0, 1and 2 are 8-bit ports, and Port 3 is a 2-bit port. The exact number of I/O pins available depends upon the clock and reset options chosen, as shown in Table 6.

Table 6: Number of I/O pins available

Clock source	Reset option	Number of I/O pins (28-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	26
	External $\overline{\text{RST}}$ pin supported	25
External clock input	No external reset (except during power-up)	25
	External $\overline{\text{RST}}$ pin supported	24
Low/medium/high speed oscillator (external crystal or resonator)	No external reset (except during power-up)	24
	External $\overline{\text{RST}}$ pin supported	23

8.12.1 Port configurations

All but three I/O port pins on the P89LPC932 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

P1.5 ($\overline{\text{RST}}$) can only be an input and cannot be configured.

P1.2 (SCL/T0) and P1.3 (SDA/$\overline{\text{INT0}}$) may only be configured to be either input-only or open-drain.

8.12.2 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC932 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.12.3 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic ‘0’. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

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8.12.4 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt-triggered input that also has a glitch suppression circuit.

8.12.5 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic ‘1’. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.12.6 Port 0 analog functions

The P89LPC932 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high impedance) mode.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD[1:5] defaults to ‘0’s to enable digital functions.

8.12.7 Additional port features

After power-up, all pins are in Input-Only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 and are configurable for either input-only or open-drain.

Every output on the P89LPC932 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 8 “DC electrical characteristics” for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

8.13 Power monitoring functions

The P89LPC932 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on Detect and Brownout detect.

8.13.1 Brownout detection

The Brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a Brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

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If Brownout detection is enabled, the operating voltage range for V_{DD} is 2.7 V to 3.6 V, and the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{BO} (see Table 8 “DC electrical characteristics”), and is negated when V_{DD} rises above V_{BO}. If brownout detection is disabled, the operating voltage range for V_{DD} is 2.4 V to 3.6 V. If the P89LPC932 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of Brownout detect, the V_{DD} rise and fall times must be observed. Please see Table 8 “DC electrical characteristics” for specifications.

8.13.2 Power-on detection

The Power-on Detect has a function similar to the Brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where Brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

8.14 Power reduction modes

The P89LPC932 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

8.14.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

8.14.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC932 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM}. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{RAM}, therefore it is highly recommended to wake up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during Power-down. These include: Brownout detect, Watchdog Timer, Comparators (note that Comparators can be powered-down separately), and Real-Time Clock (RTC)/System Timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock and the RTC is enabled.

8.14.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock

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the RTC during Power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the Real-Time Clock running during Power-down.

8.15 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either an active-LOW reset input or as a digital input, P1.5. The RPE (Reset Pin Enable) bit in UCFG1, when set to '1', enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin will always function as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Remark: During a power cycle, V_{DD} must fall below V_{POR} (see Table 8 "DC electrical characteristics" on page 45) before power is reapplied, in order to ensure a power-on reset.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1);
- Power-on detect;
- Brownout detect;
- Watchdog Timer;
- Software reset;
- UART break character detect reset.

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a '0' to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

8.15.1 Reset vector

Following reset, the P89LPC932 will fetch instructions from either address 0000h or the Boot address. The Boot address is formed by using the Boot Vector as the high byte of the address and the low byte of the address = 00h.

The Boot address will be used if a UART break reset occurs, or the non-volatile Boot Status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see *P89LPC932 User's Manual*). Otherwise, instructions will be fetched from address 0000H.

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8.16 Timers/counters 0 and 1

The P89LPC932 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counter. An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the 'Timer' function, the register is incremented every machine cycle.

In the 'Counter' function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle.

Timer 0 and Timer 1 have five operating modes (modes 0, 1, 2, 3 and 6). Modes 0, 1, 2 and 6 are the same for both Timers/Counters. Mode 3 is different.

8.16.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

8.16.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

8.16.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

8.16.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

8.16.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

8.16.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

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8.17 Real-Time clock/system timer

The P89LPC932 has a simple Real-Time clock that allows a user to continue running an accurate timer while the rest of the device is powered-down. The Real-Time clock can be a wake-up or an interrupt source. The Real-Time clock is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all ‘0’s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the Real-Time clock and its associated SFRs to the default state.

8.18 Capture/Compare Unit (CCU)

This unit features:

- A 16-bit timer with 16-bit reload on overflow.
- Selectable clock, with prescaler to divide clock source by any integral number between 1 and 1024.
- 4 Compare/PWM outputs with selectable polarity
- Symmetrical/Asymmetrical PWM selection
- 2 Capture inputs with event counter and digital noise rejection filter
- 7 interrupts with common interrupt vector (one Overflow, 2 Capture, 4 Compare)
- Safe 16-bit read/write via shadow registers.

8.18.1 CCU clock (CCUCLK)

The CCU runs on the CCUCLK, which is either PCLK in basic timer mode, or the output of a PLL. The PLL is designed to use a clock source between 0.5 MHz to 1 MHz that is multiplied by 32 to produce a CCUCLK between 16 MHz and 32 MHz in PWM mode (asymmetrical or symmetrical). The PLL contains a 4-bit divider to help divide PCLK into a frequency between 0.5 MHz and 1 MHz.

8.18.2 CCU clock prescaling

This CCUCLK can further be divided down by a prescaler. The prescaler is implemented as a 10-bit free-running counter with programmable reload at overflow.

8.18.3 Basic timer operation

The Timer is a free-running up/down counter with a direction control bit. If the timer counting direction is changed while the counter is running, the count sequence will be reversed. The timer can be written or read at any time.

When a reload occurs, the CCU Timer Overflow Interrupt Flag will be set, and an interrupt generated if enabled. The 16-bit CCU Timer may also be used as an 8-bit up/down timer.

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8.18.4 Output compare

There are four output compare channels A, B, C and D. Each output compare channel needs to be enabled in order to operate and the user will have to set the associated I/O pin to the desired output mode to connect the pin. When the contents of the timer matches that of a capture compare control register, the Timer Output Compare Interrupt Flag (TOCFx) becomes set. An interrupt will occur if enabled.

8.18.5 Input capture

Input capture is always enabled. Each time a capture event occurs on one of the two input capture pins, the contents of the timer is transferred to the corresponding 16-bit input capture register. The capture event can be programmed to be either rising or falling edge triggered. A simple noise filter can be enabled on the input capture by enabling the Input Capture Noise Filter bit. If set, the capture logic needs to see four consecutive samples of the same value in order to recognize an edge as a capture event. An event counter can be set to delay a capture by a number of capture events.

8.18.6 PWM operation

PWM operation has two main modes, symmetrical and asymmetrical.

In asymmetrical PWM operation the CCU Timer operates in downcounting mode regardless of the direction control bit.

In symmetrical mode, the timer counts up/down alternately. The main difference from basic timer operation is the operation of the compare module, which in PWM mode is used for PWM waveform generation.

As with basic timer operation, when the PWM (compare) pins are connected to the compare logic, their logic state remains unchanged. However, since bit FCO is used to hold the halt value, only a compare event can change the state of the pin.

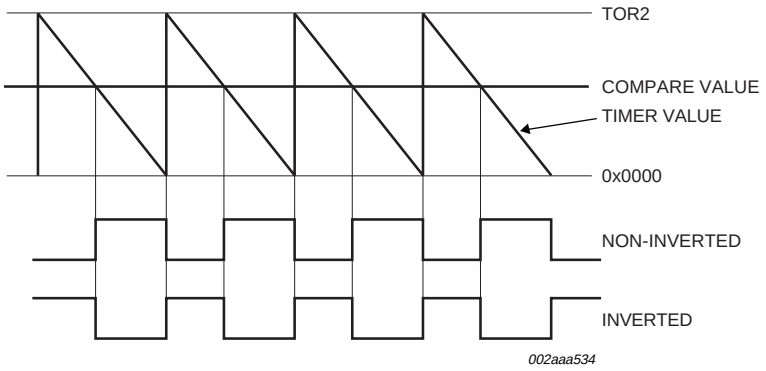

Fig 8. Asymmetrical PWM, downcounting.

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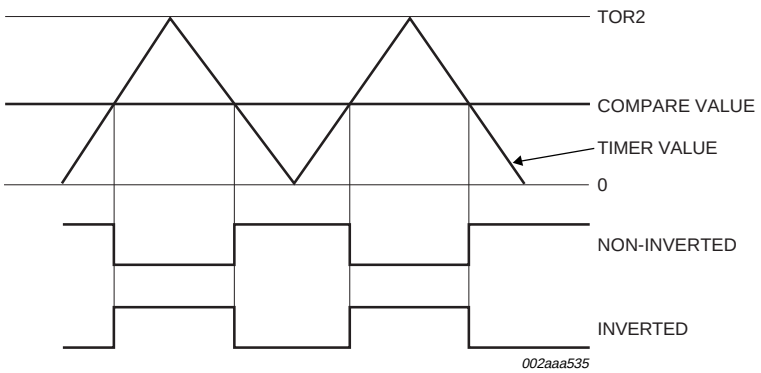

Fig 9. Symmetrical PWM.

8.18.7 Alternating output mode

In asymmetrical mode, the user can set up PWM channels A/B and C/D as alternating pairs for bridge drive control. In this mode the output of these PWM channels are alternately gated on every counter cycle.

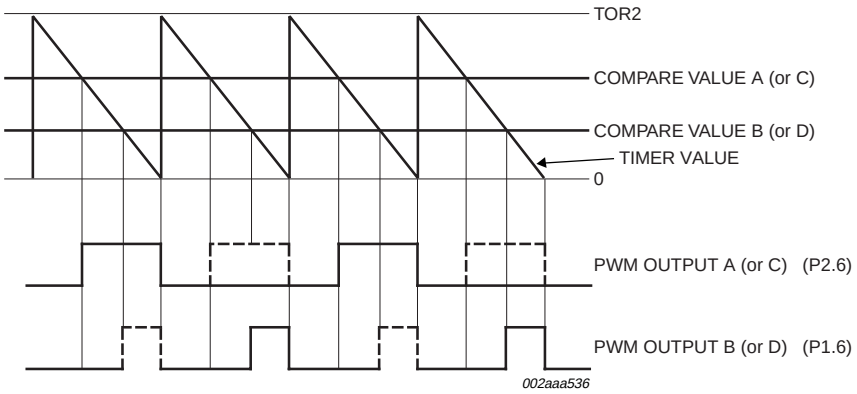

Fig 10. Alternate output mode.

8.18.8 PLL operation

The PWM module features a Phase Locked Loop that can be used to generate a CCUCLK frequency between 16 MHz and 32 MHz. At this frequency the PWM module provides ultrasonic PWM frequency with 10-bit resolution provided that the crystal frequency is 1 MHz or higher. The PLL is fed an input signal of 0.5 - 1 MHz and generates an output signal of 32 times the input frequency. This signal is used to clock the timer. The user will have to set a divider that scales PCLK by a factor of 1-16. This divider is found in the SFR register TCR21. The PLL frequency can be expressed as shown in Equation 1.

$$\text{PLL frequency} = \frac{\text{PLCK}}{(N+1)} \quad (1)$$

Where: N is the value of PLLDV3:0.

Since N ranges in 0 - 15, the CCLK frequency can be in the range of PCLK to $^{PCLK}/_{16}$.

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8.18.9 CCU interrupts

There are seven interrupt sources on the CCU which share a common interrupt vector.

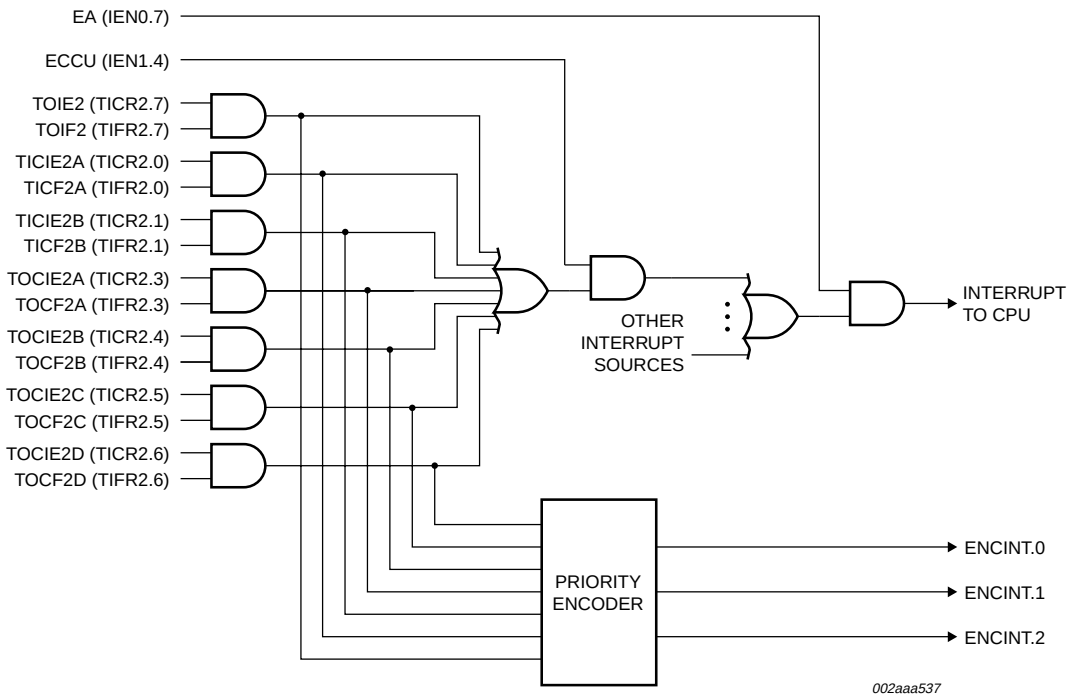

Fig 11. Capture/Compare Unit interrupts.

8.19 UART

The P89LPC932 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC932 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in 4 modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

8.19.1 Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $1/16$ of the CPU clock frequency.

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8.19.2 Mode 1

10 bits are transmitted (through TxD) or received (through RxD): a start bit (logical ‘0’), 8 data bits (LSB first), and a stop bit (logical ‘1’). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 8.19.5 “Baud rate generator and selection”).

8.19.3 Mode 2

11 bits are transmitted (through TxD) or received (through RxD): start bit (logical ‘0’), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical ‘1’). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of ‘0’ or ‘1’. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is not saved. The baud rate is programmable to either $^{1}/_{16}$ or $^{1}/_{32}$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

8.19.4 Mode 3

11 bits are transmitted (through TxD) or received (through RxD): a start bit (logical ‘0’), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical ‘1’). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 8.19.5 “Baud rate generator and selection”).

8.19.5 Baud rate generator and selection

The P89LPC932 enhanced UART has an independent Baud Rate Generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see Figure 12). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent Baud Rate Generator uses OSCCLK.

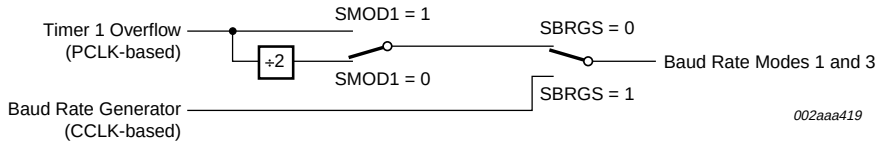

Fig 12. Baud rate sources for UART (Modes 1, 3).

8.19.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is ‘1’, framing errors can be made available in SCON.7 respectively. If SMOD0 is ‘0’, SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON.7:6) are set up when SMOD0 is ‘0’.

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8.19.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

8.19.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = '0'), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = '0').

8.19.9 Transmit interrupts with double buffering enabled (Modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the Tx interrupt is generated when the double buffer is ready to receive new data.

8.19.10 The 9th bit (bit 8) in double buffering (Modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the Tx interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

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8.20 I²C-bus serial interface

I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bi-directional data transfer between masters and slaves
- Multimaster bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus configuration is shown in Figure 13. The P89LPC932 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz.

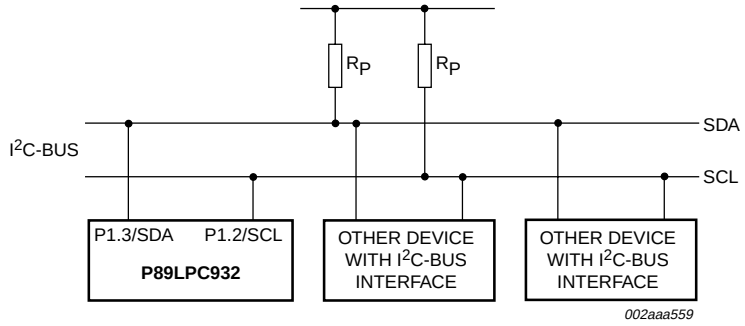

Fig 13. I²C-bus configuration.

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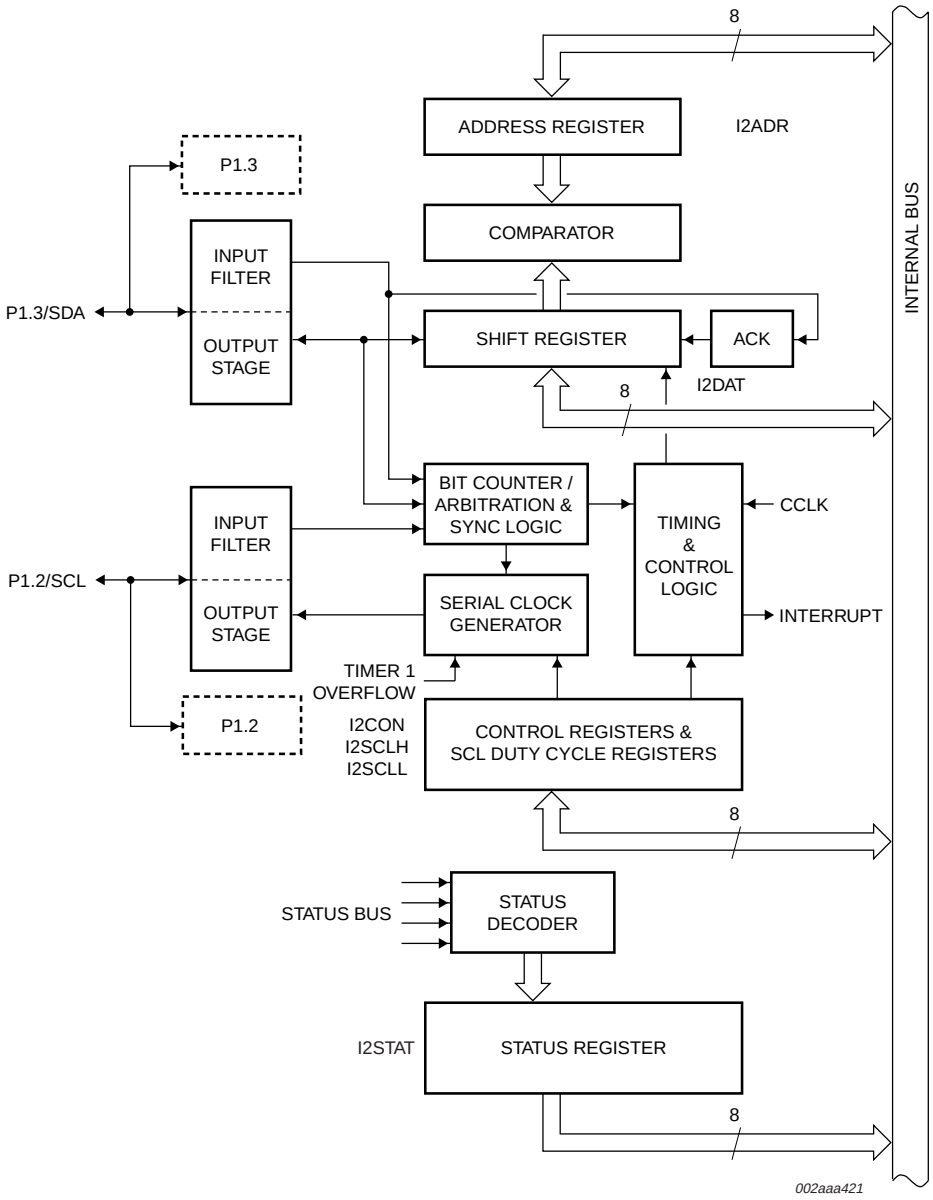

Fig 14. I²C-bus serial interface block diagram.

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8.21 Serial Peripheral Interface (SPI)

The P89LPC932 provides another high-speed serial communication interface—the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 3 Mbit/s can be supported in either Master or Slave mode. It has a Transfer Completion Flag and Write Collision Flag Protection.

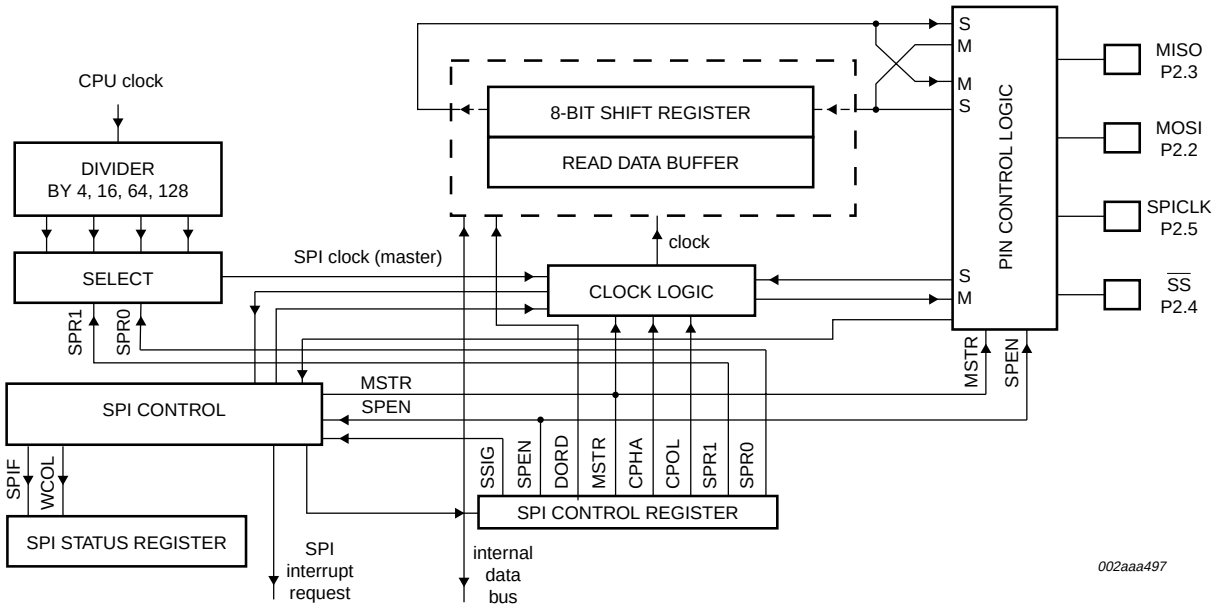

Fig 15. SPI block diagram.

The SPI interface has four pins: SPICLK, MOSI, MISO and $\overline{SS}$:

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the master mode and is input in the slave mode. If the SPI system is disabled, i.e., SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.
- $\overline{SS}$ is the optional slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its $\overline{SS}$ pin to determine whether it is selected.

Typical connections are shown in Figures 16 through 18.

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8.21.1 Typical SPI configurations

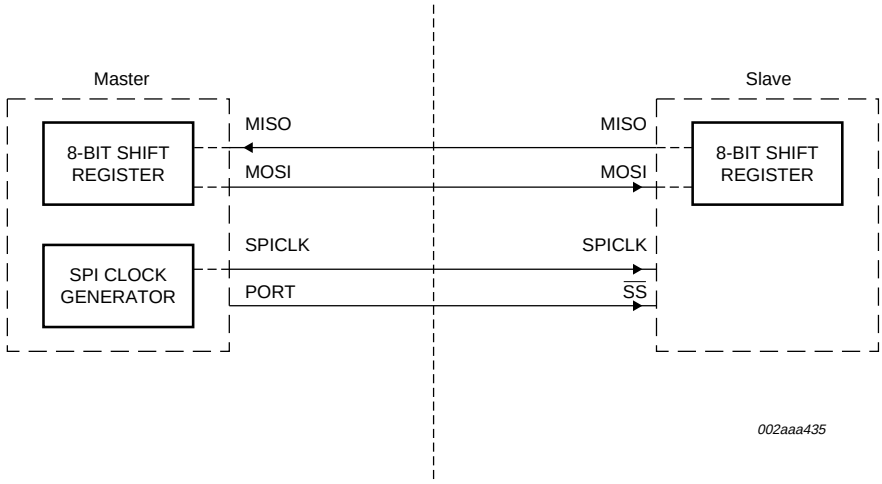

Fig 16. SPI single master single slave configuration.

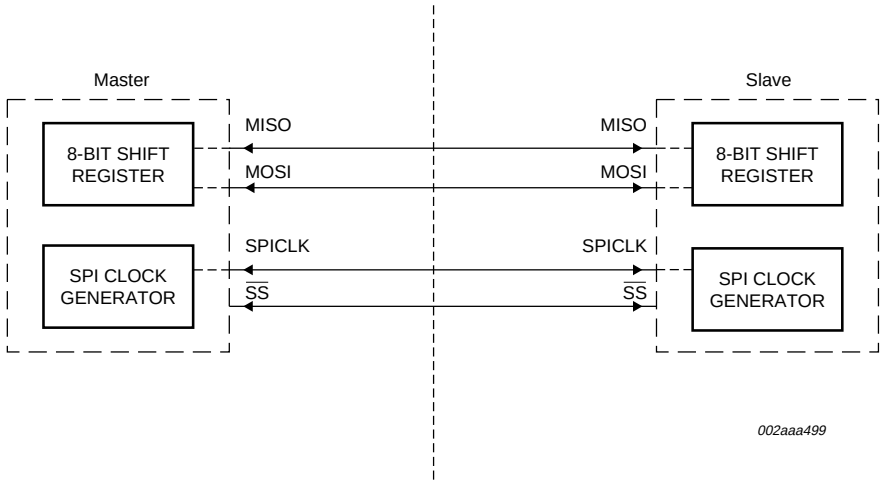

Fig 17. SPI dual device configuration, where either can be a master or a slave.

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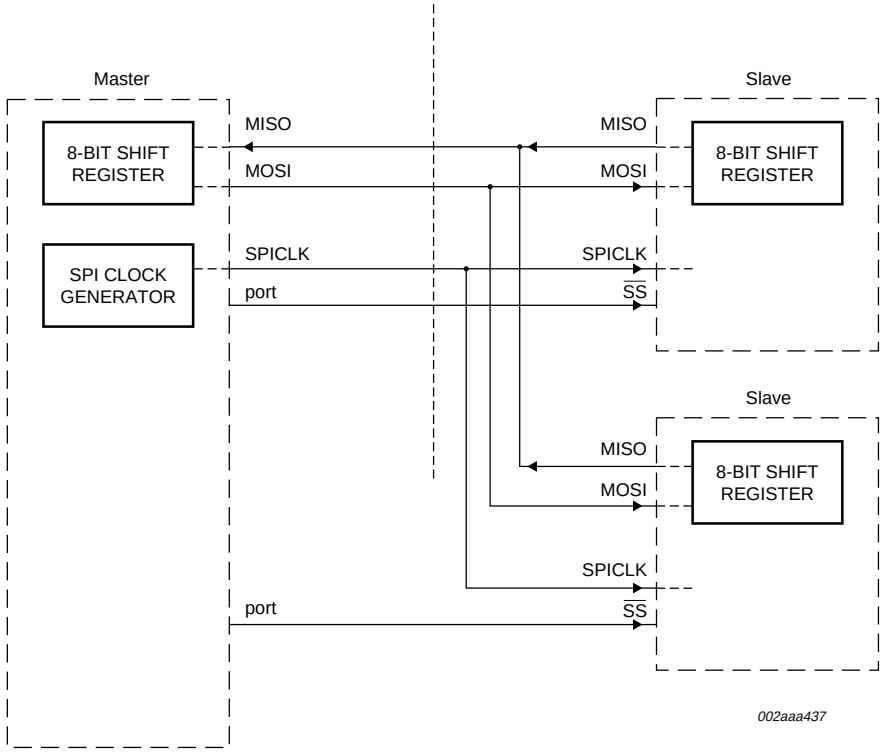

Fig 18. SPI single master multiple slaves configuration.

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8.22 Analog comparators

Two analog comparators are provided on the P89LPC932. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logical one (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

The overall connections to both comparators are shown in Figure 19. The comparators function to V_{DD} = 2.4 V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

When a comparator is disabled the comparator's output, COx, goes HIGH. If the comparator output was LOW and then is disabled, the resulting transition of the comparator output from a LOW to HIGH state will set the comparator flag, CMFx. This will cause an interrupt if the comparator interrupt is enabled. The user should therefore disable the comparator interrupt prior to disabling the comparator. Additionally, the user should clear the comparator flag, CMFx, after disabling the comparator.

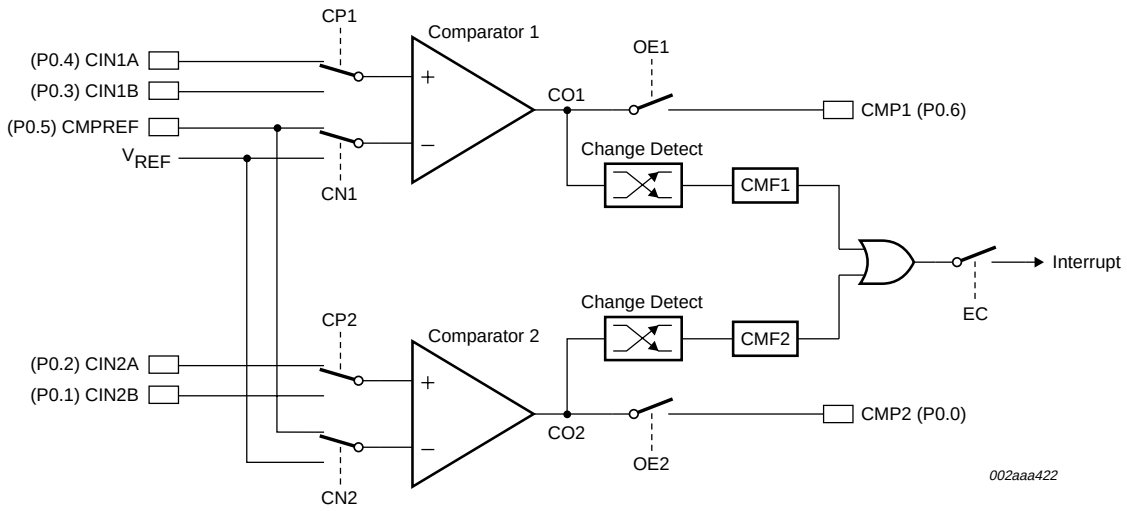

Fig 19. Comparator input and output connections.

8.22.1 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as V_{REF}, is 1.23 V ±10%.

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8.22.2 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

8.22.3 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode.

If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the **oscillator** stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

8.23 Keypad interrupt (KBI)

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than 6 CCLKs.

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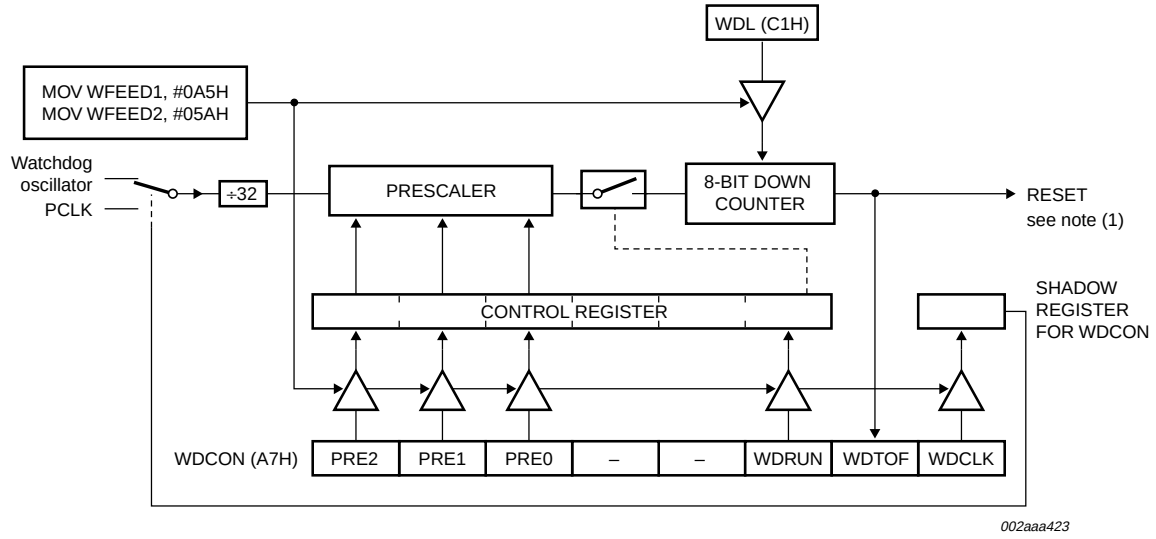
8.24 Watchdog timer

The Watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler is either the PCLK or the nominal 400 kHz Watchdog oscillator. The Watchdog timer can only be reset by a power-on reset. When the watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 20 shows the Watchdog timer in watchdog mode. Feeding the watchdog requires a two-byte sequence. If PCLK is selected as the watchdog clock and the CPU is powered-down, the watchdog is disabled. The Watchdog timer has a time-out period that ranges from a few µs to a few seconds. Please refer to the *P89LPC932 User's Manual* for more details.



(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 20. Watchdog timer in watchdog mode (WDTE = '1').

8.25 Additional features

8.25.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

8.25.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic '0' so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

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8.26 Data EEPROM

The P89LPC932 has 512 bytes of on-chip Data EEPROM. The Data EEPROM is SFR based, byte readable, byte writable, and erasable (via row fill and sector fill). The user can read, write and fill the memory via SFRs and one interrupt. This Data EEPROM provides 100,000 minimum erase/program cycles for each byte.

- **Byte Mode:** In this mode, data can be read and written one byte at a time.
- **Row Fill:** In this mode, the addressed row (64 bytes) is filled with a single value. The entire row can be erased by writing 00h.
- **Sector Fill:** In this mode, all 512 bytes are filled with a single value. The entire sector can be erased by writing 00h.

After the operation finishes, the hardware will set the EEIF bit, which if enabled will generate an interrupt. The flag is cleared by software.

8.27 Flash program memory

8.27.1 General description

The P89LPC932 Flash memory provides in-circuit electrical erasure and programming. The Flash can be read, erased, or written as bytes. The Sector and Page Erase functions can erase any Flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. In-System Programming and standard parallel programming are both available. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC932 Flash reliably stores memory contents even after 10,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC932 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

8.27.2 Features

- Internal fixed boot ROM, containing low-level In-Application Programming (IAP) routines
- User programs can call these routines to perform In-Application Programming (IAP).
- Default loader providing In-System Programming via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided Flash loader code to reside anywhere in the Flash memory space, providing flexibility to the user.
- Programming and erase over the full operating voltage range.
- Read/Programming/Erase using ISP/IAP.
- Any flash program/erase operation in 2 ms.
- Parallel programming with industry-standard commercial programmers.
- Programmable security for the code in the Flash for each sector.
- 100,000 typical erase/program cycles for each byte.
- 10 year minimum data retention.

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8.27.3 ISP and IAP capabilities of the P89LPC932

Flash organization: The P89LPC932 program memory consists of eight 1 kB sectors. Each sector can be further divided into 64-byte pages. In addition to sector erase and page erase, a 64-byte page register is included which allows from 1 to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time. An In-Application Programming (IAP) interface is provided to allow the end user's application to erase and reprogram the user code memory. In addition, erasing and reprogramming of user-programmable bytes including UCFG1, the Boot Status Bit and the Boot Vector are supported. As shipped from the factory, the upper 512 bytes of user code space contains a serial In-System Programming (ISP) routine allowing for the device to be programmed in circuit through the serial port.

Flash programming and erasing: There are three methods of erasing or programming of the Flash memory that may be used. First, the Flash may be programmed or erased in the end-user application by calling low-level routines through a common entry point. Second, the on-chip ISP boot loader may be invoked. This ISP boot loader will, in turn, call low-level routines through the same common entry point that can be used by the end-user application. Third, the Flash may be programmed or erased using the parallel method by using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire 8 kB of user code space.

Boot ROM: When the microcontroller programs its own Flash memory, all of the low-level details are handled by code that is contained in a Boot ROM that is separate from the Flash memory. A user program simply calls the common entry point in the Boot ROM with appropriate parameters to accomplish the desired operation. The Boot ROM include operations such as erase sector, erase page, program page, CRC, program security bit, etc. The Boot ROM occupies the program memory space at the top of the address space from FF00 to FEFF hex, thereby not conflicting with the user program memory space.

Power-on reset code execution: The P89LPC932 contains two special Flash elements: the Boot Vector and the Boot Status Bit. Following reset, the P89LPC932 examines the contents of the Boot Status Bit. If the Boot Status Bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status Bit is set to a value other than zero, the contents of the Boot Vector is used as the high byte of the execution address and the low byte is set to 00H. The factory default setting is 01EH and corresponds to the address 1E00H for the default ISP boot loader. This boot loader is pre-programmed at the factory into this address space and can be erased by the user. **Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector from 1C00H to 1FFFH. Instead, the page erase function can be used to erase the eight 64-byte pages located from 1C00H to 1DFFH.** A custom boot loader can be written with the Boot Vector set to the custom boot loader, if desired.

Hardware activation of the boot loader: The boot loader can also be executed by forcing the device into ISP mode during a power-on sequence (see the *P89LPC932 User's Manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting

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for the Boot Vector (1EH) is changed, it will no longer point to the factory pre-programmed ISP boot loader code. If this happens, the only way it is possible to change the contents of the Boot Vector is through the parallel programming method, provided that the end user application does not contain a customized loader that provides for erasing and reprogramming of the Boot Vector and Boot Status Bit. After programming the Flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

In-System Programming (ISP): In-System Programming is performed without removing the microcontroller from the system. The In-System Programming facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC932 through the serial port. This firmware is provided by Philips and embedded within each P89LPC932 device. The Philips In-System Programming facility has made in-system programming in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins (V_{DD}, V_{SS}, TXD, RXD, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

In-Application Programming (IAP): Several In-Application Programming (IAP) calls are available for use by an application program to permit selective erasing and programming of Flash sectors, pages, security bits, configuration bytes, and device identification. All calls are made through a common interface, PGM_MTP. The programming functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF00H.

8.28 User configuration bytes

A number of user-configurable features of the P89LPC932 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the Flash byte UCFG1. Please see the *P89LPC932 User's Manual* for additional details.

8.29 User sector security bytes

There are eight User Sector Security Bytes, each corresponding to one sector. Please see the *P89LPC932 User's Manual* for additional details.

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9. Limiting values

Table 7: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	operating bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature range		–65	+150	°C
V_{xtal}	voltage on XTAL1, XTAL2 pin to V_{SS}		-	V_{DD} + 0.5	V
V_n	voltage on any other pin (except XTAL1, XTAL2) to V_{SS}		–0.5	+5.5	V
$I_{OH(I/O)}$	HIGH-level output current per I/O pin		-	20	mA
$I_{OL(I/O)}$	LOW-level output current per I/O pin		-	20	mA
$I_{I/O(tot)(max)}$	maximum total I/O current		-	100	mA
$P_{tot(pack)}$	total power dissipation per package	based on package heat transfer, not device power consumption	-	1.5	W

[1] Stresses above those listed under Table 7 “Limiting values” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in Table 8 “DC electrical characteristics” and Table 9 “AC characteristics” of this specification are not implied.

[2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

[3] Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

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10. Static characteristics

Table 8: DC electrical characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = 0 °C to +70 °C for commercial, −40 °C to +85 °C for industrial, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{DD}	power supply current, operating	3.6 V; 12 MHz	[7]	-	11	18	mA
I_{ID}	power supply current, Idle mode	3.6 V; 12 MHz	[7]	-	3.25	5	mA
I_{PD}	Power supply current, Power-down mode, voltage comparators powered-down	3.6 V	[7]	-	-	<t.b.d.>	µA
I_{PD1}	Power supply current, Total Power-down mode	3.6 V	[7]	-	1	5	µA
V_{DDR}	V_{DD} rise time			-	-	2	mV/µs
V_{DDF}	V_{DD} fall time			-	-	50	mV/µs
V_{POR}	Power-on reset detect voltage			-	-	0.2	V
V_{RAM}	RAM keep-alive voltage			1.5	-	-	V
$V_{th(HL)}$	negative-going threshold voltage	except SCL, SDA		$0.22V_{DD}$	$0.4V_{DD}$	-	V
V_{IL1}	LOW-level input voltage	SCL, SDA only		−0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	positive-going threshold voltage	except SCL, SDA		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{IH1}	HIGH-level input voltage	SCL, SDA only		$0.7V_{DD}$	-	5.5	V
V_{hys}	hysteresis voltage	Port 1		-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage, all ports, all modes except Hi-Z	I_{OL} = 20 mA; V_{DD} = 2.4 V – 3.6 V	[5]	-	0.6	1.0	V
		I_{OL} = 3.2 mA; V_{DD} = 2.4 V – 3.6 V	[5]	-	0.2	0.3	V
V_{OH}	HIGH-level output voltage, all ports	I_{OH} = −20 µA; V_{DD} = 2.4 V – 3.6 V; quasi-bidirectional mode		V_{DD} – 0.3	V_{DD} – 0.2	-	V
		I_{OH} = −3.2 mA; V_{DD} = 2.4 V – 3.6 V; push-pull mode		V_{DD} – 0.7	V_{DD} – 0.4	-	V
		I_{OH} = −20 mA; V_{DD} = 2.4 V – 3.6 V; push-pull mode		<t.b.d>	-	-	V
C_{io}	input/output pin capacitance		[6]	-	-	15	pF
I_{IL}	logical 0 input current, all ports	V_{IN} = 0.4 V	[4]	-	-	−80	µA
I_{LI}	input leakage current, all ports	V_{IN} = V_{IL} or V_{IH}	[3]	-	-	±10	µA
I_{TL}	logical 1-to-0 transition current, all ports	V_{IN} = 2.0 V at V_{DD} = 3.6 V	[2]	−30	-	−450	µA
R_{RST}	internal reset pull-up resistor			10	-	30	kΩ
V_{BO}	brownout trip voltage with BOV = '1', BOPD = '0'	2.4 V < V_{DD} < 3.6 V		2.40	-	2.70	V
V_{REF}	bandgap reference voltage			1.11	1.23	1.34	V
$TC_{(VREF)}$	bandgap temperature coefficient			-	10	20	ppm/°C

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[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from ‘1’ to ‘0’. This current is highest when V_{IN} is approximately 2 V.

[3] Measured with port in high-impedance mode.

[4] Measured with port in quasi-bidirectional mode.

[5] See Section 9 “Limiting values” on page 44 for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[6] Pin capacitance is characterized but not tested.

[7] The I_{DD}, I_{ID}, and I_{PD} specifications are measured using an external clock with the following functions disabled: comparators, brownout detect, and Watchdog timer.

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11. Dynamic characteristics

Table 9: AC characteristics

T_{amb} = 0 °C to +70 °C for commercial, −40 °C to +85 °C for industrial, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Variable clock		f_{OSC} = 12 MHz		Unit
			Min	Max	Min	Max	
f_{RCOSC}	internal RC oscillator frequency		7.189	7.557	7.189	7.557	MHz
f_{WDOSC}	internal Watchdog oscillator frequency		280	480	280	480	kHz
f_{OSC}	oscillator frequency		0	12	-	-	MHz
t_{CLCL}	clock cycle	see Figure 22	83	-	-	-	ns
f_{CLKLP}	CLKLP active frequency		0	8	-	-	MHz
Glitch filter							
	glitch rejection, P1.5/$\overline{RST}$ pin		-	50	-	50	ns
	signal acceptance, P1.5/$\overline{RST}$ pin		125	-	125	-	ns
	glitch rejection, any pin except P1.5/$\overline{RST}$		-	15	-	15	ns
	signal acceptance, any pin except P1.5/$\overline{RST}$		50	-	50	-	ns
External clock							
t_{CHCX}	HIGH time	see Figure 22	33	$t_{CLCL} - t_{CLCX}$	33	-	ns
t_{CLCX}	LOW time	see Figure 22	33	$t_{CLCL} - t_{CHCX}$	33	-	ns
t_{CLCH}	rise time	see Figure 22	-	8	-	8	ns
t_{CHCL}	fall time	see Figure 22	-	8	-	8	ns
Shift register (UART mode 0)							
t_{XLXL}	serial port clock cycle time	see Figure 21	16 t_{CLCL}	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge	see Figure 21	13 t_{CLCL}	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge	see Figure 21	-	t_{CLCL} + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge	see Figure 21	-	0	-	0	ns
t_{DVXH}	input data valid to clock rising edge	see Figure 21	150	-	150	-	ns
SPI interface							
f_{SPI}	operating frequency						
	2.0 MHz (master)		-	-	-	-	MHz
	2.0 MHz (slave)		0	2.0	0	2.0	MHz
	3.0 MHz (master)		-	-	-	-	MHz
	3.0 MHz (slave)		0	3.0	0	3.0	MHz
t_{SPICYC}	cycle time	see Figures 23, 24, 25, 26					
	2.0 MHz (master)		-	-	-	-	ns
	2.0 MHz (slave)		500	-	500	-	ns
	3.0 MHz (master)		-	-	-	-	ns
	3.0 MHz (slave)		333	-	333	-	ns

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Table 9: AC characteristics *...continued*

T_{amb} = 0 °C to +70 °C for commercial, −40 °C to +85 °C for industrial, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Variable clock		f_{OSC} = 12 MHz		Unit
			Min	Max	Min	Max	
$t_{SPILEAD}$	enable lead time (slave)	see Figures 25, 26					
	2.0 MHz		250	-	250	-	ns
	3.0 MHz		240	-	240	-	ns
t_{SPILAG}	enable lag time (slave)	see Figures 25, 26					
	2.0 MHz		250	-	250	-	ns
	3.0 MHz		240	-	240	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figures 23, 24, 25, 26					
	master		340	-	340	-	ns
	slave		190	-	190	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figures 23, 24, 25, 26					
	master		340	-	340	-	ns
	slave		190	-	190	-	ns
t_{SPIDSU}	data set-up time (master or slave)	see Figures 23, 24, 25, 26	100	-	100	-	ns
t_{SPIDH}	data hold time (master or slave)	see Figures 23, 24, 25, 26	100	-	100	-	ns
t_{SPIA}	access time (slave)	see Figures 25, 26	0	120	0	120	ns
t_{SPIDIS}	disable time (slave)	see Figures 25, 26					
	2.0 MHz		0	240	-	240	ns
	3.0 MHz		0	167	-	167	ns
t_{SPIDV}	enable to output data valid	see Figures 23, 24, 25, 26					
	2.0 MHz		-	240	-	240	ns
	3.0 MHz		-	167	-	167	ns
t_{SPIOH}	output data hold time	see Figures 23, 24, 25, 26	0	-	0	-	ns
t_{SPIR}	rise time	see Figures 23, 24, 25, 26					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	fall time	see Figures 23, 24, 25, 26					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

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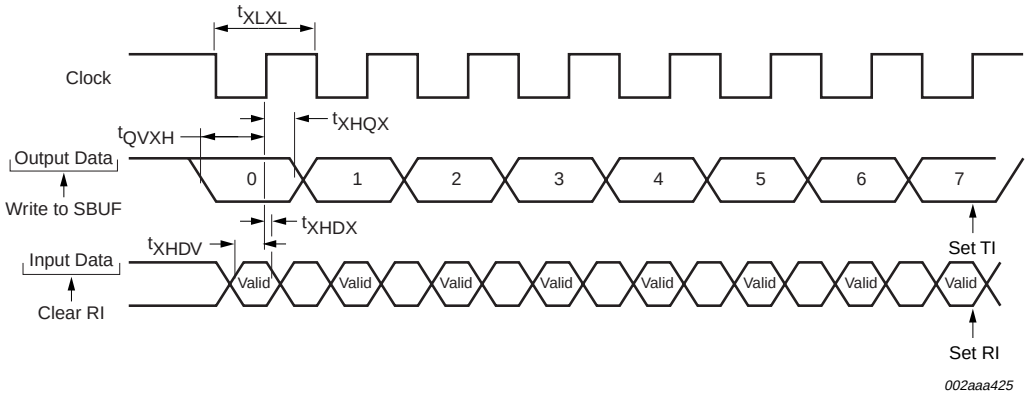

Fig 21. Shift register mode timing.

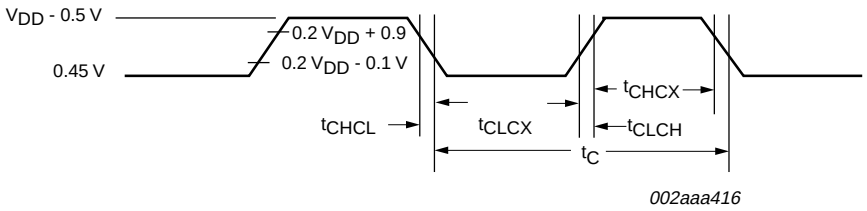

Fig 22. External clock timing.

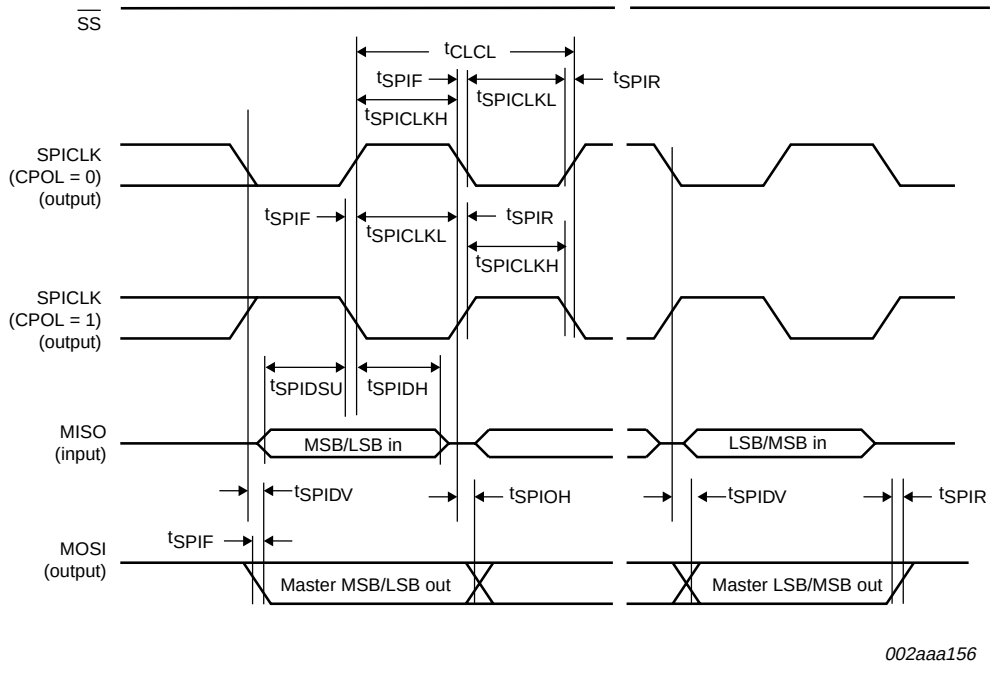

Fig 23. SPI master timing (CPHA = '0')

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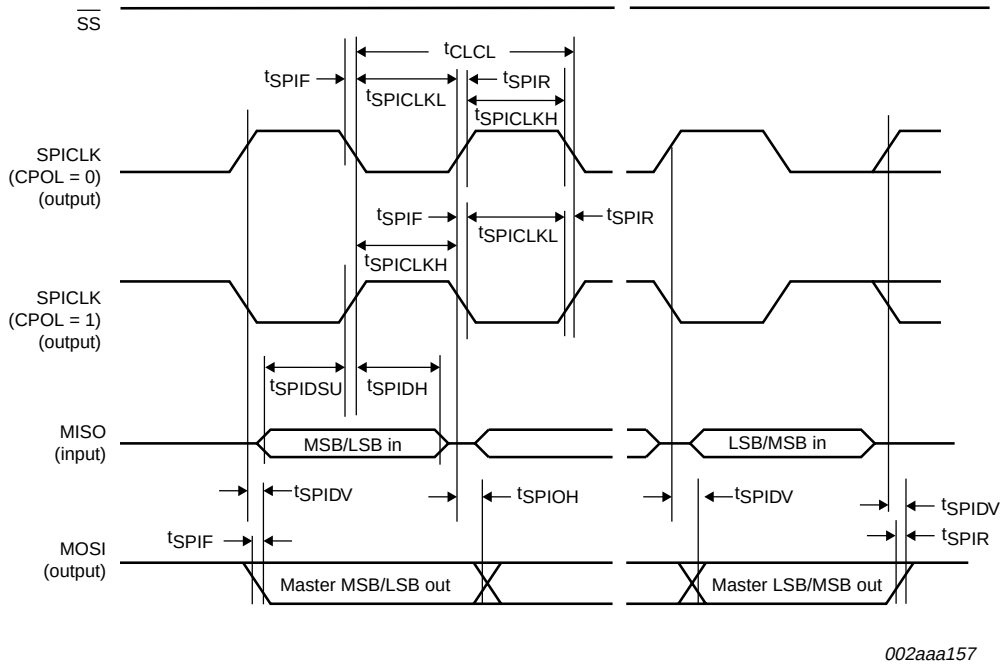

Fig 24. SPI master timing (CPHA = '1')

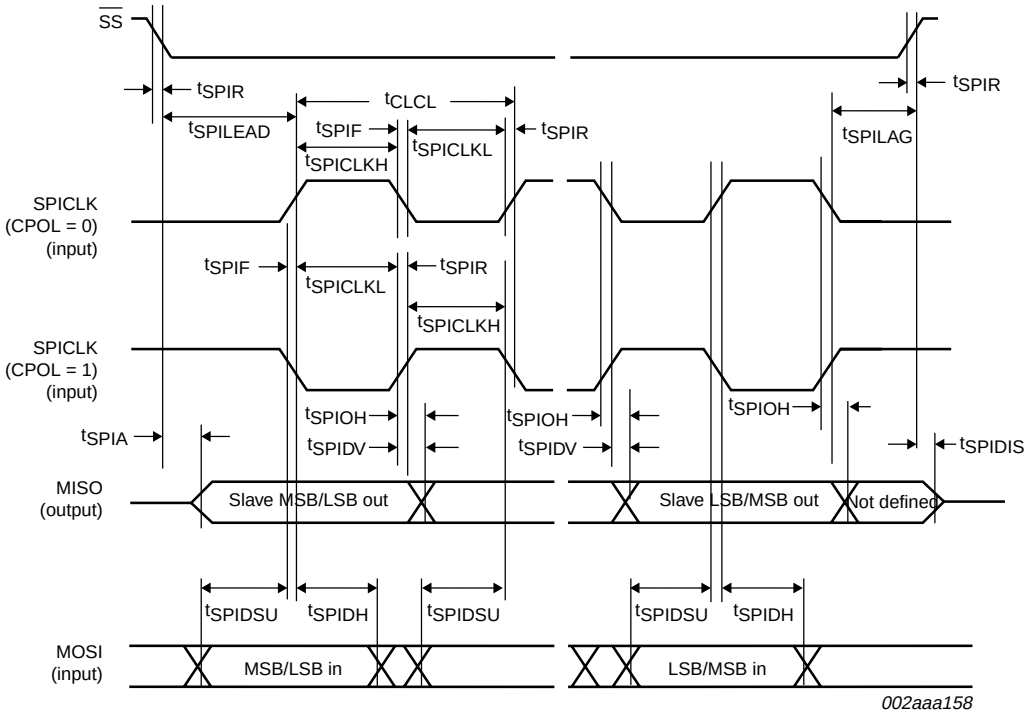

Fig 25. SPI slave timing (CPHA = '0')

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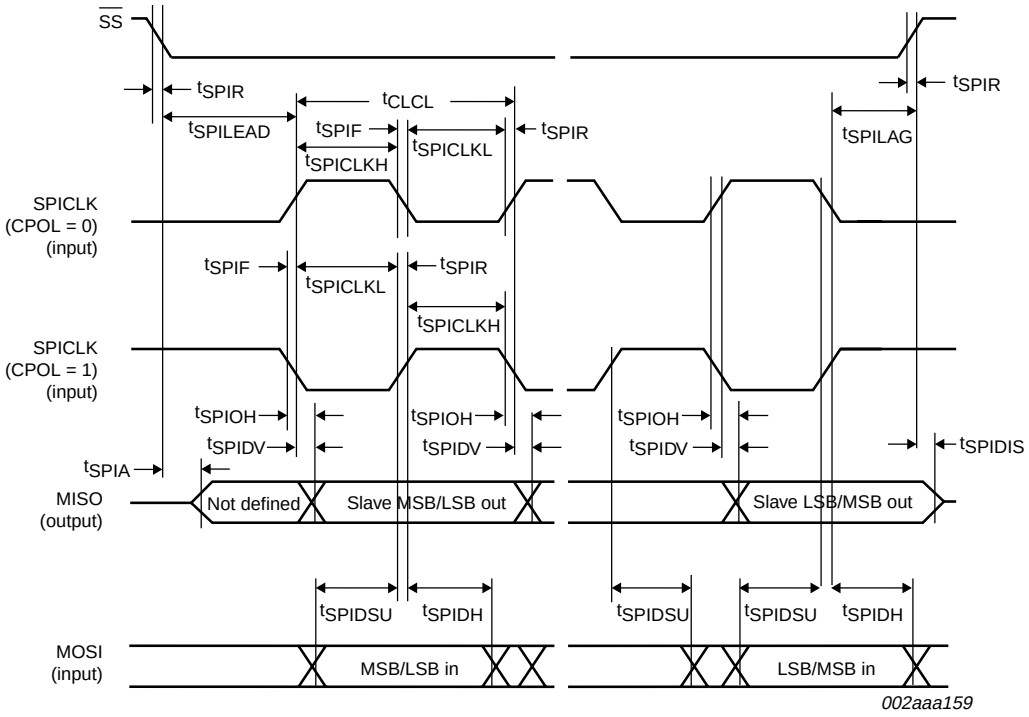

Fig 26. SPI slave timing (CPHA = '1')

Table 10: AC characteristics, ISP entry mode

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = 0 °C to +70 °C for commercial, −40 °C to +85 °C for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VR}	$\overline{RST}$ delay from V_{DD} active		50	-	-	µs
t_{RH}	$\overline{RST}$ HIGH time		1	-	32	µs
t_{RL}	$\overline{RST}$ LOW time		1	-	-	µs

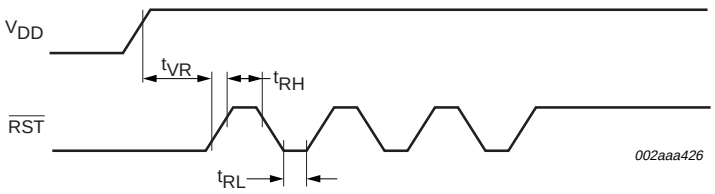

Fig 27. ISP entry waveform.

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12. Comparator electrical characteristics

Table 11: Comparator electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = 0 °C to +70 °C for commercial, −40 °C to +85 °C for industrial, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IO}	offset voltage comparator inputs			-	-	±20	mV
V_{CR}	common mode range comparator inputs			0	-	V_{DD} − 0.3	V
CMRR	common mode rejection ratio		[1]	-	-	−50	dB
	response time			-	250	500	ns
	comparator enable to output valid			-	-	10	µs
I_{IL}	input leakage current, comparator	$0 < V_{IN} < V_{DD}$		-	-	±10	µA

[1] This parameter is characterized, but not tested in production.

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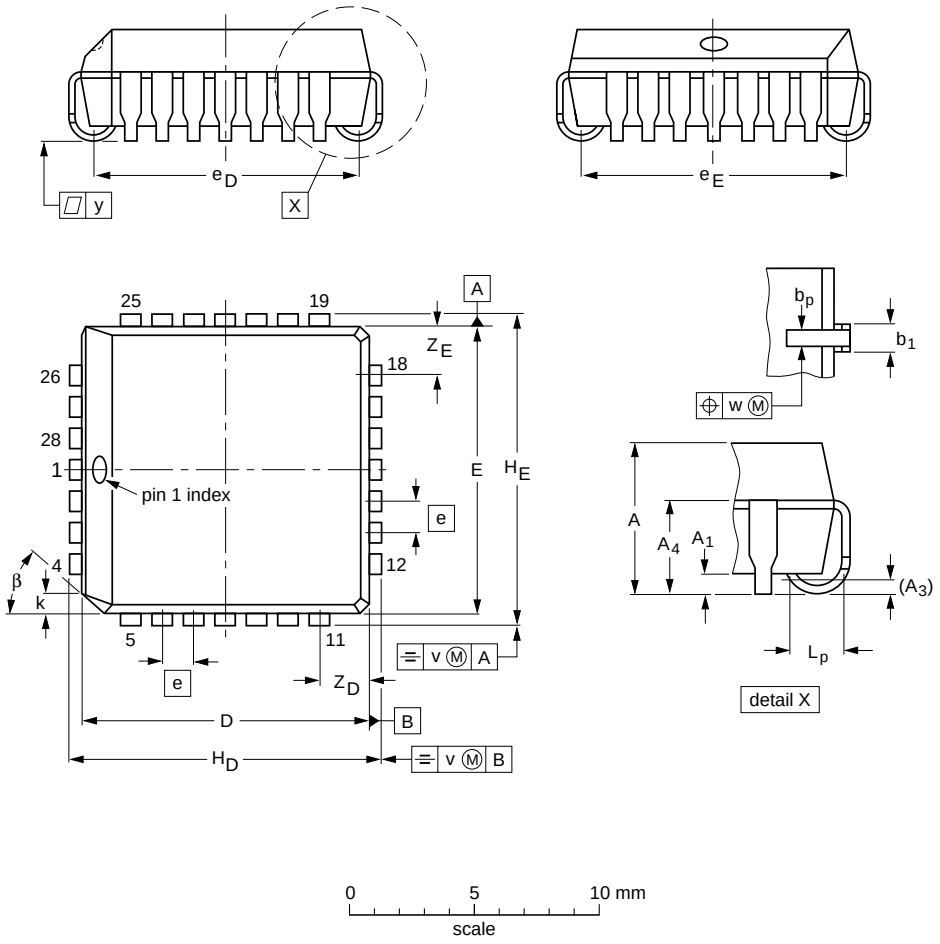
13. Package outline

PLCC28: plastic leaded chip carrier; 28 leads **SOT261-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.43 0.39	0.43 0.39	0.495 0.485	0.495 0.485	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT261-2	112E08	MS-018	EDR-7319			~~99-12-27~~ 01-11-15

Fig 28. PLCC28 package outline (SOT261-2).

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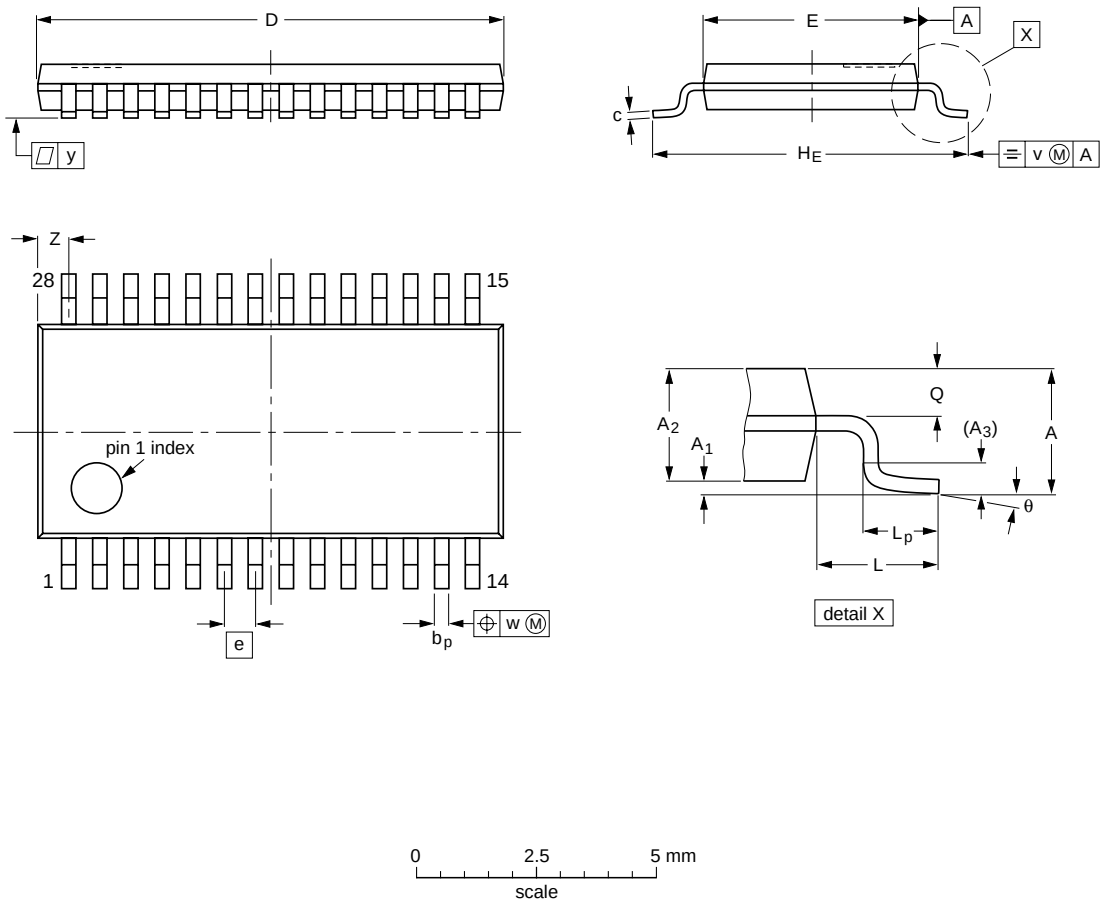
TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm **SOT361-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	9.8 9.6	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.8 0.5	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT361-1		MO-153				~~99-12-27~~ 03-02-19

Fig 29. TSSOP28 package outline (SOT361-1).

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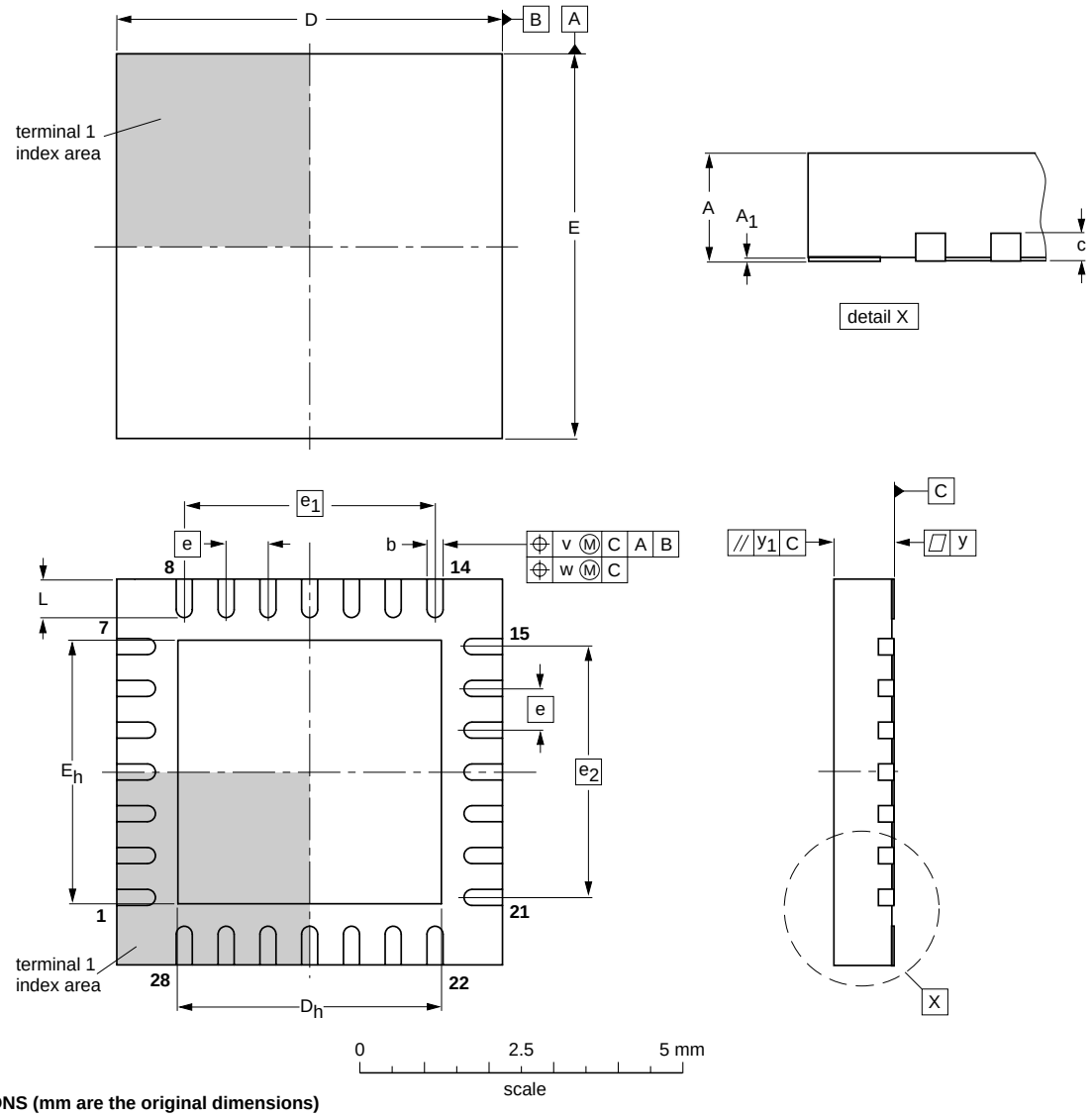
HVQFN28: plastic thermal enhanced very thin quad flat package; no leads; 28 terminals; body 6 x 6 x 0.85 mm **SOT788-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.35 0.25	0.2	6.1 5.9	4.25 3.95	6.1 5.9	4.25 3.95	0.65	3.9	3.9	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT788-1	- - -	MO-220	- - -			02-10-22

Fig 30. HVQFN28 package outline (SOT788-1).

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14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

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- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.5 Package related soldering information

Table 12: Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

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[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

15. Revision history

Table 13: Revision history

Rev	Date	CPCN	Description
04	20040106	-	**Product data (9397 750 12379); ECN 853-2433 01-A15016 dated 16 December 2003** Modifications: • Table 4 “Special function registers”: changed PLEEN to PLLEN. • Section 8.27.2 “Features” on page 41: adjusted bullet for erase/program cycles • Table 8 “DC electrical characteristics” on page 45: adjusted value for I_{TL} V_{IN}.
03	20031007	-	**Product data (9397 750 12119); ECN 853-2433 30392 dated 30 September 2003**
02	20030725	-	**Product data (9397 750 11712); ECN 853-2433 30141 dated 23 July 2003. Supersedes Preliminary data P89LPC932_1 of 21 October 2002 (9397 750 10475)**

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16. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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