

□ MN102L360C

Type	MN102L360C
ROM (×8-bit)	External
RAM (×8-bit)	5 K
Package	LQFP128-P-1818C *Lead-free
Minimum Instruction Execution Time	100 ns (at 4.5 V to 5.5 V, 20 MHz)
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • Timer counter 0 to 5 • Fixed-length serial ch.0,1 transmission • Fixed-length serial ch.0,1 reception • Timer counter 6 to 7 • Timer counter 6 to 7 compare capture A • Timer counter 6 to 7 compare capture B • ATC transfer finish • External 0 to 7 • Serial ch.0,1 transmission • Serial ch.0,1 reception • NMI pin • A/D conversion finish
Timer Counter	<p>Timer counter 0: 8-bit × 1 (timer output, event count) Clock source 1/1, 1/128 of system clock frequency; 1/4 of low speed clock frequency; external clock Interrupt source timer counter 0 underflow</p> <p>Timer counter 1: 8-bit × 1 (timer output, even count, A/D conversion start) Clock source system clock; 1/4 of low speed clock frequency; external clock; timer counter 0 output Interrupt source timer counter 1 underflow</p> <p>Timer counter 2 to 3: 8-bit × 1 (timer output, event count, UART baud rate generation) Clock source system clock; external clock; timer counter 0 output; timer counter 1, 2 output Interrupt source timer counter 2, 3 underflow</p> <p>Timer counter 4,5: 8-bit × 1 (timer output, event count) Clock source 1/4 of low speed clock frequency; external clock; timer counter 0 output; timer counter 3, 4 output Interrupt source timer counter 4, 5 underflow</p> <p>Timer counter 6, 7: 16-bit × 2 (timer output, event count, input capture, output compare, PWM output, 2-phase encoder input) Clock source system clock; external clock; timer counter 4, 5 output Interrupt source coincidence with compare capture A or at capture; coincidence with compare capture B or at capture; underflow of timer counter 6, 7</p> <p>Connectable timer counter 0 to 5</p>
Serial Interface	<p>Serial 0: 7, 8-bit × 1 (common use with UART, transfer direction of MSB/LSB selectable) Clock source 1/16 of timer counter 2 frequency; 1/16 of timer counter 3 frequency; external clock; 1/2 of timer counter 2 frequency I²C mode (master transmission/reception is possible in the single master system.)</p> <p>Serial 1: 7, 8-bit × 1 (common use with UART, transfer direction of MSB/LSB selectable) Clock source 1/16 of timer counter 2 frequency; 1/16 of timer counter 3 frequency; external clock; 1/2 of timer counter 3 frequency I²C mode (master transmission/reception is possible in the single master system.)</p> <p>Fixed-length serial 0: 8-bit × 1 Clock source external clock Sending direction LSB</p> <p>Fixed-length serial 1: 8-bit × 1 Clock source external clock Sending direction LSB</p>
I/O Pins	I/O 83 • Common use: 8 (by 4 bits), 75 (by bit)
A/D Inputs	8-bit × 8-ch. (with S/H)

D/A Outputs	8-bit × 2-ch.
PWM	16-bit × 2-ch.
Notes	Burst ROM interface support, ATC (between serial 0 ch and built-in RAM) support

Electric Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 20 MHz , VDD = 5.0 V			75	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output			50	μA
Supply current at HALT	IDDH	pins are simultaneously applied VDD or VSS level f = 20 MHz , VDD = 5.0 V, output open			30	mA

(Ta = -40°C to +85°C , VDD = 5.0 V , VSS = 0 V)

Pin Assignment



LQFP128-P-1818C *Lead-free

* Port unusable

See the next page for support tool.

Support Tool

■ In-circuit Emulator	PX-ICE102L00 + PX-PRB102L36-LQFP128-P-1818C	
■ EPROM Built-in Type	Type	MN102LP36Z
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	10 K
	Minimum instruction execution time	100 ns (at 4.5 V to 5.5 V, 20 MHz)
	Package	LQFP128-P-1818C *Lead-free

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