❑ MN103E0600YD

Type		MN103E0600YD (under development)
Instruction Cache		16 K-byte (4-way, set-associative)
Data Cashe		16 K-byte (4-way, set-associative)
Package		MLGA239-C-1111
Minimum Instruction Execution Time		7.5 ns (at 1.8 V tolerance = ±5% , 133 MHz)
Interrupts		• XIRQ × 8 • NMI • Timer × 14 • DMAC × 4 • WDT • SIO × 6 • I^2C × 2 • Asynchronous bus error
Timer Counter		8-bit timer × 4 (all down counters) Cascade connection possible (usable as a 16/24/32-bit timer) Timer output possible (Duty = 1:1) Internal clock source or external clock source selectable Selectable as a serial interface clock 16-bit timer × 7 (down counters) Cascade connection possible (usable as a 32-bit timer) Timer output possible (Duty = 1:1) Internal clock source or external clock source selectable Partially selectable as a serial interface clock 16-bit timer × 1 (up counter) Internal clock source or external clock source selectable Input capture function (rising edge, falling edges, or both selectable) PWM generating function (compare/capture register × 2 contained) Watchdog timer × 1
DMA Contoroller		Number of channels: 4 Transfer unit: 1/2/4/16 byte Maximum number of bytes transferred: 1Mbyte Start factor: External request, interrupt, software Transfer mode: 2-bus cycle transfer Transfer mode: Batch transfer, intermittent transfer Addressing mode: Source/destination each fixed, increment/decrement specification possible Increment/decrement automatically executed according to the transfer unit
Serial Interface		UART/synchronous (co-used) × 2-ch. UART (with CTS control) × 1-ch.
I/O Pins	**I/O**	19 • Common use : 19
Memory Management Function		32-entry full-associative TLB loaded (instructions/data separated from each other) Address conversion by paging (page size: 1 K-byte. 4 K-byte, 128 K-byte, 4 M-byte variable)
On-chip Bus Controller		Concurrent access from three types of master devices to four types of slave devices possible

System Bus Interface	External memory space allocation to 8 banks possible
Memory Bus Interface	SDRAM directly connected interface contained
I²C Interface	2 ports Master-slave interface (multi-master supported) 3.3 V interface (open drain output)

Electrical Characteristics

Supply current

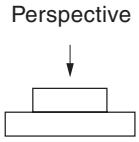
Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	I_{DD18A}	VDD18 = 1.8 V ; VDD33, PVDD = 3.3 V fOSC = 33.33 MHz (core 133 MHz) ; FRQS[1:0] = 0.0 ; Output open	–	–	460	mA
Supply current at stopping	I_{DD18D}	VDD18 = 1.89 V ; VDD33, PVDD = 3.465 V fOSC = Stop ; FRQS[1:0] = 0.0 ; Output open ; Tj = 70°C	–	–	70	mA

(Ta = −20°C to +70°C)

See the next page for pin assignment and support tool.

Pin Assignment

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
16	ND		XSCS5	XSCS2	SD31	SD27	SD21	SD17	SD12	SD8	SD6	SD1	XIRQ7	SD2	ND	
15			XSCS0	XSCS7	SD28	SD29	SD25	SD19	SD13	SD11	SD4	SD3	SD7	XIRQ6		
14	TCP OUT	PIO0[0]	XSCS6	XSCS3	XSDK	SD26	SD24	SD23	SD15	SD18	SD14	SD9	SD0	PIO1[1]	PIO1[3]	PIO1[0]
13	PVDD	XSWE2	PIO0[1]	XSCS4	XSCS1	VDD33	SD22	SD20	SD16	VDD18	SD10	SD5	XIRQ5	PIO1[2]	XIRQ4	XRST OUT
12	PVSS	XSAS	XSWE0	PIO0[2]	VSS	VSS	SD30	VSS	VSS	VDD33	VSS	XNMI	XIRQ1	XIRQ0	XIRQ2	XRE SET
11	OSCI	SRXW	XSWE3	XSWE1	VDD33	VDD18	VSS	VDD33	ND	ND	VSS	XIRQ3	SBT2	SBO2	PIO1[4]	SBI2
10	OSCO	SA1	XSRE	VDD18	VSS	ND	ND	ND	ND	ND	VDD18	PIO1[5]	PIO2[7]	PIO2[5]	PIO2[1]	SBI1
09	SYS CLK	SA3	SA0	VSS	VDD33	ND	ND	ND	ND	ND	VDD33	VSS	PIO2[3]	PIO1[7]	PIO1[6]	SBI0
08	SA2	SA5	SA7	SA8	VSS	ND	ND	ND	ND	ND	ND	VSS	TMS	PIO2[6]	PIO2[4]	PIO2[2]
07	SA9	SA11	SA14	SA4	VDD18	VDD33	ND	ND	ND	ND	ND	VDD33	EXTRG	TRST MOD	TCK	PIO2[0]
06	SA12	SA16	SA6	SA10	SA15	VSS	VSS	VSS	VDD33	VSS	VDD18	VDD18	TRCD6	TRCD7	TDI	TDO
05	SA17	SA20	SA13	SA18	SA21	VSS	VDD33	XMRAS	XMBE1	MD9	VSS	VSS	VSS	TRCD4	TRCD3	TRCD5
04	SA19	SA22	SA24	SA26	VDD33	MA8	MA14	MA12	XMWE	MD6	VDD33	MD12	VDD33	TRCD2	TRCD1	TRC CLK
03	SA23	SA25	SA27	VSS	MA6	MA10	MA9	XMCS1	XMCAS	MD8	MD10	MD3	MD1	MD15	TRCST	TRCD0
02	ND		MA3	MA2	MA1	MA7	VDD18	XMCS0	SDCKE	MD7	MD5	MD11	MD13	MD0	ND	
01			NP	MA4	MA5	MA0	MA13	MA11	SDCLK	XMBE0	SDCKI	MD4	MD2	MD14		



* ND has an electrode (pin) but NC is not guaranteed. Please design so as not to cause short circuit with other wiring on the user board.

* The NDs on the four corners are the lands intended for reinforcement. You are required to connect them to the PCB.

* NP (No pin.) has no electrode.

Support Tool

ROM Emulator	PARTNER-ETII (KMC product)
On-board Development Tools	PX-ODB103E-J (On-board debug unit) PX-ODB-AMT-20 (Trace unit) PARTNER-J (KMC product)

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