☐ MN103001G

Type	MN103001G
Command ROM (×64-bit)	128 K-byte
Data RAM (×32-bit)	8 K-byte
Package	LQFP100-P-1414 *Lead-free
Minimum Instruction Execution Time	17 ns (at 3.0 V to 3.6 V, 60 MHz)
Interrupts	• RESET • IRQ × 8 • NMI • Timer × 18 • SIF × 8 • WDT • A/D • System error

Timer Counter

Timer counter 0 to 3: 32-bit × 1
  (interval timer, event count, timer output, interrupt, clock source for serial I/F, A/D conversion trigger)
    Clock source ····················· IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter
    Interrupt source ·············· underflow of timer counter 0, 1, 2, 3

Timer counter 4 to 7: 32-bit × 1 (interval timer, event count, timer output, PWM output, interrupt)
    Clock source ····················· IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter
    Interrupt source ·············· underflow of timer counter 4, 5, 6, 7

Timer counter 8 to B: 32-bit × 1
  (interval timer, event count, timer output, PWM output, interrupt, clock source for serial I/F)
    Clock source ····················· IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter
    Interrupt source ·············· underflow of timer counter 8, 9, A, B

*: each of timer counters 0 to 3, 4 to 7, and 8 to B can be changed to an 8-, 16-, or 24-bit timer counter.

Timer counter 10: 16-bit × 1
  (interval timer, event count, PWM output, toggle output (2 lines), interrupt, input capture (2 lines), one-shot output)
    Clock source ····················· IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter
    Interrupt source ·············· overflow of timer counter 10; coincidence with compare capture (2 lines) or at capture

Timer counter 11: 16-bit × 1 (interval timer, event count, toggle output, interrupt)
    Clock source ····················· IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter
    Interrupt source ·············· underflow of timer counter

Timer counter 12: 16-bit × 1 (same functions as those of timer counter 11)

Timer counter 13: 16-bit × 1 (same functions as those of timer counter 11)

Watchdog timer: 16- to 25-bit × 1-ch.

Serial Interface

Serial 0: 7-, 8-bit × 1 (clock synchronous, start-stop synchronous, I²C mode)

Serial 1, 2: 7-, 8-bit × 2 (clock synchronous mode)

Serial 3: 7-, 8-bit × 1 (start-stop synchronous mode)
    Clock source ····················· (clock synchronous mode, start-stop synchronous mode)
        IOCLK; underflow of timer counter; external clock
        (I²C mode)
        IOCLK; underflow of timer counter

I/O Pins	**I/O**	53	• Common use
	Output	15	• Common use
	Input	4	• Common use

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■ **A/D Inputs**	10-bit × 4-ch.	
■ **PWM**	16-bit × 1-ch., 8-bit × 8-ch. (common with timer)	
■ **ICR**	16-bit × 2-ch. (common with OCR)	
■ **OCR**	16-bit × 2-ch., 8-bit × 8-ch. (common partially with ICR)	

■ **Electrical Characteristics**

Supply current

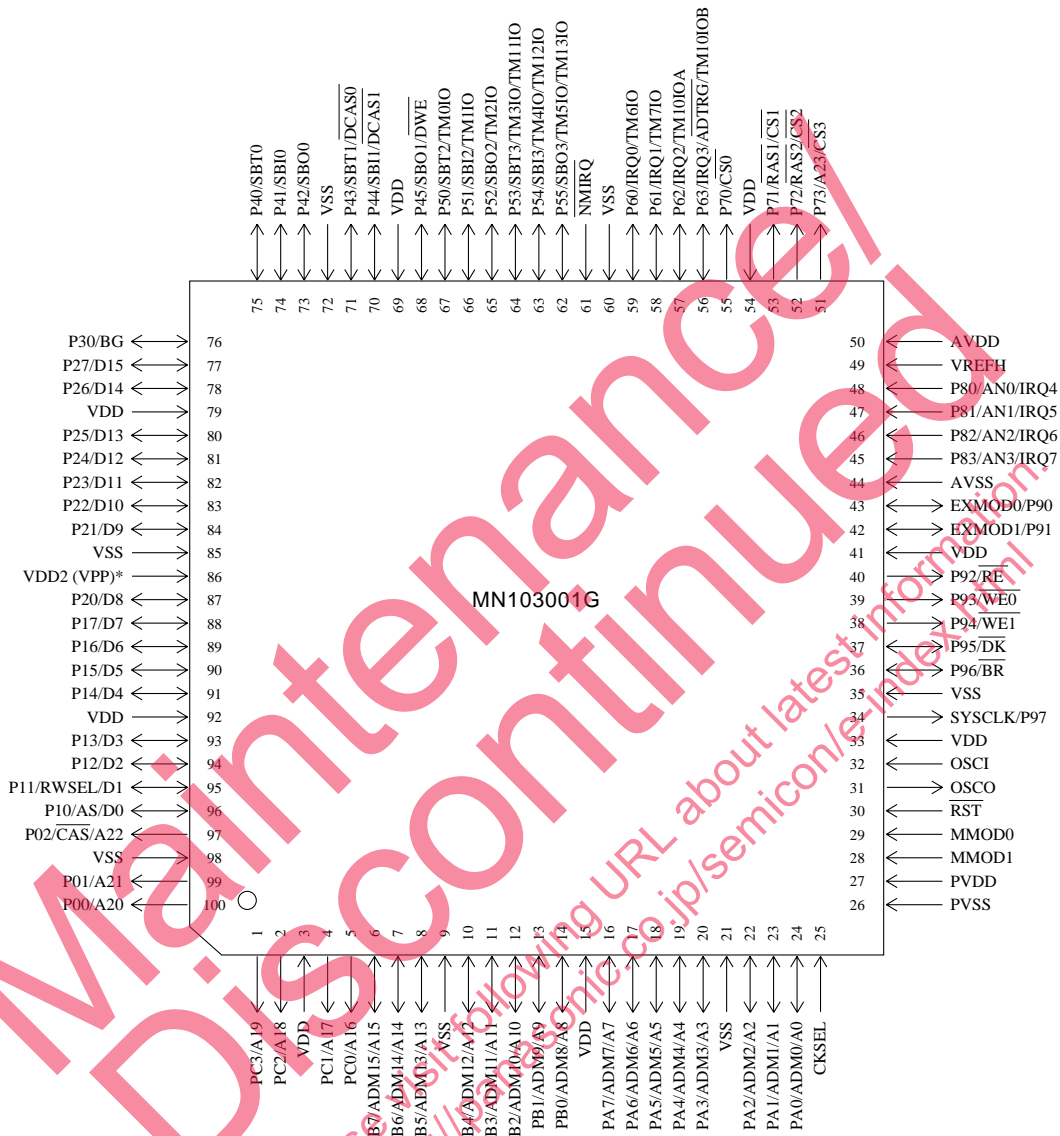| Parameter	Symbol	Condition	Limit min	Limit typ	Limit max	Unit
Operating supply current	IDD1	VDD , PVDD , AVDD = 3.3 V VI = VDD or VSS fosc = 15.0 MHz CKSEL pin = Hi level At internal = 60 MHz Output open			180	mA
Supply current at stopping	IDD4	VDD , PVDD , AVDD = 3.6 V VI = VDD or VSS fosc = Oscillation stopped Output open			100	μA

(Ta = −20°C to +70°C)

A/D conversion performance

Parameter	Symbol	Condition	Limit min	Limit typ	Limit max	Unit
Resolution					10	Bits
A/D conversion absolute error		VREF+ = 3.3 V A/D conversion clock = 5 MHz			± 7	LSB
A/D conversion relative error					± 5	LSB
A/D conversion time			2.8			μ s

(Ta = −20°C to +70°C, AVDD = 3.3 V, AVSS = 0 V)

See the next page for pin assignment and support tool.

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Pin Assignment

MN103001G

Top (pins 75–51):
75 P40/SBT0
74 P41/SBI0
73 P42/SBO0
72 VSS
71 P43/SBT1/DCAS0
70 P44/SBI1/DCAS1
69 VDD
68 P45/SBO1/DWE
67 P50/SBT2/TM0IO
66 P51/SBI2/TM1IO
65 P52/SBO2/TM2IO
64 P53/SBT3/TM3IO/TM11IO
63 P54/SBI3/TM4IO/TM12IO
62 P55/SBO3/TM5IO/TM13IO
61 NMIRQ
60 VSS
59 P60/IRQ0/TM6IO
58 P61/IRQ1/TM7IO
57 P62/IRQ2/TM10IOA
56 P63/IRQ3/ADTRG/TM10IOB
55 P70/CS0
54 VDD
53 P71/RAS1/CS1
52 P72/RAS2/CS2
51 P73/A23/CS3

Left (pins 76–100):
76 P30/BG
77 P27/D15
78 P26/D14
79 VDD
80 P25/D13
81 P24/D12
82 P23/D11
83 P22/D10
84 P21/D9
85 VSS
86 VDD2 (VPP)*
87 P20/D8
88 P17/D7
89 P16/D6
90 P15/D5
91 P14/D4
92 VDD
93 P13/D3
94 P12/D2
95 P11/RWSEL/D1
96 P10/AS/D0
97 P02/CAS/A22
98 VSS
99 P01/A21
100 P00/A20

Right (pins 50–26):
50 AVDD
49 VREFH
48 P80/AN0/IRQ4
47 P81/AN1/IRQ5
46 P82/AN2/IRQ6
45 P83/AN3/IRQ7
44 AVSS
43 EXMOD0/P90
42 EXMOD1/P91
41 VDD
40 P92/RE
39 P93/WE0
38 P94/WE1
37 P95/DK
36 P96/BR
35 VSS
34 SYSCLK/P97
33 VDD
32 OSCI
31 OSCO
30 RST
29 MMOD0
28 MMOD1
27 PVDD
26 PVSS

Bottom (pins 1–25):
1 PC3/A19
2 PC2/A18
3 VDD
4 PC1/A17
5 PC0/A16
6 PB7/ADM15/A15
7 PB6/ADM14/A14
8 PB5/ADM13/A13
9 VSS
10 PB4/ADM12/A12
11 PB3/ADM11/A11
12 PB2/ADM10/A10
13 PB1/ADM9/A9
14 PB0/ADM8/A8
15 VDD
16 PA7/ADM7/A7
17 PA6/ADM6/A6
18 PA5/ADM5/A5
19 PA4/ADM4/A4
20 PA3/ADM3/A3
21 VSS
22 PA2/ADM2/A2
23 PA1/ADM1/A1
24 PA0/ADM0/A0
25 CKSEL

LQFP100-P-1414 *Lead-free

* VDD2 for MN103001G and VPP for MN1030F01K

Support Tool

In-circuit Emulator	PX-ICE103001-LQFP100-P-1414	
On-board Development Tools	PX-ODB103S-O CSIDE-MN10300 (Computex Co., Ltd, product)	
Flash Memory Built-in Type	Type	MN1030F01K
	Command ROM (× 64-bit)	256 K-byte
	Data RAM (× 32-bit)	8 K-byte
	Minimum instruction execution time	25 ns (at 3.0 V to 3.6 V, 40 MHz)
	Package	LQFP100-P-1414 *Lead-free

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