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Digital UpConverter

The HSP50215 Digital UpConverter (DUC) is a QASK/FM modulator/FDM upconverter designed for high dynamic range applications such as cellular basestations. The DUC combines shaping and interpolation filters, a complex modulator, and Timing and Carrier NCO's into a single package. Each DUC can create a single FDM channel. Multiple DUC's can be cascaded digitally for multi-channel applications.

The HSP50215 supports both vector and FM modulation. In vector modulation mode, the DUC accepts 16-bit I and Q samples to generate virtually any quadrature AM or PM modulation format. The DUC also has two FM modulation modes. In the FM with pulse shaping mode, the 16-bit frequency samples are pulse shaped/bandlimited prior to FM modulation. No bandlimiting filter follows the FM modulator. This FM mode is useful for GMSK type modulation formats. In the FM with bandlimiting filter mode, the 16-bit frequency samples directly drive the FM modulator. The FM modulator output is filtered to limit the spectral occupancy. This FM mode is useful for analog FM or FSK modulation formats.

The DUC includes an NCO driven interpolation filter, which allows the input and output sample rate to have a non-integer or variable relationship. This re-sampling feature simplifies cascading modulators with sample rates that do not have harmonic or integer frequency relationships.

The DUC offers digital output spectral purity that exceeds 85dB at the maximum output sample rate of 52 MSPS, for input sample rates as high as 300 KSPS.

A 16-bit microprocessor compatible interface is used to load configuration and baseband data. A programmable FIFO depth interrupt simplifies the interface to the I and Q input FIFOs.

Features

- Output Sample Rates Up to 52 MSPS (48 MSPS Industrial); Input Data Rates Up to 3.25 MSPS
- I/Q Vector, FM, and Shaped FM Modulation Formats
- 32-Bit Programmable Carrier NCO; 30-Bit Programmable Symbol Timing NCO
- Programmable I and Q, 256 Tap, Shaping FIR Filters with Interpolation by 4, 8 or 16
- Interpolation Filter Up Samples Shaping Filter Output to Output Sample Rate Under NCO Control
- Processing Capable of >90dB SFDR
- Cascade Input for Multiple Channel Transmissions
- 16-Bit µProcessor Interface for Configuration and User Data Input

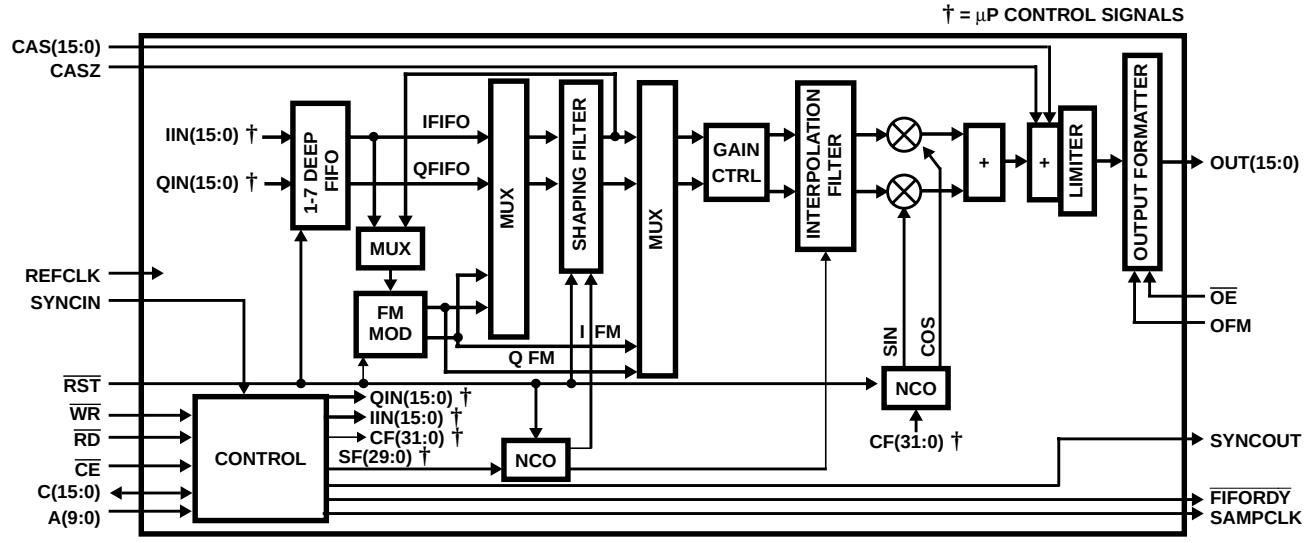
Applications

- Single or Multiple Channel Digital Software Radio Transmitters (Wide-Band or Narrow-Band)
- Base Station Transceivers
- Operates with HSP50214 in Software Radio Solutions
- Compatible with the HI5741 D/A Converter
- HSP50215EVAL Evaluation Board Available

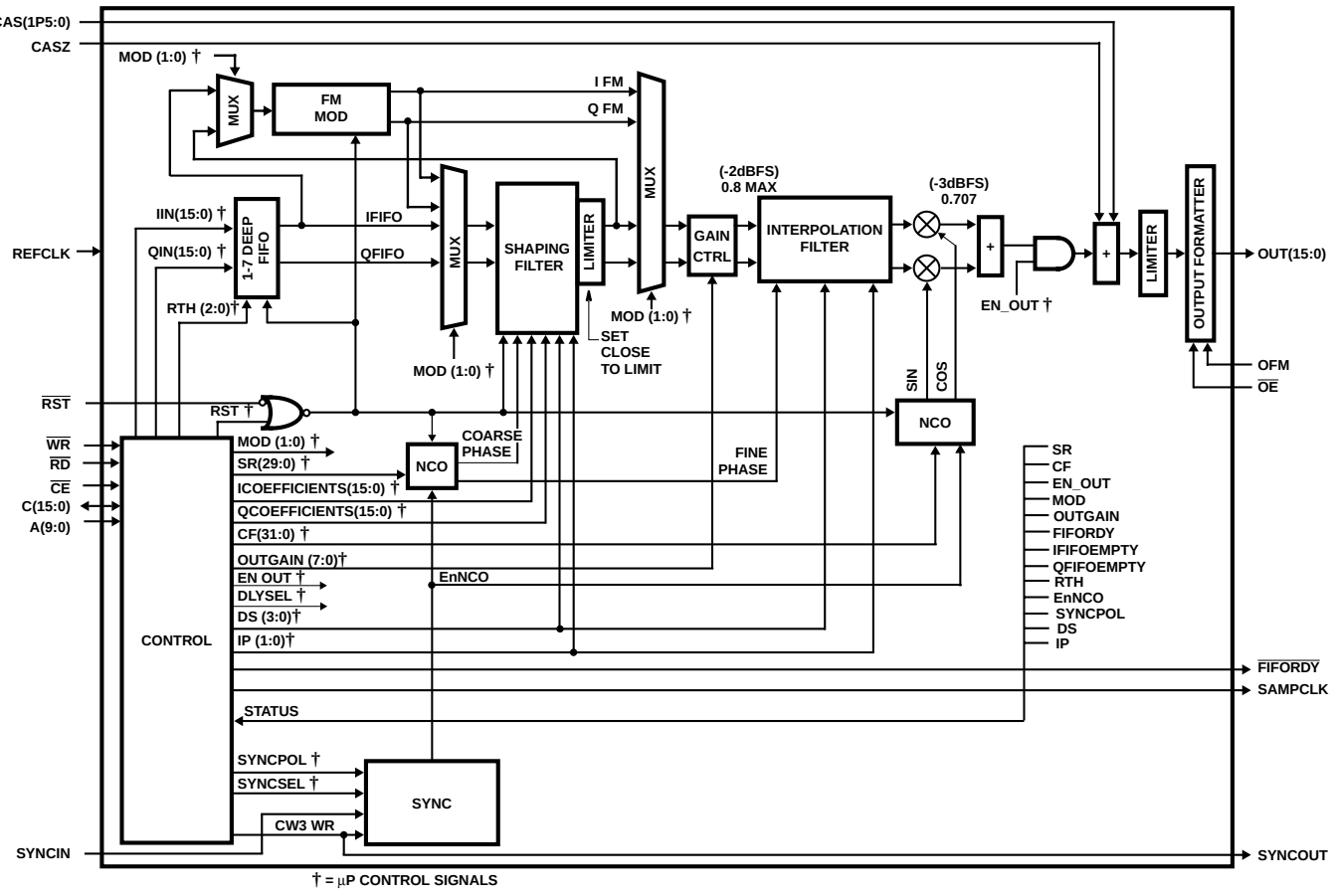
Ordering Information

PART NUMBER	TEMP RANGE (^{o}C)	PACKAGE	PKG. NO
HSP50215VC	0 to 70	100 Ld MQFP	Q100 .14x20
HSP50215VI	-40 to 85	s100 Ld MQFP	Q100 .14x20

Block Diagram

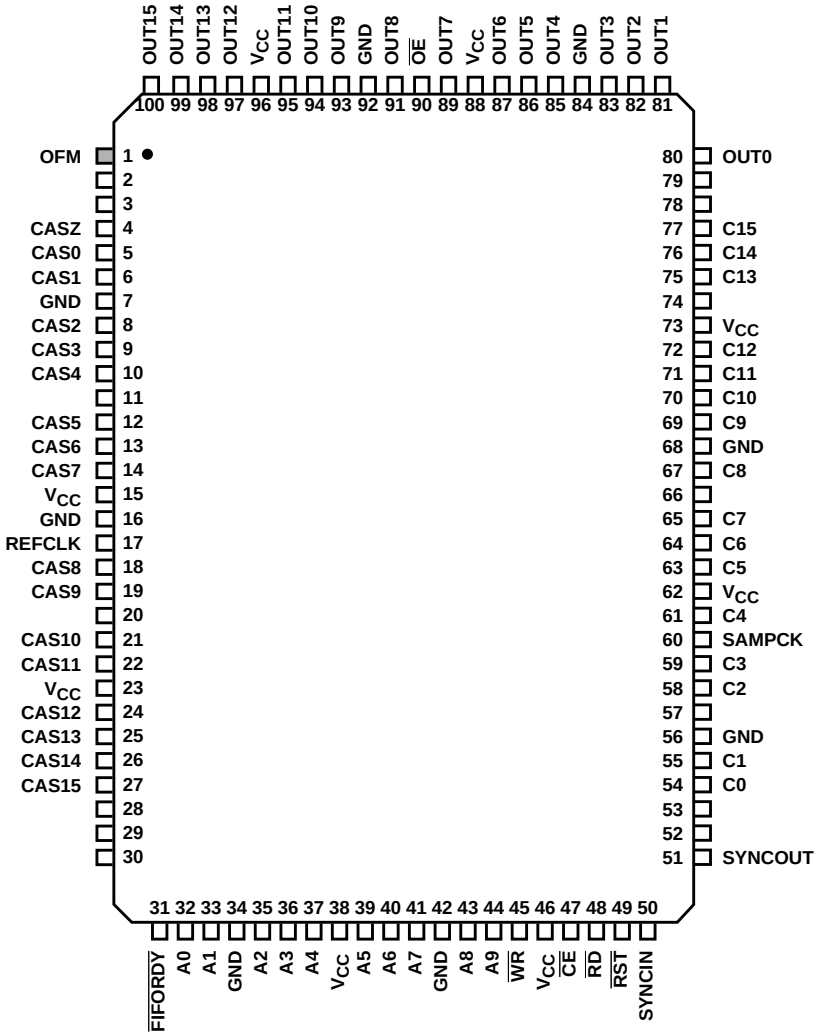


Functional Block Diagram



Pinout

100 LEAD MQFP
TOP VIEW



Pin Descriptions

NAME	TYPE	DESCRIPTION
V_{CC}	-	+5V Power supply input.
GND	-	Power supply ground input.
C(15:0)	I/O	µP Bidirectional Data bus. The C(15:0) bus is used for loading the configuration data and sample vectors for modulation. C15 is the MSB.
A(9:0)	I	µP Address Bus. The A(9:0) bus is used for addressing the proper registers for loading the configuration data and sample vectors for modulation. A9 is the MSB.
$\overline{WR}$	I	µP Write Strobe. When $\overline{CE}$ is asserted, data on the C(15:0) data bus is loaded into the address location found on the A(9:0) bus on the rising edge of the $\overline{WR}$ signal. In some cases, there is an internal synchronization to the master clock that must be completed before the next data is written. See the µP interface section for more information.
$\overline{RD}$	I	µP Read Control. When $\overline{RD}$ and $\overline{CE}$ are low, the data found in the address location defined by A(9:0) is routed to the C(15:0) µP data bus on the next rising edge of REFCLK.
$\overline{CE}$	I	µP Chip Enable. Used to gate the $\overline{WR}$ and $\overline{RD}$ µP interface control signals.
$\overline{FIFORDY}$	O	FIFO Ready. A $\overline{FIFORDY}$ assertion indicates that the I and Q FIFOs have reached the programmed FIFO depth and more samples are required to maintain that FIFO depth.
REFCLK	I	Reference Clock. REFCLK is the master clock for the DUC. All timing is relative to the REFCLK rising edge. The frequency of the reference clock is denoted f_{CLK}, and is the rate at which data is output from the part.
CAS(15:0)	I	Cascade Input Bus. This input bus is used to cascade multiple parts by routing the digital modulated signal from one DUC into the output summer of a second DUC. CAS(15:0) is 2's complement format and is sampled on the rising edge of REFCLK. CAS15 is the MSB.
CASZ	I	Cascade Input Bus Zero. When CASZ is asserted (pulled high), the part places zeroes on the CAS(15:0) data path. CASZ is asynchronous (not registered) to REFCLK and should not be changed on the fly. When unused, pull high with a pull up resistor (~22kΩ).
OUT(15:0)	O	Output Data Bus. OUT(15:0) contains the digital modulated DUC output samples and is updated on the rising edge of the REFCLK. OUT15 is the MSB.
OFM	I	Output Data Bus Format. When OFM is asserted (pulled high), the output bus format is 2's complement. When not asserted, the output format is offset binary. The OFM input is asynchronous (not registered) to REFCLK and should not be changed on the fly.
$\overline{OE}$	I	Output Data Bus Enable. When $\overline{OE}$ is asserted (dropped low), the output data bus OUT(15:0) is enabled. When $\overline{OE}$ is not asserted (pulled high), the output data bus OUT(15:0) is placed in the high impedance state.
SYNCIN	I	Sync Input. The SYNCIN input is used to synchronize the processing of multiple parts. The SYNCOUT of one part acts as a master and is connected to the SYNCIN of all of the DUC's that are to by synchronized. The DUC can be programmed so that either rising or falling edge of this signal initiates the processing.
SYNCOUT	O	Sync Output. The SYNCOUT output is used to synchronize the processing of multiple parts. The SYNCOUT of one part acts as a master, and is connected to the SYNCIN of all of the DUC's that are to be synchronized.
SAMPCLK	O	Sample Clock. This clock is provided to the data source to indicate when data is being transferred from the FIFO to the shaping filter. The SAMPCLK output is generated by the sample rate NCO when the digital filter takes a new sample. It has approximately 50% duty cycle. The sample is taken on the high-to-low transition. SAMPCLK may be used instead of $\overline{FIFORDY}$.
$\overline{RST}$	I	Reset. When the $\overline{RST}$ input is asserted (dropped low), the DUC is reset and all processing halts. The DUC may also be reset on µP command. Processing remains halted until a sync is generated either by µP command or assertion of SYNCIN. See the Reset section details of the specific functions halted by this control signal.

Functional Description

The HSP50215 Digital UpConverter (DUC) converts digital baseband data into modulated or frequency translated digital samples. The DUC can be configured to create any quadrature amplitude shift-keyed (QASK) data modulated signal, including QPSK, BPSK, and m-ary QAM. The DUC can also be configured to create both shaped and unfiltered FM signals. A minimum of 16 bits of resolution is maintained throughout the internal processing.

The DUC is configured via the 16-bit microprocessor data bus, using the address bus and $\overline{RD}$, $\overline{WR}$ and $\overline{CE}$ control signals. Configuration data that is loaded via this bus includes the 30-bit Sample Rate NCO center frequency, the 32-bit Carrier NCO center frequency, the modulation format, gain control, FIFO control, reset control and sync control. The I and Q baseband channels each have a 256 tap FIR filter whose coefficients and configuration are also programmed via the µP interface. Similarly, the control signals for the I and Q channel interpolation filters are programmed via the µP interface. Once the operational configuration for the device has been set, the 16-bit µP interface is used to input the I and Q data into the associated FIFOs.

The FIFOs provide the data interface between the µP and either the FM modulator or the shaping filters. Multiplexers route the I data to the FM modulator in the FM with bandlimiting filter mode. Both I and Q are routed to the 256 tap FIR shaping filters in the QASK mode. The shaping filter serves to both shape and interpolate the sample rate to 4, 8, or 16 times the input sample rate. The I shaping filter output can also be routed to the FM modulator for the FM with pulse shaping mode. Multiplexers select either the FM modulator output or the shaping filter output to be scaled and routed to the interpolation filters.

The I and Q interpolation filters allow a non-integer increase in sample rate, up to the reference clock rate. The interpolation filter output data is upconverted or modulated by the Carrier NCO and multipliers. The modulated signal is added to modulated inputs from other cascaded DUC's. The output formatter sets the output buffer state and the output data format.

Programmable FIFO

The Programmable FIFOs provide a data storage and interface between the microprocessor data write holding register and the shaping filter or the FM modulator. Signal routing out of the FIFO is set by the modulation format. Each FIFO has seven 16-bit registers. Figure 1 shows the conceptual details of the I and Q FIFOs.

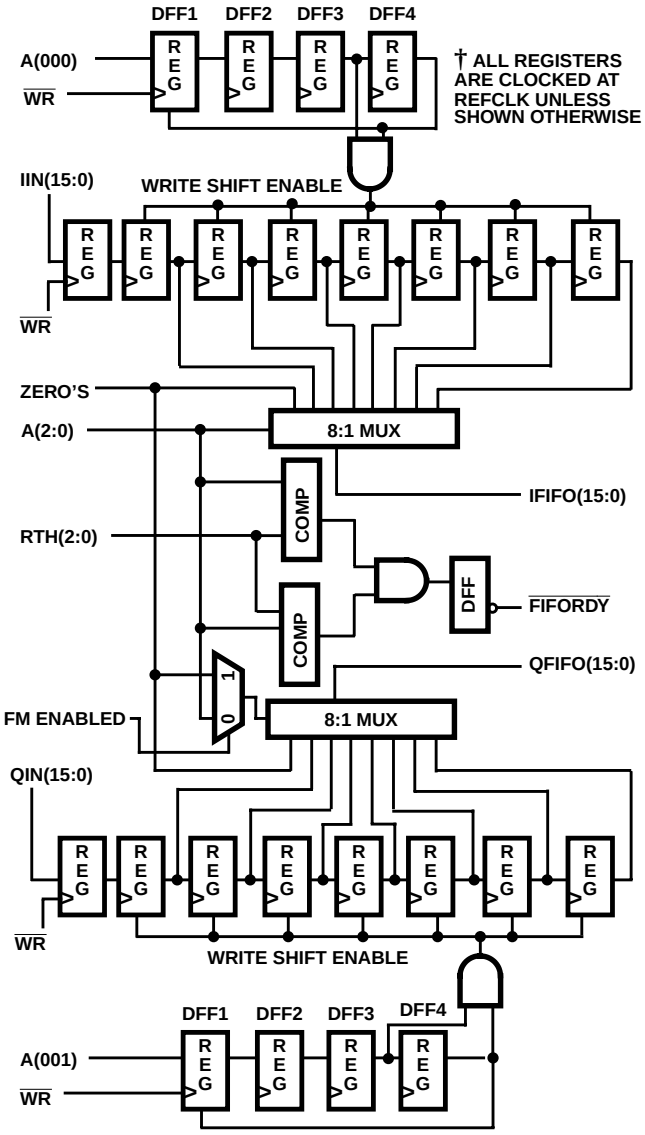


FIGURE 1. I AND Q FIFO BLOCK DIAGRAM

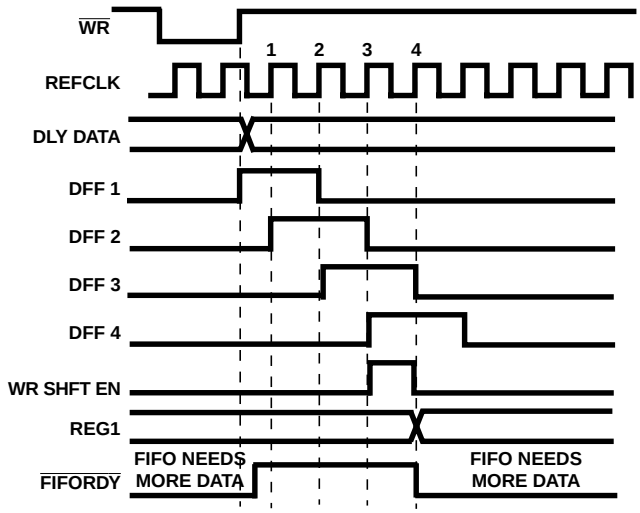


FIGURE 2. $\overline{FIFORDY}$ AND DATA DELAY TIMING

Data enters the FIFO with a write command to either Control Word 0 (for I data), or Control Word 1 (for Q data). This transfers data from the microprocessor holding register into the first 16-bit register of the FIFO. The FIFO counter is incremented every time data is written into the FIFO. Four REFCLK periods are required from the rising edge of a WR signal before another WR rising edge can occur, (i.e., before data can once again be written into either the I or Q FIFO). This limits the maximum data input (write) rate to 52MHz/4 = 13MHz.

NOTE: The Write rate is not the parameter that determines the maximum input rate, the shaping filter is. The maximum input for the shaping filter is 52MHz/(IP)(DS), which is 52MHz/16 = 3.25 MHz for a minimal shaping filter (DS = IP = 4). See the Shaping Filter Section for more details.

The timing details of these FIFO registers are shown in Figure 2. While the data for the I and Q inputs are independent, the Write cycle limitations of the FIFO constrains the maximum input symbol rate of quadrature symbols (both I and Q data) as noted.

When the Shaping Filter requires another sample of data, a request is made to the FIFO for data and the FIFO counter is decremented. Figure 3 indicates the timing of a request for data from the Shaping filter to the actual appearance of data at the FIFO output. The FIFO has circuitry for detecting an empty FIFO as well as a full FIFO. An “empty” FIFO detection causes “zero” data to be entered into the shaping filter. A “full” FIFO detection prevents data from being pushed out of the FIFO before the filter requests it.

NOTE: Do not write to a full FIFO. Writing to a full FIFO is an error condition and the part will be reset to prevent transmission of erroneous data over the air.

A programmable FIFO depth threshold sets when the $\overline{\text{FIFORDY}}$ signal is asserted, alerting the data source that more data is required. The $\overline{\text{FIFORDY}}$ signal assists a data source in maintaining the desired FIFO data depth. Control Word 18, bits 0-2 are used to set the data FIFO depth threshold for both I and Q inputs.

NOTE: SAMPCLK may be used instead of $\overline{\text{FIFORDY}}$ to indicate that data is transferred from the FIFO to the shaping filter. See the Pin Description Table.

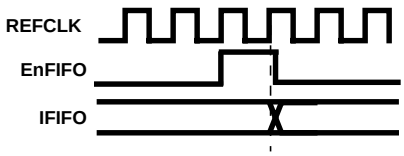


FIGURE 3. FIFO DATA AND ENABLE TIMING

Data Modulation Path

Three data path options are provided, one for each modulation format. The modulation format is selected using Control Word 16 (See the Microprocessor Write section). Control Word 16 bits (1:0) are defined as: 00:QASK, 01:FM with post-modulation filtering, and 10:FM with pre-modulation pulse shaping. These modulation paths are defined in the following subsections.

Modulation Mode 00 - QASK

This modulation mode configures the PUC as a BPSK, QPSK, OQPSK, MSK or m-QAM modulator. The filter configuration is shown in Figure 4. The data FIFO outputs are routed to the shaping filters. Here the samples are interpolated by 4, 8, or 16 and shaped using a FIR filter with up to a 256 taps. The filter impulse response can span 4-16 input samples. A half (input) sample delay can be set in the I channel for implementing OQPSK modulation. The output of the shaping filter is routed through a gain adjust multiplier and into the interpolation filter. The interpolation filter interpolates by a factor set in the resampling NCO. The output of the interpolation filter is at the master clock frequency, REFCLK. The samples are then mixed with the carrier L.O. for quadrature upconversion. The output is then summed with the cascade input signal, saturated (in the case of overflow), and formatted for output.

FIGURE 4. QASK

Modulation Mode 01 - FM with BANDLIMITING Filter

This mode configures the PUC as an FM modulator with post-modulation filtering. This mode provides for FSK and FM modulation schemes. In this mode, the I input samples drive the frequency control section of a quadrature NCO to produce a zero IF FM signal. The FM quadrature signals are then routed to the shaping FIR filter and into the interpolation filter for bandlimiting and interpolation up to the master clock rate as shown in Figure 5. The quadrature filtered FM signals are then upconverted to the carrier frequency by the carrier NCO and mixers. The output is then summed with the cascade input signal, saturated (in the case of overflow), and formatted for output. Note that pulse shaping in this mode must be provided prior to the PUC.

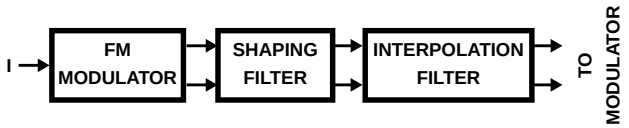


FIGURE 5. FM WITH BANDLIMITING

Modulation Mode 10 - FM with Pulse Shaping

This mode configures the PUC as an FM modulator with pre-modulation baseband pulse shaping. The data from the FIFO (I channel only) is routed to the FIR shaping filter. The FIR shaping filter output drives the frequency control section

of a quadrature NCO to produce a zero I.F. FM signal. These FM modulated quadrature samples are then up sampled in the interpolation filter to the output sample rate. The baseband modulated signal is then upconverted to the carrier frequency by the carrier NCO and mixers. The output is then summed with the cascade input signal, saturated, and formatted for output.

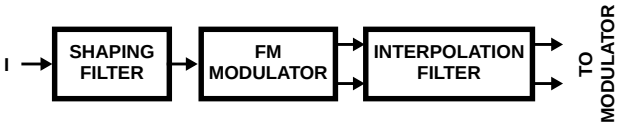


FIGURE 6. FM WITH PULSE SHAPING

In Mode 10, the amplitude out of the shaping filter needs to be limited in order to prevent frequency excursions that cannot be filtered out in the interpolation filter. The quality of the FM signal is affected by the amplitude slew rate out of the shaping filter. As a rule of thumb, limiting this slew rate to less than 1/8 the sample rate will minimize this distortion.

FM Modulator

The FM modulator provides for frequency modulation of the carrier center frequency by the PUC input data. The FM modulator is driven either directly by the PUC I input (Mode 1) or by the output of the FIR shaping filter (Mode 2). The input data to the FM Modulator, is defined as $d\phi(n)/dt$, where $\phi(nT)$ is the phase of a theoretical sinusoid described by:

$$s(n) = A(\cos[\phi(nT)] + j\sin[\phi(nT)]);\ A \approx 1 \text{ in Modulator} \quad \text{(EQ. 1)}$$

Figure 7 illustrates the conceptual design of the FM modulator. The input to the FM modulator, $d\phi(n)/dt$, is integrated via the carrier NCO accumulator. The NCO accumulator output represents phase and is used to address a SIN/COS generator, synthesizing a sinusoid of the form described in Equation 1. The phase accumulator feedback of the NCO is 16 bits and sixteen bits of the phase word are routed to the SIN/COS generator. Sixteen bits of resolution are provided on the Sine and Cosine outputs.

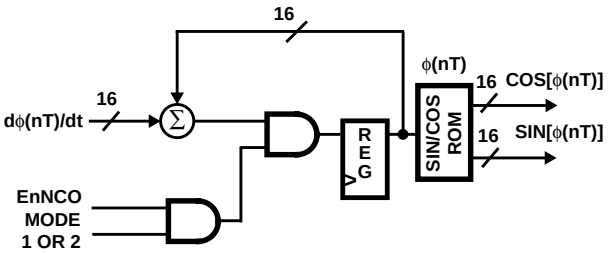


FIGURE 7. FM MODULATOR BLOCK DIAGRAM

The transfer function of the FM modulator is defined by the change in degrees per sample value, $d\phi(nT)/dt$, where $d\phi(nT)/dt$ is a 16-bit, twos complement, fractionally notated frequency control word with a range from $-F_{SAMP}/2$ to $+F_{SAMP}/2$. F_{SAMP} is defined as the sample rate into FM modulator. The maximum phase step that can occur in one clock is ±180 degrees. Table 1 provides the change in phase weighting of the input bits.

TABLE 1. FM MODULATOR TRANSFER FUNCTION

dφ(nT)/dt	DEGREES/SAMPLE
1000 0000 0000 0000	-180
0000 0000 0000 0000	0
0111 1111 1111 1111	~+180

Shaping Filter

The shaping filter provides the necessary pulse shaping required on the input data to implement various quadrature ASK and shaped FM modulation formats. Two identical shaping filters (one each for the I and Q channels) are provided. The filters can implement a 4-16 input sample span impulse response using up to 256 taps with 16 bits of resolution in the coefficients.

The range of valid digital values for the coefficients is from 8001 to 7FFF. The value 8000 is not allowed. The coefficient format is 2's complement. The span of the Impulse response of the polyphase filter can be from 4-16 samples. The desired sample span value minus one is programmed into the Data Samples (DS) field in Control Word 19, bits 2-5. The filter has a programmable interpolation rate (IP) of 4, 8, or 16. This interpolation rate is programmed by Control Address 19, bits 0 and 1. Thus, the required number of coefficients (or filter span) becomes

$$\#\ \text{Coefficients} = (DS)(IP) \quad \text{(EQ. 2)}$$

with 256 being the maximum number of coefficients.

Note that

$$REFCLK > (DS)(IP)(f_S) \quad \text{(EQ. 3)}$$

where f_S is the input sample rate of the shaping filter. For a 16 input sample impulse response span, the total impulse response is 64, 128 or 256 filter taps for interpolation rates of 4, 8 or 16, respectively. The filter structure precludes coefficient re-use for symmetric filters, so both asymmetric and symmetric filters have up to 256 taps available and are loaded in identical manner.

The maximum input sample rate is:

$$f_S = f_{CLK}/[(IP)(DS)] \quad \text{(EQ. 4)}$$

where f_{CLK} is the frequency of the reference clock, IP is the shaping filter interpolate rate; and DS is the number of data samples in the filter span. For example, if f_{CLK} = 52MHz, the filter span is 16 samples, and the interpolation rate is 16, then the maximum input sample rate, f_S is 52/256 = 203kHz. Table 2 shows several examples of calculations for FIR input sample rates based on master reference clock rate, number of data samples, and interpolation rate.

TABLE 2. EXAMPLES OF THE DIFFERENT CASES AND DIFFERENT FIR INPUT SAMPLING FREQUENCIES

EXAMPLE	f_{CLK}	DS	IP	MAX f_S
1	52MHz	16	16	52/256 = 203kHz
2	52MHz	16	8	52/128 = 406kHz
3	52MHz	16	4	52/64 = 813kHz
4	52MHz	10	4	52/40 = 1300kHz
5	52MHz	8	4	52/32 = 1625kHz
6	52MHz	4	4	52/16 = 3,250kHz

(f_{CLK} = 48MHz for industrial temperature range).

Shaping Filter Application Issues

Note that when using quadrature modulation, saturation/overflow can occur when the input values for I and Q exceed 0.707 peak. Also note that there is gain in Interpolation filter. Because of these two implementation constraints, the Shaping filter coefficients may need to be reduced from full scale to provide unity gain in the PUC and to prevent saturation in the shaping filter. After the shaping filter computation, a gain scaling control is provided. It is possible to allow the shaping filter computation to approach unity on each channel and then scale the I/Q magnitudes in the Gain Control.

The delay through the shaping and interpolation filters is 20 CLKs and the shaping filter delay.

Gain Control

Between the Shaping filter and the Interpolation filter is a gain adjustment stage that provides for identical scaling of the I and Q shaped signals. Gain adjustment is from 0 to slightly less than unity. This gain control can be used to prevent signal overflow in the Interpolation filter or saturation in the quadrature mixer.

The interpolation filter can have a gain of 2dB. If a full scale signal is required at the output of the shaping filter, apply 2dB back off in the Gain Adjust Circuit. For worst case conditions, the interpolation filter can have 25% overshoot. (See the annotations on the Functional Block Diagram). Gain control can also be used to set the level of a signal prior to summing multiple signals in the Modulated Output Section.

The scaling multiplier value is programmed using an bits 0-7 in Control Word 17. The attenuation is set by:

$$Gain = OutGain/2^8 \quad \text{(EQ. 5)}$$

$$Gain_{dB} = 20\log[OutGain/2^8] \quad \text{(EQ. 5A)}$$

$$OutGain = [(Gain)2^8]Hex \quad \text{(EQ. 5B)}$$

$$OutGain = \left[10^{(Gain_{dB}/20)}2^8\right]Hex \quad \text{(EQ. 5C)}$$

where Gain is the desired signal level relative to fullscale, $Gain_{dB}$ is the desired signal level in dB relative to fullscale, and OutGain is the control word value.

Table 3 details a few key control words and the associated attenuations for the I and Q signals.

TABLE 3. SCALING GAIN ATTENUATION

CONTROL WORD	GAIN (dBFS)	SCALING GAIN (V_{OUT}/V_{IN})%
1111 1111yt	-0.033996	99.6
1000 0000	-6.021	50.0
0100 0000	-12.041	25.0
0010 0000	-18.062	12.5
0001 0000	-24.082	6.25
0000 1000	-30.103	3.125
0000 0100	-36.124	1.5625
0000 0010	-42.144	0.78125
0000 0001	-48.165	0.390625

Re-Sampling NCO

The Sample Rate NCO provides the sample clock and sample clock phase information to both the shaping and Interpolation filters. Figure 8 details the conceptual design. The sample frequency is set with 30-bit resolution. The LSB is REFCLK/2^{32}. The internal accumulator resolution in 32 bits. The MSB of the accumulator is the sample clock for the filters. Four bits of coarse timing phase resolution control the Shaping filter, while twelve bits of fine timing phase resolution control the Interpolation filter.

The Resampling NCO frequency control word is double buffered. The 30-bit timing NCO frequency is written to Control Addresses 2 and 3. The frequency control word is transferred from the buffer into the Re-Sampling NCO on a pulse from SYNCIN or on a write to Control Word 2. Control Word 22, bit 0, sets which action, (the SYNCIN or write to CW2), causes a frequency control word transfer in the NCO. Assertion of $\overline{RST}$ stops the Re-Sampling NCO and clears the accumulator contents. It is held disabled until a SYNCIN or write to Control Word 3 generates an EnNCO signal to restart the NCO.

The PUC input sample rate is set by the Re-Sampling NCO. The maximum error is 52MHz/(2^{32}) = 0.012Hz for the commercial part and 48MHz/(2^{32}) = 0.011Hz for the industrial part. The frequency control word is computed by:

$$F_{RESAMP} = SR(29:0) \times f_{CLK} \times 2^{-32} \quad \text{(EQ. 6)}$$

where SR(29:0) is the 30-bit frequency control word and f_{CLK} is REFCLK.

Equation 6 can be rearranged to solve for SR(29:0).

$$SR(29:0) = RND\left[\frac{f_{RESAMP}}{f_{CLK}} \times 2^{32}\right]$$

The range of SR(29:0) is: [0 to $2^{30} - 1$]

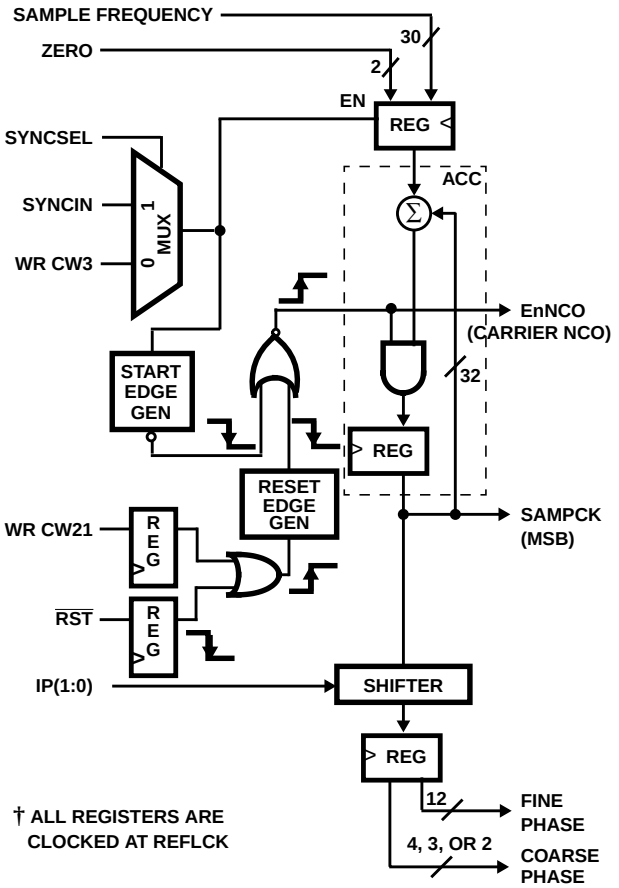


FIGURE 8. RE-SAMPLING NCO BLOCK DIAGRAM

Re-Sampling NCO Application Issues

1. Common clocking of the PUC and PDC:

Note that at a board level, the HSP50214 (PDC) and HSP50215 (DUC) sample rate NCO's typically utilize different clocks. The DUC circuitry is clocked at the master clock, REFCLK, rate. The PDC output circuitry runs off the decimated sample rate. If a common sample clock is used for both parts, then synchronization can be achieved by scaling and/or truncating the PDC frequency control word to match the PUC frequency control word. Powers of 2 are handled by simply truncating the PDC frequency control word to match the bit width of the DUC frequency control word. If the PDC decimation factor is not power of 2, then errors will accumulate.

2. Improving the NCO Accuracy

The Re-Sampler NCO frequency can be adjusted to maintain phase and frequency lock to a reference clock, if more accuracy is required.

Interpolation Filter

The Interpolation filter provides sampling rate conversion from the shaping filter output rate to the final output sample rate. The nulls in the interpolation filter frequency response align with the interpolation images of the shaping filter. The impulse response of the Interpolation filter is shown in Figures 9A through 9C for an interpolate by 16 filter (the interpolation ratio, L, is equal to 16). The Interpolation filter has a pipeline delay of 3 coarse input samples plus 3 REFCLK cycles.

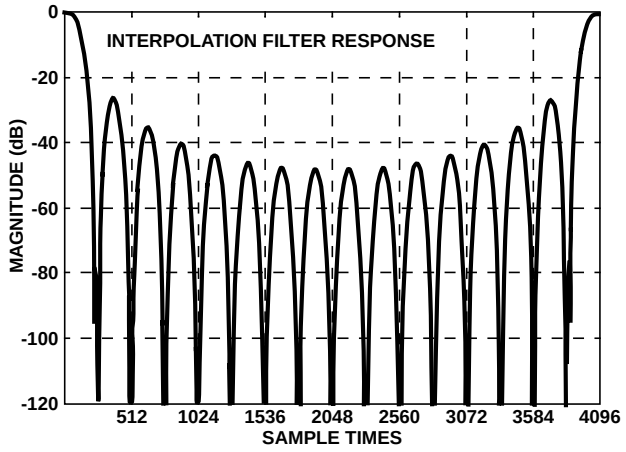


FIGURE 9A. INTERPOLATION FILTER IMPULSE RESPONSE L = 16; FOUT = 4096

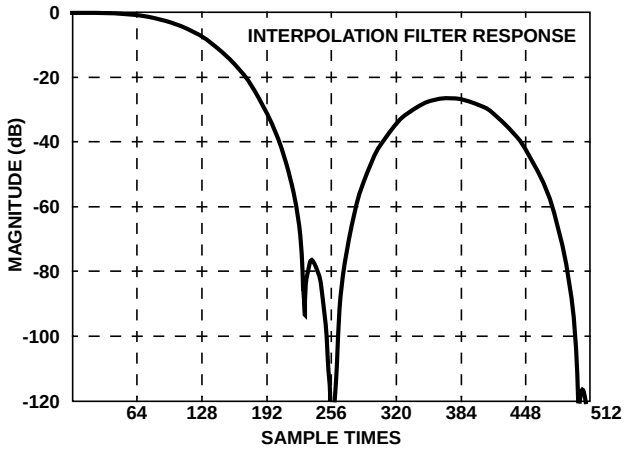


FIGURE 9B. INTERPOLATION FILTER IMPULSE RESPONSE L = 16; FOUT = 4096

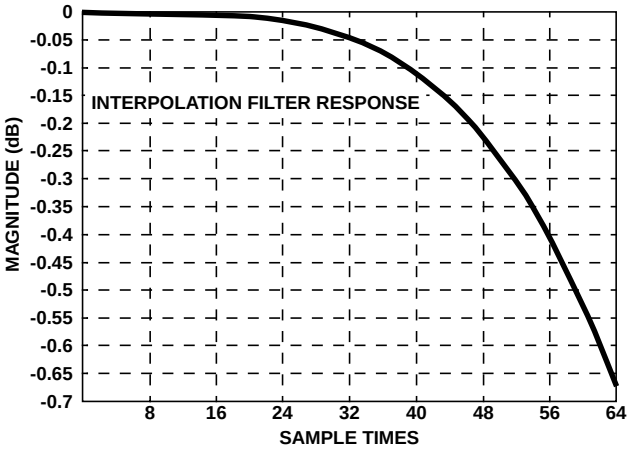


FIGURE 9C. INTERPOLATION FILTER IMPULSE RESPONSE L = 16; FOUT = 4096

Carrier NCO

The Carrier NCO provides the quadrature local oscillator references for the Vector Modulator/Mixer. The Carrier NCO input carrier frequency control word has 32 bits of resolution. The block diagram is shown in Figure 10.

The carrier frequency is a single buffered 32-bit frequency control, loaded 16 bits at a time into Control Words 4 and 5. Since the DUC requires two loads, there is a possibility of a phase glitch.

The Carrier NCO is disabled during a $\overline{RST}$ assertion or a reset caused by writing to CW21. The Carrier NCO stays disabled until a sync assertion is detected independent of the initiating sync source (SYNCIN or WR CW3). The Carrier NCO is also disabled by programming a zero in Control Word 16 bit 3. This bit freezes the NCO and also disables the output of the modulator.

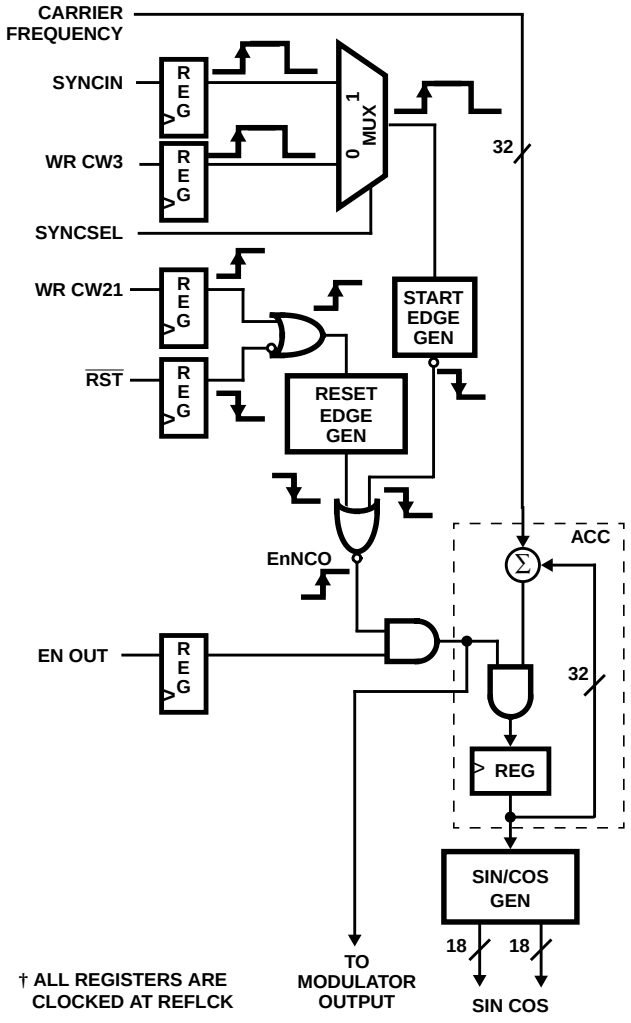


FIGURE 10. CARRIER NCO BLOCK DIAGRAM

To avoid the phase glitch, noted above, the phase accumulator can be disabled at reset, and the frequency can be pre-loaded prior to asserting sync.

The maximum error is 52MHz/(2^{32}) = 0.012Hz for the commercial part and 0.011Hz for the industrial part. The carrier frequency can be calculated from the value loaded into Control Address 4 and 5 by:

$$F_{CARRIER} = CR(31:0) \times f_{CLK} \times 2^{-32} \quad \text{(EQ. 7)}$$

where CR(31:0) is the 32-bit frequency control word which can range from -2^{31} to $\sim 2^{31}$ for a NCO output range of $-f_{CLK}/2$ to $\sim f_{CLK}/2$. f_{CLK} is the REFCLK frequency.

This NCO frequency range allows for spectral inversion. Given a desired carrier frequency, the value for CR(31:0) loaded into the part can be calculated by:

$$CR(31:0) = INT[F_C / f_{CLK} * 2^{32}] \quad \text{(EQ. 8)}$$

where INT[X] is the integer part of the real number X.

The most significant 18 bits of the 32-bit phase word from the Carrier NCO drives a Sin/Cos generator. Eighteen bit resolution is supplied on the sinusoid outputs.

Assertion of $\overline{RST}$ stops the Carrier NCO and clears the accumulator contents. It is held disabled until a SYNCIN or write to Control Word 3 generates an EnNCO signal to restart the NCO.

Vector Modulator/Mixer

The frequency resolution of the vector modulator is 32 bits. The conceptual block diagram of the Vector Modulator/Mixer is shown in Figure 11. The modulator operates at maximum frequency of 52MHz (commercial). The mixer takes the sin/cos terms generated by the carrier NCO sin/cos generator and mixes it with the input data lines I and Q. The resulting output is given by

$$Output = I * \cos - Q * \sin \quad \text{(EQ. 9)}$$

NOTE: ***There is no overflow protection provided at the output of the modulator summer, so care must be taken to ensure that the input signals are scaled prior to input to prevent overflow.***

The mixers can be bypassed by programming Control Words 4 and 5 to zero, which sets COS = 1 and SIN = 0.

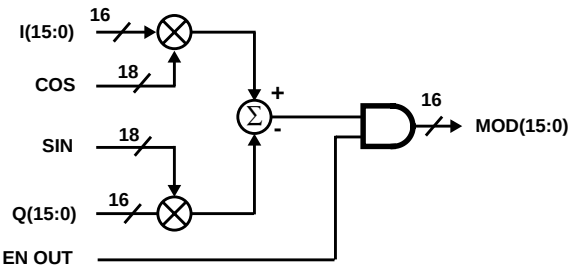


FIGURE 11. VECTOR MODULATOR/MIXER BLOCK DIAGRAM

Cascade Input

The cascade input allows multiple modulated signals to be summed together prior to routing to a DAC. Figure 12 is a block diagram of the cascade circuitry. CAS(15:0) is the input when cascading with other DUC's. The CASZ is used to zero the CAS(15:0) input when it is not used. Both the CAS(15:0) and the modulator data path are registered, prior to summation. The output of the summation is saturated to prevent roll-over.

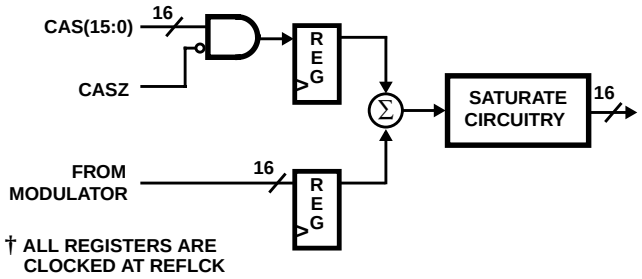


FIGURE 12. CASCADE INPUT BLOCK DIAGRAM

Output Formatter

The output can be either twos complement or offset binary format. The OFM signal is used to select the output format. OFM = 1 is twos complement. OFM = 0 is Offset Binary format. The $\overline{OE}$ signal is used to enable the data bus output. $\overline{OE}$ = 0 enables the output.

NOTE: The HSP43216 can be used to double the output sample rate of the DUC, in applications where a higher sample rate into the DAC is required.

Microprocessor Interface

The microprocessor interface is a memory mapped direct access interface. The control pins are $\overline{RD}$, $\overline{WR}$ and $\overline{CE}$. The 10-bit address bus is A(9:0) [address space is 1024 words] and the 16-bit data bus is C(15:0). The $\overline{CE}$ signal gates the $\overline{RD}$ and $\overline{WR}$. Care must be taken in changing the address and data lines, as the addresses are updated asynchronous to REFCLK except in the cases noted in the Microprocessor Write Section. Most addresses are intended to be programmed after RESET and before the Start Sequence, and left alone after that. See the RESET and Start Sequence sections from more details on initiating operation of the part.

Reads are asynchronous to clock. The shaping filter coefficients cannot be read. See the Configuration Control Register Bit Definitions section for programming details of the 14 Control Words and the 512 Coefficient Registers.

Microprocessor Write

The Microprocessor Write Interface is used for loading data into the DUC control registers. Write registers are accessed via the 10-bit address bus (A9:0) and the 16-bit data bus (C15:0). The address map for these registers is given in the Configuration Control Register Bit Definition section.

Configuration data is written into the HSP50215 by setting up the address (A9:0) and data (C15:0) and generating a rising edge on $\overline{WR}$. A DUC configuration sequence is shown in Figure 13. Figure 13 assumes that $\overline{CE}$ is asserted. The filter coefficients for the shaping filter are loaded in a similar manner into Control Word addresses 512 - 1023.

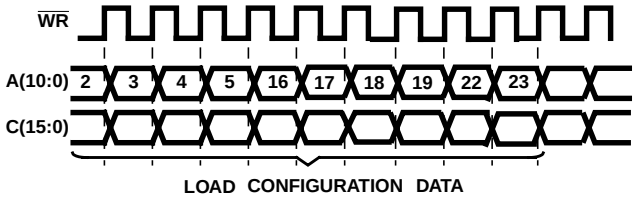


FIGURE 13. CONTROL REGISTER LOADING SEQUENCE

The Re-Sampler NCO Center Frequency data is double buffered and transfers from the Microprocessor Interface holding registers to the Center Frequency Register on the assertion of SYNCIN or a Write to Configuration Control Word 3. The timing waveforms for this process are shown in Figure 14.

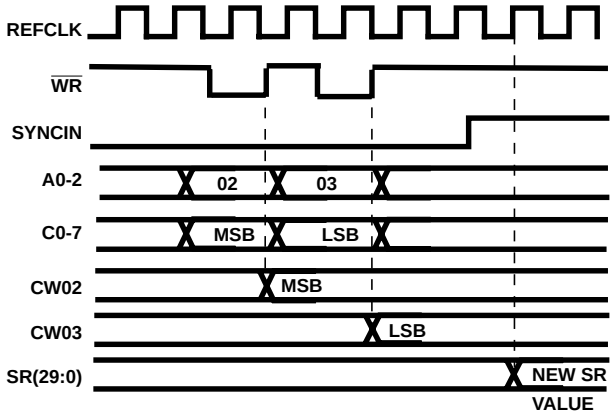


FIGURE 14. RESAMPLER CENTER FREQUENCY CONTROL REGISTER LOADING SEQUENCE

When SYNCIN is sampled "high" by the rising edge of clock, the contents of the holding registers are transferred to the Sample Center Frequency Register. Caution should be taken when using the SYNCIN since the holding register contents will be transferred to the Sample Center Frequency Register whenever SYNCIN is asserted (and external sync is selected via CW22).

Shaping filter I coefficients are loaded from the first coefficient (C0) in address 0x200h to the last address in 0x2FFh.

Because interpolation by 16 is possible, the coefficient addresses are structured in blocks of 16, one address for each phase of the interpolation. With a 256 tap filter using an interpolation of 16, there are 16 multiplies required to implement the filter. Tables 4 and 5 detail the coefficient address allocation, with the Interpolation Phase indicated by the IP number on the left, and the multiplier number indicated by the numbers 0 through 15 across the top.

TABLE 4. I SHAPING FILTER COEFFICIENT ADDRESSES

	DS_0	DS_1	DS_2	DS_3	DS_4	DS_5	DS_6	DS_7	DS_8	DS_9	DS_{10}	DS_{11}	DS_{12}	DS_{13}	DS_{14}	DS_{15}
IP0	512	528	544	560	576	592	608	624	640	656	672	688	704	720	736	752
IP1	513	529	545	561	577	593	609	625	641	657	673	689	705	721	737	753
IP2	514	530	546	562	578	594	610	626	642	658	674	690	706	722	738	754
IP3	515	531	547	563	579	595	611	627	643	659	675	691	707	723	739	755
IP4	516	532	548	564	580	596	612	628	644	660	676	692	708	724	740	756
IP5	517	533	549	565	581	597	613	629	645	661	677	693	709	725	741	757
IP6	518	534	550	566	582	598	614	630	646	662	678	694	710	726	742	758
IP7	519	535	551	567	583	599	615	631	647	663	679	695	711	727	743	759
IP8	520	536	552	568	584	600	616	632	648	664	680	696	712	728	744	760
IP9	521	537	553	569	585	601	617	633	649	665	681	697	713	729	745	761
IP10	522	538	554	570	586	602	618	634	650	666	682	698	714	730	746	762
IP11	523	539	555	571	587	603	619	635	651	667	683	699	715	731	747	763
IP12	524	540	556	572	588	604	620	636	652	668	684	700	716	732	748	764
IP13	525	541	557	573	589	605	621	637	653	669	685	701	717	733	749	765
IP14	526	542	558	574	590	606	622	638	654	670	686	702	718	734	750	766
IP15	527	543	559	575	591	607	623	639	655	671	687	703	719	735	751	767

TABLE 5. I COEFFICIENT ADDRESSING FOR A 16 TAP INTERPOLATED BY 4 FILTER

	DS_0	DS_1	DS_2	DS_3	DS_4	DS_5	DS_6	DS_7	DS_8	DS_9	DS_{10}	DS_{11}	DS_{12}	DS_{13}	DS_{14}	DS_{15}
IP0	512 = C0	528 = C4	544 = C8	560 = C12	576	592	608	624	640	656	672	688	704	720	736	752
IP1	513 = C1	529 = C5	545 = C9	561 = C13	577	593	609	625	641	657	673	689	705	721	737	753
IP2	514 = C2	530 = C6	546 = C10	562 = C14	578	594	610	626	642	658	674	690	706	722	738	754
IP3	515 = C3	531 = C7	547 = C11	563 = C15	579	595	611	627	643	659	675	691	707	723	739	755
IP4	516	532	548	564	580	596	612	628	644	660	676	692	708	724	740	756
IP5	517	533	549	565	581	597	613	629	645	661	677	693	709	725	741	757
IP6	518	534	550	566	582	598	614	630	646	662	678	694	710	726	742	758
IP7	519	535	551	567	583	599	615	631	647	663	679	695	711	727	743	759
IP8	520	536	552	568	584	600	616	632	648	664	680	696	712	728	744	760
IP9	521	537	553	569	585	601	617	633	649	665	681	697	713	729	745	761
IP10	522	538	554	570	586	602	618	634	650	666	682	698	714	730	746	762
IP11	523	539	555	571	587	603	619	635	651	667	683	699	715	731	747	763
IP12	524	540	556	572	588	604	620	636	652	668	684	700	716	732	748	764
IP13	525	541	557	573	589	605	621	637	653	669	685	701	717	733	749	765
IP14	526	542	558	574	590	606	622	638	654	670	686	702	718	734	750	766
IP15	527	543	559	575	591	607	623	639	655	671	687	703	719	735	751	767

TABLE 6. Q SHAPING FILTER COEFFICIENT ADDRESSES

	DS_0	DS_1	DS_2	DS_3	DS_4	DS_5	DS_6	DS_7	DS_8	DS_9	DS_{10}	DS_{11}	DS_{12}	DS_{13}	DS_{14}	DS_{15}
IP0	768	784	800	816	832	848	864	880	896	912	928	944	960	976	992	1008
IP1	769	785	801	817	833	849	865	881	897	913	929	945	961	977	993	1009
IP2	770	786	802	818	834	850	866	882	898	914	930	946	962	978	994	1010
IP3	771	787	803	819	835	851	867	883	899	915	931	947	963	979	995	1011
IP4	772	788	804	820	836	852	868	884	900	916	932	948	964	980	996	1012
IP5	773	789	805	821	837	853	869	885	901	917	933	949	965	981	997	1013
IP6	774	790	806	822	838	854	870	886	902	918	934	950	966	982	998	1014
IP7	775	791	807	823	839	855	871	887	903	919	935	951	967	983	999	1015
IP8	776	792	808	824	840	856	872	888	904	920	936	952	968	984	1000	1016
IP9	777	793	809	825	841	857	873	889	905	921	937	953	969	985	1001	1017
IP10	778	794	810	826	842	858	874	890	906	922	938	954	970	986	1002	1018
IP11	779	795	811	827	843	859	875	891	907	923	939	955	971	987	1003	1019
IP12	780	796	812	828	844	860	876	892	908	924	940	956	972	988	1004	1020
IP13	781	797	813	829	845	861	877	893	909	925	941	957	973	989	1005	1021
IP14	782	798	814	830	846	862	878	894	910	926	942	958	974	990	1006	1022
IP15	783	799	815	831	847	863	879	895	911	927	943	959	975	991	1007	1023

The convolution multiplies C0 by the most recent data sample. For a 16 tap, interpolate-by-4 filter, the calculations are:

OUTPUT0 = (C0*D[n]) + (C4*D[n-1]) + (C8*D[n-2]) + (C12*D[n-3])

OUTPUT1 = (C1*D[n]) + (C5*D[n-1]) + (C9*D[n-2]) + (C13*D[n-3])

OUTPUT2 = (C2*D[n]) + (C6*D[n-1]) + (C10*D[n-2]) + (C14*D[n-3])

OUTPUT3 = (C3*D[n]) + (C7*D[n-1]) + (C11*D[n-2]) + (C15*D[n-3])

Table 6 indicates how the I coefficients should be loaded for this example. Notice that 16 filter coefficients are required. All other addresses not used. The filter interpolates by 4 and the coefficients are loaded sequentially through the 4 interpolation phases starting at 512 - 515, then jumping to 528 - 531 for the next four addresses, and so on until 16 coefficients have been loaded.

Shaping filter Q coefficients are loaded from the first coefficient (B0) in address 0x300h to the last address in 0x3FFh. The convolution multiplies B0 by the most recent data sample. For a 16 tap, interpolate-by-4 filter, the calculations are:

OUTPUT0 = (B0*D[n]) + (B4*D[n-1]) + (B8*D[n-2]) + (B12*D[n-3])

OUTPUT1 = (B1*D[n]) + (B5*D[n-1]) + (B9*D[n-2]) + (B13*D[n-3])

OUTPUT2 = (B2*D[n]) + (B6*D[n-1]) + (B10*D[n-2]) + (B14*D[n-3])

OUTPUT3 = (B3*D[n]) + (B7*D[n-1]) + (B11*D[n-2]) + (B15*D[n-3])

Table 7 indicates how the Q coefficients should be loaded for this example. Identical to the I filter, notice that since 16 filter coefficients are required. All other addresses not used. The filter interpolates by 4, and the coefficients are loaded sequentially through the 4 interpolation phases, starting at 768-771, then jumping to 784-787 for the next four addresses, and so on until 16 coefficients have been loaded.

Microprocessor Read

The DUC offers the microprocessor access to all of the control data configuration registers through a read process. The shaping filter coefficients, however, cannot be read. With $\overline{CE}$ asserted, a “read” consists of dropping the $\overline{RD}$ line low to transfer data from the register addresses selected by A(9:0). The read address mapping is provided in Table 8. The timing is detailed in Figure 15.

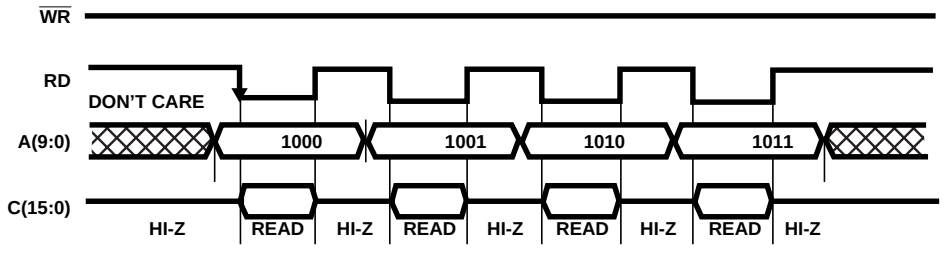
TABLE 7. Q COEFFICIENT ADDRESSING FOR A 16 TAP INTERPOLATED BY 4 FILTER

	DS_0	DS_1	DS_2	DS_3	DS_4	DS_5	DS_6	DS_7	DS_8	DS_9	DS_{10}	DS_{11}	DS_{12}	DS_{13}	DS_{14}	DS_{15}
IP0	**768 = D0**	**784 = D4**	**800 = D8**	**816 = D12**	832	848	864	880	896	912	928	944	960	976	992	1008
IP1	**769 = D1**	**785 = D5**	**801 = D9**	**817 = D13**	833	849	865	881	897	913	929	945	961	977	993	1009
IP2	**770 = D2**	**786 = D6**	**802 = D10**	**818 = D14**	834	850	866	882	898	914	930	946	962	978	994	1010
IP3	**771 = D3**	**787 = D7**	**803 = D11**	**819 = D15**	835	851	867	883	899	915	931	947	963	979	995	1011
IP4	772	788	804	820	836	852	868	884	900	916	932	948	964	980	996	1012
IP5	773	789	805	821	837	853	869	885	901	917	933	949	965	981	997	1013
IP6	774	790	806	822	838	854	870	886	902	918	934	950	966	982	998	1014
IP7	775	791	807	823	839	855	871	887	903	919	935	951	967	983	999	1015
IP8	776	792	808	824	840	856	872	888	904	920	936	952	968	984	1000	1016
IP9	777	793	809	825	841	857	873	889	905	921	937	953	969	985	1001	1017
IP10	778	794	810	826	842	858	874	890	906	922	938	954	970	986	1002	1018
IP11	779	795	811	827	843	859	875	891	907	923	939	955	971	987	1003	1019
IP12	780	796	812	828	844	860	876	892	908	924	940	956	972	988	1004	1020
IP13	781	797	813	829	845	861	877	893	909	925	941	957	973	989	1005	1021
IP14	782	798	814	830	846	862	878	894	910	926	942	958	974	990	1006	1022
IP15	783	799	815	831	847	863	879	895	911	927	943	959	975	991	1007	1023

TABLE 8. READ ADDRESS MAP FOR MICRO PROCESSOR INTERFACE

A4	A2	A1	A0	DESCRIPTION
0	X	0	0	Carrier Center Frequency: CF(31:16)
0	X	0	1	Carrier Center Frequency: CF(15:0)
0	X	1	0	Re-Sampler Center Frequency: SF(29:16)
0	X	1	1	Re-Sampler Center Frequency: SF(15:0)
1	0	0	0	Modulation Control: En Out bit 3; Mod(2:0)
1	0	0	1	Gain Control: OUTGAIN(7:0)
1	0	1	0	FIFO Control: FIFO Ready bit 5; I FIFO Empty bit 4; Q FIFO Empty bit 3; RTH(2:0)
1	0	1	1	Poly-Phase Control: DS(3:0) = b5-2; IP(1:0)
1	1	0	X	EnNCO
1	1	1	0	Sync Control: Ext Sync Polarity bit 1; Sync Sel bit 0
1	1	1	1	Test Control

FIFO Ready is the logical inverse of the $\overline{\text{FIFORDY}}$ output. I and Q FIFO empty bits are the output of a “zero” state detector operating on the address bus for the respective FIFO.



NOTE: See Table 8 for valid Read Addresses.

FIGURE 15. TYPICAL READ SEQUENCE

Reset

There are two ways to invoke a reset in the DUC: Assert the $\overline{RST}$ signal, or write to Control Word 21. While a reset does not stop the internal clocking, the data processing halts because of the following actions:

- Zeros are placed into the Sample Rate and Carrier NCO accumulator registers. These registers will be held at zero until a sync enables the NCOs to again accept the frequency input word.
- The I and Q FIFO depth counters are reset to zero and the FIFORDY flipflop is Cleared, pulling the DUC $\overline{FIFORDY}$ output high.
- The data path is disabled between the shaping filter and the FM modulator in the prefiltered FM mode, and the Gain adjust circuit in the QASK mode.
- In the interpolation filter, the coefficient RAM select is disabled, the data into the data RAM is set to zeroes, the Q channel data RAM select is disabled and the Data RAM address is zeroed, beginning a 16 address increment to both the I and Q Data RAMS. This enables the data RAMS to be written with zeros.

Commanding the DUC to reset by asserting the $\overline{RST}$ signal causes the all internal processing to halt. Furthermore, asserting $\overline{RST}$ clears both the Sampling and Carrier NCO frequency accumulator registers (sets the outputs = 0). The center and offset frequency registers ***are not*** cleared by $\overline{RST}$. The NCO accumulator registers are held at zero until the NCO is loaded with the first frequency value. The Sampling and Carrier NCO center and offset frequency registers are held at zero until an input sync has been detected. Because the Sampling NCO does not start until the detection of a sync (after a $\overline{RST}$ assertion), the shaping FIR filter is also kept from processing data. Reset is performed by either dropping the $\overline{RST}$ low or writing to Control Word 21 (see Microprocessor Write).

Starting Sequence

DUC internal processing can be initiated by either pulsing the SYNCIN pin (when it must be synchronized to a system event) or by writing to the LSByte of the Sampling NCO center frequency Control Word. The start up for the SYNCIN pin occurs on either the rising or falling edge of the pulse, whichever is selected in CW22, Bit 1.

For multiple DUC operation, the SYNCOUT of the first chip acts as a master and is tied to the SYNCIN of the remaining chips, as shown in Figure 16. When the first chip receives an input sync from a write to the LSByte of the timing NCO control word, then the SYNCOUT will synchronize all other DUC's slaved to that chip.

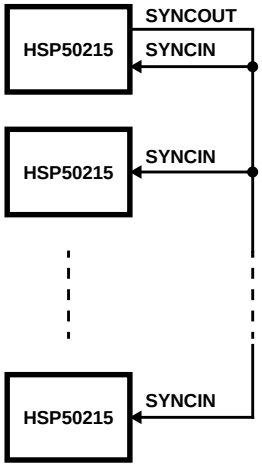


FIGURE 16. CONFIGURATION FOR SYNCHRONIZATION OF MULTIPLE DUCs

Configuration Control Register Bit Definitions

CONTROL ADDRESS 0: I CHANNEL INPUT

BIT POSITION	FUNCTION	DESCRIPTION
15-0	I Channel QASK Input or FM Input	IIN(15:0). In QASK mode, this is the I input vector. The format is 2's complement. The MSB is bit 15. The mixer operation is: OUT = (I*COS) - (Q*SIN). In FM mode, this is interpreted as an offset frequency to the center frequency. The modulation index depends on the mode and the filter coefficients. In FM with post filter mode, the phase change per input sample can range from -180 to 180 degrees, so the deviation is limited to ±(input sample rate)/2.

CONTROL ADDRESS 1: Q CHANNEL INPUT

BIT POSITION	FUNCTION	DESCRIPTION
15-0	Q Channel Input	QIN(15:0). In QASK mode, this is the Q input vector. See address 0 above. In FM mode, this input is not used.

CONTROL ADDRESS 2: TIMING NCO FREQUENCY MSBYTE CONTROL WORD

BIT POSITION	FUNCTION	DESCRIPTION
15-14	Reserved (Note 1)	Reserved (Note 1).
13-0	Sample Rate Ratio's Most Significant 14 Bits	SR(29:16). The sample rate is controlled by a 30-bit NCO clocked at the output clock rate. The upper MSByte of the sample rate ratio SR(29:0), or SR(29:16), is loaded in this address. The sample rate is computed by the formula: $F_{RESAMP} = SR(29:0) \times f_{CLK} \times 2^{-32}$; $SR(29:0) = INT[(F_{RESAMP}/f_{CLK}) \times 2^{32}]$.

CONTROL ADDRESS 3: TIMING NCO FREQUENCY LSBYTE CONTROL WORD

BIT POSITION	FUNCTION	DESCRIPTION
15-0	Sample Rate Ratio's Least Significant 16 Bits	SR(15:0). See Control Address 2. SR(15:0) is loaded in this address.

CONTROL ADDRESS 4: CARRIER CENTER FREQUENCY MSBYTE CONTROL WORD

BIT POSITION	FUNCTION	DESCRIPTION
15-0	Carrier Center Frequency's Most Significant 16 Bits	CF(31:16). The SIN/COS ROM is controlled by a 32-bit NCO clocked at the input clock rate. The upper MSByte of the sample rate ratio CF(31:0), or CF(31:16), is loaded in this address. The center frequency is computed by the formula: $f_C = CF(31:0) \times f_{CLK} \times 2^{-32}$; $CF(31:0) = INT(f_C/f_{CLK} \times 2^{32})$. Setting CW 4 and 5 to zero bypasses the mixers (COS = 1; SIN = 0).

CONTROL ADDRESS 5: CARRIER CENTER FREQUENCY LSBYTE CONTROL WORD

BIT POSITION	FUNCTION	DESCRIPTION
15-0	Carrier Center Frequency's Least Significant 16 Bits	CF(15:0). See Control Address 4. CF(15:0) is loaded in this address. Setting CW 4 and 5 to zero bypasses the mixers (COS = 1; SIN = 0).

CONTROL ADDRESS 16: MODULATION CONTROL

BIT POSITION	FUNCTION	DESCRIPTION
15-4	Reserved (Note 1)	Reserved (Note 1).
3	Enable Output	EN OUT.

CONTROL ADDRESS 16: MODULATION CONTROL (Continued)

BIT POSITION	FUNCTION	DESCRIPTION
2	Delay Select	DLYSEL. 1 = no delay. 0 = 1/2 coarse sample delay.
1-0	Mod Type	MOD(1:0): 00 = QASK. 01 = FM with filtering after modulation (analog FM with baseband filtering provided before HSP50215). In this mode, both I and Q filters are used. 10 = FM with filtering before modulation (FSK, GMSK). This mode uses only the I filter bank. 11 = not used.

CONTROL ADDRESS 17: GAIN CONTROL

BIT POSITION	FUNCTION	DESCRIPTION
15-8	Reserved	Reserved.
7-0	Output Gain	OUTGAIN(7:0)

OUTGAIN (7:0)	ATTENUATION (dBFS)	SCALING GAIN ((V_{OUT}/V_{IN})%)
1111 1111	-0.033996	99.6
1000 0000	-6.021	50.0
0100 0000	-12.041	25.0
0010 0000	-18.062	12.5
0001 0000	-24.082	6.25
0000 1000	-30.103	3.125
0000 0100	-36.124	1.5625
0000 0010	-42.144	0.78125
0000 0001	-48.165	0.390625

CONTROL WORDS 18: FIFO CONTROL

BIT POSITION	FUNCTION	DESCRIPTION
15-3	Reserved (Note 1)	Reserved (Note 1).
2-0	$\overline{\text{FIFORDY}}$ Threshold	RTH(2:0). Programmable FIFO READY Threshold. This digital word represents the FIFO depth threshold (number of data samples in the FIFO) at which the $\overline{\text{FIFORDY}}$ will be asserted, alerting the data source that more input data is required in the FIFO. The FIFO threshold sets both the I and Q FIFO thresholds. RTH2 is the MSB.

CONTROL WORDS 19: POLYPHASE CONTROL

BIT POSITION	FUNCTION	DESCRIPTION
15-6	Reserved (Note 1)	Reserved (Note 1).
5-2	DS	DS(3:0). Number of data samples in shaping filter, 4-16. Load with number of data samples minus 1.
1-0	IP	IP(1:0). Number of interpolation phases: 00 = not valid. 01 = 4. 10 = 8. 11 = 16.

CONTROL ADDRESS 20: SPARE

BIT POSITION	FUNCTION	DESCRIPTION
15-0	Reserved (Note 1)	Reserved (Note 1).

CONTROL ADDRESS 21: RESET CONTROL

BIT POSITION	FUNCTION	DESCRIPTION
15-0	Reset	RST. Writing to this registers will reset this part.

CONTROL ADDRESS 22: SYNC CONTROL

BIT POSITION	FUNCTION	DESCRIPTION
15-2	Reserved (Note 1)	Reserved (Note 1).
1	External Sync Polarity	SYNCPOL. 0 defines a Sync assertion as a transition from a logic low to a logic high; 1 defines a Sync assertion as a transition from a logic high to a logic low: 0 =  1 = 
0	Sync Select	SYNCSEL. 0 = Sync via a Write to Control Word 3; 1 = Sync via SYNCIN control input.

CONTROL WORDS 23: TEST CONTROL

BIT POSITION	FUNCTION	DESCRIPTION
15-0	Reserved (Note 1)	Reserved (Note 1).

CONTROL WORDS 512-767: I CHANNEL POLY-PHASE COEFFICIENTS 512-767 (0X200H = 0X2FFH)

BIT POSITION	FUNCTION	DESCRIPTION
15:0	I Coefficients	ICOEFFICIENTS(15:0). Coefficients are loaded from the first coefficient (C0) in address 0x200h to the last address in 0x2FFh. The convolution multiplies C0 by the most recent data sample. For a 16 tap, interpolate-by-4 filter, the calculations are: OUTPUT0 = (C0*D[n]) + (C4*D[n-1]) + (C8*D[n-2]) + (C12*D[n-3]). OUTPUT1 = (C1*D[n]) + (C5*D[n-1]) + (C9*D[n-2]) + (C13*D[n-3]). OUTPUT2 = (C2*D[n]) + (C6*D[n-1]) + (C10*D[n-2]) + (C14*D[n-3]). OUTPUT3 = (C3*D[n]) + (C7*D[n-1]) + (C11*D[n-2]) + (C15*D[n-3]). See Microprocessor Write section for more detail.

CONTROL WORDS 768-1023: Q CHANNEL POLY-PHASE COEFFICIENTS 768-1023 (0X300H = 0X3FFH)

BIT POSITION	FUNCTION	DESCRIPTION
15:0	Q Coefficients	QCOEFFICIENTS(15:0). Coefficients are loaded from the first coefficient (B0) in address 0x300h to the last address in 0x3FFh. The convolution multiplies B0 by the most recent data sample. For a 16 tap, interpolate-by-4 filter, the calculations are: OUTPUT0 = (B0*D[n]) + (B4*D[n-1]) + (B8*D[n-2]) + (B12*D[n-3]). OUTPUT1 = (B1*D[n]) + (B5*D[n-1]) + (B9*D[n-2]) + (B13*D[n-3]). OUTPUT2 = (B2*D[n]) + (B6*D[n-1]) + (B10*D[n-2]) + (B14*D[n-3]). OUTPUT3 = (B3*D[n]) + (B7*D[n-1]) + (B11*D[n-2]) + (B15*D[n-3]). See Microprocessor Write section for more detail.

NOTE:

1. Reserved bits should be set to logic 0.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
Typical De-rating Factor . . . . . 2mA/MHz Increase in I_{CCOP}
ESD Classification . . . . . Class 2

Operating Conditions

Voltage Range . . . . . +4.75V to +5.25V
Temperature Range
Commercial . . . . . 0^oC to 70^oC
Industrial. . . . . 40^oC to 85^oC
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . 2V to V_{CC}
Input Rise and Fall Time . . . . . 1V/ns Max

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
MQFP Package	36

Maximum Package Power Dissipation at 70^oC
MQFP Package 2.22W
Maximum Package Power Dissipation at 85^oC
MQFP Package 1.81W
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Junction Temperature . . . . . 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(MQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 5 ±5%, T_A = 0^oC to 70^oC, Commercial; T_A = -40^oC to 85^oC Industrial

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.25V	2.0	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.75V	-	0.8	V
Clock Input High	V_{IHC}	V_{CC} = 5.25V	3.0	-	V
Clock Input Low	V_{IHL}	V_{CC} = 4.75V	-	0.8	V
Output High Voltage	V_{OH}	I_{OH} = -400µA, V_{CC} = 4.75V	2.6	-	V
Output Low Voltage	V_{OL}	I_{OL} = +2.0mA, V_{CC} = 4.75V	-	0.4	V
Input Leakage Current	I_L	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V	-10	+10	µA
Output Leakage Current	I_O	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V	-10	+10	µA
Standby Power Supply Current	I_{CCSB}	V_{CC} = 5.25V, Outputs Not Loaded	-	500	µA
Operating Power Supply Current (Commercial)	I_{CCOP}	f = 52MHz, V_{IN} = V_{CC} or GND, V_{CC} = 5.25V	-	156	mA (Note 3)
Operating Power Supply Current (Industrial)	I_{CCOP}	f = 48MHz, V_{IN} = V_{CC} or GND, V_{CC} = 5.25V	-	144	mA (Note 3)
Input Capacitance	C_{IN}	Freq = 1MHz, V_{CC} Open, All Measurements Are Referenced To Device Ground	-	10	pF (Note 4)
Output Capacitance	C_{OUT}		-	12	pF (Note 4)

NOTES:

3. Power Supply current is proportional to operation frequency. Typical rating for I_{CCOP} is 2mA/MHz.
4. Capacitance T_A = 25^oC, controlled via design or process parameters and not directly tested. Characterized upon initial design and at major process or design changes.

AC Electrical Specifications

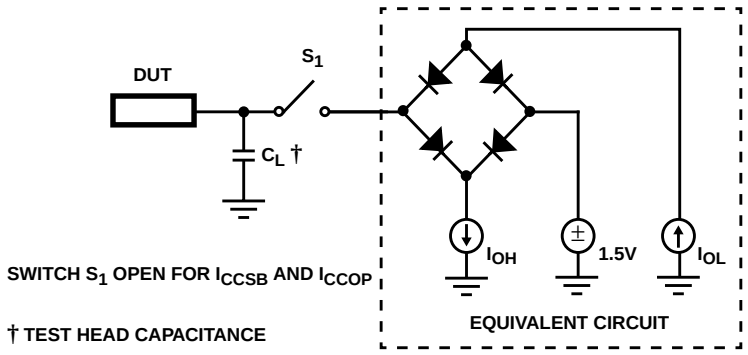
V_{CC} = 5 ±5%, T_A = 0°C to 70°C, Commercial; T_A = -40°C to 85°C, Industrial (Note 5)

PARAMETER	SYMBOL	52MHz		UNITS
		MIN	MAX	
REFCLK Clock Period (Commercial)	t_{CP}	19	-	ns
REFCLK Clock Period (Industrial)	t_{CP}	21	-	ns
REFCLK High	t_{CH}	7	-	ns
REFCLK Low	t_{CL}	7	-	ns
Setup Time CAS(15:0), SYNCIN to REFCLK	t_{DS}	6	-	ns
Hold Time CAS(15:0), SYNCIN to REFCLK	t_{DH}	1	-	ns
Setup Time A(9:0) to Rising Edges of $\overline{WR}$ or $\overline{CE}$ Low	t_{AS}	12	-	ns
Setup Time C(15:0) to Rising Edges of $\overline{WR}$ or $\overline{CE}$ Low	t_{CS}	6	-	ns
Hold Time A(9:0) to Rising Edges of $\overline{WR}$ or $\overline{CE}$ Low	t_{AH}	2	-	ns
Hold Time C(15:0) to Rising Edges of $\overline{WR}$ or $\overline{CE}$ Low	t_{CH}	2	-	ns
Read Address Low to Data Valid	t_{ADO}	-	16	ns
Rising Edge of $\overline{WR}$ or $\overline{CE}$ to FIFORDY High (FIFO Write)	t_{WF}	12	-	ns
REFCLK to OUT(15:0)	t_{DO}	-	8	ns
REFCLK to SYNCOUT, SAMPCLK and $\overline{FIFORDY}$ Valid	t_{DOC}	-	12	ns
$\overline{WR}$ High	t_{WRH}	7	-	ns
$\overline{WR}$ Low	t_{WRL}	7	-	ns
$\overline{RD}$ Low	t_{RL}	9	-	ns
$\overline{RD}$ LOW and $\overline{CE}$ LOW to Data Valid	t_{RDO}	-	8	ns
$\overline{RD}$ HIGH and $\overline{CE}$ HIGH to Output Disable	t_{ROD}	-	10 (Note 6)	ns
Output Enable Time	t_{OE}	-	7	ns
Output Disable Time	t_{OD}	-	8 (Note 6)	ns
Output Rise, Fall Time	t_{RF}	-	5 (Note 6)	ns

NOTE:

5. AC tests performed with C_L = 40pF, I_{OL} = 2mA, and I_{OH} = -400µA. Input reference level for CLK is 2.0V, all other inputs 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V.
6. Controlled via design or process parameters and not directly tested. Characterized upon initial design and at major process or design changes.

AC Test Load Circuit



Waveforms

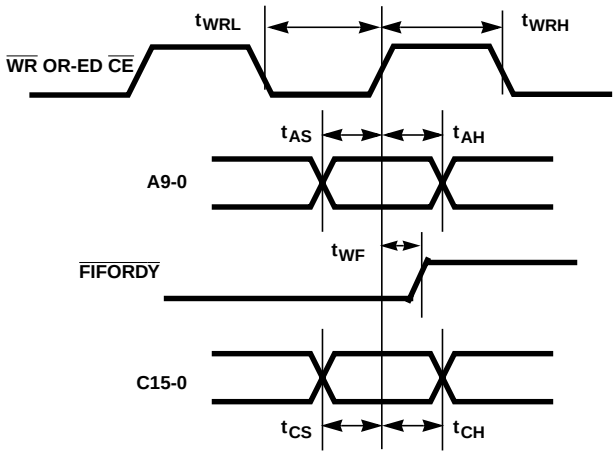


FIGURE 17. TIMING RELATIVE TO $\overline{WR}$ OR WITH $\overline{CE}$

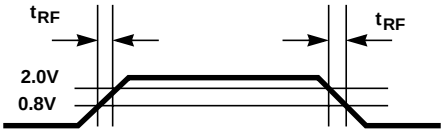
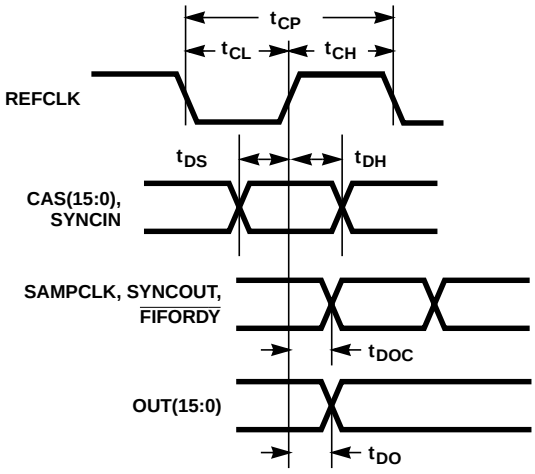


FIGURE 18. OUTPUT RISE AND FALL TIMES



NOTE: CASZ, OFM, $\overline{OE}$ are signals that must remain constant with respect to REFCLK until the part is reset. In the write mode, either $\overline{CE}$ or $\overline{WR}$ must be clocked while the other is tied low. In read mode, either $\overline{CE}$ or $\overline{RD}$ must be clocked while the other is tied low. Never tie all three interface signals ($\overline{CE}$, $\overline{RD}$ and $\overline{WR}$) low at the same time.

FIGURE 19. TIMING RELATIVE TO REFCLK

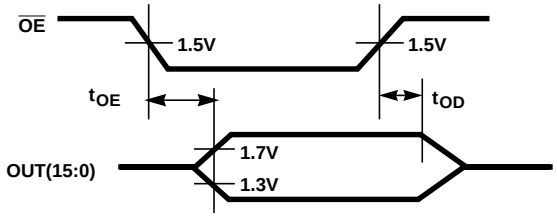


FIGURE 20. OUTPUT ENABLE/DISABLE

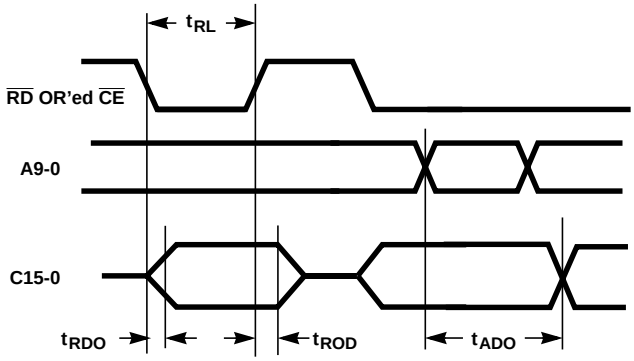


FIGURE 21. TIMING RELATIVE TO READ OR TO $\overline{CE}$