# GENNUM CORPORATION

# *GENLINX*™ GS9022
# Digital Video Serializer

DATA SHEET

## FEATURES

- **built-in 75 Ω cable driver with two serial outputs**
- **standard independent operation**
- **space saving 28 pin PLCC package**
- **650 mW typical power dissipation (data output driving 75 Ω load).**
- **supports bit rates to 400 Mb/s**
- **accepts 8 bit and 10 bit TTL and CMOS compatible parallel data inputs**
- **fully compatible with SMPTE 259M serial digital standard**
- **single +5 or -5 volt supply**

## APPLICATIONS

- $4f_{SC}$, 4:2:2 and 360 Mb/s serial digital interfaces for:

| | |
|---|---|
| Video cameras | VTRs |
| Signal generators | Portable equipment |

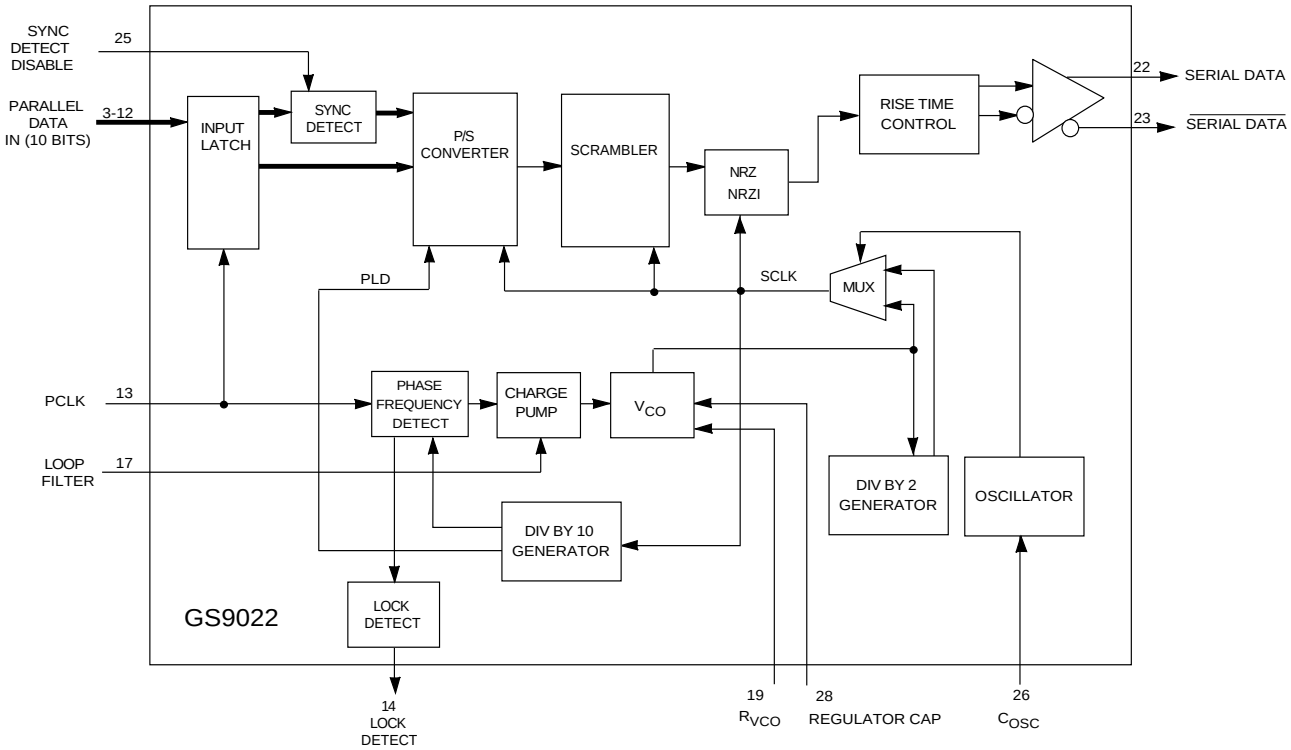
## DEVICE DESCRIPTION

The GS9022 is a monolithic bipolar integrated circuit designed to serialize SMPTE 125M and SMPTE 244M bit parallel digital signals as well as other 8 or 10 bit parallel formats. This device performs the functions of sync detection, parallel to serial conversion, data scrambling (using the $X^9 + X^4 + 1$ algorithm), 10x parallel clock multiplication and conversion of NRZ to NRZI serial data. The data rate is automatically set for SMPTE 259M data rates to 400 Mb/s. Other features include a lock detect output and an internal cable driver capable of driving two 75Ω loads.

The device requires a single +5 volt or -5 volt supply and typically consumes 650 mW of power while driving two 75 Ω loads. The 28 pin PLCC packaging assures a small footprint for the complete encoder function.

## ORDERING INFORMATION

| Part Number | Package | Temperature |
|---|---|---|
| GS9022-CPJ | 28 pin PLCC | 0°C to 70°C |
| GS9022-CTJ | 28 pin PLCC Tape | 0°C to 70°C |




**FUNCTIONAL BLOCK DIAGRAM**

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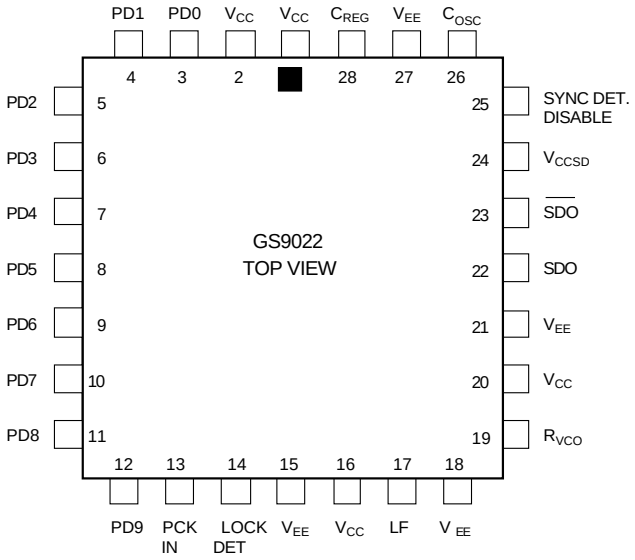
## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | VALUE/UNITS |
|---|---|
| Supply Voltage | 5.5 V |
| Input Voltage Range (any input) | $-V_{EE} < V_I < V_{CC}$ |
| DC Input Current (any one input) | 10 mA |
| Power Dissipation ($V_S$ = 5.25 V) | 910 mW |
| Operating Temperature Range | $0^{\circ}C \le T_A \le 70^{\circ}C$ |
| Storage Temperature Range | $-65^{\circ}C \le T_S \le 150^{\circ}C$ |
| Lead Temperature (soldering 10 seconds) | $260^{\circ}C$ |

**CAUTION**
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

## PIN CONNECTIONS




## GS9022 - ENCODER DC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 5V, $V_{EE}$ = 0V, $T_A$ = 0°C to 70°C unless otherwise shown

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_S$ | Operating Range | 4.75 | 5.0 | 5.25 | V | |
| Power Consumption | $P_D$ | Data outputs driving two 75Ω loads | - | 650 | - | mW | $T_A$ = 25°C |
| Supply Current | $I_S$ | Data outputs driving two 75Ω loads | - | 160 | 190 | mA | |
| TTL Inputs-HIGH | $V_{IH}$ | $T_A$ = 25°C | 2.0 | - | - | V | |
| TTL Inputs-LOW | $V_{IL}$ | $T_A$ = 25°C | - | - | 0.8 | V | |
| Logic Input Current | $I_{IN}$ | | - | 2.5 | 6.0 | µA | |
| TTL Outputs-HIGH | $V_{OH}$ | $T_A$ = 25°C | 2.4 | - | - | V | |
| TTL Outputs-LOW | $V_{OL}$ | $T_A$ = 25°C | - | - | 0.5 | V | |

## GS9022 - ENCODER AC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 5V, $V_{EE}$ = 0V, $T_A$ = 0°C to 70°C, unless otherwise shown

| PARAMETER | | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|
| Serial Data Outputs | | | | | | | | |
| SDATA, $\overline{SDATA}$ | bit rates | $BR_{SDO}$ | | 100 | - | 400 | Mb/s | |
| | signal swing | $V_{SDO}$ | $R_L$ = 75Ω | 720 | 800 | 880 | mVp-p | |
| | rise/fall times | $t_r$, $t_f$ | (20 - 80%) | 400 | 550 | 800 | ps | |
| | jitter | $t_j$ | 270 Mb/s | | 240 | - | ps p-p | Note 1 |
| Lock Time | | $t_{lock}$ | $C_{Loop\ filt}$ = 0.1µF<br>$R_{Loop\ filt}$ = 3.9kΩ<br>$C_{OSC}$ = 0.1µF | - | 5 | - | ms | Auto Standard |
| Parallel Data & Clock Inputs | | | | | | | | |
| | risetime | $t_R$ | $T_A$ = 25°C | 500 | - | - | ps | |
| | setup | $t_{SU}$ | | 3 | - | - | ns | |
| | hold | $t_{HOLD}$ | | 3 | - | - | ns | |

Note 1: Measured using PCLK as trigger source on 1 GHz oscilloscope

## GS9022 Digital Video Serializer - Detailed Device Description

The GS9022 Serializer is a bipolar integrated circuit used to convert parallel data into a serial format according to the SMPTE 259M standard. The device encodes both eight and ten bit TTL-compatible parallel signals producing serial data rates up to 400 Mb/s. It operates from a single five volt supply and is packaged in a 28 pin PLCC.

Functional blocks within the device include the input latches, sync detector, parallel to serial converter, scrambler, NRZ to NRZI converter, internal cable driver, PLL for 10 x parallel clock multiplication and lock detect.

The parallel data (PD0-PD9) and parallel clock (PCKIN) are applied via pins 3 through 13 respectively.

### Sync Detector

The Sync Detector looks for the reserved words 000-003 and 3FC-3FF, in ten bit hexadecimal, or 00 and FF in eight bit hexadecimal, used in the TRS-ID sync word. When the occurrence of either all zeros or all ones at inputs PD2-PD9 is detected, the lower two bits PD0 and PD1 are forced to zeros or ones, respectively. This makes the system compatible with eight or ten bit data. For non - SMPTE standard parallel data, a logic input, Sync Detect Disable (25) is available to disable this feature.

### Scrambler

The Scrambler is a linear feedback shift register used to pseudo-randomize the incoming serial data according to the fixed polynomial ($X^9+X^4+1$). This minimizes the DC component in the output serial data stream. The NRZ to NRZI converter uses another polynomial (X+1) to convert a long sequence of ones to a series of transitions, minimizing polarity effects.

### Phase Locked Loop

The PLL performs parallel clock multiplication and provides the timing signal for the serializer. It is composed of a phase/frequency detector, charge pump, VCO, a divide-by-ten counter, and a divide by two counter.

The phase/frequency detector allows a wider capture range and faster lock time than that which can be achieved with a phase discriminator alone. The discrimination of frequency also eliminates harmonic locking. With this type of discriminator, the PLL can be over-damped for good stability without sacrificing lock time.

The charge pump delivers a 'charge packet' to the loop filter which is proportional to the system phase error. Internal voltage clamps are used to constrain the loop filter voltage between approximately 1.8 and 3.4 volts.

The VCO, constructed from a current-controlled multivibrator, features operation in excess of 400 Mb/s and a wide pull range (≈ ± 40% of centre frequency).

### VCO Centre Frequency Selection

The wide VCO pull range allows the PLL to compensate for variations in device processing, temperature variations and changes in power supply voltage, without external adjustment. A single external resistor is used to set the VCO current for all standards.

The $C_{OSC}$ pin is used to configure the VCO of the GS9022 in one of three modes, as shown below:

| $C_{OSC}$ | Mode |
|---|---|
| 0.1µF to GND | Auto Standard |
| 10k Resistor to VCC | $f/2$ ON |
| 10k Resistor to GND | $f/2$ OFF |

In auto standard mode, the capacitor sets the sweep rate at which the VCO toggles between $f$ and $f/2$.

The $f/2$ ON and $f/2$ OFF modes are used to configure the GS9022 VCO for single standard operation.

The lock detect circuit disables the serial data output when the loop is not locked. The Lock Detect output is available from pin 14 and is HIGH when the loop is locked.

The true and complement serial data, SDO and $\overline{SDO}$ are available from pins 22 and 23. These outputs will drive two 75 Ω co-axial cables with SMPTE level serial digital video signals.

## GS9022 PIN DESCRIPTIONS

| PIN NO. | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{CC}$ | | Power Supply: Most positive power supply connection for the PLL and Scrambler. |
| 2 | $V_{CC}$ | | Power Supply: Most positive power supply connection for the parallel data inputs and P/S converter. |
| 3-12 | PD0-PD9 | I | TTL level inputs of the parallel data words. PD0 is the LSB and PD9 is the MSB. |
| 13 | PCKIN | I | TTL level input of the parallel clock. |
| 14 | LOCK DET | O | TTL level output which goes high when the internal PLL is locked. |
| 15 | $V_{EE}$ | | Power Supply: Most negative power supply connection. |
| 16 | $V_{CC}$ | | Power Supply: Most positive power supply connection for the PLL and Scrambler. |
| 17 | LF | I | Connection for the R-C loop filter components. |
| 18 | $V_{EE}$ | | Power Supply: Most negative power supply connection. |
| 19 | $R_{VCO}$ | I | VCO frequency setting resistor. A 1% resistor is required. |
| 20 | $V_{CC}$ | | Power Supply: Most positive power supply connection for the PLL and Scrambler. |
| 21 | $V_{EE}$ | | Power Supply: Most negative power supply connection. |
| 22, 23 | SDO, $\overline{SDO}$ | I | 75 Ω cable driver outputs (true and inverse). |
| 24 | $V_{CCSD}$ | | Power Supply: Most positive power supply for cable driver outputs. |
| 25 | SYNC DET DISABLE | I | TTL level input that disables the internal sync detector when high. This allows the GS9022 to serialize 8 or 10 bit non-SMPTE standard parallel data. |
| 26 | $C_{OSC}$ | I | Toggles VCO between $f$ and $f/2$. |
| 27 | $V_{EE}$ | I | Power Supply: Most negative power supply connection. |
| 28 | $C_{REG}$ | I | Compensation capacitor for internal voltage regulator that requires decoupling with a 0.1 µF capacitor located as close as possible to the pin in series with an 820 Ω Resistor. |

## INPUT / OUTPUT CIRCUITS

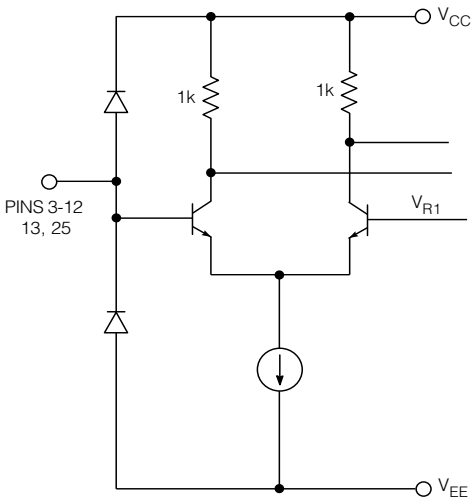



Fig. 1 Sync Detect Disable, Parallel Data, Parallel Clock

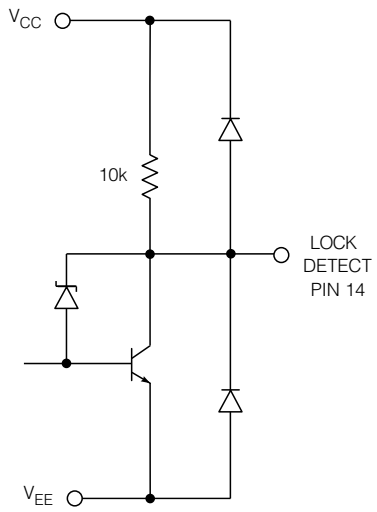



Fig. 2 Lock Detect

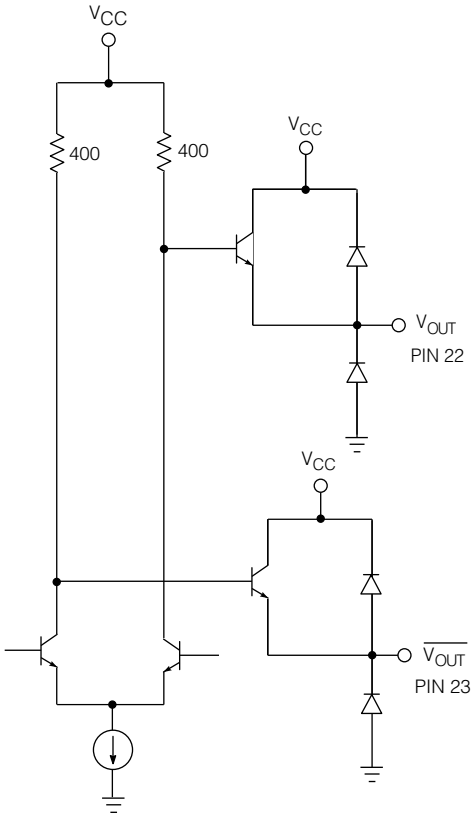



Fig. 3 Output Circuit

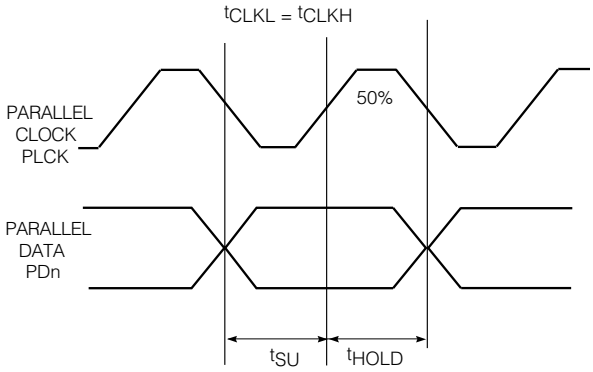



Fig. 4 Input Clock / Data Timing

## TYPICAL PERFORMANCE CURVES ($V_S$ = 5V, $T_A$ = 25° C unless otherwise shown)

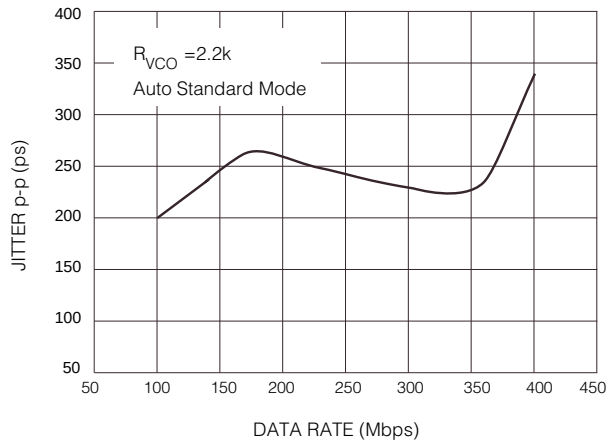



Fig. 5 Output Jitter

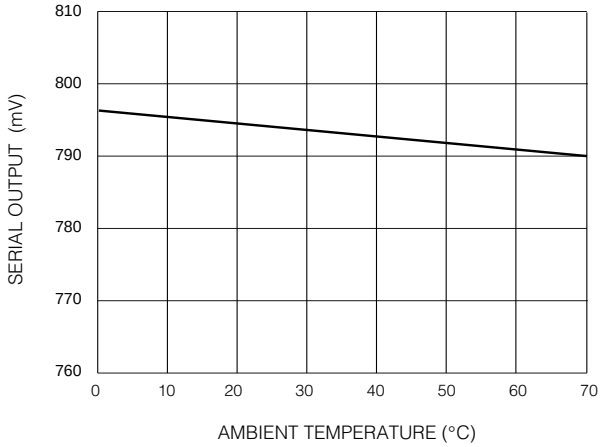



Fig. 6 Serial Data Output Level vs Temperature

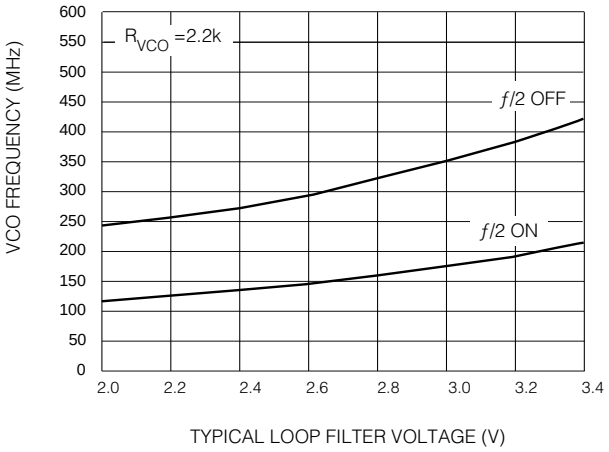



Fig. 7 VCO Frequency vs Loop Filter Voltage

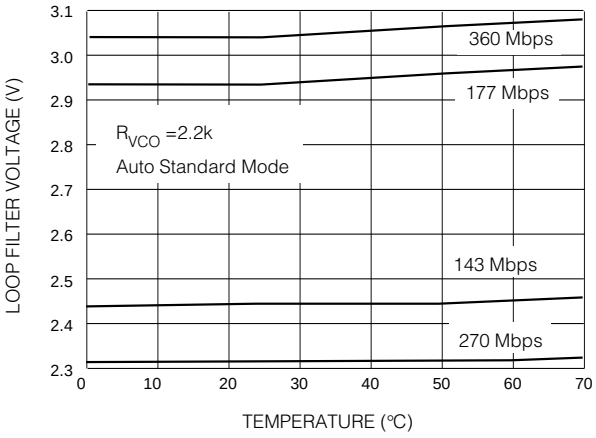



Fig. 8 Loop Filter Voltage vs Temperature

## APPLICATION CIRUIT

Figure 9 shows a typical application circuit of the GS9022 driving a 75Ω cable.

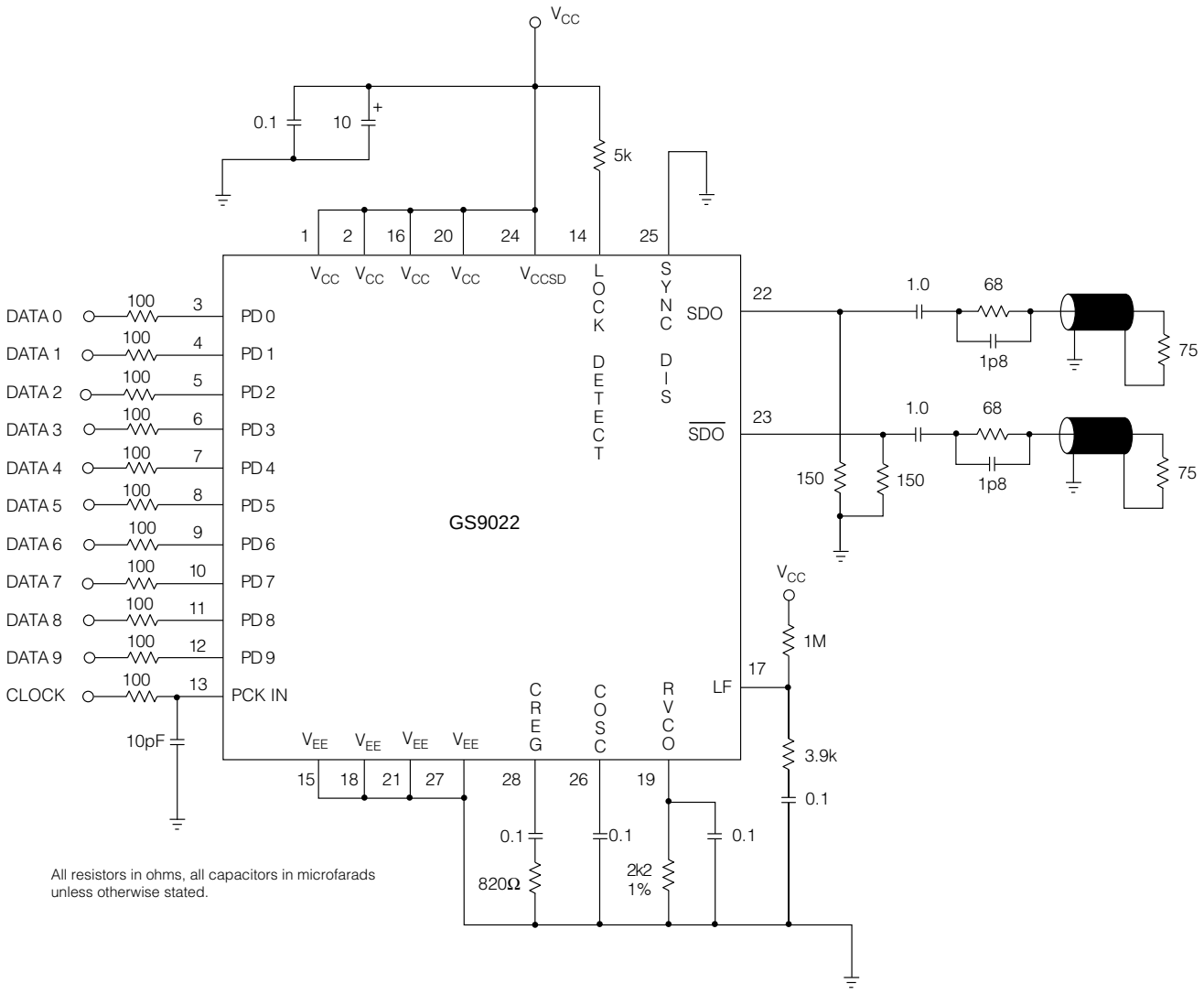



Fig. 9 GS9022 Application Circuit

**DOCUMENT IDENTIFICATION**

PRODUCT PROPOSAL
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PRELIMINARY
The product is in a preproduction phase and specifications are subject to change without notice.

DATA SHEET
The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

REVISION NOTE:
Changes to Figure 9.