Advance Data Sheet

CADEKA
Amplify the Human Experience

COMLINEAR® CLC2500

Dual Ultrafast Voltage Comparator

FEATURES

- 650ps propagation delay
- 100ps overdrive delay variation
- 70dB CMRR
- Differential latch control
- 10V/ns slew rate
- ECL compatible
- 350mW power dissipation
- 900MHz bandwidth
- Lead-free QFN and SOIC packages

APPLICATIONS

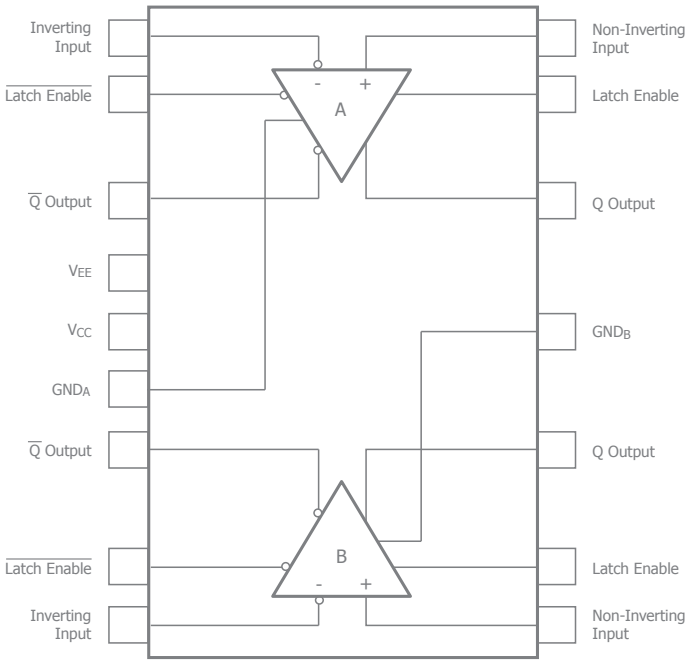
- Automated test equipment
- High-speed instrumentation
- Window comparators
- High-speed timing
- Line receivers
- High-speed triggers
- Threshold detection
- Peak detection

General Description

The COMLINEAR CLC2500 is a sub-nanosecond dual comparator with propagation delay variation less than 100ps from 5 to 50mV input overdrive voltage. The input slew rate is 10V/ns and the differential input stage has a common-mode input range of -2.5V to 4V.

The COMLINEAR CLC2500 has ECL-compatible complementary digital outputs that are capable of driving 50Ω terminated transmission lines. The CLC2500 is ideally suited for automated test equipment (ATE) applications, high-speed instrumentation, and peak detection.

CLC2500 - Functional Block Diagram

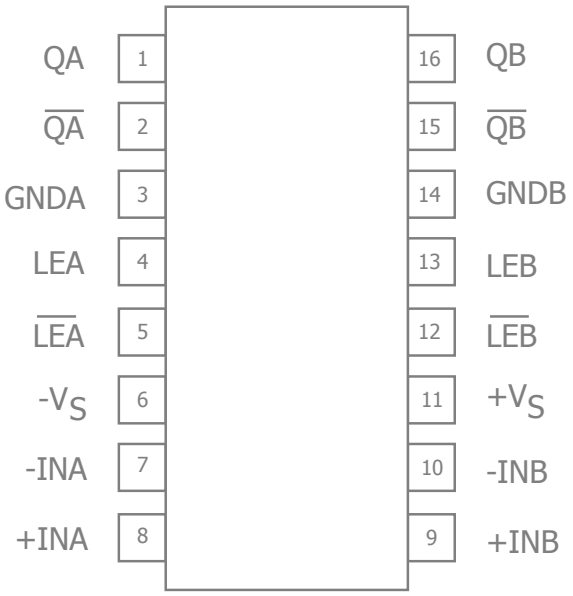


Ordering Information

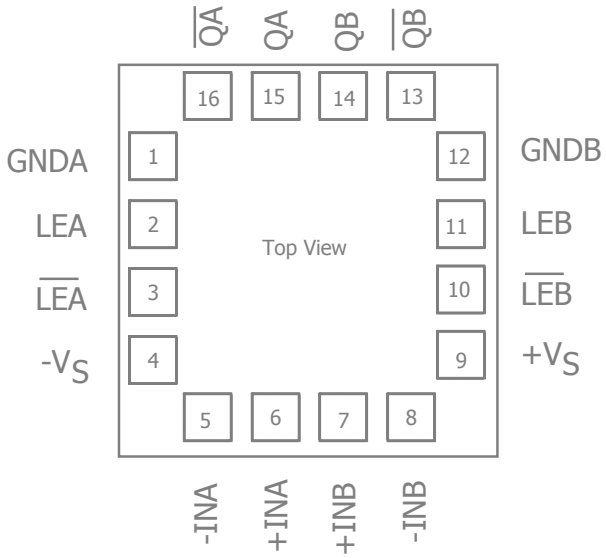
Part Number	Package	V_{IO}	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CLC2500AILP16X*	QFN-16	10mV	Yes	Yes	-40°C to +85°C	Reel
CLC2500AISO16X*	SOIC-16	10mV	Yes	Yes	-40°C to +85°C	Reel
CLC2500BILP16X*	QFN-16	25mV	Yes	Yes	-40°C to +85°C	Reel
CLC2500BISO16X*	SOIC-16	25mV	Yes	Yes	-40°C to +85°C	Reel

*Advance Information. Moisture sensitivity level for all parts is MSL-1.

SOIC Pin Configuration



QFN Pin Configuration



CLC2500 Pin Assignments

SOIC Pin No.	QFN Pin No.	Pin Name	Description
1	15	QA	Output A
2	16	$\overline{QA}$	Inverted Output A
3	1	GNDA	Ground
4	2	LEA	Latch Enable A
5	3	$\overline{LEA}$	Inverted Latch Enable A
6	4	VEE	Negative Supply Voltage
7	5	-INA	Inverting Input A
8	6	+INA	Non-Inverting Input A
9	7	+INB	Non-Inverting Input B
10	8	-INB	Inverting Input B
11	9	VCC	Positive Supply Voltage
12	10	$\overline{LEB}$	Inverted Latch Enable B
13	11	LEB	Latch Enable B
14	12	GNDB	Ground
15	13	$\overline{QB}$	Output B
16	14	QB	Inverted Output B

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Positive Supply Voltage	-0.5	+6.0	V
Negative Supply Voltage	-6.0	+0.5	V
Ground Voltage Differential	-0.5V	+0.5V	V
Input Common Mode Voltage	-4.0V	+5.0V	V
Differential Input Voltage	-3.0V	+3.0V	V
Input Voltage, Latch Controls	VEE	+0.5V	V
Output Current		30	mA

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
16-Lead SOIC		68		°C/W
16-Lead QFN		TBD		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	SOIC-16	QFN-16
Human Body Model (HBM), output ESD protection	TBD	TBD
Charged Device Model (CDM)	TBD	TBD

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Positive Supply Voltage		5.0		V
Negative Supply Voltage		-5.2		V

Electrical Characteristics

T_A = 25°C, V_{CC} = +5.0V, V_{EE} = -5.2V, R_L = 50Ω to -2V; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Units
			CLC2500A			CLC2500B			
Frequency Domain Response									
BW_{SS}	-3dB Bandwidth			900			900		MHz
SR	Slew Rate			10			10		V/ns
Time Domain Response									
PD	Propogation Delay	20mV overdrive		650			750		ps
t_{LATCH}	Latch Set-up Time	250mV overdrive		150			150		ps
LATCHD	Latch to Output Delay	250mV overdrive		500			500		ps
t_{PULSE}	Latch Pulse Width	250mV overdrive		500			500		ps
t_{HOLD}	Latch Hold Time	250mV overdrive		0			0		ps
t_R	Rise Time	20% to 80%		180			180		ps
t_F	Fall Time	20% to 80%		80			80		ps
DC Performance									
V_{IO}	Input Offset Voltage (1)		-10	3	10	-25	12	25	mV
dV_{IO}	Average Drift			10			40		µV/°C
I_{OS}	Input Offset Current (1)		-3	1	3	-5	2	5	µA
I_b	Input Bias Current (1)		-25	8	25	-25	8	25	µA
$+I_S$	Positive Supply Current			18	30		18	30	mA
$-I_S$	Negative Supply Current			40	55		40	55	mA
V_{CC}	Positive Supply Voltage		4.75	5.0	5.25	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage		-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
CMIR	Input Common Mode Range		-2.5		4.0	-2.5		4.0	V
V_{LATCH}	Latch Enable	Common Mode Range	-2.0		0	-2.0		0	V
AOL	Open Loop Gain			66			66		dB
R_{IN}	Differential Input Resistance			500			500		kΩ
C_{IN}	Input Capacitance			0.6			0.6		pF
PSRR	Power Supply Rejection Ratio			70			70		dB
CMRR	Common Mode Rejection Ratio	V_{CM} = -2.5V to 4V		70			70		dB
P_D	Power Dissipation	Both Channels, No Load		350	425		350	425	mW
		Both Channels, with Load		400	550		400	550	mW
OUT_{HIGH}	Output High Level	ECL 50Ω to -2V	-1.00		-0.81	-1.00		-0.81	V
OUT_{LOW}	Output Low Level	ECL 50Ω to -2V	-1.95		-1.54	-1.95		-1.54	V

Notes:
1. 100% tested at 25°C

Timing Information

The timing diagram for the comparator is shown in Figure 1. If LE is high and $\overline{LE}$ low in the CLC2500, the comparator tracks the input difference voltage. When LE is driven low and $\overline{LE}$ high, the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of a 20 mV overdrive voltage) changes the comparator output after a time of tpdL or tpdH (Q or $\overline{Q}$). The input signal must be maintained for a time t_S (set-up time) before the LE falling edge and $\overline{LE}$ rising edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signals occurring before t_S will be detected and held; those occurring after t_H will not be detected. Changes between t_S and t_H may not be detected.

Switching Terms

Symbol	Description
t_{pdH}	INPUT TO OUTPUT HIGH DELAY – the propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output LOW to HIGH transition
t_{pdL}	INPUT TO OUTPUT LOW DELAY – the propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output HIGH to LOW transition
t_{pdLOH}	LATCH ENABLE TO OUTPUT HIGH DELAY – the propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition
V_{OD}	VOLTAGE OVERDRIVE – the difference between the differential input and reference input voltages
t_{pLOL}	LATCH ENABLE TO OUTPUT LOW DELAY – the propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition
t_H	MINIMUM HOLD TIME – the minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs
t_{pL}	MINIMUM LATCH ENABLE PULSE WIDTH – the minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change
t_S	MINIMUM SET-UP TIME – the minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs

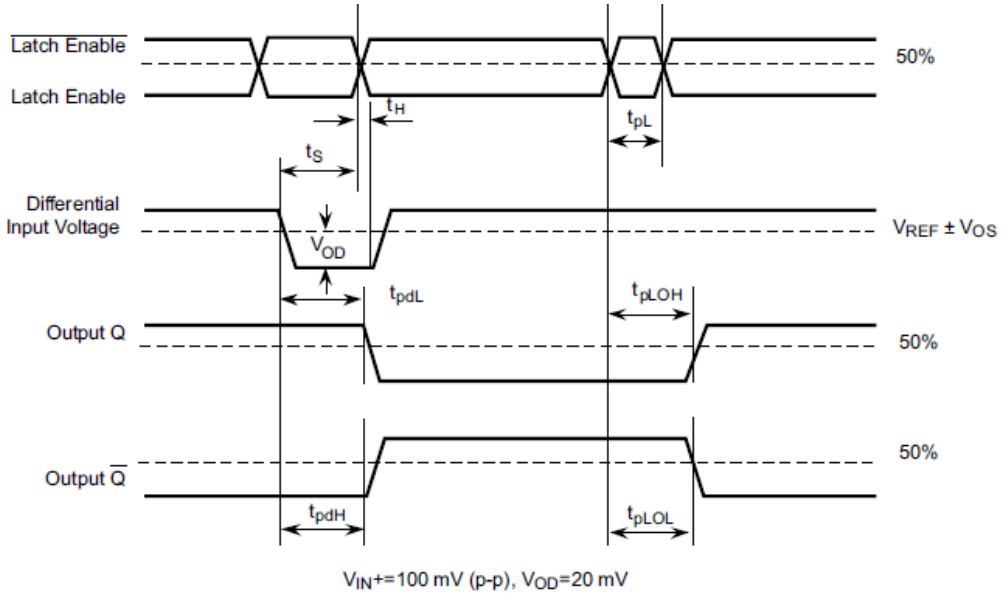


Figure 1 - Timing Diagram

General Information

The CLC2500 is an ultrahigh-speed dual voltage comparator. It offers tight absolute characteristics. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50Ω transmission lines.

The CLC2500 has a complementary latch enable control for each comparator. Both should be driven by standard ECL logic levels.

The negative common mode voltage is –2.5V. The positive common mode voltage is +4.0V. The dual comparators share the same V_{CC} and V_{EE} connections but have separate grounds for each comparator to achieve high crosstalk rejection.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF and 0.1µF ceramic capacitors for power supply decoupling
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

An evaluation board is available for the CLC2500, contact CADEKA for more information.

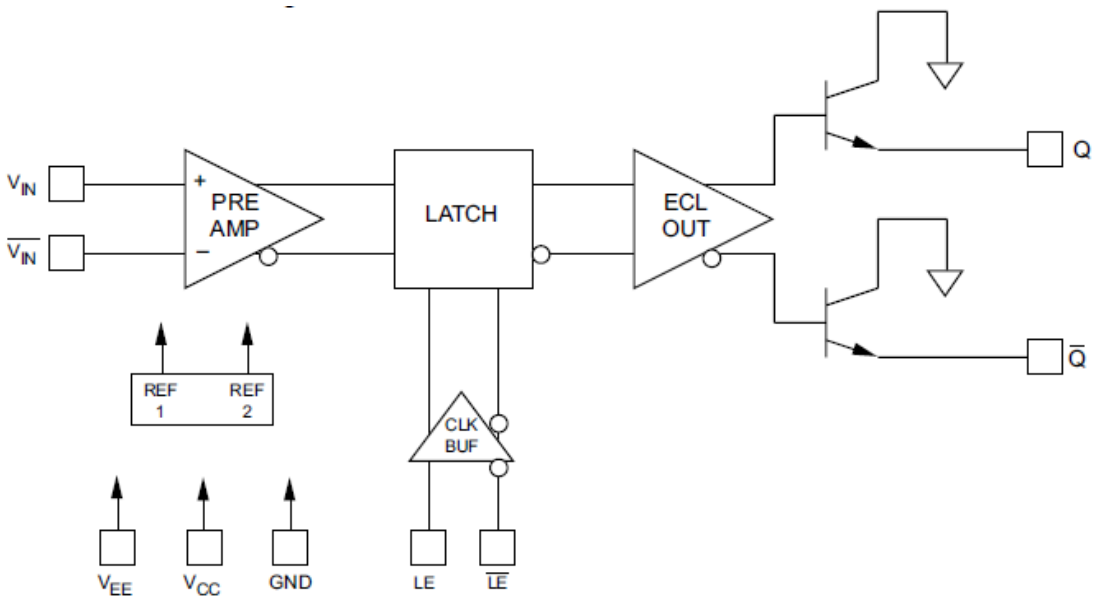


Figure 2 - Internal Function Diagram

Typical Interface Circuit

The typical interface circuit using the comparator is shown in Figure 3. Although it needs few external components and is easy to apply, there are several conditions that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the CLC2500 comparator is a very high-frequency and high-gain device, certain layout rules must be followed to avoid oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used while the input impedance to the part is kept as low as possible to decrease parasitic feedback. If the output board traces are longer than approximately half an inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. Both supply voltage pins should be decoupled with high-frequency capacitors as close to the device as possible. All ground pins and no connects should be soldered to a common ground plane to further improve noise immunity. If using the CLC2500 as a single comparator, the outputs of the inactive comparator can be grounded, left open, or terminated with 50Ω to –2V. All outputs on the active comparator, whether used or unused, should have identical terminations to minimize ground current switching transients.

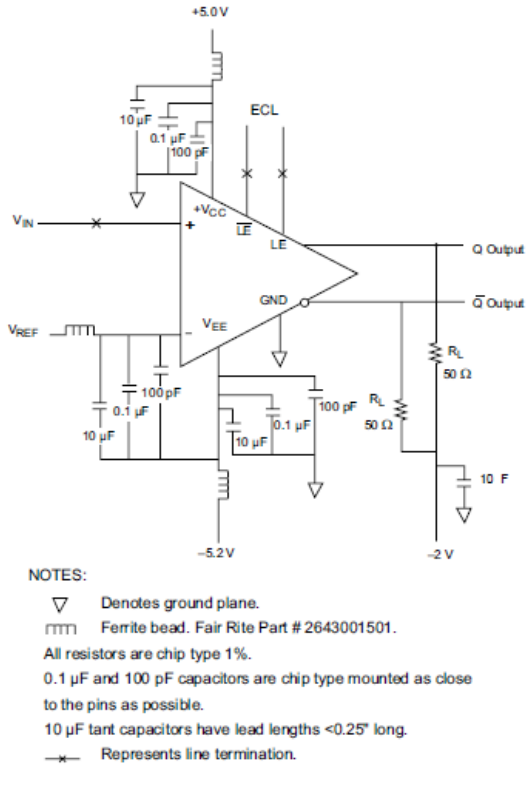


Figure 3 - CLC2500 Typical Interface Circuit

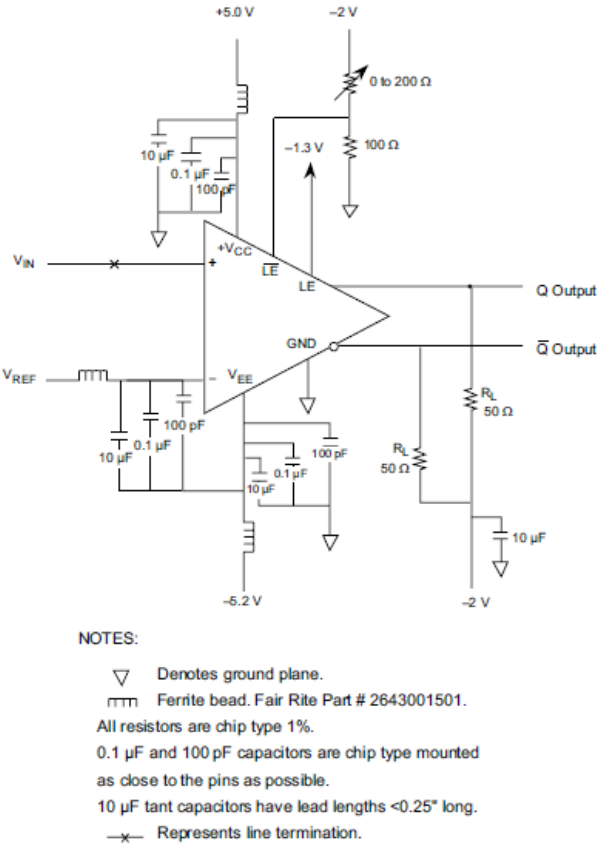
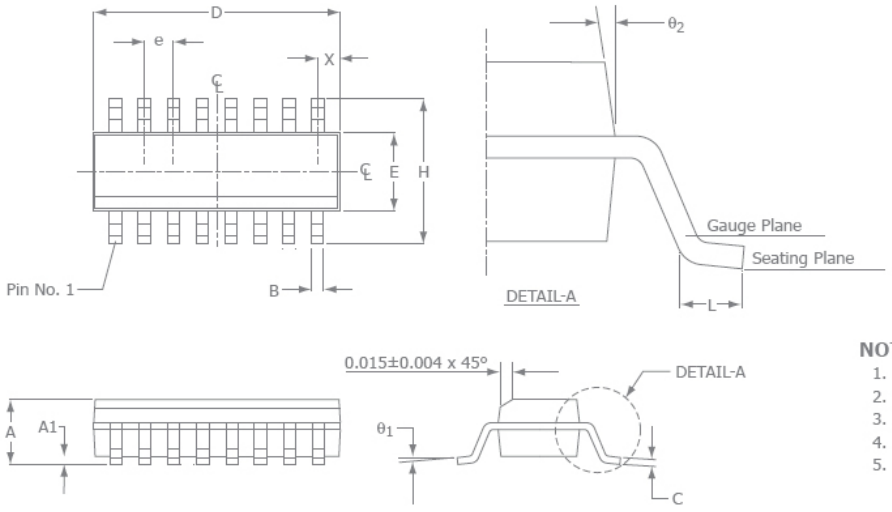


Figure 4: CLC2500 Typical Interface Circuit with Hysteresis

Mechanical Dimensions

SOIC-16 Package

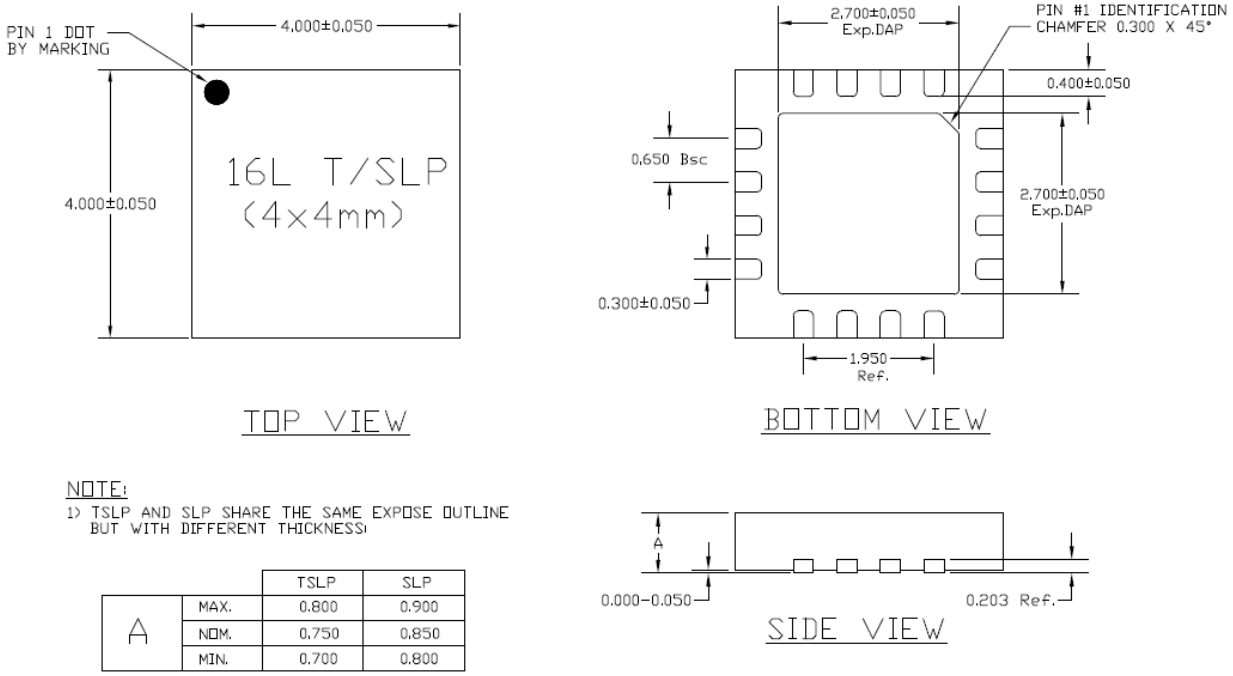


SOIC-16		
SYMBOL	MIN	MAX
A	0.054	0.068
A1	0.004	0.0098
B	0.014	0.019
D	0.386	0.393
E	0.150	0.157
H	0.229	0.244
e	0.050 BSC	
C	0.0075	0.0098
L	0.016	0.034
X	0.020 Ref	
θ_1	0°	8°
θ_2	7° BSC	

NOTE:

1. All dimensions are in inches.
2. Lead coplanarity should be 0" to 0.004" max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.0075" from the lead tip.

QFN-16 Package



NOTE:
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS.

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

For additional information regarding our products, please visit CADEKA at: cadeka.com

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