National Semiconductor

August 1996

Not Intended For New Designs

Comlinear CLC206
Overdrive-Protected Wideband Op Amp

General Description

The CLC206 is a wideband, overdrive-protected operational amplifier designed for applications needing both speed and high drive capability (100mA). Utilizing Comlinear's well-established current feedback architecture, the CLC206 exhibits performance far beyond that of conventional voltage feedback op amps. For example, the CLC206 has a bandwidth of 180MHz at a gain of +20 and settles to 0.1% in 19ns. Plus, the CLC206 has a combination of important features not found in other high-speed op amps.

The 100mA output current and the large signal bandwidth of 70MHz (20V_{pp}) make the CLC206 ideal for applications which involve both high signal amplitudes and heavy loads as in coaxial line driving applications.

Complete overdrive protection has been designed into the CLC206. This is critical for applications, such as ATE and instrumentation, which require protection from signal levels high enough to cause saturation of the amplifier. This feature allows the output of the op amp to be protected against short circuits using techniques developed for low-speed op amps. With this capability, even the fastest signal sources can feature effective short circuit protection.

The CLC206 is constructed using thin film resistor/bipolar transistor technology, and is available in the following versions:

CLC206AI	-25°C to +85°C	12-pin TO-8 can
CLC206A8C	-55°C to +125°C	12-pin TO-8 can, MIL-STD-883, Level B
CLC206AK	-55°C to +125°C	12-pin TO-8 can, features burn-in and hermetic testing
CLC206AM	-55°C to +125°C	12-pin TO-8 can, screened to Comlinear's M standard for high reliability

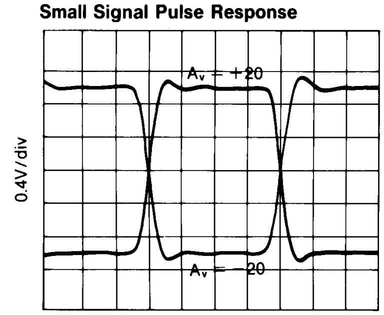
Features

- -3dB bandwidth of 180MHz
- 70MHz large signal bandwidth (20V_{pp})
- 0.1% settling in 19ns
- Overdrive protected
- Output may be current limited
- Stable without compensation
- 3MΩ inout impedance

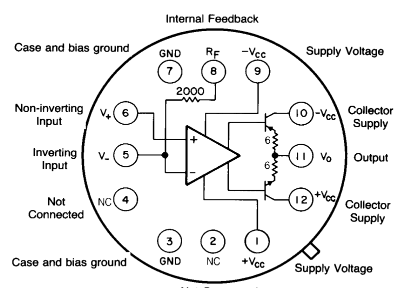
Applications

- Fast, precision A/D conversion
- Automatic test equipment
- Input/output amplifiers
- Photodiode, CCD preamps
- High-speed modems, radios
- Line drivers

Small Signal Pulse Response

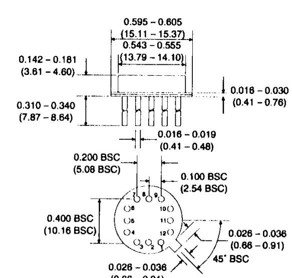


Bottom View



Pin 8 provides access to a 2000Ω feedback resistor which can be connected to the output or left open if an external feedback resistor is desired.

Package Dimensions



Typical Performance

parameter	gain setting +7	+20	+50	−1	−20	−50	units
−3dB bandwidth	220	180	90	220	145	90	MHz
rise time	1.6	2	4	1.6	2.5	4	ns
slew rate	3.4	3.4	3.4	3.4	3.4	3.4	V/ns
settling time (to 0.1%)	22	19	17	20	19	18	ns

CLC206 Electrical Characteristics (A_V = +20, V_{CC} = ±15V, R_L = 200Ω, R_f = 2kΩ; unless specified)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC206AI	+25°C	−25°C	+25°C	+85°C		
Ambient Temperature	CLC206A8/AK	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
* −3dB bandwidth	V_{out} < $2V_{pp}$	180	>150	>150	>135	MHz	SSBW
large signal bandwidth	V_{out} < $20V_{pp}$	70	>54	>60	>60	MHz	FPBW
gain flatness	V_{out} < $2V_{pp}$						
* peaking	0.1 to 40MHz	0	<0.3	<0.3	<0.5	dB	GFPL
* peaking	>40MHz	0	<0.5	<0.5	<0.8	dB	GFPH
* rolloff	at 75MHz	—	<0.7	<0.7	<0.7	dB	GFR
group delay	to 75MHz	3.0±.2	—	—	—	ns	GD
linear phase deviation	to 75MHz	0.6	<2.0	<1.5	<2.0	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.0	<2.5	<2.5	<2.7	ns	TRS
	20V step	7.0	<8.5	<8.5	<8.5	ns	TRL
settling time to 0.1%	10V step, note 2	22	<25	<25	<25	ns	TS
to 0.05%	10V step, note 2	24	<27	<27	<27	ns	TSP
overshoot	10V step	11	<15	<15	<15	%	OS
slew rate	$20V_{pp}$, 100MHz	3.4	>2.7	>3.0	>3.0	V/ns	SR
DISTORTION AND NOISE RESPONSE, note 3							
*2nd harmonic distortion	$2V_{pp}$, 20MHz	−59	<−50	<−50	<−50	dBc	HD2
*3rd harmonic distortion	$2V_{pp}$, 20MHz	−67	<−55	<−55	<−55	dBc	HD3
equivalent input noise							
voltage	>100kHz	2.1	<3.0	<3.0	<3.5	$nV/\sqrt{Hz}$	VN
inverting current	>100kHz	22	<30	<30	<35	$pA/\sqrt{Hz}$	ICN
non-inverting current	>100kHz	5.0	<7.0	<7.0	<8.0	$pA/\sqrt{Hz}$	NCN
noise floor	>100kHz	−157	<−154	<−154	<−153	dBm(1Hz)	SNF
integrated noise	1kHz to 150MHz	39	<55	<55	<61	uV	INV
noise floor	>5MHz	−157	<−154	<−154	<−153	dBm(1Hz)	SNF
integrated noise	5MHz to 150MHz	39	<55	<55	<61	uV	INV
STATIC, DC PERFORMANCE							
*input offset voltage		3.5	<8.0	<8.0	<11.0	mV	VIO
average temperature coefficient		11	<25	<25	<25	uV/°C	DVIO
*input bias current	non-inverting	4.0	<30	<20	<20	uA	IBN
average temperature coefficient		20	<125	<125	<125	nA/°C	DIBN
*input bias current	inverting	2.0	<26	<10	<30	uA	IBI
average temperature coefficient		40	<200	<200	<200	nA/°C	DIBI
*power supply rejection ratio		65	>55	>55	>55	dB	PSRR
common mode rejection ratio		60	>50	>50	>50	dB	CMRR
*supply current	no load	29	<31	<31	<33	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance	DC	3.0	>1.0	>1.0	>1.0	MΩ	RIN
non-inverting input capacitance	75MHz	5.2	<7.0	<7.0	<7.0	pF	CIN
output impedance	DC	—	<0.1	<0.1	<0.1	Ω	RO
output voltage range	no load	±12	>±11	>±11	>±11	V	VO
internal feedback resistor							
absolute tolerance		—	—	<0.2	—	%	RFA
temperature coefficient		—	—	−100±40	—	ppm/°C	RFTC
inverting input current self limit		3.3	<4.5	<4.5	<4.7	mA	ICL

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{cc}	±20V
I_{out}	±150mA
common mode input voltage	±(|V_{cc}|−1)V
differential input voltage	±3V
thermal resistance: See thermal model.	
junction temperature	+175°C
operating temperature	AI: −25°C to +85°C
	A8/AK: −55°C to +125°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C

Recommended Operating Conditions

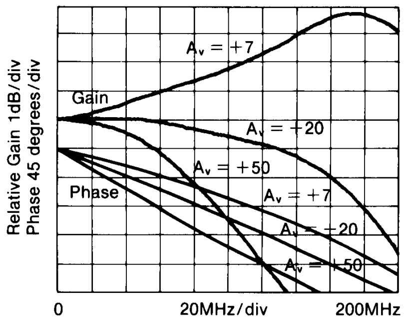
V_{cc}	±5V to ±15V
I_{out}	±100mA
common mode input voltage	±(|V_{cc}|−5)V
gain range:	+7 to +50, −1 to −50

***note: 1:** Parameters preceded by an * are 100% tested. A8 and AK units are tested at −55°C, +25°C, and +125°C. AI units tested at +25°C, although performance at −25°C and +85°C is guaranteed as shown above.

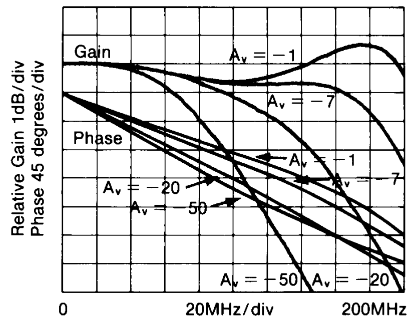
note 2: Settling time specifications require the use of an external feedback resistor (2Ω).

note 3: In AI units, the noise and distortion specifications are guaranteed (but not tested) as shown above.

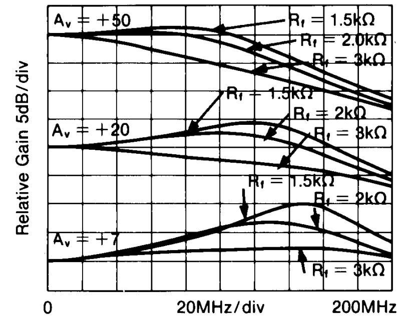
Non-Inverting Gain and Phase



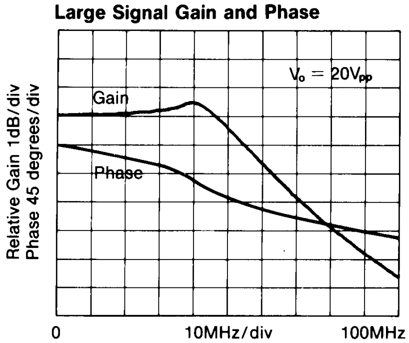
Inverting Gain and Phase



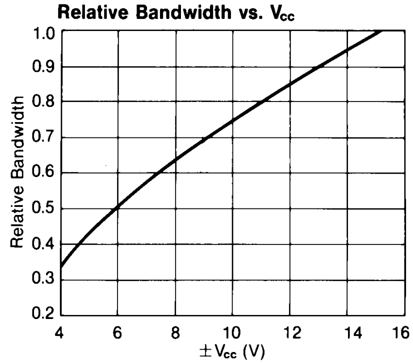
Response vs. External R_f



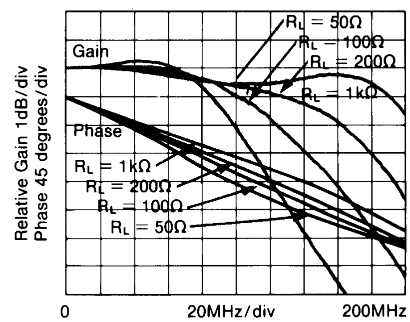
Large Signal Gain and Phase



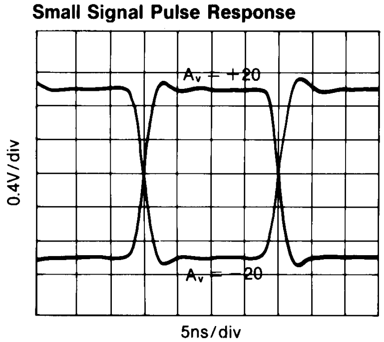
Relative Bandwidth vs. V_{cc}



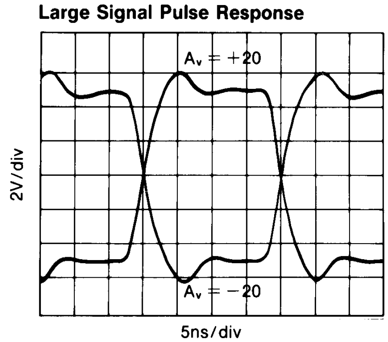
Gain and Phase for Various Loads



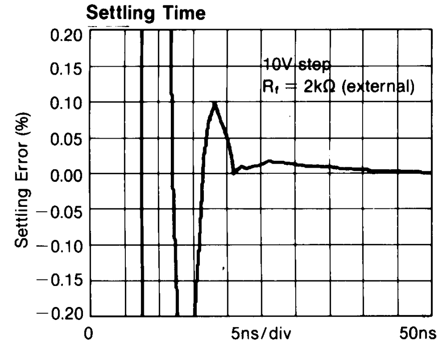
Small Signal Pulse Response



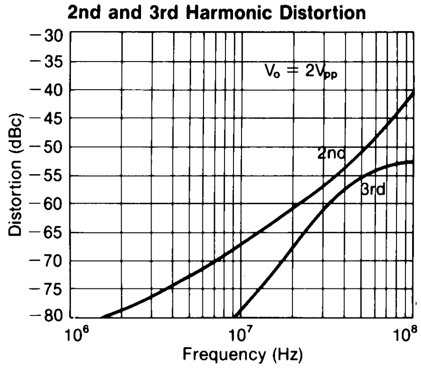
Large Signal Pulse Response



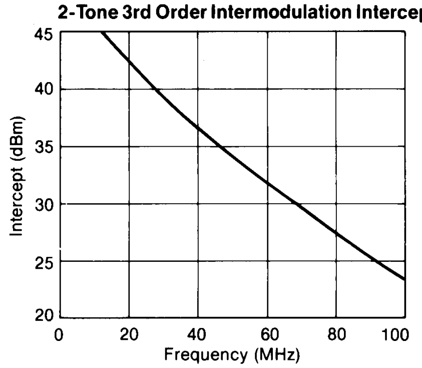
Settling Time



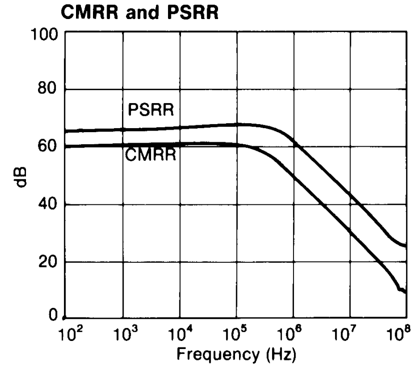
2nd and 3rd Harmonic Distortion



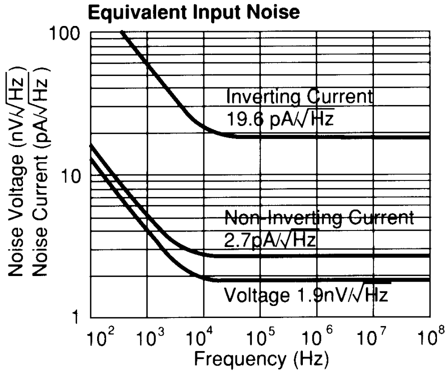
2-Tone 3rd Order Intermodulation Intercept



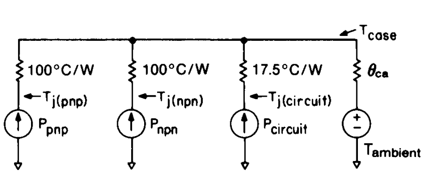
CMRR and PSRR



Equivalent Input Noise



Thermal Model



θ_{ca} = 65°C/W in still air without a heatsink
35°C/W in still air with a Thermalloy 2268
15°C/W in 300ft/min air with a Thermalloy 2268
(Thermalloy 2240 works equally well.)

$P_{circuit} = [(+V_{cc}) - (-V_{cc})]^2$ / 1.15kΩ

$P_{xxx} = [(\pm V_{cc}) - V_{out} - (I_{col})(R_{col} + 6)]\ \ (I_{col})$ (% duty cycle)

(For positive V_o and V_{cc}, this is the power in the npn output stage.)

(For negative V_o and V_{cc}, this is the power in the pnp output stage.)

$I_{col} = V_{out}/R_{load}$ or 4mA, whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and $\pm V_{cc}$.

$T_{j\ (pnp)} = P_{pnp}(100 + \theta_{ca}) + (P_{cir} + P_{npn})\ \theta_{ca} + T_a$, similar for $T_{j\ (npn)}$.

$T_{j\ (cir)} = P_{cir}(17.5 + \theta_{ca}) + (P_{pnp} + P_{npn})\ \theta_{ca} + T_a$.

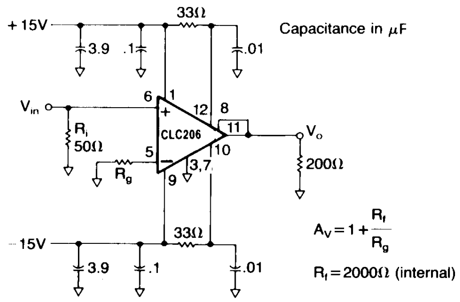


Figure 1: recommended non-inverting gain circuit

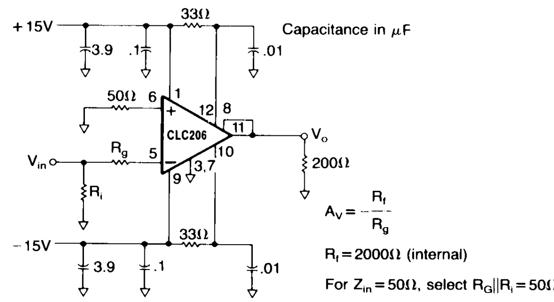


Figure 2: recommended inverting gain circuit

Test fixture schematics are available upon request.

Overdrive Protection

Unlike most other high-speed op amps, the CLC206 is not damaged by saturation caused by overdriving input signals (where V_{in}X gain> V_{out}). The CLC206 self limits the current at the inverting input when the output is saturated (see the inverting input current self limit specification); this ensures that the amplifier will not be damaged due to excessive internal currents during overdrive. For protection against input signals which would exceed either the maximum differential or common mode input voltage, the diode clamp circuits below may be used.

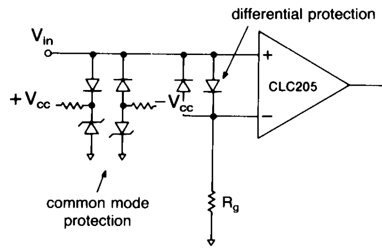


Figure 3: Diode clamp circuits for common mode and differential mode protection

Short Circuit Protection:

Damage caused by short circuits at the output may be prevented by limiting the output current to safe levels. The most simple current limit circuit calls for placing resistors between the output stage collector supplies and the output stage collectors (pins 12 and 10). The value of this resistor is determined by:

$$R_c = \frac{V_c}{I_l} - R_l$$

Where I_l is the desired limit current and R_l is the minimum expected load resistance (0Ω for a short to ground). Bypass capacitors of 0.01μF on should be used on the collectors as in Figures 1 and 2.

A more sophisticated current limit circuit which provides a limit current independent of R_l is shown below.

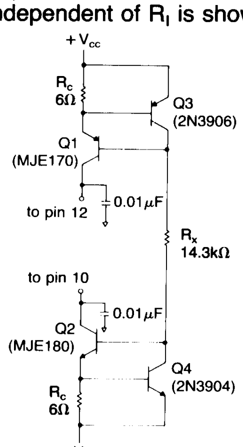


Figure 4: Active current limit circuit (100mA)

With the component values indicated, current limiting occurs at 100mA. For other values of current limit (I_l), select $R_c$to equal V_{be}/I_l. Where V_{be} is the base to emitter voltage drop of Q3 (or Q4) at a current of $[2V_{cc} - 1.4]/R_x$, where $R_x \le [(2V_{cc} - 1.4)/I_l]\ B_{min}$. Also, B_{min} is the minimum beta of Q1 (or Q2) at a current of I_l. Since the limit current depends on V_{be}, which is temperature dependent, the limit current is likewise temperature dependent. If a temperature-independent current limit circuit is needed, contact Comlinear.

Controlling Bandwidth and Passband Response

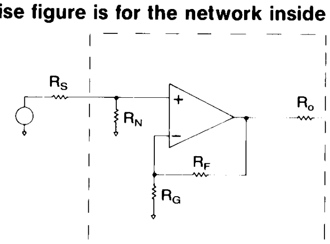
In most applications, a feedback resistor value of 2kΩ will provide optimum performance; nonetheless, some applications may require a resistor of some other value. The response versus R_f plot on the previous page shows how decreasing R_f will increase bandwidth (and frequency response peaking, which may lead to instability). Conversely, large values of feedback resistance tend to roll off the response.

The best settling time performance requires the use of an external feedback resistor (use of the internal resistor results in a 0.1% to 0.2% settling tail). The settling performance may be improved slightly by adding a capacitance of 0.4pF in parallel with the feedback resistor (settling time specifications reflect performance with an external feedback resistor but with no external capacitance).

Noise Analysis

Approximate noise figure can be determined for the CLC206 using the equivalent input noise graph on the preceding page and the equations shown below.

Noise figure is for the network inside this box



$$F = 10\log\left[1 + \frac{R_S}{R_N} + \frac{R_S}{4kT} \cdot \left(i_n^2 + \frac{V_n^2}{R_p^2} + \frac{R_F^2\ i_i^2}{R_p^2\ A_v^2}\right)\right]$$

$$\text{where } R_p = \frac{R_S\ R_N}{R_S + R_N}\ ;\ A_v = \frac{R_F}{R_G} + 1$$

$kT = 4.00 \times 10^{-21}$ Joules at 290°K

V_n is spot noise voltage ($V/\sqrt{Hz}$)

i_n is non-inverting spot noise current ($A/\sqrt{Hz}$)

i_i is inverting spot noise current ($A/\sqrt{Hz}$)

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance the performance of the CLC206. Good ground plane construction and power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal stray capacitance to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Evaluation PC boards (part number 730008 for inverting, 730009 for non-inverting) for the CLC206 are available.

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