Triple Step Down Controller IC for 2 Synchronous and 1 Linear Power Rails

DESCRIPTION

The SiP12203 is a triple-output controller designed for high performance conversion of intermediate bus voltages into the load supplies in set top boxes, base stations, wall adapters, or network applications. Each output is adjustable down to 0.6 V. This IC controls two independent PWM outputs that have 180° phase difference and are capable of driving 6 A load. It also provides a built-in LDO controller that drives a discrete P-channel MOSFET or a PNP transistor in linear mode for up to 1 A current capability.

The SiP12203 also includes, for each PWM output, independent enable, current limit, feed forward compensation and internal soft start functions. A single power good (PG) pin feeds back the regulation status of the 3 outputs. This IC is designed for minimum number of external components.

The SiP12203 incorporates several protection features. An adjustable over current protection circuit monitors the output current by sensing the voltage drop across the low-side MOSFET. The over current hiccup operation protects the DC/DC components from being damaged under overload or short circuit conditions. Other protection features include under voltage lockout, over voltage protection and thermal shutdown.

The SiP12203 is available in a lead (Pb)-free MLP55-28 package and is specified to operate within - 40 °C to 125 °C junction temperature.

FEATURES

- 4.5 V to 18 V input voltage range
- Three independent outputs with adjustable voltages of as low as 0.6 V (2 switching and 1 linear)
- Two switching channels operate with 180° out of phase
- Load current up to 6 A x 2 switching channels and 1 A linear
- > 94 % efficiency
- Drives 5 external MOSFETs
- 500 kHz fixed switching frequency
- The oscillator frequency can be externally synchronized to a range of 6.72 MHz to 9.28 MHz
- Internal soft start
- Voltage feed-forward compensation
- Independent enable pins for switching channels
- Independent adjustable output current limit
- Power good indication with optional output delay
- MLP55-28 package

Pb-free
RoHS COMPLIANT

APPLICATIONS

- DSP, ASIC and FPGA power supplies
- Dual power supply applications: µP and DSP cores, memory and logic I/Os
- Distributed and intermediate bus architectures
- LCD TV and set-top box
- Battery operated equipment
- Telecom

TYPICAL APPLICATION CIRCUIT

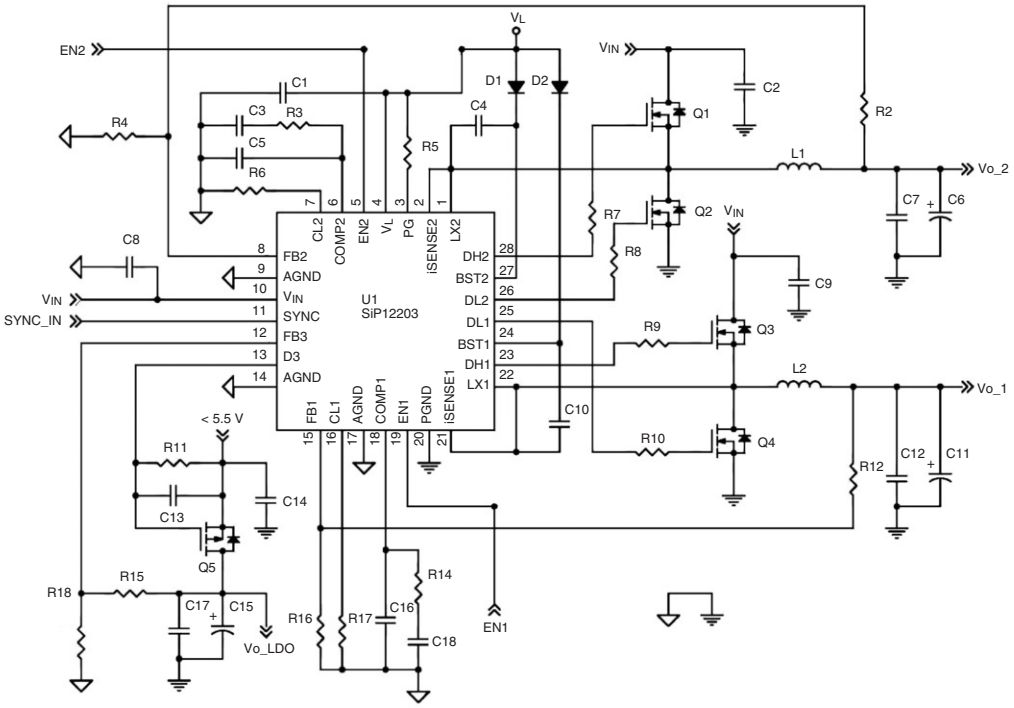


Figure 1.

ABSOLUTE MAXIMUM RATINGS

Parameter	Limit	Unit
V_{IN}, LX and I_{SENSE} to GND	30	V
DH and BST to LX	6	
All Other Pins to GND	- 0.3 to 6	
Thermal Impedance ($R_{\theta JA}$)[a]	36	°C/W
Maximum Junction Temperature	150	°C
Storage Temperature	- 55 to 150	

Notes:
a. Device mounted with all leads soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Limit	Unit
V_{IN}, LX and I_{SENSE} to GND	4.5 to 18	V
DH and BST to LX	3.5 to 5.5	
All other pins to GND	0 to 5.5	
Output Voltage	0.6 to 5	
Operating Junction Temperature	- 40 to 125	°C

ORDERING INFORMATION

Part Number	Temperature	Marking	Package
SiP12203DLP-T1-E3	- 40 °C to 125 °C	12203	PowerPAK MLP55-28

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{IN} = 12 V, T_A = - 40 °C to 85 °C	Limits Min.[a]	Typ.[b]	Max.[a]	Unit
Controller						
Input Voltage	V_{IN}		4.5		18	V
Regulated Voltage	V_L	V_{IN} > 5.6 V, I_L = 20 mA	4.8	5	5.5	
	I_L		60			mA
Oscillator Frequency[a]	f_{OSC}		400	500	600	kHz
Oscillator Ramp Amplitude	ΔV_{OSC}	Oscillator ramp peak to peak voltage		0.095 V_{IN}		V
Oscillator Ramp Offset[b]	V_{OSC_OFS}			0.6		
Output Voltage	V_O		V_{REF}		5	
Sync Frequency Range	f_{SYNC}		6.72	8	9.28	MHz
Sync Input High Level	V_{SYN_H}		0.7 V_L			V
Sync Input Low Level	I_{SYN_L}				0.3 V_L	
Sync Input Current	V_{SYN}	V_L = 5 V		55		µA
Max. Duty Cycle During Soft Start	DC_{SS}			74.5		%
Max. Duty Cycle in Steady State	DC_{NORM}			87		%
Feedback Voltage On FB Pin	V_{FB}	T_A = 25 °C	0.591	0.600	0.609	V
			0.585	0.600	0.615	

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{IN} = 12 V, T_A = - 40 °C to 85 °C	Limits Min.[a]	Typ.[b]	Max.[a]	Unit
PWM Error Amplifier						
Transconductance	GM			2		mA/V
FB Input Bias Current	I_{FB}				100	nA
Reference Voltage	V_{REF}			0.6		V
Soft Start						
Soft Start Period	T_{SOFT}			6.5		ms
Enable						
Low Level (Disable)	V_{EN_L}				0.8	V
High Level (Enable)	V_{EN_H}		2.0			
Supply						
Shutdown Current	I_{SD}	EN1 = EN2 = LOW, PG pull-up resistor is open		10	100	µA
Input Quiescent Current	I_Q	Current flowing into V_{IN} pin, non-switching		2.5		mA
MOSFET Drivers						
Break-Before-Make Time	t_{BBM}			10		ns
Highside Driver (Channel 1 and Channel 2)						
On Resistance	R_{DSPH}	Sourcing, V_{BST} - V_{LX} = 4.5 V		7.8	12	Ω
	R_{DSNH}	Sinking, V_{BST} - V_{LX} = 4.5 V		2.3	4.4	
Rise Time	t_{rH}	V_{BST} - V_{LX} = 4.5 V, C_L = 2.7 nF		51		ns
Fall Time	t_{fH}	V_{BST} - V_{LX} = 4.5 V, C_L = 2.7 nF		15		
Sink/Source Current	I_{DRH}			400		mA
Lowside Driver (Channel 1 and Channel 2)						
On Resistance	R_{DSPL}	Sourcing, V_L = 5 V		2.5	3.9	Ω
	R_{DSNL}	Sinking, V_L = 5 V		1.0	1.8	
Rise Time	t_{rL}	V_L = 5 V, C_L = 2.7 nF		13.4		ns
Fall Time	t_{fL}	V_L = 5 V, C_L = 2.7 nF		5.8		
Sink/Source Current	I_{DRL}			400		mA
LDO Controller						
Drive Sink Current On D3 Pin	I_{D3}		50			mA
FB3 Feedback Voltage	V_{FB3}	Forcing 21 mA into FB3 pin		0.6		V
Output Undervoltage Threshold	PG_{UVLO}	Value for power good logic. Percentage of feedback voltage		74		%
FB3 Input Leakage Current	$FB3_{Lkg}$	EN1 = EN2 = LOW		45	150	nA
Amplifier Transconductance		Forcing 21 mA into FB3 pin. V_{FB3} = 0.6 V		2		A/V
Power Good Function						
PG Low Level Voltage	PG_L	Pull-up resistor = 100 kΩ; V_{IN} > 2.5 V		0.1	0.5	V
PG Leakage Current	PG_{Lkg}				± 1.0	µA
PG Upper Threshold (Channels 1 and 2)	PG_{THH}	Percentage of set point when FB1 or FB2 is rising until PG = 0	105		120	%
PG Lower Threshold (Channels 1 and 2)	PG_{THL}	Percentage of set point when FB1 or FB2 is falling until PG = 0	80		95	
PG for LDO Output	PG_{LDO}	Percentage of set point when FB3 is falling until PG = 0	69	74	79	
PG Hysteresis for LDO	PG_{LDO_HYS}			4		

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{IN} = 12 V, T_A = - 40 °C to 85 °C	Limits Min.[a]	Typ.[b]	Max.[a]	Unit
Protection						
Under Voltage Lockout for V_L	V_{UVLO}	V_L rising		3.6	3.9	
Under Voltage Lockout Hysteresis	$UVLO_{HYS}$	UVLO differential voltage between rising and falling of V_L		0.180		
Thermal Shutdown Threshold	T_{JSD}			165		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		
Over Voltage Trip Threshold	V_{OVTH}	V_O rising with respect to set output voltage	105	110	120	%
Over Voltage Hysteresis	V_{OVHYS}	V_O falling		8		
Hiccup Period		Typical 7 cycles of soft start period		45		ms
Over Current Limit (Channel 1 and Channel 2)						
Current Limit Source Current	I_{CL}			20		µA
Overcurrent Limit Voltage	V_{CL}	R_{CL} = 5 kΩ		100		mV

Notes:
a. Oscillator frequency here means the switching frequency.
b. Oscillator ramp offset is the minimum voltage, at which the COMP pin needs to be charged up before the switching pulses can occur at DL and DH pins.

FUNCTIONAL BLOCK DIAGRAM

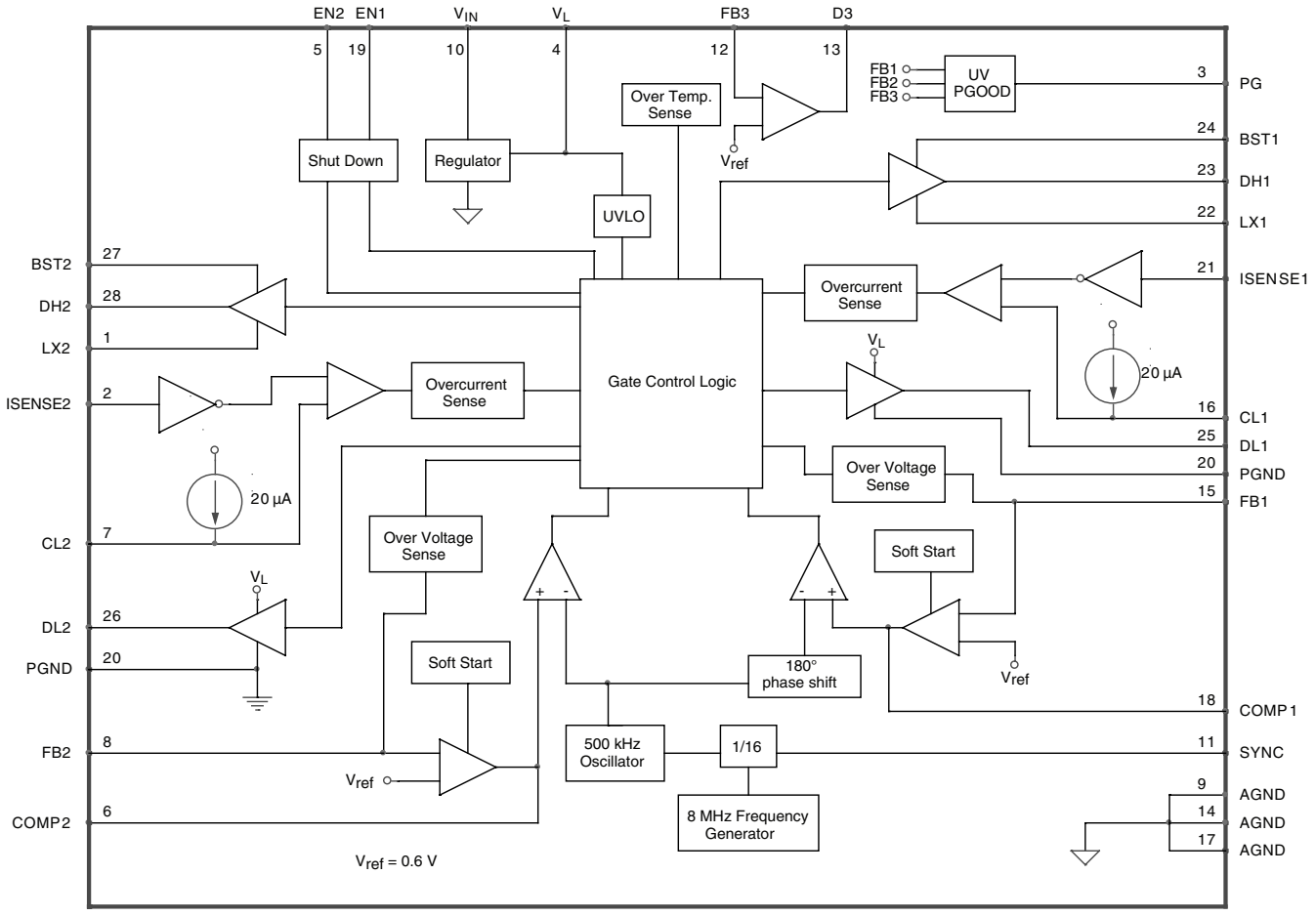


Figure 2.

OPERATIONAL DESCRIPTION

Enable

This chip can enable or shut down the 2 converter channels independently. The EN pins have internally 1 µA pull-up current, which is intended for automatic enable. The channel is enabled when its corresponding EN pin is left floating or pulled above 2.0 V. To ensure a channel is enabled, external pull-up is recommended. The channel is disabled when the pin is dropping below 0.8 V. When both channels are disabled, the voltage at V_L will drop to around 2 V.

Soft Start

Soft start is a channel-level feature. Only when a channel is enabled the soft start procedure associated with that channel can be initiated. After the channel is enabled, the soft start begins when V_L reaches its UVLO and is accomplished by ramping up the internal reference voltage (typical 0.6 V) within 15 steps. During soft start the channel cannot enter fault mode. If there is an over current condition (current limit or short circuit), the high-side MOSFET will be turned off and the low-side MOSFET be turned on. Once the soft start timing elapses, the IC enters a normal state of operation. The typical soft start time is 6.5 ms.

Under Voltage Lockout (UVLO)

The chip enters under voltage lockout mode when V_L is below 3.4 V (typical). In UVLO mode both the 2 channels and LDO controller will be disabled, and high-side MOSFET will be turned off and low-side MOSFET will be turned on. The IC will get out of UVLO mode when V_L is above 3.6 V typical.

Over Voltage Protection

When the output voltage becomes 10 % higher than its set voltage, the device goes into over voltage mode. The device will then force the controller to turn off high-side MOSFET and turn on low-side MOSFET. The IC will keep this state until the output voltage returns to its set point. (That is when the feedback voltage equals the reference voltage.) The controller will then resume normal operation.

Over Current Protection

Independent over current protection on either of the two PWM outputs is provided. The over current situation is detected when low-side MOSFET is turned on. The resistor R_{CL} connected between CL pin and ground sets the current limit and the current limit voltage equals to 20 µA · R_{CL} (typical value of I_{CL} = 20 µA). When low-side MOSFET turns on, the reverse current, equaling to inductor current, I_L, will generate a negative voltage drop through the low-side MOSFET $R_{DS(ON)}$ on I_{SENSE} pin. If the voltage of the I_{SENSE} pin falls below - 20 µA · R_{CL}, the low-side MOSFET will continue to turn on and high-side MOSFET continue to turn off. As soon as the voltage on I_{SENSE} pin is higher than - 20 µA · R_{CL}, the high-side and low-side drivers will switch normally. This is called cycle-by-cycle over current condition. Only cycle-by-cycle over current protection scheme is used during soft start period. After soft start time elapses, the over current condition has to remain for 7 consecutive cycles so that the controller can go into over current fault state. If the over current condition is removed before seven consecutive cycles the controller will revert to normal operation. Since the scheme to detect the current is to sense the low-side MOSFET $R_{DS(ON)}$ voltage drop, the actual current limit has to set to at least 150 % to 180 % of the maximum output current so that the variation of the $R_{DS(ON)}$ and the current limit is covered for all the operating temperature range of the MOSFET and this IC.

Over Current Fault State (Hiccup Mode)

Once the IC enters over current fault mode, any over current situation occurs afterwards will be ignored. In the over current fault state, the low-side MOSFET will be turned on and the high side MOSFET will be turned off. This fault state will last for seven soft start cycles and then the IC will begin to soft start. If there is no over current, the IC will operate normally, otherwise the over current sequence will be repeated.

Over Temperature Protection

When the temperature of the IC reaches 165 °C or above, the IC is in over temperature state. In this situation the high-side MOSFET will be turned off and the low-side MOSFET will be turned on, and only system monitor circuitry will be active. Once the temperature of the IC drops below typical 145 °C, the IC will resume normal operation from soft start.

LDO Controller

The linear regulator controller is a transconductance amplifier with a nominal gain of 2 A/V. This amplifier has no capability of sourcing current. It's capable of sinking a minimum current of 50 mA. The feedback reference voltage is 0.6 V. With zero differential voltage at the amplifier input, the controller sinks 21 mA of current. An external PNP transistor or a P-Ch MOSFET can be used as the pass device. A capacitor and a parallel pull-up resistor between the gate and the source of the P-Ch MOSFET or the base and the emitter of the PNP transistor can form the dominant pole for the compensation loop. For better load transient response, however, the dominant pole is preferred to be placed at the regulator output, with a capacitor to ground. Under no-load conditions, leakage current from the pass device supplies the output capacitors, even when the pass device is off. Generally this is not a problem since the feedback resistor drains the excess charge. However, charge may build up on the output capacitor making the LDO output rise above its set point. Care must be taken to insure that the feedback resistor's current exceeds the pass device leakage current over the entire temperature range. The linear regulator can be powered by either of the 2 channel outputs or external voltage. Since D3 pin has a recommended voltage rating of 5.5 V, the linear regulator supply voltage can thus not be higher than 5.5 V. If one of the 2 channels powers the linear regulator, then during startup the output of the linear regulator will track the input with the voltage differential between the input and the output of the

linear regulator being the load current times the $R_{DS(ON)}$. This is the low drop-out mode. When the supply voltage is higher than the turn-on threshold voltage of the pass device, the regulator will then exit low drop-out mode and stay in regulation mode.

Synchronization

The SYNC pin is used to synchronize the oscillator frequency to an external source in the range of 8 MHz ± 16 %. The oscillator frequency is synchronized to the rising edge of the input signal. The external oscillator/sync signal must sink and source 110 µA to pull the Sync pin low and high, since the SiP12203 has an internal 100K pull down resistor. When not used, connect this pin to an adjacent analog ground pin or leave it open.

Power good (PG)

Power good is a system level feature. PG has an open-drain output so a pull-up resistor is required.

The following truth table shows the relationship between the signals of EN1, EN2, FB1, FB2, FB3 and PG.

TRUTH TABLE

Enable Pins		Feedback Pins			PG
EN1	EN2	FB1	FB2	FB3	
H	H	In regulation	In regulation	In regulation	H
L	H	x	In regulation	In regulation	H
H	L	In regulation	x	In regulation	H
L	L	x	x	x	L
H	L	In regulation	x	Out of regulation	L
L	H	x	In regulation	Out of regulation	L
H	H	Out of regulation	In regulation	In regulation	L
H	H	In regulation	Out of regulation	In regulation	L
H	H	In regulation	In regulation	Out of regulation	L

Notes:

a. H and L mean logic high and low. See specification table for high and low definition

b. "In regulation" means FB pin voltage is in the range specified by PG_{THH}, PG_{THL}, and PG_{LDO}. "Out of regulation" means FB pin voltage is not in the range specified by PG_{THH}, PG_{THL}, and PG_{LDO}. “x” means it does not matter whether the output is regulated or not.

PIN CONFIGURATION AND PACKAGE - MLP55-28

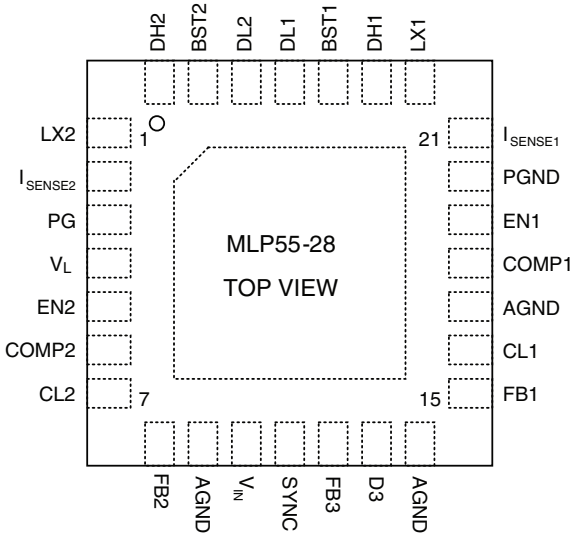


Figure 3.

PIN DESCRIPTION

Pin Number	Name	Function
1	LX2	Switching node of converter 2. Connect to the joint of high-side MOSFET source and low-side MOSFET drain of converter 2
2	I_{SENSE2}	Converter 2 current sense input. Connect to LX2
3	PG	Power Good indicator. See Power Good description for detail
4	V_L	5 V regulated voltage for internal circuitry. A 4.7 µF or higher ceramic decoupling capacitor is required for this pin
5	EN2	Converter 2 enable pin
6	COMP2	Converter 2 compensation connecting pin
7	CL2	Converter 2 current limit setting pin. A resistor connected between this pin and AGND sets converter 2 current limit.
8	FB2	Converter 2 feedback pin. Connect external resistive divider to set output voltage
9	AGND	Analog ground
10	V_{IN}	Input voltage, used to generate V_L
11	SYNC	External frequency synchronization pin. Synchronized on rising edge. When not used, connect it to analog ground
12	FB3	LDO feedback pin. Connect external resistive divider to set LDO voltage
13	D3	LDO P-Ch MOSFET drive signal. Open drain output
14	AGND	Analog ground
15	FB1	Converter 1 feedback pin. Connect external resistive divider to set output voltage
16	CL1	Converter 1 current limit setting pin. A resistor connected between this pin and AGND sets converter 1 current limit
17	AGND	Analog ground
18	COMP1	Converter 1 compensation connecting pin
19	EN1	Converter 1 enable pin
20	PGND	IC power ground
21	I_{SENSE1}	Converter 1 current sense input. Connect to LX1
22	LX1	Switching node of converter 1. Connect to the joint of high-side MOSFET source and low-side MOSFET drain of converter 1
23	DH1	Converter 1 high-side gate drive
24	BST1	Bootstrap voltage for converter 1 high-side MOSFET driver. Connect a 0.1 µF or greater capacitor between LX1 to BST1
25	DL1	Converter 1 low-side gate drive
26	DL2	Converter 2 low-side gate drive
27	BST2	Bootstrap voltage for converter 2 high-side MOSFET driver. Connect a 0.1 µF or greater capacitor between LX2 to BST2
28	DH2	Converter 2 high-side gate drive

APPLICATION INFORMATION

Startup Circuit

What is a startup circuit? Why is it needed? To answer this question, let us take a look at an application example.

V_{IN}: 12 V

V_O: 5 V

EN is pulled up to V_L through a 100k resistor.

After input power supply is turned on, V_{IN} starts to ramp up and V_L ramps up at the same rate as V_{IN} (but will stop at its regulated voltage, typical 5 V). As soon as V_L exceeds UVLO (typical 3.6 V), the converter is enabled, soft start cycle is initiated and V_{REF} starts to step up from 0 V to 0.6 V within 6.5 ms typically, for 15 steps. Since the fault mode is blocked from occurring in the soft start period, the converter can not enter hiccup mode. This guarantees that the system smoothly starts up into normal operation.

After soft start finishes, if V_{IN} has not reached a value that satisfies $V_O/V_{IN} < D_{MAX}$ = 87.5 %, (for example, V_{IN} = 13 V after soft start is done, then V_O/V_{IN} = 12/13 = 92 % > 87.5 %), then the output voltage will collapse until V_{IN} gets higher. Further more, if at any moment $V_O/V_{IN} \geq 87.5$ % and the load is light enough, then for low-side MOSFET ON time less than 12.5 % of period (= 250 ns), LX may not be discharged low enough, therefore causing boot capacitor not be able to be charged high enough and further causing high-side MOSFET not be able to be turned back on. This will then result in system hanging. To prevent this condition, an external startup circuit is recommended.

The following diagram shows the circuit. Q1A and Q1B can be a dual N-Channel MOSFET, like Vishay Siliconix's Si1972DH. The voltage of the Zener diode D1 is chosen around or higher than the output voltage. R1 provides bias current for D1. The criteria to choose R2 and R3 are (1) the voltage on Q1B gate is not higher than its V_{GS} rating (for Si1972DH, V_{GS} = ± 20 V) and (2) the total current flowing through R2 and R3 should be as small as possible. R4 can be a resistor with a value between 100k and 1M.

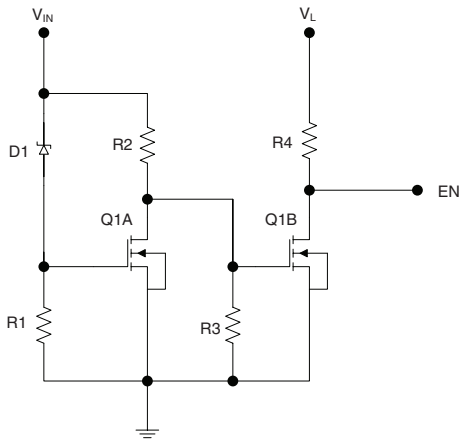
With this circuit in place, the converter will start up normally and not cause any system hanging. For above mentioned application example, the following parts can be used:

D1 - a 4.7 V to 6.8 V Vishay's BZX84V series Zener diode

R1 - 3 kΩ to 5 kΩ

R2, R3, R4 - 100 kΩ

Q1 - Si1972DH (Dual MOSFET)



Inductor Selection

The inductor is one of the energy storage components in a converter. Choosing an inductor means specifying its size, structure, material, inductance, saturation level, DC-resistance (DCR), and core loss. Fortunately, there are many inductor vendors that offer wide selections with ample specifications and test data, such as Vishay Dale.

The following are some key parameters that users should focus on. In PWM mode, inductance has a direct impact on the ripple current. Assuming 100 % efficiency, the steady state peak-to-peak inductor (L) ripple current (I_{PP}) can be calculated as

$$I_{PP} = \frac{V_O \bullet (V_{IN} - V_O)}{V_{IN} \bullet L \bullet f}$$

where f = switching frequency.

Higher inductance means lower ripple current, lower rms current, lower voltage ripple on both input and output, and higher efficiency, unless the resistive loss of the inductor dominates the overall conduction loss. However, higher inductance also means a bigger inductor size and a slower response to transients. For fixed line and load conditions, higher inductance results in a lower peak current for each pulse, a lower load capability, and a higher switching frequency. The saturation level is another important parameter in choosing inductors. Note that the saturation levels specified in datasheets are maximum currents. For a dc-to-dc converter operating in PWM mode, it is the maximum peak inductor (I_{PK}) current that is relevant, and can be calculated using these equations:

$$I_{PK} = I_O + \frac{I_{PP}}{2}$$

where I_O = output current

This peak current varies with inductance tolerance and other errors, and the rated saturation level varies over temperature. So a sufficient design margin is required when choosing current ratings. A high-frequency core material, such as ferrite, should be chosen, the core loss could lead to serious efficiency penalties. The DCR should be kept as low as possible to reduce conduction losses.

Input Capacitor Selection

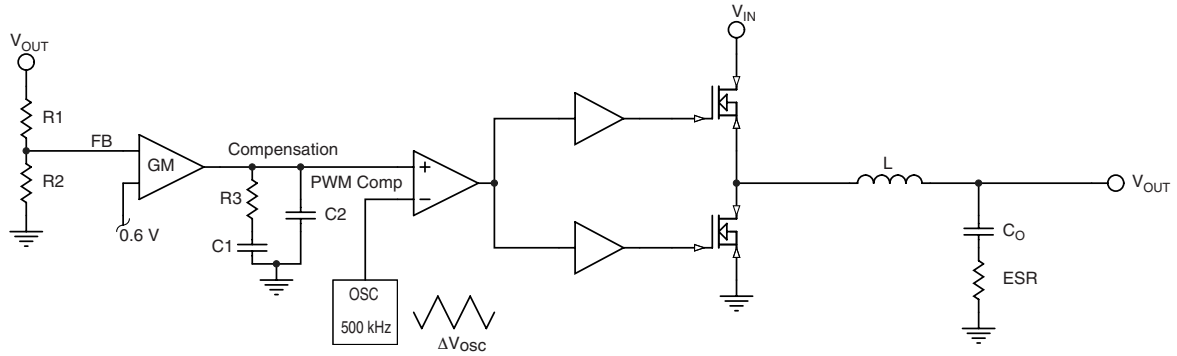
To minimize input voltage ripple caused by the step-down conversion, and interference of large voltage spikes from other circuits, a low-ESR input capacitor is required to filter the input voltage. The input capacitor should be rated for the maximum RMS input current of:

$$I_{RMS} = I_{O.MAX} \sqrt{\frac{V_O}{V_{IN}} \left(1 - \frac{V_O}{V_{IN}}\right)}$$

It is common practice to rate for the worst-case RMS ripple that occurs when the duty cycle is at 50 %:

$$I_{RMS} = \frac{I_{O.MAX}}{2}$$

Compensation



The SiP12203 uses voltage mode control in conjunction with a high frequency transconductance error amplifier. The voltage feedback loop is compensated at the COMP pin, which is the output node of the error amplifier. The feedback loop is generally compensated with an RC + C (one pole, one zero) network from COMP to AGND. Loop stability is affected by the values of the inductor, the output capacitor, the output capacitor ESR, and the error amplifier compensation network.

The ideal bode plot for a compensated system would be gain that rolls off at a slope of - 20 dB/decade, crossing 0 dB at the desired bandwidth and a phase margin greater than 90° for all frequencies below the 0 dB crossing.

Output Capacitor Selection

The output capacitor affects output voltage ripple due to 2 reasons: the capacitance and the effective series resistance (ESR). The selection of the output capacitor is primarily determined by the capacitor ESR required minimizing voltage ripple and current ripple. The relationship between output ripple · V_O, capacitance C_O and its ESR is:

$$\Delta V_O = I_{PP} \bullet \left(ESR + \frac{1}{8 \bullet f \bullet C_O} \right)$$

Multiple capacitors placed in parallel may be needed to meet the ESR requirements. However if the ESR is too low it may cause stability problems.

MOSFET Selection

The key selection criteria for the MOSFETs include maximum specifications of on-resistance, drain source voltage, gate source voltage and current, and total gate charge Q_G. The voltage ratings are fairly straightforward. It is important to carefully balance on-resistance and gate charge. In typical MOSFETs, the lower the on-resistance, the higher the gate charge. The power loss of a MOSFET consists of conduction loss, gate charge loss and crossover loss. For lower-current applications, gate charge loss becomes a significant factor. In this case low gate charge MOSFETs, such as Vishay Siliconix's LITTLE FOOT family devices, are desirable.

The compensation network used with the error amplifier must provide enough phase margin at the 0 dB crossover frequency for the overall open-loop transfer function to be stable. The following guidelines will calculate the compensation pole and zero to stabilize the SiP12203.

The inductor and output capacitor values are usually determined by efficiency, voltage and current ripple requirements. The inductor and the output capacitor create a double pole and a - 180° phase change at the frequency of:

$$f_{P(LC)} = \frac{1}{2\pi \sqrt{L \bullet C_O}}$$

The ESR of the output capacitor and the output capacitor value form a zero at the frequency of:

$$f_{Z(ESR)} = \frac{1}{2\pi \bullet ESR \bullet C_O}$$

$f_{Z(ESR)}$ is typically higher than $f_{P(LC)}$ and gives a 90° phase boost. R3 and C1 will establish a second zero at the frequency of $f_{Z(COMP)}$ in the compensation system. The frequency of this zero should be two times lower than the double pole frequency of $f_{P(LC)}$.

$$f_{Z(COMP)} = \frac{1}{2\pi \bullet R_3 \bullet C_1}$$

Choose a value for R3 usually between 1 kΩ and 10 kΩ. This second zero will provide the second 90° phase boost and will stabilize the closed loop system. R3 and C2 will create a second pole at the frequency of $f_{P(COMP)}$ and this pole should be placed at ½ the switching frequency.

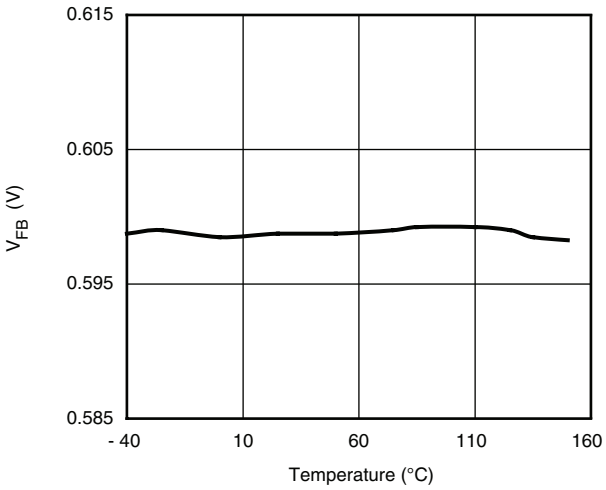
$$f_{P(COMP)} = \frac{1}{2\pi \bullet R_3 \bullet C_2}$$

Although a mathematical approach to frequency compensation can be used, the added complication of input and/or output filters, unknown capacitor ESR, and gross operating point changes with input voltage, load current variations, all suggest a more practical empirical method. This can be done by injecting at the load a variable frequency small signal voltage between the output and feedback network and using an RC network box to iterate toward the final values; or by obtaining the optimum loop response using a network analyzer to measure the loop gain and phase.

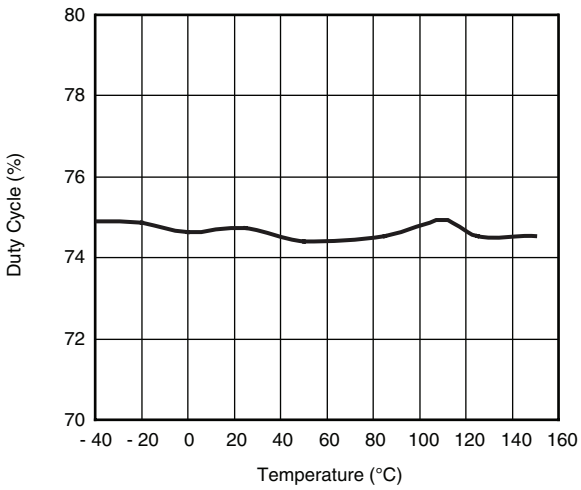
Layout

As in the design of any switching DC-to-DC converter, driver careful layout will ensure that there is a successful transition from design to production. One of the few drawbacks of switching DC-to-DC converters is the noise induced by their high-frequency switching. Parasitic inductance and capacitance may become significant when a converter is switching at 500 kHz. However, noise levels can be minimized by properly laying out the components. Here are some general guidelines for laying out a step-down converter with the SiP12203. Since power traces in step down converters carry pulsating current, energy stored in trace inductance during the pulse can cause high-frequency ringing with input and output capacitors. Minimizing the length of the power traces will minimize the parasitic inductance in the trace. The same pulsating currents can cause voltage drops due to the trace resistance and cause effects such as ground bounce. Increasing the width of the power trace, which increases the cross sectional area, will minimize the trace resistance. In all DC-to-DC converters the decoupling capacitors should be placed as close as possible to the pins being decoupled to reduce the noise. The connections to both terminals should be as short as possible with low-inductance (wide) traces. In the SiP12203 converters, the V_{IN} is decoupled to PGND. It may be necessary to decouple V_L to AGND, with the decoupling capacitor being placed adjacent to the pin. AGND and PGND traces should be isolated from each other and only connected at a single node such as a "star ground".

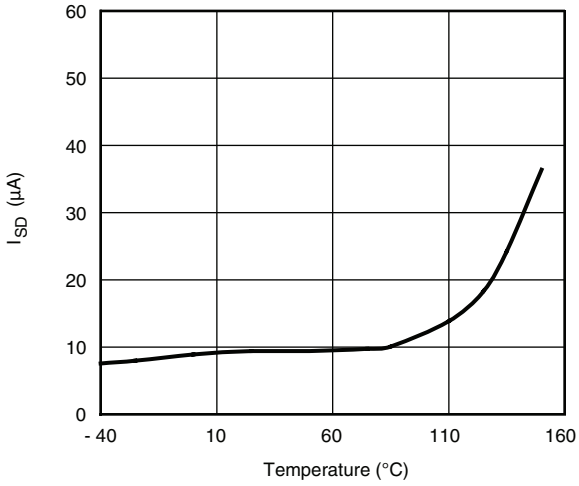
TYPICAL CHARACTERISTICS



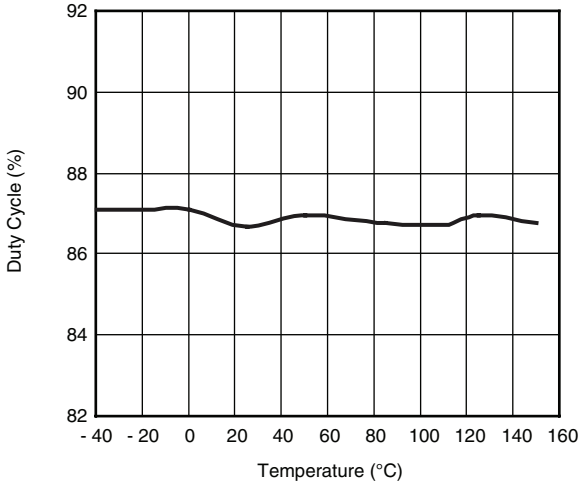
Feedback Voltage V_{FB} vs. Temperature



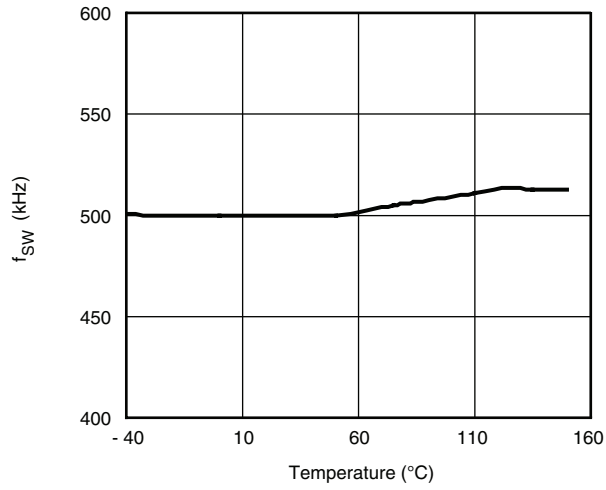
Max. Duty Cycle vs. Temperature in Soft Start Mode



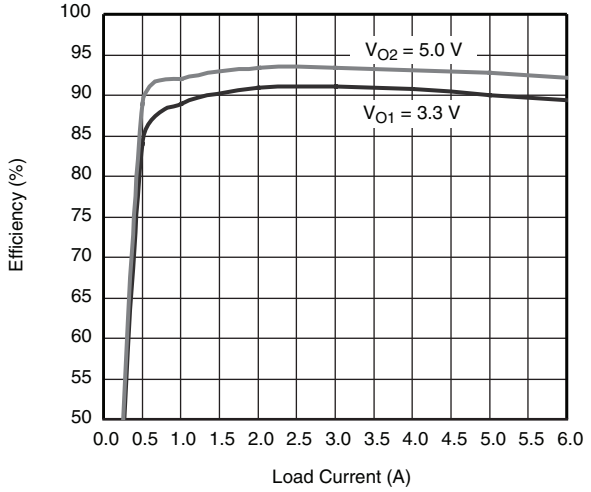
Shutdown Current I_{SD} vs. Temperature



Max. Duty Cycle vs. Temperature in Steady State Mode

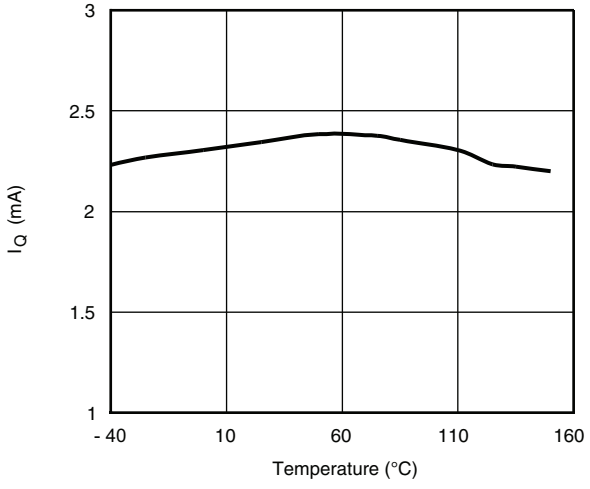


Switching Frequency f_{SW} vs. Temperature

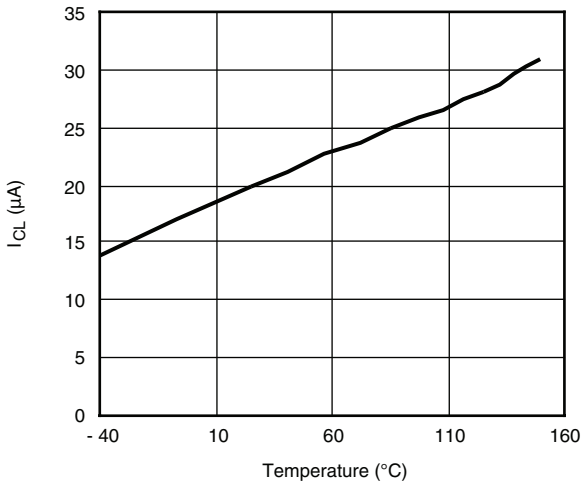


Efficiency vs. Load Current at V_{IN} = 12 V

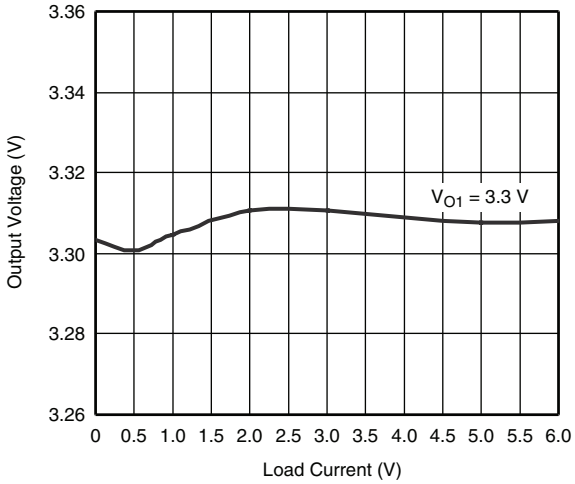
TYPICAL CHARACTERISTICS



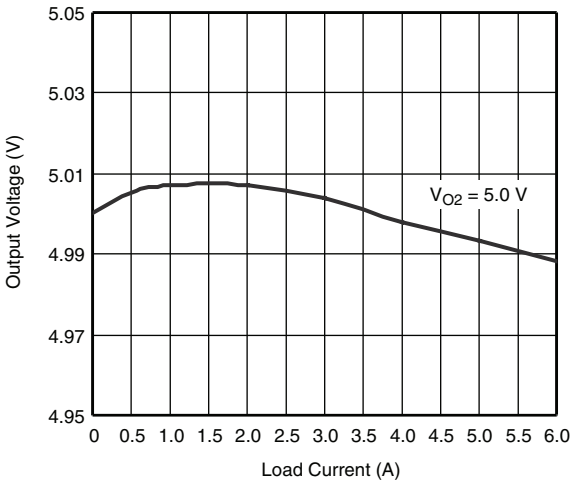
Quiescent Current I_Q vs. Temperature



Current Limit I_{CL} vs Temperature

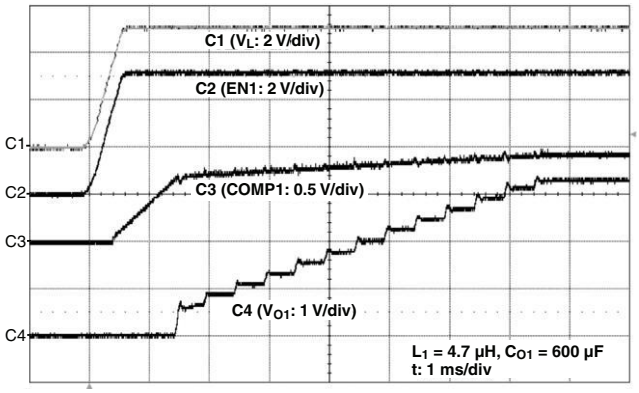


Channel 1 Load Regulation

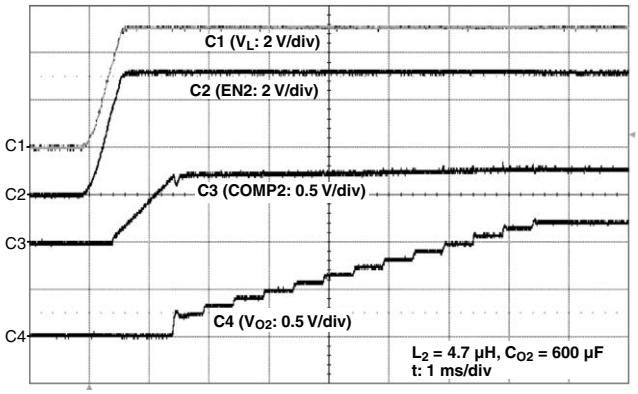


Channel 2 Load Regulation

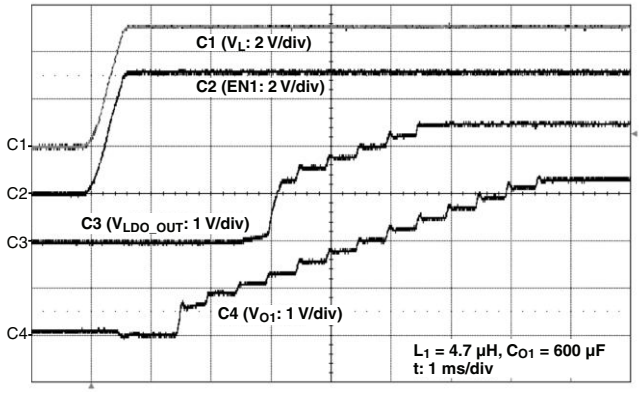
TYPICAL WAVEFORMS



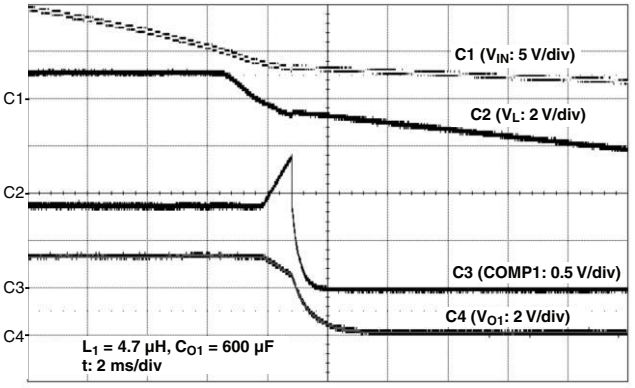
Channel 1 Startup



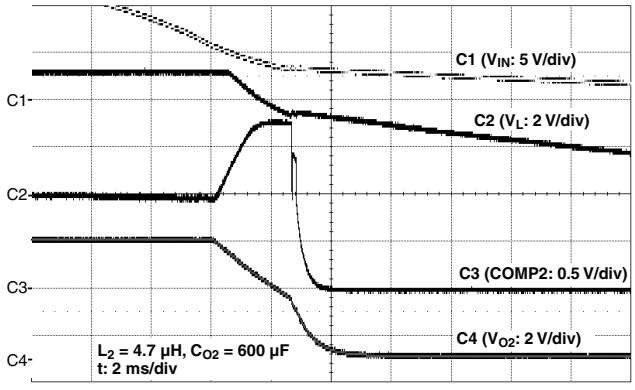
Channel 2 Startup



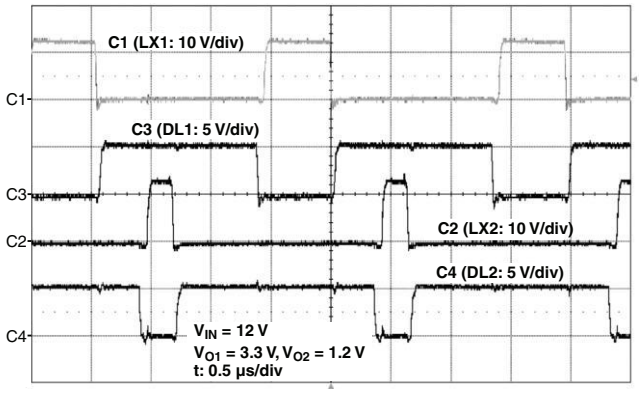
LDO Startup when Powered by Channel 1



Channel 1 Shutdown

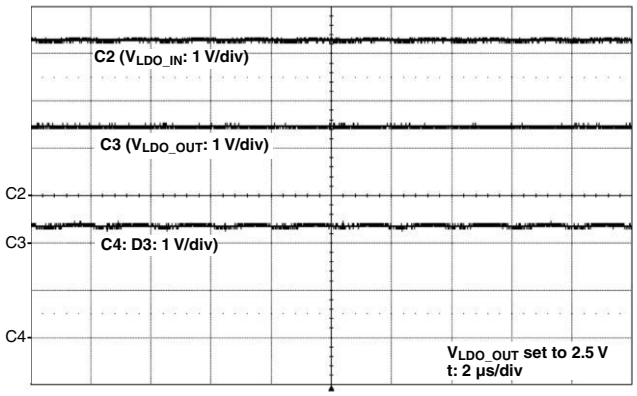


Channel 2 Shutdown

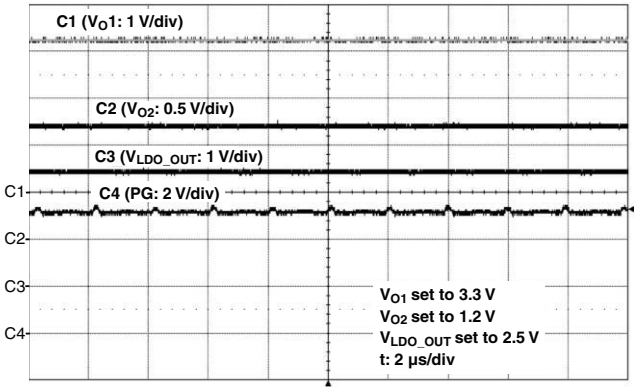


Steady State Switching

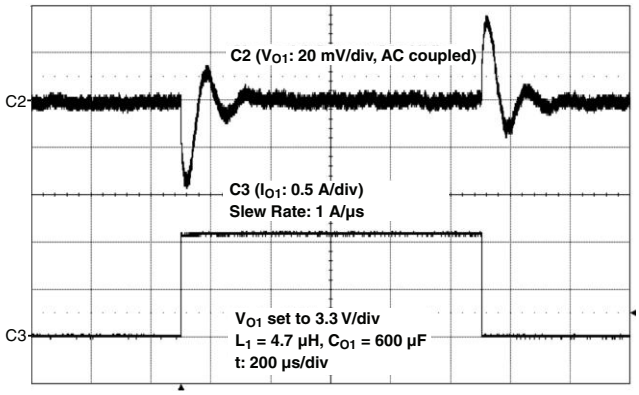
TYPICAL WAVEFORMS



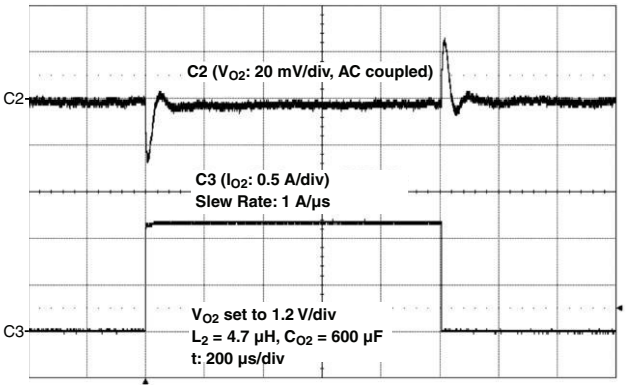
LDO Steady State



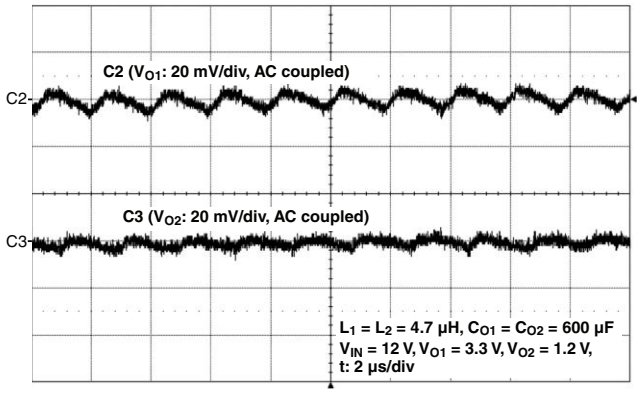
Power Good



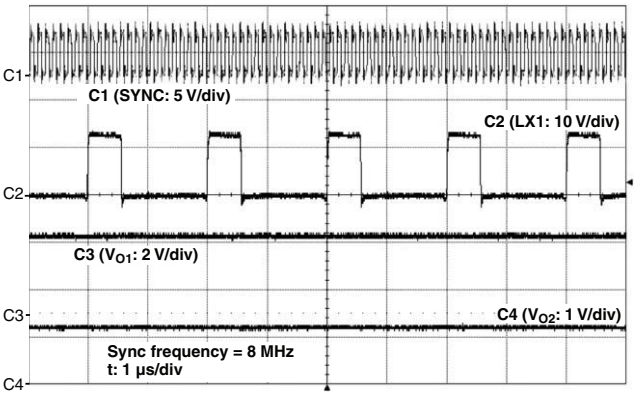
Channel 1 Transient Response



Channel 2 Transient Response

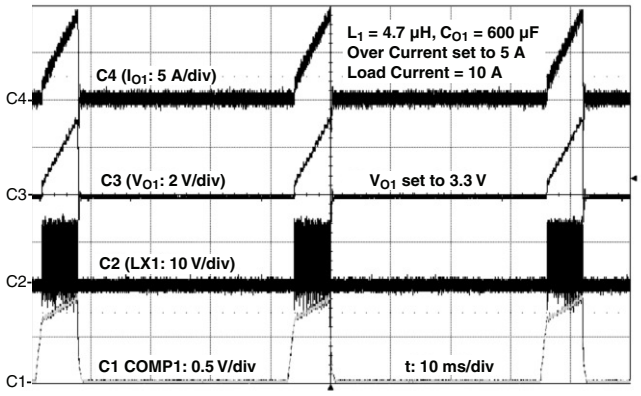


Output Ripple

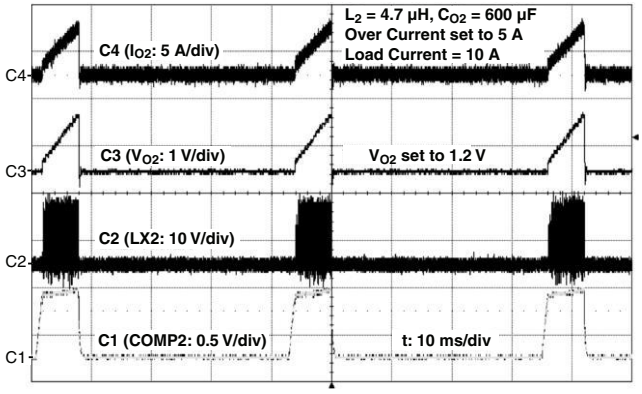


Frequency Synchronization at 8 MHz

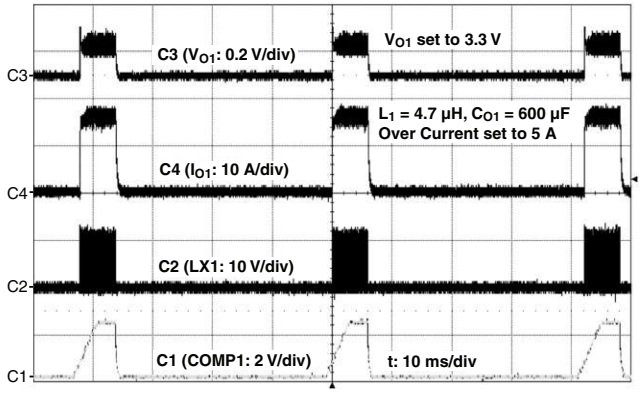
TYPICAL WAVEFORMS



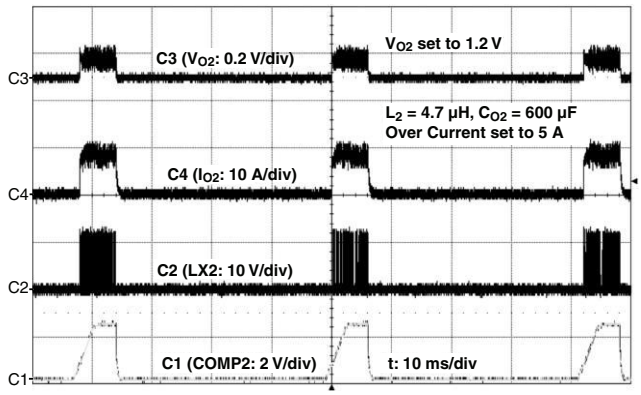
Channel 1 Over Current Protection



Channel 2 Over Current Protection



Channel 1 Short Circuit Protection



Channel 2 Short Circuit Protection

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