National Semiconductor

PRELIMINARY
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LMH1981
Multi-Format Video Sync Separator

General Description

The LMH1981 is a high performance multi-format sync separator ideal for use in a wide range of video applications, such as broadcast and professional video equipment and HDTV/DTV systems.

The input accepts standard analog SD/ED/HD video signals with either bi-level or tri-level sync, and the outputs provide all of the critical timing signals in CMOS logic, including Composite, Horizontal, and Vertical Syncs, Burst/Back Porch Timing, Odd/Even Field, and Video Format Outputs. HSync features very low jitter on its leading (falling) edge, minimizing external circuitry needed to clean and reduce jitter in subsequent clock generation stages.

The LMH1981 automatically detects the input video format, eliminating the need for programming using a microcontroller, and applies precise 50% sync slicing to ensure accurate sync extraction at O_H, even for inputs with irregular amplitude from improper termination or transmission loss. Its unique Video Format Output conveys the total horizontal line count per field as an 11-bit binary serial data stream, which can be decoded by the video system to determine the input video format and enable dynamic adjustment of system parameters, i.e.: color space or scaler conversions. The LMH1981 is available in a 14-pin TSSOP package and operates over a temperature range of –40˚C to +85˚C.

Features

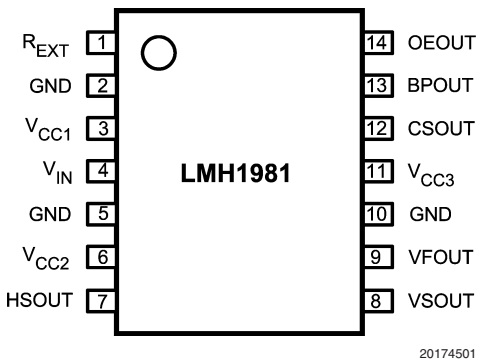
- Standard analog video sync separation for NTSC, PAL, SECAM, 480I/P, 576I/P, 720P, and 1080I/P/PsF from Composite Video (CVBS), S-Video (Y/C), and Component Video (YP_BP_R/GBR) interfaces
- Bi-level & tri-level sync compatible
- Composite, Horizontal, and Vertical Sync Outputs
- Burst/Back Porch Timing, Odd/Even Field, and Video Format Outputs
- Superior jitter performance on leading edge of HSync
- Automatic video format detection
- 50% sync slicing for video inputs from 0.5 V_{PP} to 2 V_{PP}
- Macrovision compatible
- 3.3V to 5V supply operation

Applications

- Broadcast and Professional Video Equipment
- HDTV/DTV Systems
- Genlock Circuits
- Video Capture Devices
- Set-Top Boxes (STB) & Digital Video Recorders (DVR)
- Video Displays

Connection Diagram

14-Pin TSSOP



Top View

FIGURE 1. Pinout

Pin Descriptions

Pin No.	Pin Name	Pin Description
1	R_{EXT}	Bias Current External Resistor
2, 5, 10	GND	Ground
3, 6, 11	V_{CC}	Supply Voltage
4	V_{IN}	Video Input
7	HSOUT	Horizontal Sync Output
8	VSOUT	Vertical Sync Output
9	VFOUT	Video Format Output
12	CSOUT	Composite Sync Output
13	BPOUT	Burst/Back Porch Timing Output
14	OEOUT	Odd/Even Field Output

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
14-Pin TSSOP	LMH1981MT	LMH1981MT	94 Units/Rail	MTC14
	LMH1981MTX		2.5k Units Tape and Reel	

Absolute Maximum Ratings (Notes 1, 7)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	3.5 kV
Machine Model	350V
Supply Voltage V_S,	0V to 5.5V
Video Input, V_{IN}	−0.3V to V_S + 0.3V
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (soldering 10 sec.)	300˚C
Junction Temperature (T_{JMAX}) (Note 3)	+150˚C
Thermal Resistance (θ_{JA})	52˚C/W

Operating Ratings (Note 1)

Temperature Range	−40˚C to +85˚C
V_S	3.3V to 5V
V_{IN}	0V to V_{CC}

Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for T_A = 25˚C, V_S = V_{CC1} = V_{CC2} = V_{CC3} = 3.3V, R_{EXT} = 10 kΩ 1%. **Boldface** limits apply at the temperature extremes. See *Figure 2* for Test Circuit.

Symbol	Parameter	Conditions		Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_{CC}	Supply Current	No input signal	V_{CC} = 3.3V		8		mA
			V_{CC} = 5V		9		
Video Input Specifications							
$V_{IN-AMPL}$	Input Video Amplitude	Amplitude from negative sync tip to maximum video level (Note 8)		0.5	1.0	2.0	V_{PP}
$V_{IN-SYNC}$	Input Sync Amplitude	Amplitude from negative sync tip to video blanking level for both bi-level and tri-level sync inputs (Note 8)		140	300	600	mV_{PP}
$V_{IN-CLAMP}$	Input Sync Tip Clamp Level						V
$V_{IN-SLICE}$	Input Sync Slice Level	Level between video blanking & sync tip for SD/EDTV and between negative & positive sync tips for HDTV			50		%
Logic Output Specifications							
V_{OL}	Output Logic 0				0		V
V_{OH}	Output Logic 1		V_{CC} = 3.3V		3.3		V
			V_{CC} = 5V		5.0		
$T_{SYNC-LOCK}$	Sync Lock Period	Start-up period after a significant change to the input signal before the LMH1981 outputs are accurate					
	Composite Sync Output	See *Figures 9, 10* for SDTV, EDTV & HDTV Horizontal Interval Timing					
	Horizontal Sync Output	See *Figures 9, 10*					
	Burst/Back Porch Clamp Output	See *Figures 9, 10*					
T_{VSOUT}	Vertical Sync Output Pulse Width	See *Figures 3, 4, 5, 6, 7, 8* for SDTV, EDTV & HDTV Vertical Interval Timing			3		H periods
	Odd/Even Field Output	See *Figures 3, 4, 5, 6, 7, 8*					
	Video Format Output	See *Figures 12, 13, 14*					

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)

Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 4: Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

Note 5: Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 6: Limits are 100% production tested at 25˚C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

Note 7: All voltages are measured with respect to GND, unless otherwise specified.

Note 8: $V_{IN-AMPL}$ plus $V_{IN-CLAMP}$ should not exceed V_S.

Note 9: Outputs are negative-polarity logic signals, except for composite sync, odd/even field, and video format outputs.

LMH1981 Test Circuit

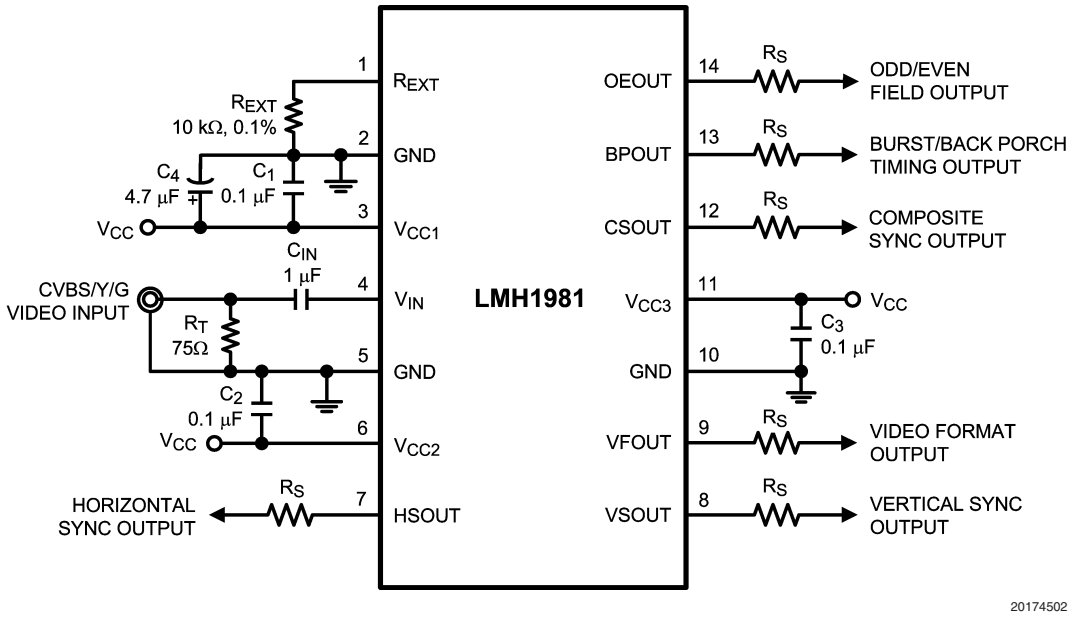


FIGURE 2. Test Circuit

The LMH1981 test circuit is shown in *Figure 2*. The video generator should provide a low-noise, broadcast-quality signal over 75Ω coaxial cable which should be impedance-matched with a 75Ω load termination resistor to prevent unwanted signal distortion. The output waveforms should be monitored using a low-capacitance probe on an oscilloscope with at least 500 MHz bandwidth. See the **PCB LAYOUT CONSIDERATIONS** section for more information about signal and supply trace routing and component placement.

SDTV Vertical Interval Timing (NTSC, PAL SECAM, 480I, 576I)

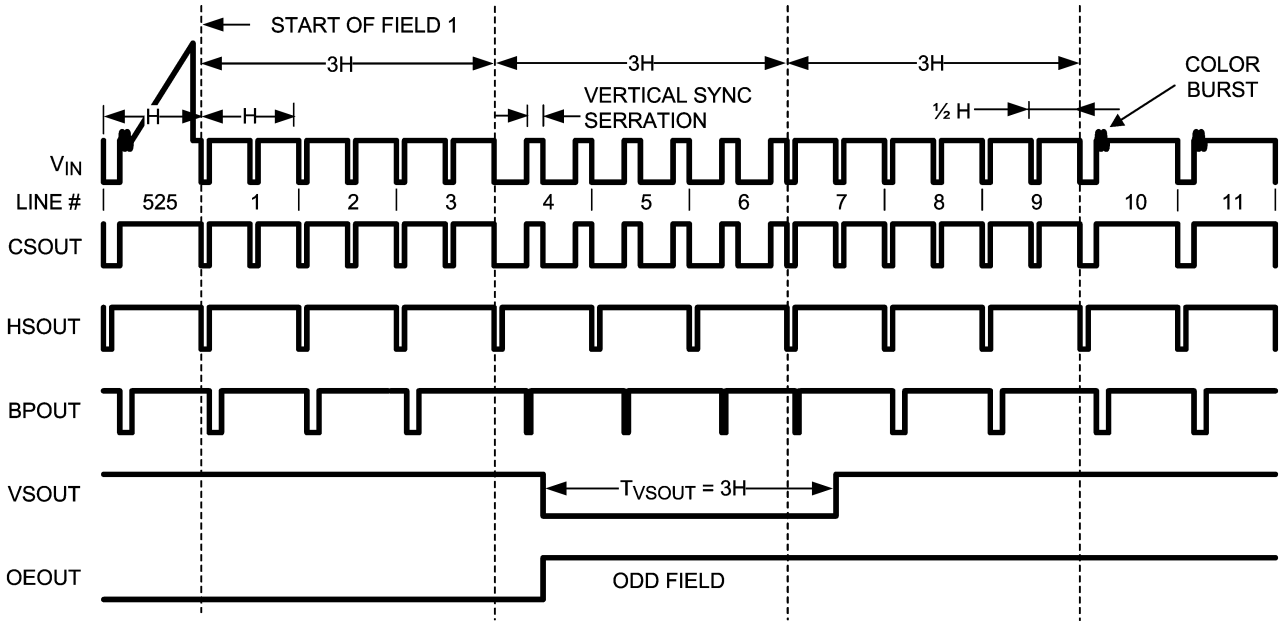


FIGURE 3. NTSC Odd Field Vertical Interval

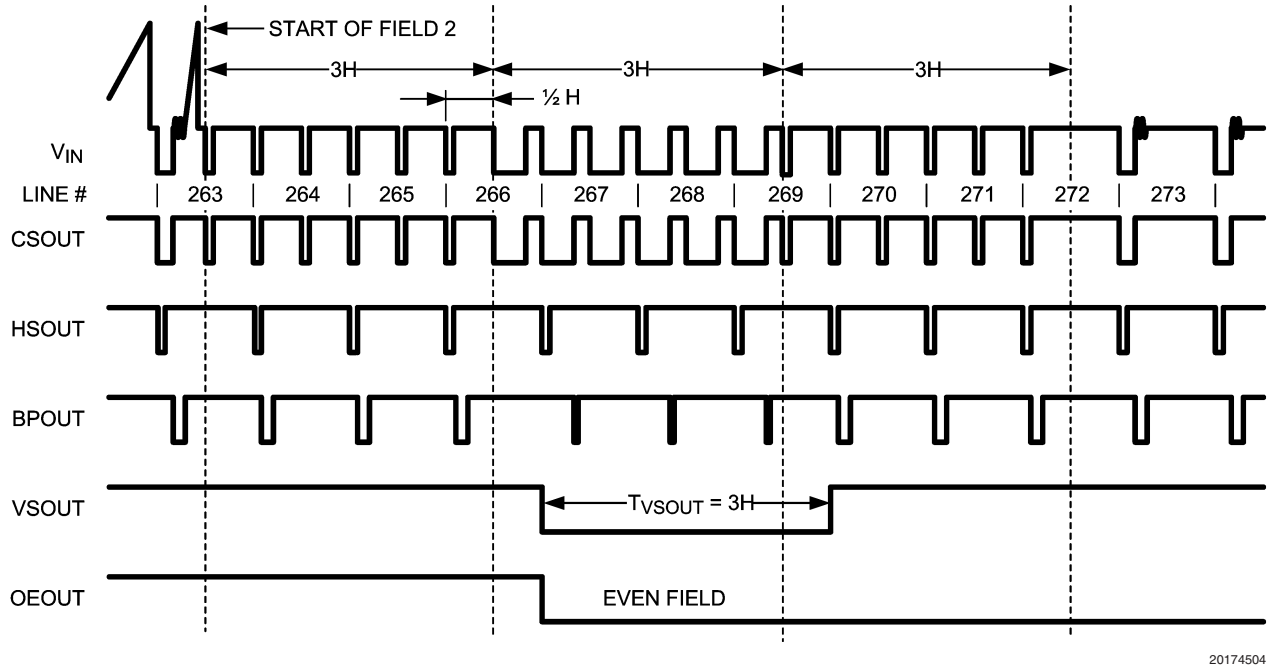


FIGURE 4. NTSC Even Field Vertical Interval

EDTV Vertical Interval Timing (480P, 576P)

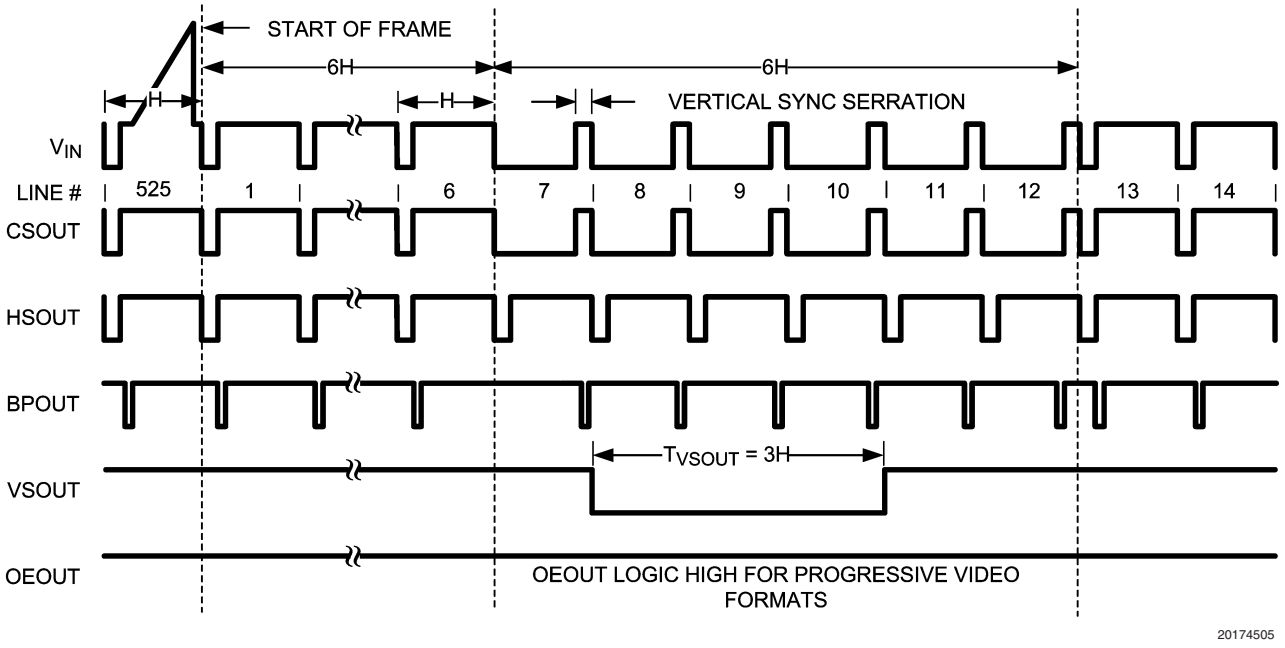


FIGURE 5. 480P Vertical Interval

HDTV Vertical Interval Timing (720P, 1080P)

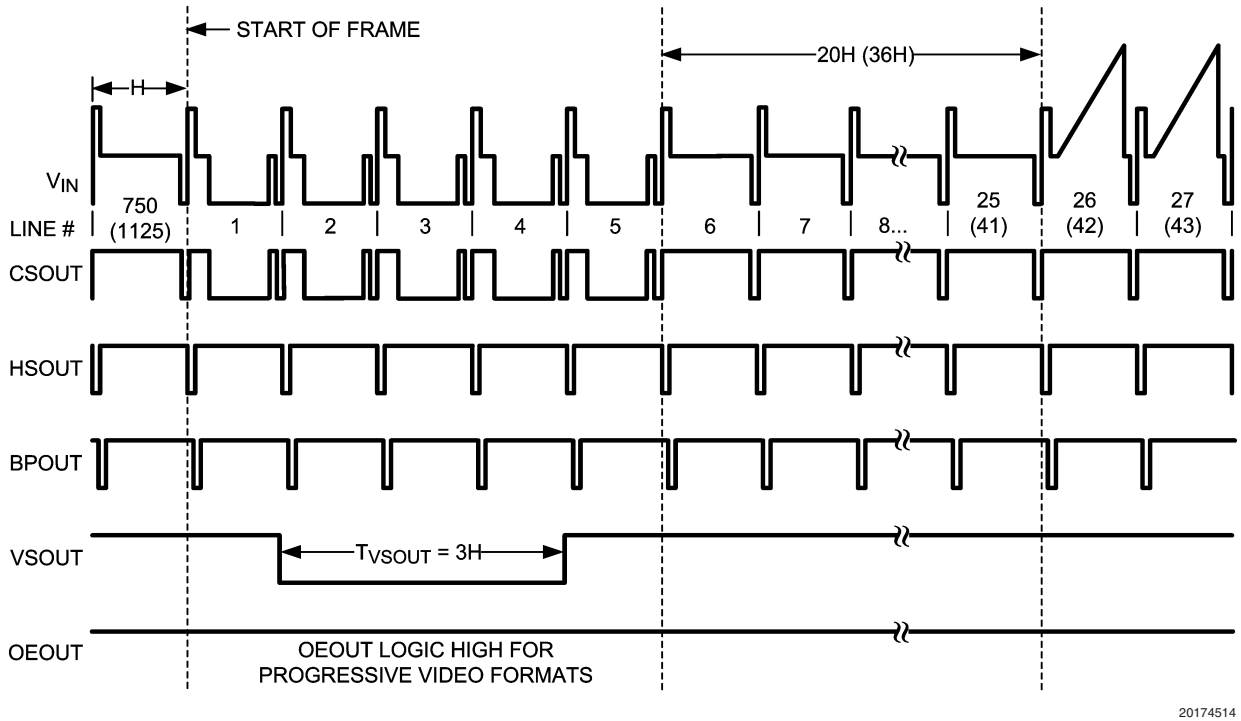


FIGURE 6. 720P (1080P) Vertical Interval

HDTV Vertical Interval Timing (1080I)

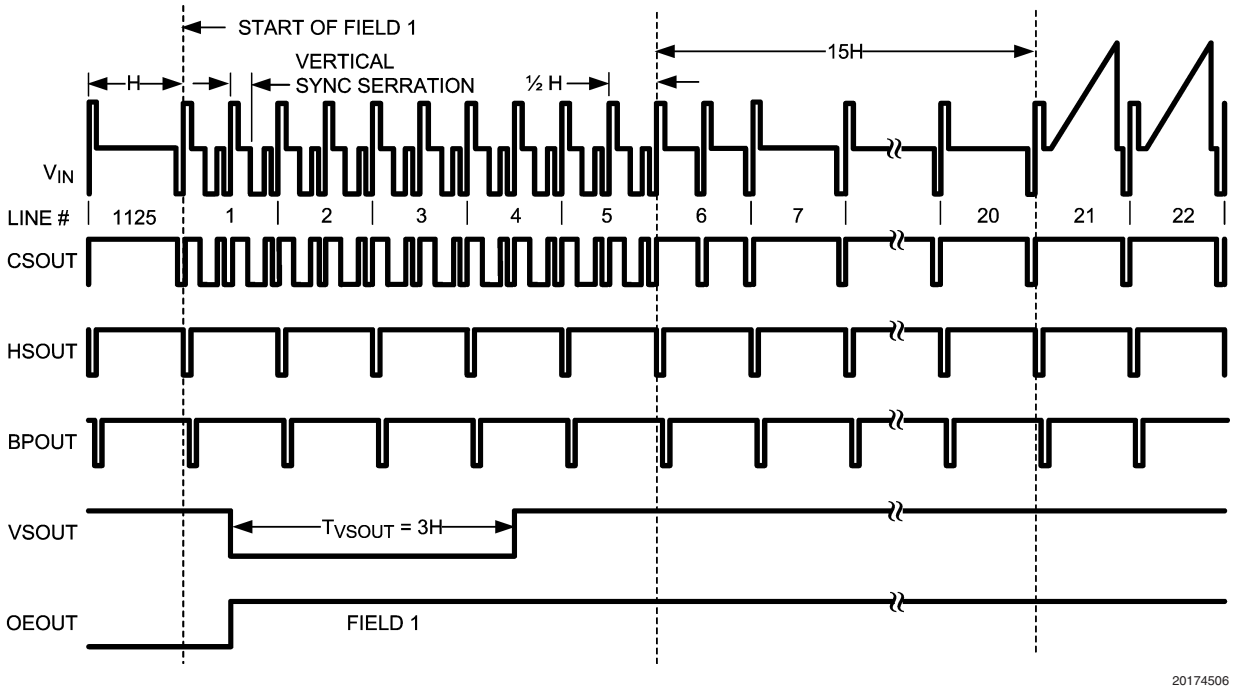


FIGURE 7. 1080I Field 1 Vertical Interval

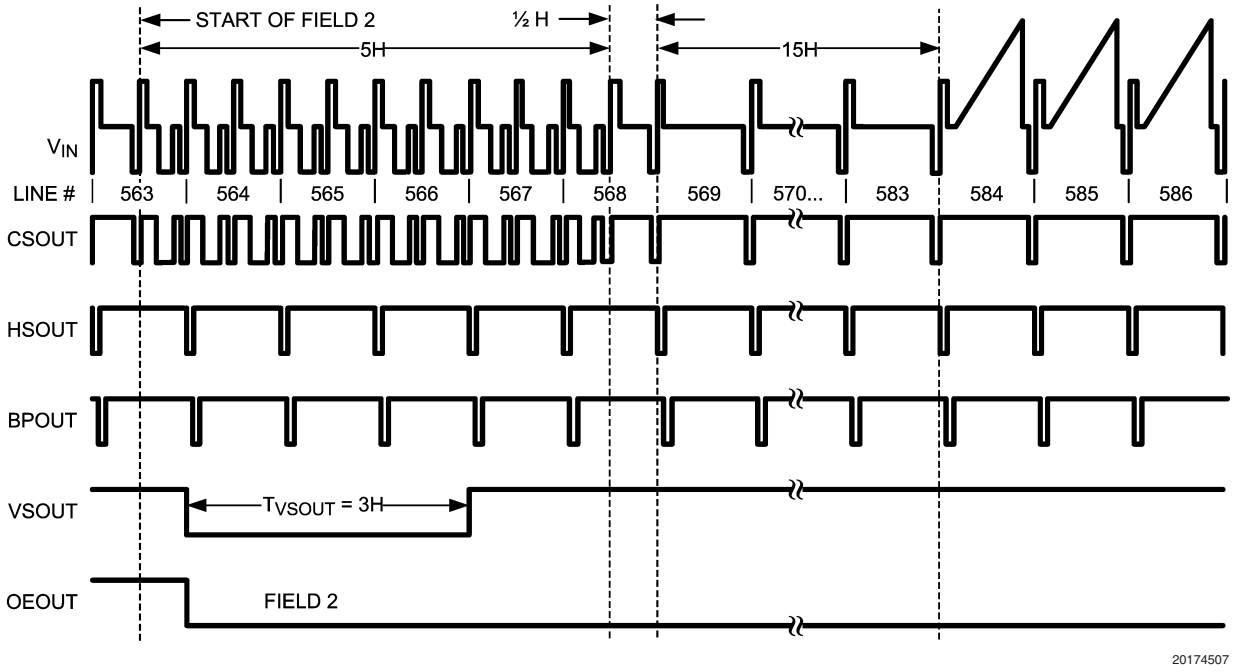


FIGURE 8. 1080I Field 2 Vertical Interval

SD/EDTV Horizontal Interval Timing

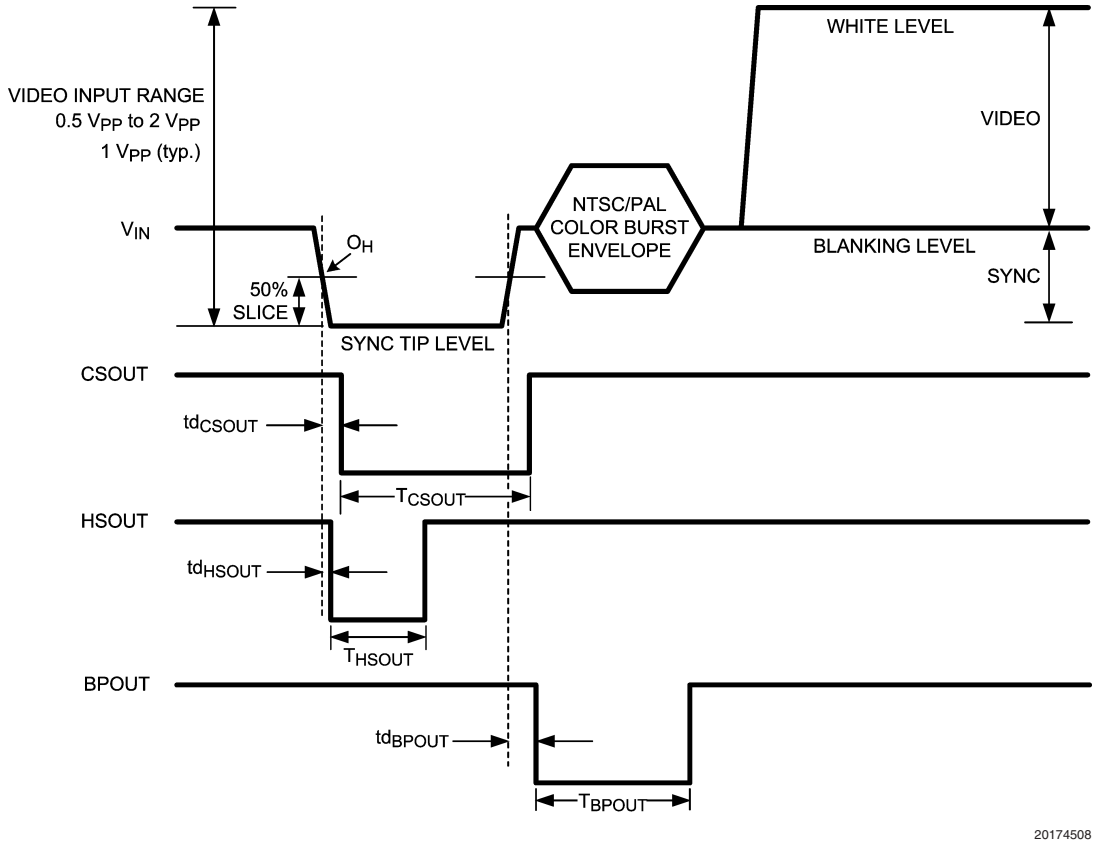


FIGURE 9. SD/EDTV Horizontal Interval with Bi-level Sync

SDTV Horizontal Interval Timing Characteristics (NTSC, PAL, SECAM, 480I, 576I)

Symbol	Parameter	Conditions	Typ	Units
td_{CSOUT}	Composite Sync Output Propagation Delay from Input Sync Reference (O_H)	See *Figure 9*	425	ns
td_{HSOUT}	Horizontal Sync Output Propagation Delay from Input Sync Reference (O_H)	See *Figure 9*	40	ns
td_{BPOUT}	Burst/Back Porch Timing Output Propagation Delay from Input Sync Trailing Edge	See *Figure 9*	315	ns
T_{HSOUT}	Horizontal Sync Output Pulse Width	See *Figure 9*	2.49	µs
T_{BPOUT}	Burst/Back Porch Timing Output Pulse Width	See *Figure 9*	3.2	µs

Note: Delay variation less than **TBD** ns over 0˚C to 70˚C temperature range.

EDTV Horizontal Interval Timing Characteristics (480P, 576P)

Symbol	Parameter	Conditions	Typ	Units
td_{CSOUT}	Composite Sync Output Propagation Delay from Input Sync Reference (O_H)	See *Figure 9*	375	ns
td_{HSOUT}	Horizontal Sync Output Propagation Delay from Input Sync Reference (O_H)	See *Figure 9*	30	ns
td_{BPOUT}	Burst/Back Porch Timing Output Propagation Delay from Input Sync Trailing Edge	See *Figure 9*	575	ns
T_{HSOUT}	Horizontal Sync Output Pulse Width	See*Figure 9*	2.34	µs
T_{BPOUT}	Burst/Back Porch Timing Output Pulse Width	See *Figure 9*	630	ns

Note: Delay variation less than **TBD** ns over 0˚C to 70˚C temperature range.

HDTV Horizontal Interval Timing

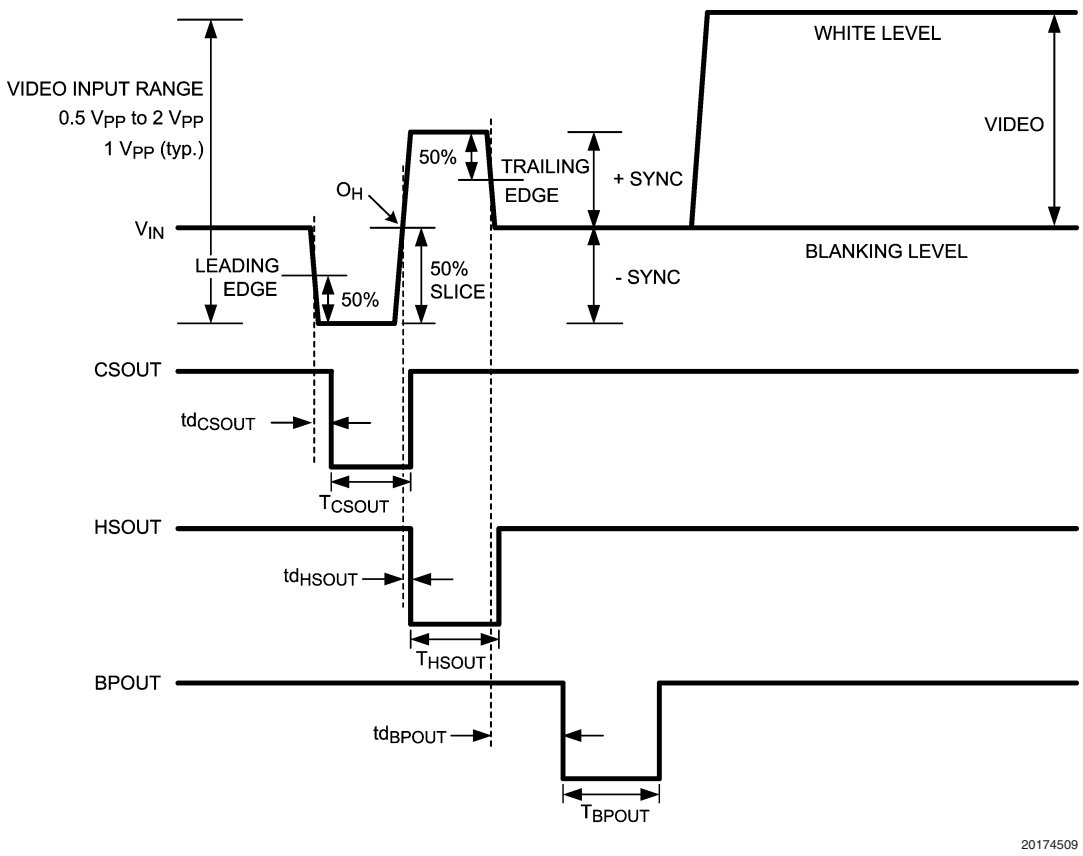


FIGURE 10. HDTV Horizontal Interval with Tri-level Sync

HDTV Horizontal Interval Timing Characteristics (720P, 1080I)

Symbol	Parameter	Conditions	Typ	Units
td_{CSOUT}	Composite Sync Output Propagation Delay from Input Sync Leading Edge	See *Figure 10*	180	ns
td_{HSOUT}	Horizontal Sync Output Propagation Delay from Input Sync Reference (O_H)	See *Figure 10*	30	ns
td_{BPOUT}	Burst/Back Porch Timing Output Propagation Delay from Input Sync Trailing Edge	See *Figure 10*	400	ns
T_{HSOUT}	Horizontal Sync Output Pulse Width	See *Figure 10*	550	ns
T_{BPOUT}	Burst/Back Porch Timing Output Propagation Delay from Input	See *Figure 10*	630	ns

Note: Delay variation less than **TBD** ns over 0˚C to 70˚C temperature range.

Application Information

GENERAL DESCRIPTION

The LMH1981 is designed to extract the timing information from various video formats with vertical serration and output the syncs and relevant timing signals in CMOS logic. Its high performance, advanced features and easy application make it ideal for broadcast and professional video systems where low jitter is a crucial parameter. The device can operate from a supply voltage between 3.3V and 5V. The only required external components are bypass capacitors at the power supply pins, an input coupling capacitor at pin 4, and a precision R_{EXT} resistor at pin 1. Refer to the test circuit in *Figure 2*.

R_{EXT} Resistor

The R_{EXT} external resistor establishes the internal bias current and precise reference voltage for the LMH1981. For optimal performance, R_{EXT} should be a 10 kΩ 1% precision resistor with a low temperature coefficient to ensure proper operation over a wide temperature range. Using a R_{EXT} resistor with less precision may result in reduced performance (like worse jitter performance, increased propagation

Application Information (Continued)

delay, or reduced input sync amplitude range) against temperature, supply voltage, input signal, or part-to-part variations.

Note: The R_{EXT} resistor serves a different function than the "R_{SET} resistor" used in the LM1881 sync separator. In the older LM1881, the R_{SET} value was adjusted to accommodate different input line rates. For the LMH1981, the R_{EXT} value is fixed, and the device automatically detects the input line rate to support various video formats without electrical or physical intervention.

Automatic Format Detection and Switching

Automatic format detection eliminates the need for external programming via a microcontroller or R_{SET} resistor. The device outputs will respond correctly to video format switching after a sync lock period has been satisfied. Unlike other sync separators, the LMH1981 does not require the power to be cycled in order to guarantee correct outputs after a significant change to the input signal. See the **Sync Lock Period** sub-section for more details.

50% Sync Slicing

The LMH1981 features 50% sync slicing to provide accurate sync separation for a video input amplitudes from 0.5 V_{PP} to 2 V_{PP}, which enables excellent HSync jitter performance even for improperly terminated or attenuated source signals and stability against variations in temperature. The sync separator is compatible with SD/EDTV bi-level and HDTV tri-level sync inputs. Bi-level syncs will be sliced at the 50% point between the video blanking level and negative sync tip, indicated by the input's sync timing reference or "O_H" in *Figure 9*. Tri-level syncs will be sliced at the 50% point between the negative and positive sync tips (or positive zero-crossing), indicated by O_H in *Figure 10*.

Macrovision Compatibility

The LMH1981 is compatible with the Macrovision Video Copy Protection System commonly used in VHS and DVD video sources, which inserts pseudo-sync pulses in the video signal during the vertical blanking interval. These Macrovision-embedded pulses will be effectively ignored by the sync separator, and the outputs will not be affected.

VIDEO INPUT

Supported Video Standards

The LMH1981 supports sync separation for the following video interfaces and standards:

- Composite Video (CVBS) and S-Video (Y/C):
  - — SDTV: SMPTE 170M (NTSC), ITU-R BT.470 (PAL), SECAM
- Component Video (YP_BP_R/GBR):
  - — SDTV: SMPTE 125M, SMPTE 267M, ITU-R BT.601 (480I, 576I)
  - — EDTV: ITU-R BT.1358 (480P, 576P)
  - — HDTV: SMPTE 296M (720P), SMPTE 274M (1080I/P), SMPTE RP 211 (1080PsF)

The LMH1981 does not support RGB formats that conform to VESA standards used for PC graphics.

Video Input Requirements

V_{IN} (pin 4) accepts CVBS, Y (Luma) from Y/C and YP_BP_R, and G (Sync on Green) from GBR with bi-level sync or tri-level sync. The video source should be terminated with a 75Ω load resistor to ensure correct input signal amplitude and minimize video & sync distortion due to reflections. In extreme cases, the LMH1981 can handle unterminated and double-terminated input conditions assuming a typical 1 V_{PP} video signal.

The video input signal should be AC coupled through a properly chosen capacitor value in order to optimize the trade-off between the sync lock period and the line droop voltage at V_{IN}, which can affect jitter performance. A larger AC coupling capacitor will reduce the jitter on HSync but increase the sync lock period, since higher value capacitors take more time to reach a quiescent DC voltage via the clamp charging current. A 1 µF coupling capacitor is a good starting value for typical applications and can be adjusted to meet the specific application requirements.

Sync Lock Period

When there is a significant change to the video input condition, such as applying a new signal, switching the video format, or looping-through (which may cause double input termination), the steady-state operation of the LMH1981 will be affected while its outputs begin to produce new timing signals. These signals may not be accurate until after an appropriate start-up time or "sync lock period" has been satisfied. This is because the AC coupling capacitor needs time to reestablish its quiescent DC voltage while the internal 50% sync slicing circuitry regains steady-state operation before the outputs are accurate. $T_{SYNC\text{-}LOCK}$ is the maximum period from when the new input signal starts and stabilizes at V_{IN} to when the output sync signals are accurate and valid to use. It is recommended that the outputs are used only after $T_{SYNC\text{-}LOCK}$ condition has been satisfied.

LOGIC OUTPUTS

In the absence of a video input signal, the LMH1981 outputs are logic high except for the odd/even field and video format outputs, which are both undefined, and the composite sync output.

Composite Sync Output

CSOUT (pin 12) simply reproduces the video input sync pulses below the video blanking level. This is obtained by clamping the video signal sync tip to the internal clamp voltage at V_{IN} and using 50% sync slicing to extract the resultant composite sync signal, or CSync. For both bi-level and tri-level syncs, CSync's negative-going leading edge is derived from the input's negative-going leading edge with a propagation delay.

Horizontal Sync Output

HSOUT (pin 7) produces a negative-polarity horizontal sync signal, or HSync, with very low jitter on its negative-going leading edge (reference edge). For bi-level and tri-level sync signals, the horizontal sync leading edge is triggered from the input's sync reference, O_H, with a propagation delay.

HSync was optimized for excellent jitter performance on its leading edge because most video systems are negative-edge triggered. When HSync is used in a positive-edge triggered system, like an FPGA PLL input, it must be inverted beforehand to produce positive-going leading edges. The trailing edge of HSync should **never** be used as the reference or triggered edge. This is because some trailing edges of HSync are reconstructed for the broad serration pulses during the vertical interval.

Application Information (Continued)

HSync's typical peak-to-peak jitter can be measured using the input-referred jitter test methodology on a real-time digital oscilloscope by triggering at or near the input's O_H reference and monitoring HSync's leading edge with 4-sec. variable persistence. This is one way to measure HSync's typical peak-to-peak jitter in the time domain. *Figure 11* shows an oscilloscope screenshot demonstrating very low jitter on HSync's leading edge for a 1080I video input.

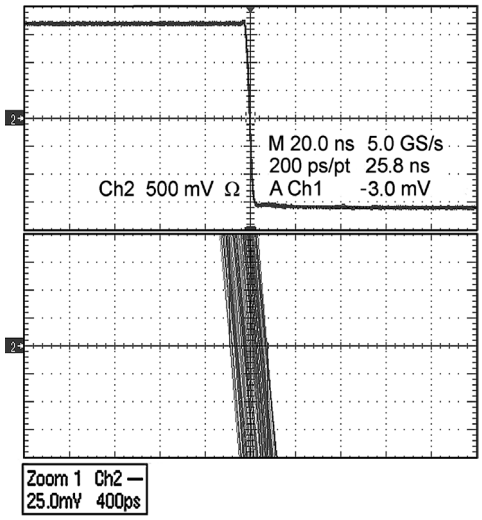


FIGURE 11. Typical HSync Jitter for 1080I Input
Upper: Horizontal Sync Leading Edge (Reference)
Lower: Zoomed In — 400 ps/DIV, 25 mV/DIV

Vertical Sync Output

VSOUT (pin 8) produces a negative-polarity vertical sync signal, or VSync. VSync's negative-going leading edge is derived from O_H of the first vertical serration pulse with a propagation delay, and its output pulse width, T_{VSOUT}, spans approximately three horizontal periods (3H).

Burst/Back Porch Timing Output

BPOUT (pin 13) provides a negative-polarity burst/back porch signal, which is pulsed low for a fixed width during the back porch interval following the input's sync pulse. The burst/back porch timing pulse is useful as a burst gate signal for NTSC/PAL color burst synchronization and as a clamp signal for black level clamping (DC restoration) and sync stripping applications.

For SDTV formats, the back porch pulse's negative-going leading edge is derived from the input's positive-going sync edge with a propagation delay, and the pulse width spans an appropriate duration of the color burst envelope for NTSC/PAL. During the vertical interval, its pulse width is shorter to correspond with the narrow serration pulses. For EDTV formats, the back porch pulse behaves similar to the SDTV case except that the shorter pulse width is always maintained. For HDTV formats, the pulse's leading edge is derived from the input's negative-going trailing sync edge with a propagation delay, and the pulse width is even narrower to correspond with the shortest back porch duration of HDTV formats.

Odd/Even Field Output

OEOUT (pin 14) provides an odd/even field output signal, which facilitates identification of odd and even fields for interlaced or segmented frame (sF) formats. For interlaced or segmented frame formats, the odd/even output is logic high during an odd field (field 1) and logic low during an even field (field 2). The odd/even output edge transitions align with VSync's leading edge to designate the start of odd and even fields. For progressive (non-interlaced) video formats, the output is held constantly at logic high.

Video Format Output (Lines-per-Field Data)

The LMH1981 counts the number of HSync pulses per field to approximate the total horizontal line count per field (vertical resolution). This can be used to identify the video format and enable dynamic adjustment of video system parameters, such as color space or scaler conversions. The line count per field is output to VFOUT (pin 9) as an 11-bit binary data stream. The video format data stream is clocked out on the 11 consecutive leading edges of HSync, starting at the 3rd HSync **after** each VSync leading edge. Outside of these active 11-bits of data, the video format output can be either 0 or 1 and should be treated as undefined. Refer to *Figure 12* and *Figure 13* to see the VFOUT data timing for the 1080I interlaced format and *Figure 14* for the 480P progressive format.

A FPGA/MCU can be used to decode the 11-bit VFOUT data stream by using HSync as the clock source signal and VSync as the enable signal. Using the FPGA's clock delay capability, a delayed clock derived from HSync can be used as the sampling clock to latch the VFOUT data in the middle of the horizontal line period rather than near the VFOUT data-bit transitions in order to avoid setup time requirements.

Application Information (Continued)

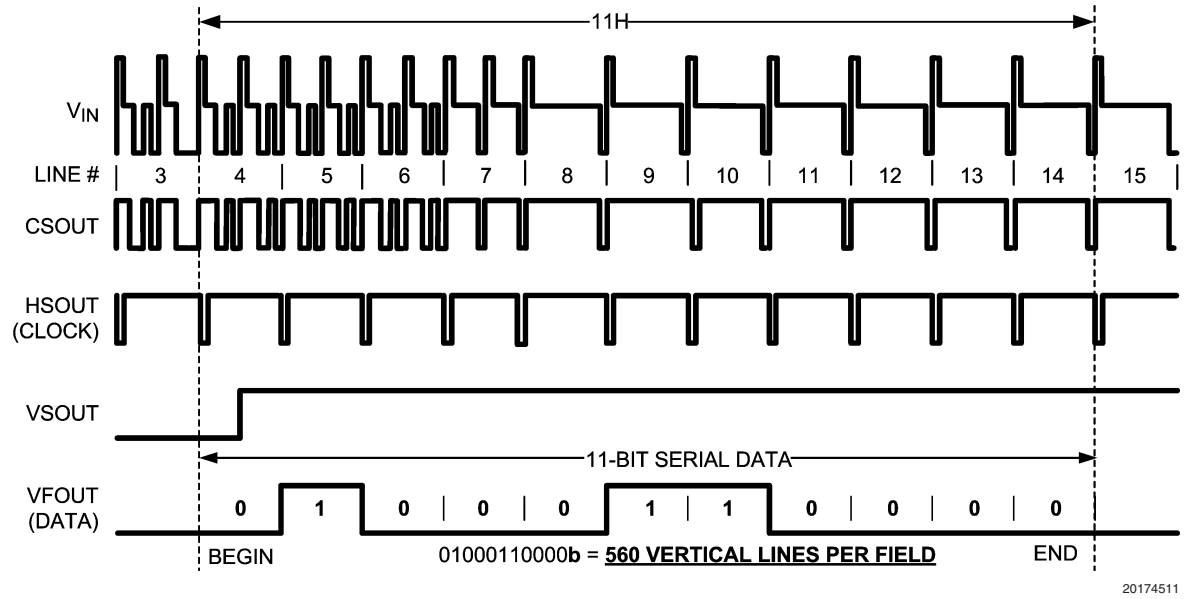


FIGURE 12. Video Format Output for Interlaced Format, 1080I Field 1

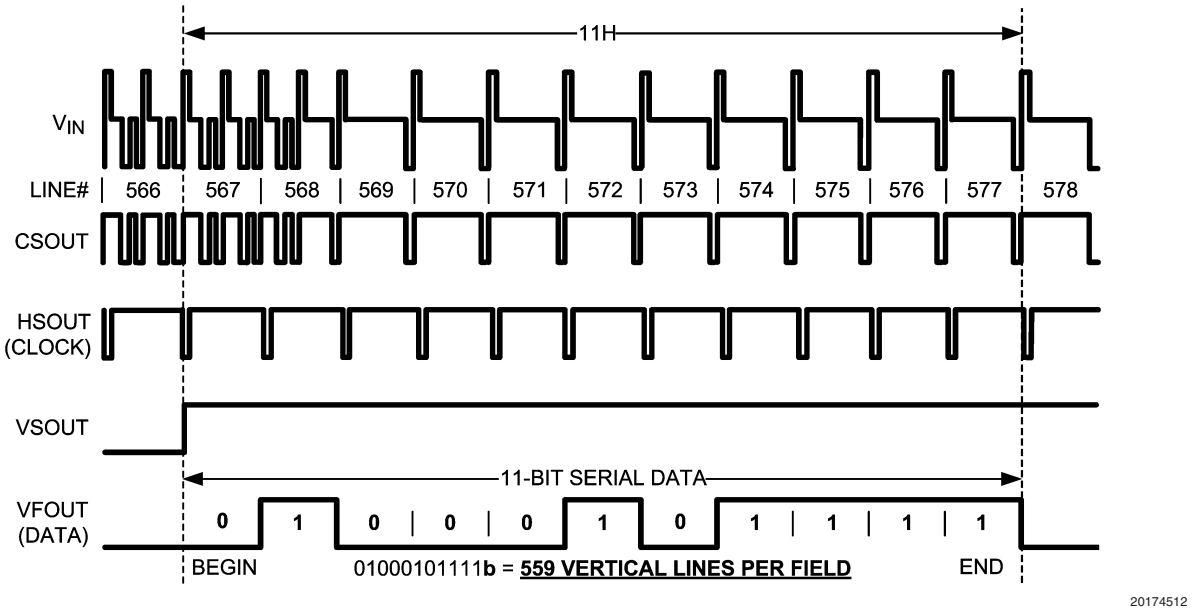


FIGURE 13. Video Format Output for Interlaced Format, 1080I Field 2

Application Information (Continued)

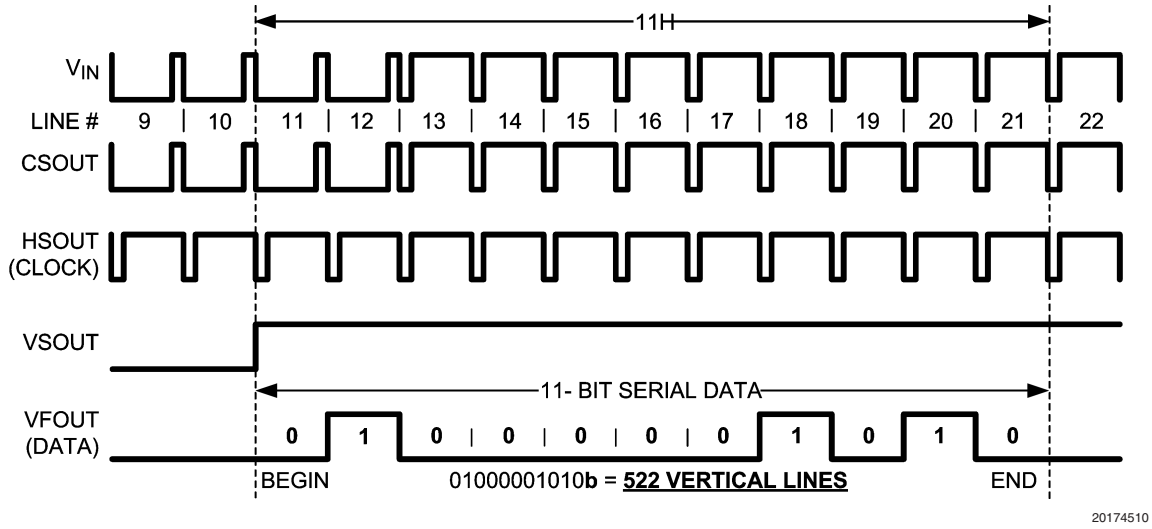


FIGURE 14. Video Format Output for Progressive Format, 480P

PCB LAYOUT CONSIDERATIONS

LMH1981 IC Placement

The LMH1981 should be placed such that critical signal paths are short and direct to minimize PCB parasitics from degrading the high-speed video input and logic output signals.

Ground Plane

A two-layer, FR-4 PCB is sufficient for this device. One of the PCB layers should be dedicated to a single, solid ground plane that runs underneath the device and connects the device GND pins together. The ground plane should be used to connect other components and serve as the common ground reference. It also helps to reduce trace inductances and minimize ground loops. Try to route supply and signal traces on another layer to maintain as much ground plane continuity as possible.

Power Supply Pins

The power supply pins should be connected together using short traces with minimal inductance. When routing the supply traces, be careful not to disrupt the solid ground plane.

For high frequency bypassing, place 0.1 µF SMD ceramic bypass capacitors with very short connections to power supply and GND pins. Two or three ceramic bypass capacitors can be used depending on how the supply pins are connected together. Place a 4.7 µF SMD tantalum bypass capacitor nearby all three power supply pins for low frequency supply bypassing.

R_{EXT} Resistor

The R_{EXT} resistor should be a 10 kΩ 1% SMD precision resistor. Place R_{EXT} as close as possible to the device and connect to pin 1 and the ground plane using the shortest possible connections. All input and output signals must be kept away from this pin to prevent unwanted signals from coupling into this pin.

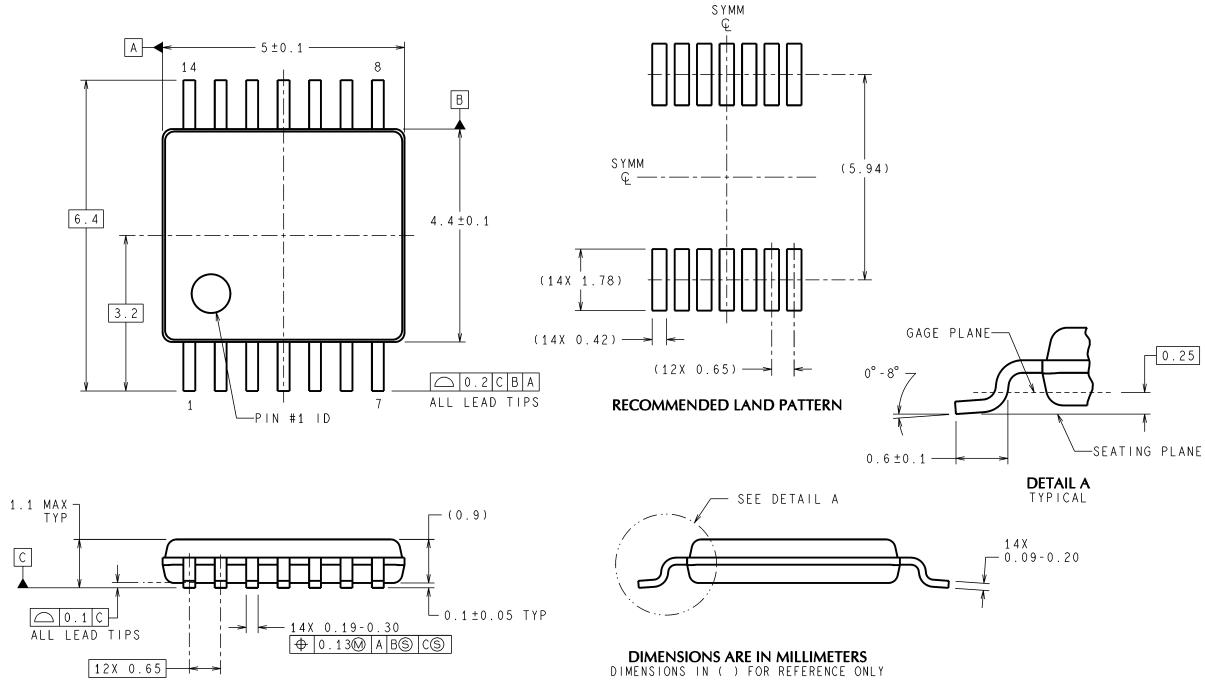
Video Input

The input signal path should be routed using short, direct traces between video source and input pin. Use a 75Ω input termination and a SMD capacitor for AC coupling the video input to pin 4.

Output Routing

The output signal paths should be routed using short, direct traces to minimize parasitic effects that may degrade these high-speed logic signals. This is especially important for the horizontal sync output, in which it is critical to minimize timing jitter. Each output can be protected by current limiting with a small series resistor, like 100Ω.

Physical Dimensions inches (millimeters) unless otherwise noted



MTC14 (Rev D)

14-Pin TSSOP
NS Package Number MTC14

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