National Semiconductor

LMH0341, LMH0041, LMH0071, LMH0051
3G, HD, SD, DVB-ASI SDI Deserializer with Loopthrough and LVDS Interface

General Description

The LMH0041 family of products provide a very simple 1:5 deserializer and receiver function. The device is intended to be paired with an FPGA host which will receive the raw 5 bit data words and will decode the data appropriately such that a SMPTE standard signal may be recovered. The devices are designed to receive data compliant with DVB-ASI, SMPTE 259M, SMPTE 292M and/or SMPTE 424M. The interface between the LMH0041 and the FPGA consists of a 5 bit wide LVDS bus, an LVDS clock and an SMBus interface. All devices except for the LMH0051 includes a reclocked feedthrough output with a SMPTE compliant cable driver. The LMH0341 includes support for SMPTE424M, and the LMH0071 is a Stadard Definition (SD) only variant. The product is packaged in a physically small 48 pin LLP package.

Key Specifications

- Output compliant with SMPTE 259M-C, SMPTE 292M, SMPTE 424M and DVB-ASI
- Typical power dissipation: 410 mW (loopthrough disabled)
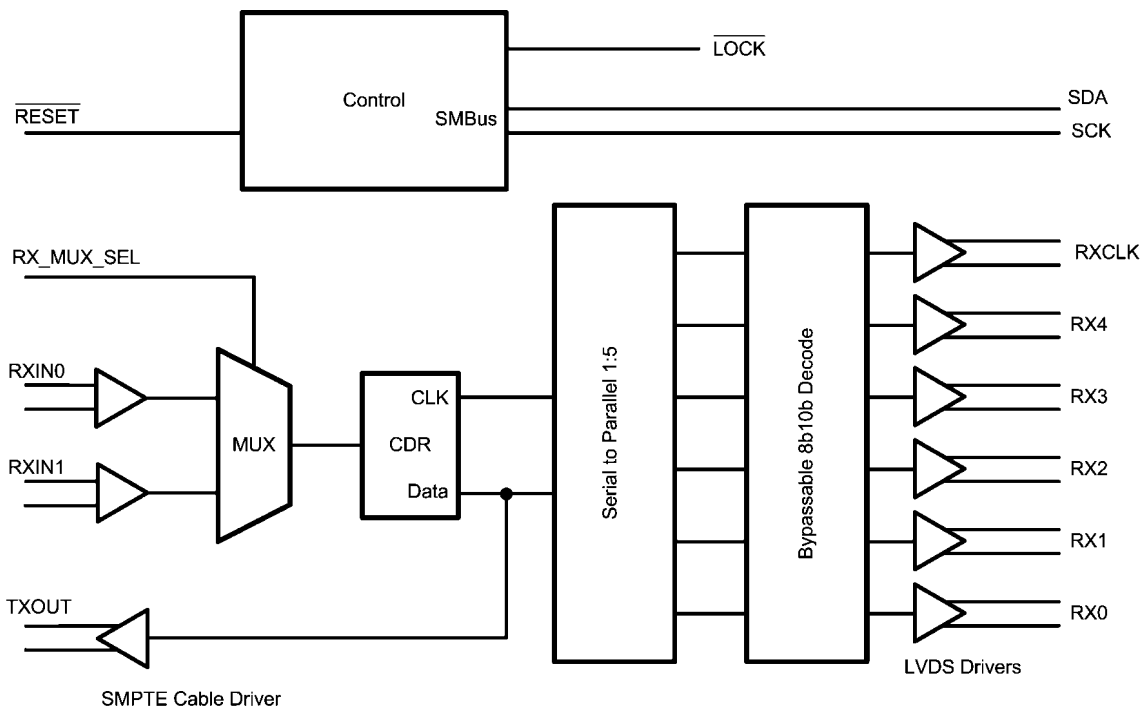- 0.6 UI Input Jitter Tolerance

Features

- LVDS Interface
- Dual multiplexed inputs
- No external VCO or clock required
- Loopthrough with Cable Driver
- SMBus configuration interface
- 48 pin LLP package

Applications

- SDI interfaces for:
  — Video Cameras
  — DVRs
  — Video Switchers
  — Video Editing Systems

Block Diagram

30017201

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TABLE 1. Feature Table

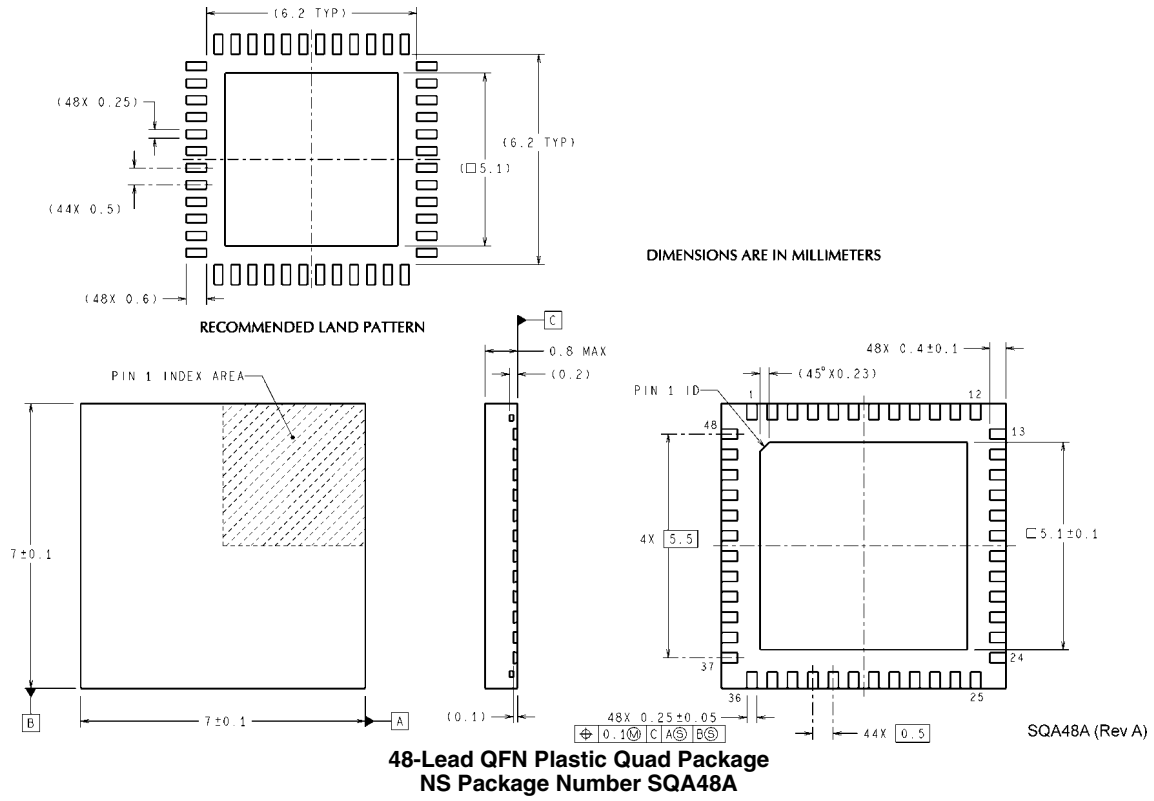| Device	SMPTE 424M Support	SMPTE 292M Support	SMPTE 259M Support	DVB-ASI Support	Active Loopthrough
LMH0341	×	×	×	×	×
LMH0041		×	×	×	×
LMH0071			×	×	×
LMH0051		×	×	×	

Device Operation

The LMH0041 deserializer is used in digital video signal origination equipment. It is intended to be operated in conjunction with an FPGA host which processes the received data to recover the original parallel data from the five bit wide datapath that comes from the LMH0041. The LMH0041 requires the use of an external equalizer such as the LMH0044, which can be directly connected to the LMH0041.

DVB-ASI Mode

DVB-ASI mode is enabled when the DVB-ASI pin is brought to a high state. When the DVB-ASI mode is enabled, an internal framer and 8b10b decoder is engaged such that the data appearing on RX0-RX3 will represent a nibble of the decoded 8b10b data. RX4 is an Idle character detect and can be used as an enable to allow the receiver to not write data into a FIFO. RX4 is high if the data being presented on RX0-RX3 represents the idle character. The Most Significant Nibble of data is presented on the rising edge of RXCLK, and the lease significant on the falling edge of RXCLK.

Physical Dimensions   inches (millimeters) unless otherwise noted

(6.2 TYP)

(48X 0.25)

(6.2 TYP)

(□ 5.1)

(44X 0.5)

(48X 0.6)

DIMENSIONS ARE IN MILLIMETERS

RECOMMENDED LAND PATTERN

C

0.8 MAX

(0.2)

PIN 1 ID

48X 0.4±0.1

(45° X0.23)

PIN 1 INDEX AREA

7±0.1

48

1

12

13

4X 5.5

□ 5.1±0.1

B

7±0.1

A

(0.1)

37

36

25

24

48X 0.25±0.05

⊕ 0.1Ⓜ C AⓈ BⓈ

44X 0.5

SQA48A (Rev A)

48-Lead QFN Plastic Quad Package
NS Package Number SQA48A

Notes

National Semiconductor Americas Customer Support Center	National Semiconductor Europe Customer Support Center	National Semiconductor Asia Pacific Customer Support Center	National Semiconductor Japan Customer Support Center
Email: new.feedback@nsc.com Tel: 1-800-272-9959	Fax: +49 (0) 180-530-85-86 Email: europe.support@nsc.com Deutsch Tel: +49 (0) 69 9508 6208 English Tel: +49 (0) 870 24 0 2171 Français Tel: +33 (0) 1 41 91 8790	Email: ap.support@nsc.com	Fax: 81-3-5639-7507 Email: jpn.feedback@nsc.com Tel: 81-3-5639-7560