BSI

Ultra Low Power CMOS SRAM
32K X 8 bit
Pb-Free and Green package materials are compliant to RoHS

BS62UV256

n FEATURES

Ÿ Wide V_{CC} low operation voltage : 1.8V ~ 3.6V

Ÿ Ultra low power consumption :

  V_{CC} = 2.0V Operation current : 15mA (Max.) at 150ns
                                  0.5mA (Max.) at 1MHz
             Standby current : 0.005uA(Typ.) at 25°C

  V_{CC} = 3.0V Operation current : 25mA (Max.) at 150ns
                                    1mA (Max.) at 1MHz
             Standby current : 0.01uA (Typ.) at 25°C

Ÿ High speed access time :

  -10   100ns (Max.)
  -15   150ns (Max.)

Ÿ Automatic power down when chip is deselected

Ÿ Easy expansion with $\overline{CE}$ and $\overline{OE}$ options

Ÿ Three state outputs and TTL compatible

Ÿ Fully static operation

Ÿ Data retention supply voltage as low as 1.5V

n DESCRIPTION

The BS62UV256 is a high performance, ultra low power CMOS Static Random Access Memory organized as 32,768 by 8 bits and operates form a wide range of 1.8V to 3.6V supply voltage.

Advanced CMOS technology and circuit techniques provide both high speed and low power features with typical CMOS standby current of 0.005uA and maximum access time of 150ns in 2.0V operation.

Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), and active LOW output enable ($\overline{OE}$) and three-state output drivers.

The BS62UV256 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.

The BS62UV256 is available in DICE form, JEDEC standard 28 pin 330mil Plastic SOP, 600mil Plastic DIP, 8mmx13.4mm TSOP (normal type).

n POWER CONSUMPTION

PRODUCT FAMILY	OPERATING TEMPERATURE	POWER DISSIPATION						PKG TYPE
		STANDBY (I_{CCSB1}, Max)		Operating (I_{CC}, Max)				
		V_{CC}=3.0V	V_{CC}=2.0V	V_{CC}=3.0V		V_{CC}=2.0V		
				1MHz	$f_{Max.}$	1MHz	$f_{Max.}$	
BS62UV256DC	Commercial +0°C to +70°C	0.4uA	0.4uA	0.9mA	20mA	0.6mA	10mA	DICE
BS62UV256PC								PDIP-28
BS62UV256SC								SOP-28
BS62UV256TC								TSOP-28
BS62UV256PI	Industrial -40°C to +85°C	0.7uA	0.7uA	1.0mA	25mA	0.8mA	15mA	PDIP-28
BS62UV256SI								SOP-28
BS62UV256TI								TSOP-28

n PIN CONFIGURATIONS
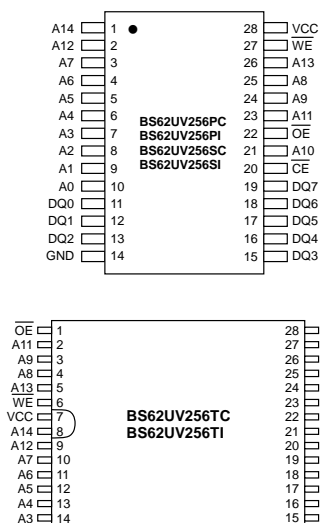
n BLOCK DIAGRAM
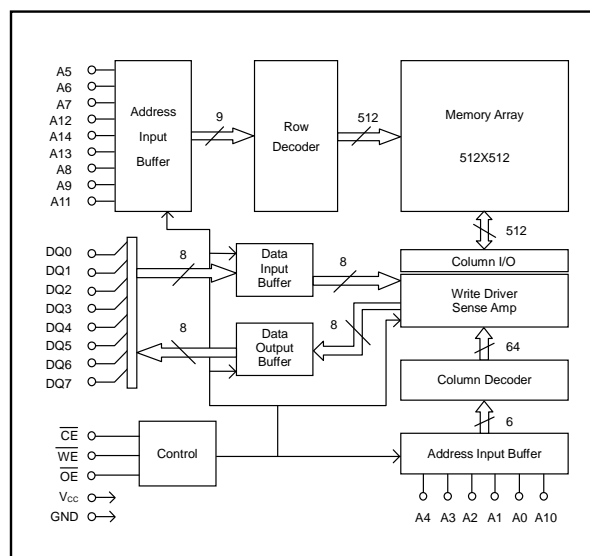
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n PIN DESCRIPTIONS

Name	Function
A0-A14 Address Input	These 15 address inputs select one of the 32,768 x 8-bit in the RAM
$\overline{CE}$ Chip Enable Input	$\overline{CE}$ is active LOW. Chip enable must be active when data read form or write to the device. If chip enable is not active, the device is deselected and is in standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
$\overline{WE}$ Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
$\overline{OE}$ Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impendence state when $\overline{OE}$ is inactive.
DQ0-DQ7 Data Input/Output Ports	There 8 bi-directional ports are used to read data from or write data into the RAM.
V_{CC}	Power Supply
GND	Ground

n TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O OPERATION	V_{CC} CURRENT
Not selected (Power Down)	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	L	H	H	High Z	I_{CC}
Read	L	H	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

NOTES: H means V_{IH}; L means V_{IL}; X means don't care (Must be V_{IH} or V_{IL} state)

n ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5[2] to 5.0	V
T_{BIAS}	Temperature Under Bias	-40 to +125	^{O}C
T_{STG}	Storage Temperature	-60 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. –2.0V in case of AC pulse width less than 30 ns.

n OPERATING RANGE

RANG	AMBIENT TEMPERATURE	V_{CC}
Commercial	$0^{O}C$ to $+70^{O}C$	1.8V ~ 3.6V
Industrial	$-40^{O}C$ to $+85^{O}C$	1.8V ~ 3.6V

n CAPACITANCE [1] ($T_A = 25^{O}C$, f = 1.0MHz)

SYMBOL	PAMAMETER	CONDITIONS	MAX.	UNITS
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	pF
C_{IO}	Input/Output Capacitance	$V_{I/O} = 0V$	8	pF

1. This parameter is guaranteed and not 100% tested.

n DC ELECTRICAL CHARACTERISTICS (T$_A$ = -40°C to +85°C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS		MIN.	TYP.[1]	MAX.	UNITS
V$_{CC}$	Power Supply			1.8	--	3.6	V
V$_{IL}$	Input Low Voltage		V$_{CC}$=2.0V	-0.5[2]	--	0.6	V
			V$_{CC}$=3.0V			0.8	
V$_{IH}$	Input High Voltage		V$_{CC}$=2.0V	1.4	--	V$_{CC}$+0.3[3]	V
			V$_{CC}$=3.0V	2.2			
I$_{IL}$	Input Leakage Current	V$_{IN}$ = 0V to V$_{CC}$		--	--	1	uA
I$_{LO}$	Output Leakage Current	$\overline{CE}$= V$_{IH}$, or $\overline{OE}$ = V$_{IH}$, V$_{I/O}$ = 0V to V$_{CC}$		--	--	1	uA
V$_{OL}$	Output Low Voltage	V$_{CC}$ = Max, I$_{OL}$ = 0.1mA	V$_{CC}$=2.0V	--	--	0.2	V
		V$_{CC}$ = Max, I$_{OL}$ = 2.0mA	V$_{CC}$=3.0V			0.4	
V$_{OH}$	Output High Voltage	V$_{CC}$ = Min, I$_{OH}$ = -0.1mA	V$_{CC}$=2.0V	1.6	--	--	V
		V$_{CC}$ = Min, I$_{OH}$ = -1.0mA	V$_{CC}$=3.0V	2.4			
I$_{CC}$[5]	Operating Power Supply Current	$\overline{CE}$ = V$_{IL}$, I$_{DQ}$ = 0mA, f = F$_{MAX}$[4]	V$_{CC}$=2.0V	--	--	15	mA
			V$_{CC}$=3.0V	--	--	25	
I$_{CC1}$	Operating Power Supply Current	$\overline{CE}$ = V$_{IL}$, I$_{DQ}$ = 0mA, f = 1MHz	V$_{CC}$=2.0V	--	--	0.8	mA
			V$_{CC}$=3.0V	--	--	1.0	
I$_{CCSB}$	Standby Current – TTL	$\overline{CE}$ = V$_{IH}$, I$_{DQ}$ = 0mA	V$_{CC}$=2.0V	--	--	0.5	mA
			V$_{CC}$=3.0V	--	--	1.0	
I$_{CCSB1}$[6]	Standby Current – CMOS	$\overline{CE}\geq$V$_{CC}$-0.2V, V$_{IN}\geq$V$_{CC}$-0.2V or V$_{IN}\leq$0.2V	V$_{CC}$=2.0V	--	0.005	0.7	uA
			V$_{CC}$=3.0V	--	0.01	0.7	

1. Typical characteristics are at T$_A$=25°C and not 100% tested.
2. Undershoot: -1.0V in case of pulse width less than 20 ns.
3. Overshoot: V$_{CC}$+1.0V in case of pulse width less than 20 ns.
4. F$_{MAX}$=1/t$_{RC}$.
5. I$_{CC (MAX.)}$ is 10mA/20mA at V$_{CC}$=2.0V/3.0V and T$_A$=70°C.
6. I$_{CCSB1(MAX.)}$ is 0.4uA/0.4uA at V$_{CC}$=2.0V/3.0V and T$_A$=70°C.

n DATA RETENTION CHARACTERISTICS (T$_A$ = -40°C to +85°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.[1]	MAX.	UNITS
V$_{DR}$	V$_{CC}$ for Data Retention	$\overline{CE}\geq$V$_{CC}$-0.2V, V$_{IN}\geq$V$_{CC}$-0.2V or V$_{IN}\leq$0.2V	1.5	--	--	V
I$_{CCDR}$[3]	Data Retention Current	$\overline{CE}\geq$V$_{CC}$-0.2V, V$_{IN}\geq$V$_{CC}$-0.2V or V$_{IN}\leq$0.2V	--	0.005	0.7	uA
t$_{CDR}$	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t$_R$	Operation Recovery Time		t$_{RC}$[2]	--	--	ns

1. V$_{CC}$=1.5V, T$_A$=25°C and not 100% tested.
2. t$_{RC}$ = Read Cycle Time.
3. I$_{CCDR(Max.)}$ is 0.4uA at T$_A$=70°C.
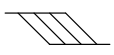
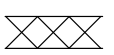## n LOW V$_{CC}$ DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)
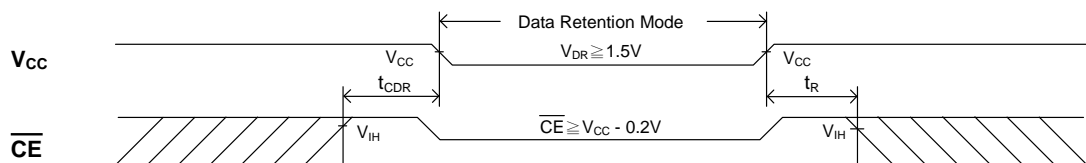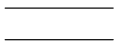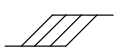
n AC TEST CONDITIONS
(Test Load and Input/Output Reference)

Input Pulse Levels	Vcc / 0V
Input Rise and Fall Times	1V/ns
Input and Output Timing Reference Level	0.5Vcc
Output Load — t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}	C_L = 5pF+1TTL
Output Load — Others	C_L = 100pF+1TTL

1 TTL

Output ⊸ ▷ ⊸
$C_L^{(1)}$

ALL INPUT PULSES

V_{CC}
GND

90% 90%
10% 10%

Rise Time : 1V/ns   Fall Time : 1V/ns
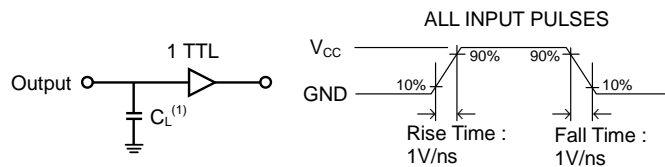
1. Including jig and scope capacitance.

n KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM "H" TO "L"	WILL BE CHANGE FROM "H" TO "L"
	MAY CHANGE FROM "L" TO "H"	WILL BE CHANGE FROM "L" TO "H"
	DON'T CARE ANY CHANGE PERMITTED	CHANGE : STATE UNKNOW
	DOES NOT APPLY	CENTER LINE IS HIGH INPEDANCE "OFF" STATE

n AC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C)

READ CYCLE

JEDEC PARAMETER NAME	PARANETER NAME	DESCRIPTION	CYCLE TIME : 100ns			CYCLE TIME : 150ns			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{RC}	Read Cycle Time	100	--	--	150	--	--	ns
t_{AVQX}	t_{AA}	Address Access Time	--	--	100	--	--	150	ns
t_{E1LQV}	t_{ACS}	Chip Select Access Time	--	--	100	--	--	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	--	--	50	--	--	100	ns
t_{E1LQX}	t_{CLZ}	Chip Select to Output Low Z	10	--	--	10	--	--	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output Low Z	10	--	--	10	--	--	ns
t_{E1HQZ}	t_{CHZ}	Chip Select to Output High Z	--	--	35	--	--	35	ns
t_{GHQZ}	t_{OHZ}	Output Enable to Output High Z	--	--	30	--	--	30	ns
t_{AVQX}	t_{OH}	Data Hold from Address Change	10	--	--	10	--	--	ns

BSI

n SWITCHING WAVEFORMS (READ CYCLE)

READ CYCLE 1 [1,2,4]
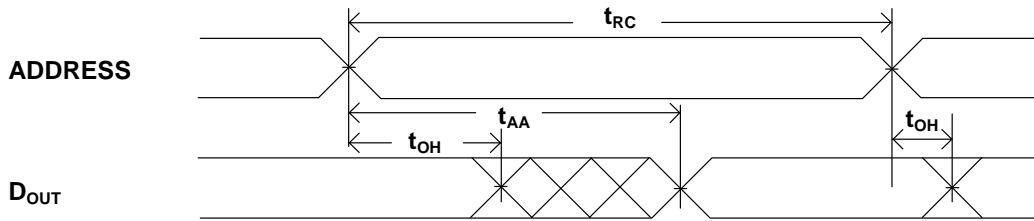
READ CYCLE 2 [1,3,4]
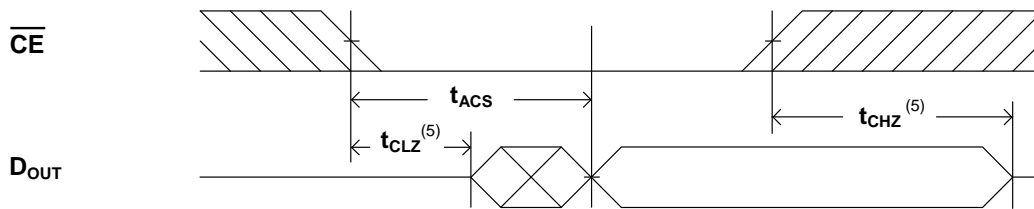
READ CYCLE 3 [1, 4]
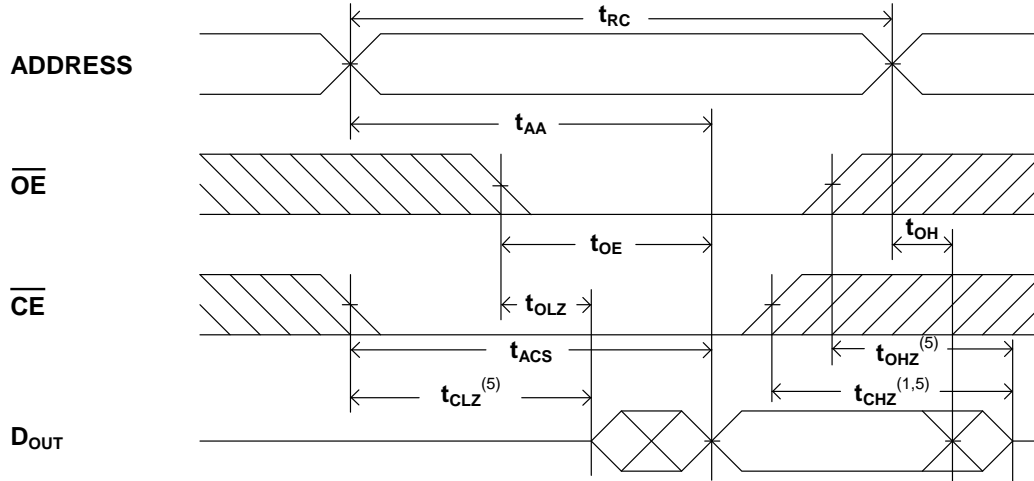
NOTES:
1. $\overline{WE}$ is high in read Cycle.
2. Device is continuously selected when $\overline{CE} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm$ 500mV from steady state with C_L = 5pF.
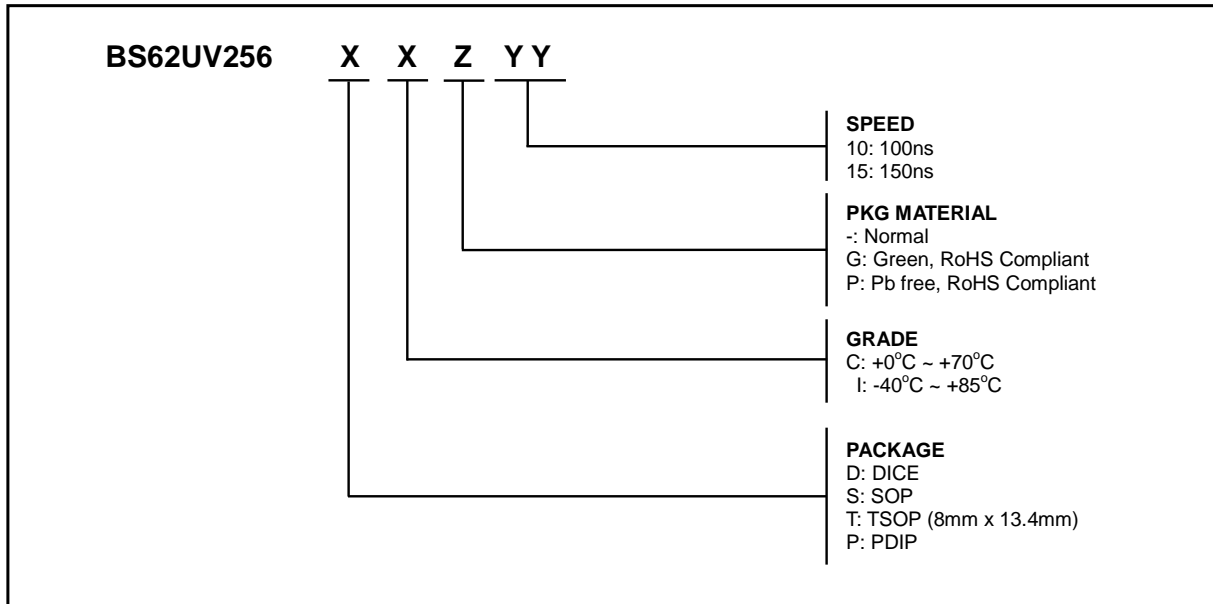   The parameter is guaranteed but not 100% tested.

n AC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C)

WRITE CYCLE

| JEDEC PARAMETER NAME	PARANETER NAME	DESCRIPTION	CYCLE TIME : 100ns			CYCLE TIME : 150ns			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{WC}	Write Cycle Time	100	--	--	150	--	--	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	100	--	--	150	--	--	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	100	--	--	150	--	--	ns
t_{WLWH}	t_{WP}	Write Pulse Width	50	--	--	80	--	--	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	--	--	0	--	--	ns
t_{WHAX}	t_{WR}	Write Recovery Time ($\overline{CE}$, $\overline{WE}$)	0	--	--	0	--	--	ns
t_{WLQZ}	t_{WHZ}	Write to Output High Z	--	--	30	--	--	30	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	40	--	--	40	--	--	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	--	--	0	--	--	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	--	--	30	--	--	30	ns
t_{WHQX}	t_{OW}	End of Write to Output Active	5	--	--	5	--	--	ns

n SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1 [(1)]
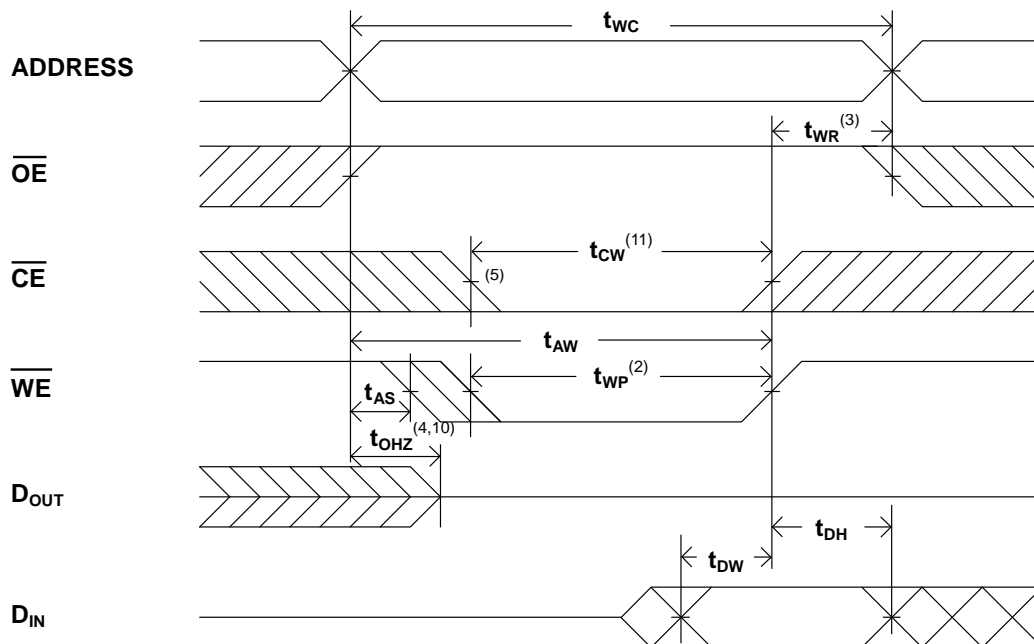
WRITE CYCLE 2 [1,6]
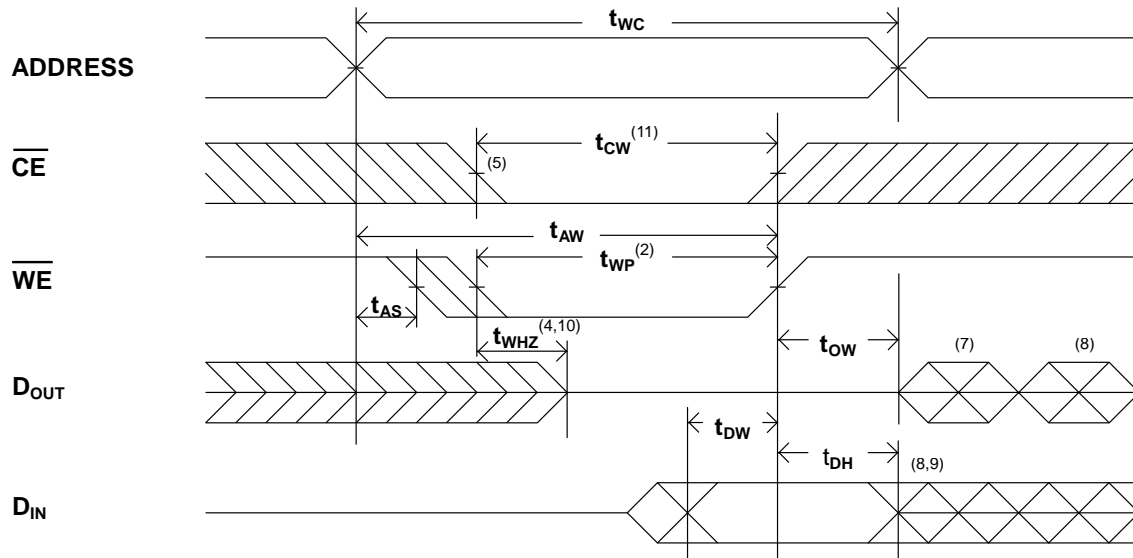
NOTES:
1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CE}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured $\pm$ 500mV from steady state with C_L = 5pF.
    The parameter is guaranteed but not 100% tested.
11. t_{CW} is measured from the later of $\overline{CE}$ going low to the end of write.

n **ORDERING INFORMATION**

BS62UV256   X X Z Y Y

SPEED
10: 100ns
15: 150ns

PKG MATERIAL
-: Normal
G: Green, RoHS Compliant
P: Pb free, RoHS Compliant

GRADE
C: +0°C ~ +70°C
 I: -40°C ~ +85°C

PACKAGE
D: DICE
S: SOP
T: TSOP (8mm x 13.4mm)
P: PDIP

Note:
BSI (Brilliance Semiconductor Inc.) assumes no responsibility for the application or use of any product or circuit described herein. BSI does not authorize its products for use as critical components in any application in which the failure of the BSI product may be expected to result in significant injury or death, including life-support systems and critical medical instruments.

n **PACKAGE DIMENSIONS**
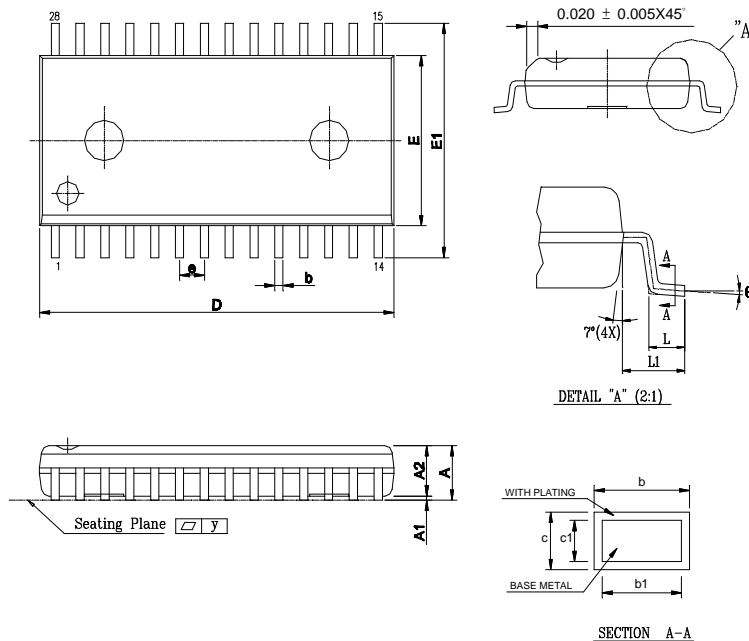
SYMBOL\UNIT	INCH	MM
A	0.106±0.006	2.692±0.152
A1	0.009±0.005	0.226±0.124
A2	0.098±0.005	2.489±0.127
b	0.014 ~ 0.020	0.35 ~ 0.50
b1	0.014 ~ 0.018	0.35 ~ 0.45
c	0.008 ~ 0.012	0.20 ~ 0.32
c1	0.008 ~ 0.011	0.20 ~ 0.28
D	0.713±0.005	18.110±0.127
E	0.331±0.005	8.407±0.127
E1	0.465±0.012	11.811±0.305
e	0.050±0.006	1.270±0.152
L	0.0380±0.0104	0.964±0.264
L1	0.0677±0.0079	1.72±0.2
y	0.004 Max.	0.1 Max.
θ	0° ~ 10°	0° ~ 10°

DETAIL "A" (2:1)

Seating Plane

SECTION A-A

SOP - 28

n PACKAGE DIMENSIONS (continued)
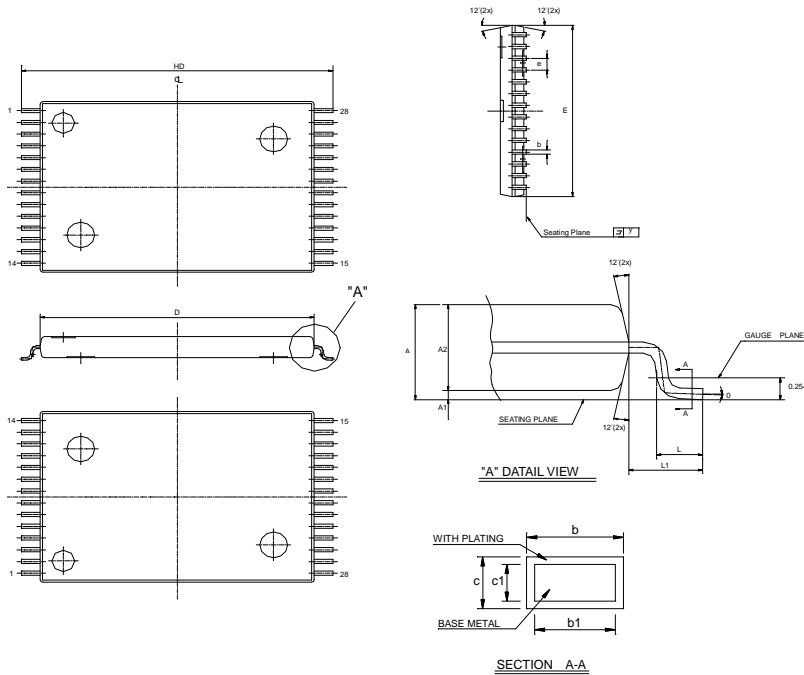
UNIT SYMBOL	INCH	MM
A	0.0433±0.004	1.10±0.10
A1	0.0045±0.0026	0.115±0.065
A2	0.039±0.002	1.00±0.05
b	0.009±0.002	0.22±0.05
b1	0.008±0.001	0.20±0.03
c	0.004 ~ 0.008	0.10 ~ 0.21
c1	0.004 ~ 0.006	0.10 ~ 0.16
D	0.465±0.004	11.80±0.10
E	0.315±0.004	8.00±0.10
e	0.022±0.004	0.55±0.10
HD	0.528±0.008	13.40±0.20
L	0.0197 +0.008 -0.004	0.50 +0.20 -0.10
L1	0.0315±0.004	0.80±0.10
y	0.004 Max.	0.1 Max.
θ	0˚~ 8˚	0˚~ 8˚

TSOP - 28
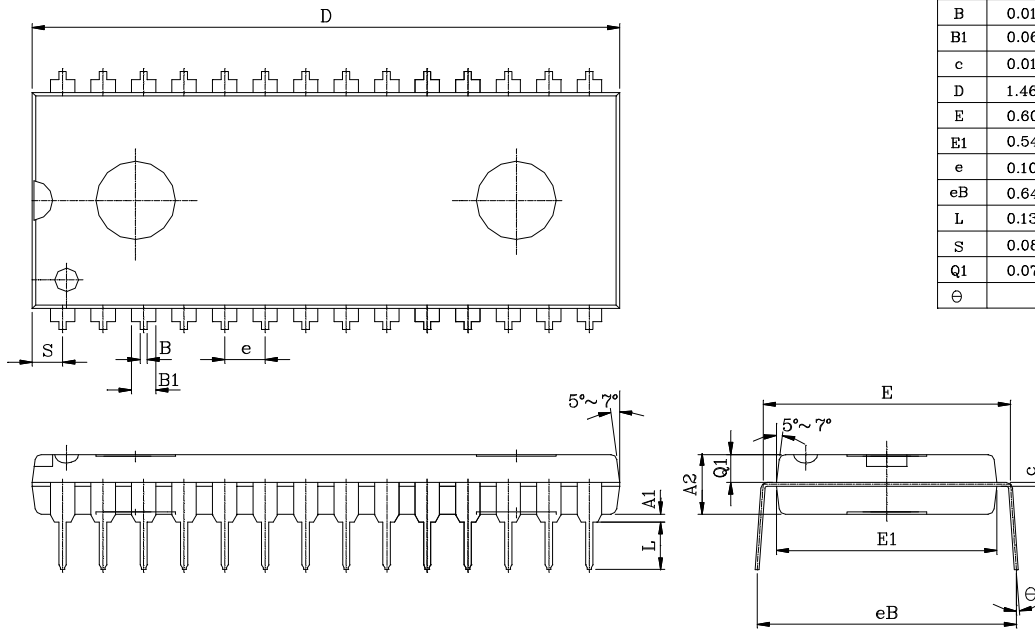
UNIT SYMBOL	INCH(BASE)	MM(REF)
A1	0.010(MIN)	0.254(MIN)
A2	0.150±0.005	3.810±0.127
B	0.018±0.005	0.457±0.127
B1	0.060±0.010	1.524±0.254
c	0.010±0.004	0.254±0.102
D	1.460±0.005	37.084±0.127
E	0.600±0.010	15.240±0.254
E1	0.544±0.004	13.818±0.102
e	0.100(TYP)	2.540(TYP)
eB	0.640±0.020	16.256±0.508
L	0.130±0.010	3.302±0.254
S	0.080±0.010	2.032±0.254
Q1	0.070±0.005	1.778±0.127
θ	6°±3°	6°±3°

PDIP - 28

n **Revision History**

Revision No.	History	Draft Date	Remark
2.4	Add Icc1 characteristic parameter	Jan. 13, 2006	
2.5	Change I-grade operation temperature range - from -25°C to -40°C	May. 25, 2006	
2.6	Add speed grade -10 for 100ns	Sep. 10, 2006	

Revised I_{CCSB1} sepc.
- from 0.2uA to 0.4uA for C-grade
- from 0.4uA to 0.7uA for I-grade

Revised I_{CCDR} sepc.
- from 0.1uA to 0.4uA for C-grade
- from 0.2uA to 0.7uA for I-grade