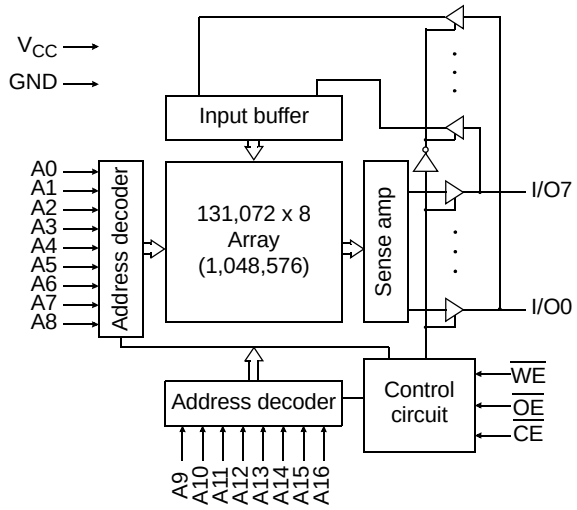
5V 128K X 8 CMOS SRAM (Center power and ground)

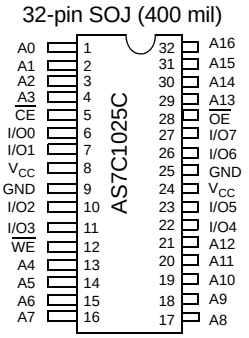
Features

- Industrial (-40^{o} to 85^{o}C) temperature.
- Organization: 131,072 x 8 bits
- High speed
  - 12 ns address access time
  - 6 ns output enable access time
- Low power consumption via chip deselect
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- Center power and ground
- TTL/LVTTL-compatible, three-state I/O
- JEDEC-standard package
  - 32-pin, 400 mil SOJ
- ESD protection ≥ 2000 volts

Pin arrangement

Logic block diagram





Functional description

The AS7C1025C is a 5V high-performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) devices organized as 131,072 x 8 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 12 ns with output enable access times (t_{OE}) of 6 ns are ideal for high-performance applications. The chip enable input $\overline{CE}$ permits easy memory and expansion with multiple-bank memory systems.

When $\overline{CE}$ is high, the device enters standby mode. If inputs are still toggling, the device will consume I_{SB} power. If the bus is static, then full standby power is reached (I_{SB1}).

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O0 through I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) high. The chips drive I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5 V supply. The AS7C1025C is packaged in common industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	V_{t1}	–0.50	+7.0	V
Voltage on any pin relative to GND	V_{t2}	–0.50	V_{CC} + 0.5	V
Power dissipation	P_D	–	1.25	W
Storage temperature (plastic)	T_{stg}	–55	+125	^{o}C
Ambient temperature with V_{CC} applied	T_{bias}	–55	+125	^{o}C
DC current into outputs (low)	I_{OUT}	–	50	mA

Note:
Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	High Z	Output disable (I_{CC})
L	H	L	D_{OUT}	Read (I_{CC})
L	L	X	D_{IN}	Write (I_{CC})

Key: X = don't care, L = low, H = high.

Recommended operating conditions

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	–	V_{CC} + 0.5	V
	V_{IL}	–0.5	–	0.8	V
Ambient operating temperature (Industrial)	T_A	–40	–	85	^{o}C

Notes:

V_{IL} min = -1.0V for pulse width less than 5ns, once per cycle.

V_{IH} max = V_{CC}+2.0V for pulse width less than 5ns, once per cycle.

DC operating characteristics (over the operating range)[1]

Parameter	Symbol	Test conditions	AS7C1025C-12		Unit
			Min	Max	
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = Max, V_{IN} = GND to V_{CC}	–	5	µA
Output leakage current	$\lvert I_{LO} \rvert$	V_{CC} = Max, $\overline{CE}$ = V_{IH}, V_{out} = GND to V_{CC}	–	5	µA
Operating power supply current	I_{CC}	V_{CC} = Max $\overline{CE} \le V_{IL}$, f = f_{Max}, I_{OUT} = 0 mA	–	160	mA
Standby power supply current[1]	I_{SB}	V_{CC} = Max $\overline{CE} \ge V_{IH}$, f = f_{Max}	–	40	mA
	I_{SB1}	V_{CC} = Max $\overline{CE} \ge V_{CC}$–0.2 V, $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC}$ –0.2 V, f = 0		10	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min	2.4	–	V

Capacitance (f = 1 MHz, T_a = 25^{o} C, V_{CC} = NOMINAL)[2]

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$	V_{IN} = 3dV	8	pF
I/O capacitance	$C_{I/O}$	I/O	V_{IN} = V_{OUT} = 3dV	8	pF

Note:

This parameter is guaranteed by device characterization, but is not production tested.

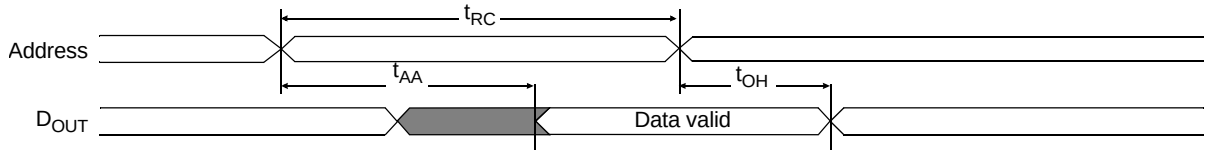
Read cycle (over the operating range)[3,9]

Parameter	Symbol	AS7C1025C-12		Unit	Notes
		Min	Max		
Read cycle time	t_{RC}	12	–	ns	
Address access time	t_{AA}	–	12	ns	3
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	12	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	6	ns	
Output hold from address change	t_{OH}	4	–	ns	5
$\overline{CE}$ low to output in low Z	t_{CLZ}	3	–	ns	4, 5
$\overline{CE}$ low to output in high Z	t_{CHZ}	0	6	ns	4, 5
$\overline{OE}$ low to output in low Z	t_{OLZ}	0	–	ns	4, 5
$\overline{OE}$ high to output in high Z	t_{OHZ}	0	5	ns	4, 5
Power up time	t_{PU}	0	–	ns	4, 5
Power down time	t_{PD}	–	12	ns	4, 5

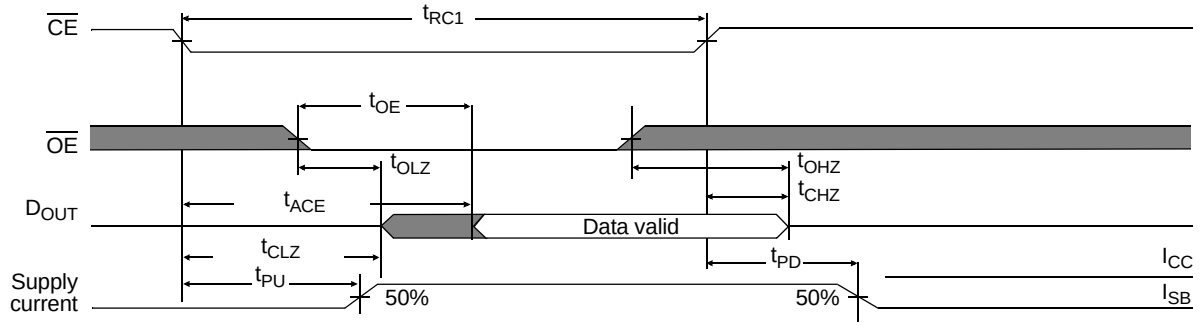
Key to switching waveforms

Rising input Falling input Undefined/don't care

Read waveform 1 (address controlled)[3,6,7,9]



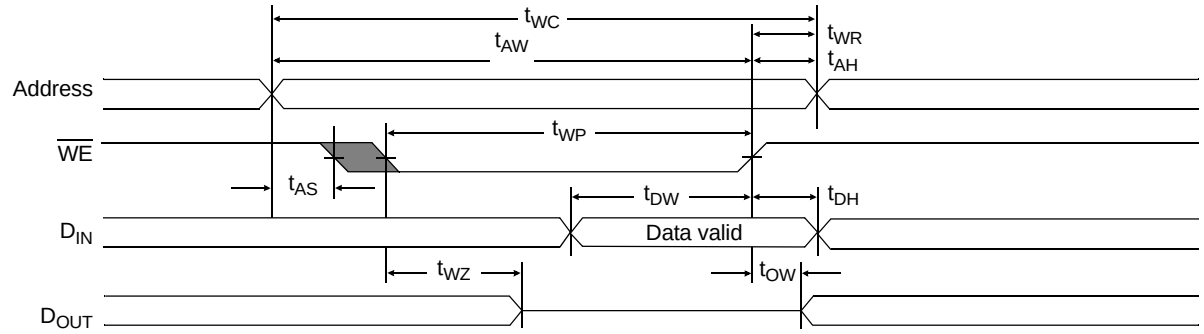
Read waveform 2 ($\overline{CE}$ and $\overline{OE}$ controlled)[3,6,8,9]



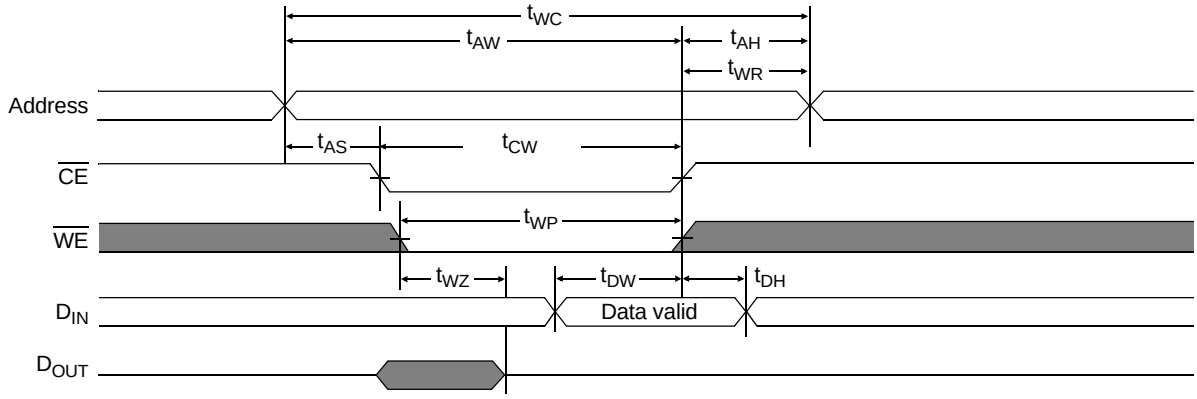
Write cycle (over the operating range)[11]

Parameter	Symbol	AS7C1025C-12		Unit	Notes
		Min	Max		
Write cycle time	t_{WC}	12	–	ns	
Chip enable ($\overline{CE}$) to write end	t_{CW}	8	–	ns	
Address setup to write end	t_{AW}	8	–	ns	
Address setup time	t_{AS}	0	–	ns	
Write pulse width	t_{WP}	8	–	ns	
Write recovery time	t_{WR}	0	–	ns	
Address hold from end of write	t_{AH}	0	–	ns	
Data valid to write end	t_{DW}	6	–	ns	
Data hold time	t_{DH}	0	–	ns	4, 5
Write enable to output in high Z	t_{WZ}	–	5	ns	4, 5
Output active from write end	t_{OW}	3	–	ns	4, 5

Write waveform 1 ($\overline{WE}$ controlled)[10,11]



Write waveform 2 ($\overline{CE}$ controlled)[10,11]



AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to 30 V. See Figure A.
- Input rise and fall times: 3 ns. See Figure A.
- Input and output timing reference levels: 1.5 V.

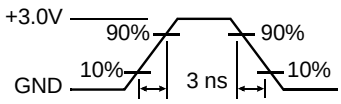


Figure A: Input pulse

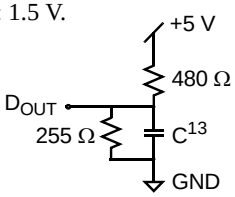
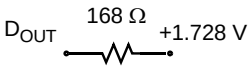


Figure B: 5 V Output load

Thevenin equivalent:

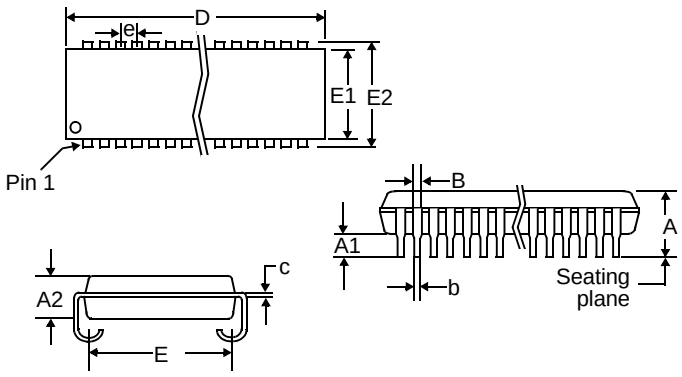


Notes:

1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled, but not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A and B.
4 t_{CLZ} and t_{CHZ} are specified with CL = 5 pF, as in Figure B. Transition is measured ±200 mV from steady-state voltage.
5 This parameter is guaranteed, but not 100% tested.
6 $\overline{WE}$ is high for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are low for read cycle.
8 Address is valid prior to or coincident with $\overline{CE}$ transition low.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 N/A
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 N/A.
13 C = 30 pF, except all high Z and low Z parameters where C = 5 pF.

Package dimensions

32-pin SOJ
400 mil



Symbol	32-pin SOJ 400 mil	
	Min	Max
A	0.132	0.146
A1	0.025	-
A2	0.105	0.115
B	0.026	0.032
b	0.015	0.020
c	0.007	0.013
D	0.820	0.830
E	0.354	0.378
E1	0.395	0.405
E2	0.435	0.445
e	0.050 BSC	

Note: This part is compatible with both pin numbering conventions used by various manufacturers.

Ordering Codes

Package	Volt/Temp	12 ns
Plastic SOJ, 400 mil	5V industrial	AS7C1025C-12JIN

Part numbering system

AS7C	1025C	–XX	X	X	X
SRAM prefix	Device number	Access time	Package: J = SOJ 400 mil	Temperature range I = industrial, -40° C to 85° C	N = LEAD FREE PART

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