

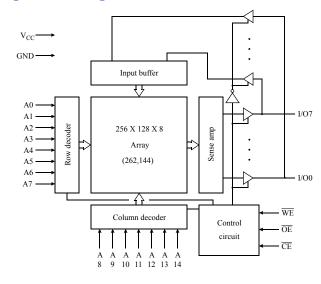
3.3V 32K X 8 CMOS SRAM (Common I/O)

Features

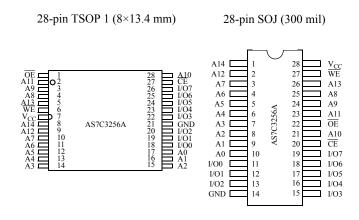
- Pin compatible with AS7C3256
- Industrial and commercial temperature options
- Organization: 32,768 words × 8 bits
- High speed
 - 10/12/15/20 ns address access time
 - 5, 6, 7, 8 ns output enable access time
- Very low power consumption: ACTIVE
 - 180mW max @ 10 ns
- Very low power consumption: STANDBY
- 7.2 mW max CMOS I/O
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ inputs

- TTL-compatible, three-state I/O
- 28-pin JEDEC standard packages
 - 300 mil SOJ
 - 8×13.4 mm TSOP 1
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangement



Selection guide

	-10	-12	-15	-20	Unit
Maximum address access time	10	12	15	20	ns
Maximum output enable access time	5	6	7	8	ns
Maximum operating current	50	45	40	35	mA
Maximum CMOS standby current	2	2	2	2	mA



Functional description

The AS7C3256A is a 3.3V high-performance CMOS 262,144-bit Static Random-Access Memory (SRAM) device organized as 32,768 words × 8 bits. It is designed for memory applications requiring fast data access at low voltage, including PentiumTM, PowerPCTM, and portable computing. Alliance's advanced circuit design and process techniques permit 3.3V operation without sacrificing performance or operating margins.

The device enters *standby mode* when $\overline{\text{CE}}$ is high. CMOS standby mode consumes 7.2 mW. Normal operation offers 75% power reduction after initial access, resulting in significant power savings during CPU idle, suspend, and stretch mode.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 5, 6, 7, 8 ns are ideal for high-performance applications. The chip enable (\overline{CE}) input permits easy memory expansion with multiple-bank memory organizations.

A write cycle is accomplished by asserting chip enable (\overline{CE}) and write enable (\overline{WE}) LOW. Data on the input pins I/O0-I/O7 is written on the rising edge of \overline{WE} (write cycle 1) or \overline{CE} (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable (\overline{OE}) or write enable (\overline{WE}) .

A read cycle is accomplished by asserting chip enable ($\overline{\text{CE}}$) and output enable ($\overline{\text{OE}}$) LOW, with write enable ($\overline{\text{WE}}$) high. The chip drives I/O pins with the data word referenced by the input address. When chip enable or output enable is high, or write enable is low, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible. Operation is from a single 3.3 ± 0.3 V supply. The AS7C3256A is packaged in high volume industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on V _{CC} relative to GND	V _{t1}	-0.5	+5.0	V
Voltage on any pin relative to GND	V _{t2}	-0.5	$V_{CC} + 0.5$	V
Power dissipation	P_{D}	_	1.0	W
Storage temperature (plastic)	T _{stg}	-65	+150	°С
Ambient temperature with V _{CC} applied	T _{bias}	-55	+125	°C
DC current into outputs (low)	I _{OUT}	_	20	mA

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

CE	WE	OE	Data	Mode
Н	X	X	High Z	Standby (I _{SB} , I _{SB1})
L	Н	Н	High Z	Output disable (I _{CC})
L	Н	L	D _{OUT}	Read (I _{CC})
L	L	X	D _{IN}	Write (I _{CC})

Key: X = Don't care, L = Low, H = High



Recommended operating conditions

Parameter	Symbol	Min	Typical	Max	Unit	
Supply voltage	V _{CC}	3.0	3.3	3.6	V	
Input voltage	${ m V_{IH}}^{**}$	2.0	_	V _{CC} +0.5	V	
Imput voluge	input voltage			_	0.8	V
Ambient operating temperature	commercial	$T_{\mathbf{A}}$	0	_	70	°C
Amoient operating temperature	industrial	$T_{\mathbf{A}}$	-40	_	85	°C

DC operating characteristics (over the operating range)¹

			-1	10	-12		-15		-20		
Parameter	Sym	Test conditions	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input leakage current	I _{LI}	$V_{CC} = Max$, $V_{in} = GND \text{ to } V_{CC}$	_	1	_	1	_	1	_	1	μΑ
Output leakage current	$ I_{LO} $	$V_{CC} = Max,$ $V_{OUT} = GND \text{ to } V_{CC}$	_	1	_	1	_	1	_	1	μΑ
Operating power supply current	I_{CC}	$V_{CC} = Max, \overline{CE} \le V_{IL}$ $f = f_{Max}, I_{OUT} = 0mA$	-	50	-	45	-	40	-	35	mA
Standby power	I_{SB}	$V_{CC} = Max, \overline{CE} \ge V_{IH}$ $f = f_{Max}$	ı	20	ı	20	ı	20	ı	20	mA
supply current	I_{SB1}	$\begin{aligned} &V_{CC} = \text{Max}, \overline{CE} \ge V_{CC} - 0.2V \\ &V_{IN} \le 0.2V \text{ or} \\ &V_{IN} \ge V_{CC} - 0.2V, f = 0 \end{aligned}$	ı	2.0	ı	2.0	ı	2.0	1	2.0	mA
Output voltage	V_{OL}	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$	_	0.4	ı	0.4	_	0.4	ı	0.4	V
output voltage	V _{OH}	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$	2.4	_	2.4	_	2.4	_	2.4	_	V

Capacitance (f = 1MHz, T_a = room temperature, V_{CC} = NOMINAL)²

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	$A, \overline{CE}, \overline{WE}, \overline{OE}$	$V_{in} = 0V$	5	pF
I/O capacitance	$C_{I/O}$	I/O	$V_{in} = V_{out} = 0V$	7	pF

 $V_{IL} = -1.0V$ for pulse width less than 5ns. $V_{IH} = -1.0V$ for pulse width less than 5ns.



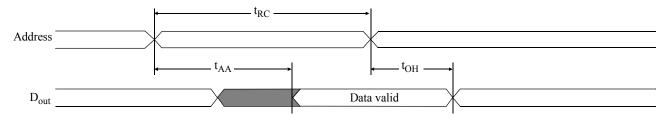
Read cycle (over the operating range)^{3,9}

		-10		-12		-15		-20			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t _{RC}	10	-	12	_	15	_	20	-	ns	
Address access time	t_{AA}	_	10	-	12	_	15	_	20	ns	3
Chip enable (\overline{CE}) access time	t _{ACE}	-	10	_	12	_	15	-	20	ns	3
Output enable (OE) access time	t _{OE}	_	5	_	6	_	7	_	8	ns	
Output hold from address change	t _{OH}	3	-	3	_	3	_	3	-	ns	5
CE LOW to output in low Z	t_{CLZ}	3	_	3	_	3	_	3	_	ns	4, 5
CE HIGH to output in high Z	t _{CHZ}	_	3	_	3	_	4	_	5	ns	4, 5
OE LOW to output in low Z	t_{OLZ}	0	_	0		0	_	0	_	ns	4, 5
OE HIGH to output in high Z	t _{OHZ}	_	3	_	3	-	4		5	ns	4, 5
Power up time	t_{PU}	0	1	0	_	0	_	0	_	ns	4, 5
Power down time	t _{PD}	_	10	_	12	-	15	_	20	ns	4, 5

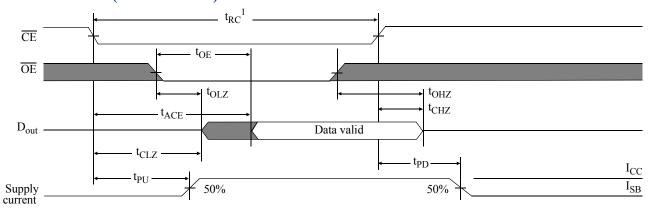
Key to switching waveforms

Rising input Falling input Undefined output/don't care

Read waveform 1 (address controlled)^{3,6,7,9}



Read waveform 2 (CE controlled)^{3,6,8,9}

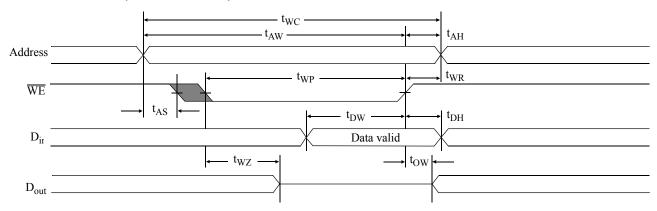




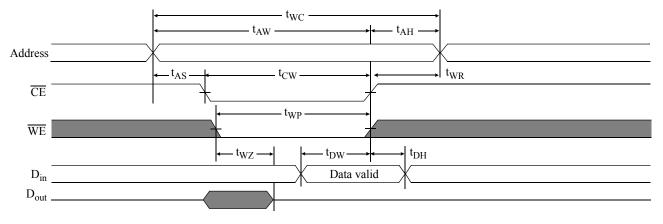
Write cycle (over the operating range) II

		-10		-12		-15		-20			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t _{WC}	10	_	12	_	15	_	20	_	ns	
Chip enable to write end	t_{CW}	8	_	8	_	10	_	12	_	ns	
Address setup to write end	t_{AW}	8	_	8	_	10	_	12	_	ns	
Address setup time	t _{AS}	0	_	0	_	0	_	0	_	ns	
Write pulse width	t_{WP}	7	_	8	_	9	_	12	_	ns	
Write recovery time	t _{WR}	0	_	0	_	0	_	0	_	ns	
Address hold from end of write	t _{AH}	0	_	0	_	0	_	0	_	ns	
Data valid to write end	t_{DW}	5	_	6	_	8	_	10	_	ns	
Data hold time	t _{DH}	0	_	0	_	0	_	0	_	ns	4, 5
Write enable to output in high Z	t_{WZ}	_	5	_	6	_	7	_	8	ns	4, 5
Output active from write end	t _{OW}	3	_	3	_	3	_	3	_	ns	4, 5

Write waveform 1 ($\overline{\text{WE}}$ controlled)^{10,11}



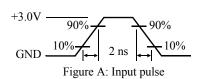
Write waveform 2 ($\overline{\text{CE}}$ controlled)^{10,11}

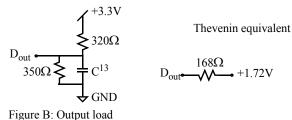




AC test conditions

- Output load: see Figure B
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.





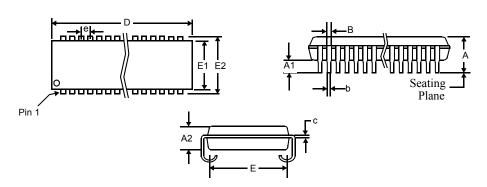
Notes

- 1 During V_{CC} power-up, a pull-up resistor to V_{CC} on \overline{CE} is required to meet I_{SB} specification.
- 2 This parameter is sampled, but not 100% tested.
- 3 For test conditions, see AC Test Conditions, Figures A, B.
- 4 These parameters are specified with CL = 5pF, as in Figures B. Transition is measured $\pm 500mV$ from steady-state voltage.
- 5 This parameter is guaranteed, but not tested.
- $\overline{\text{WE}}$ is High for read cycle.
- 7 $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are Low for read cycle.
- 8 Address valid prior to or coincident with $\overline{\text{CE}}$ transition Low.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 N/A
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 N/A
- 13 C=30pF, except on High Z and Low Z parameters, where C=5pF.



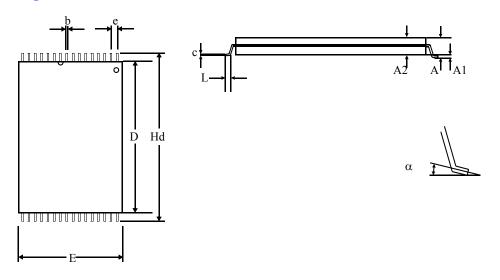
Package diagrams

28-pin SOJ



	28-pii	n SOJ
	Min	Max
	in in	ches
A	0.128	0.148
A1	0.026	-
A2	0.095	0.105
В	0.026	0.032
b	0.016	0.020
c	0.007	0.010
D	0.720	0.730
E	0.255	0.275
E 1	0.295	0.305
E2	0.330	0.340
e	0.050	BSC

28-pin TSOP1



	28-pin TSOP1 8×13.4 mm						
	Min	Max					
A	1.00	1.20					
A1	0.05	0.15					
A2	0.91	1.05					
b	0.17	0.27					
c	0.10	0.20					
D	11.70	11.90					
e	0.55 n	ominal					
E	7.90	8.10					
Hd	13.20	13.60					
L	0.50	0.70					
α	0°	5°					



Ordering information

Package / Access time	Temperature	10 ns	12 ns	15 ns	20 ns
Plastic SOJ, 300 mil	Commercial	AS7C3256A-10JC	AS7C3256A-12JC	AS7C3256A-15JC	AS7C3256A-20JC
rastic 500, 500 mm	Industrial	AS7C3256A-10JI	AS7C3256A-12JI	AS7C3256A-15JI	AS7C3256A-20JI
TSOP 8x13.4mm	Commercial	AS7C3256A-10TC	AS7C3256A-12TC	AS7C3256A-15TC	AS7C3256A-20TC
1501 6x15.411111	Industrial	AS7C3256A-10TI	AS7C3256A-12TI	AS7C3256A-15TI	AS7C3256A-20TI

Note: Add suffix 'N'to the above part number for lead free parts. (Ex. AS7C3256A-10JIN)

Part numbering system

AS7C	3	256A	-XX	X	C or I	X
SRAM prefix	Voltage: 3 = 3.3V supply	Device number	Access time	0 000 000 11111	Temperature range: C = 0 °C to 70 °C I = -40C to 85C	N= Lead Free Part





Alliance Semiconductor Corporation 2575, Augustine Drive, Santa Clara, CA 95054 Tel: 408 - 855 - 4900

Fax: 408 - 855 - 4999

www.alsc.com

Copyright © Alliance Semiconductor All Rights Reserved Part Number: AS7C3256A Document Version: v.2.0

© Copyright 2003 Alliance Semiconductor Corporation. All rights reserved. Our three-point logo, our name and Intelliwatt are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at any time, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warrantee to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as express agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance products are made exclusively according to Alliance's Terms and Conditions of Sale. The purchase of products from Alliance does not convey a license under any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life-supporting systems