# January 2001 Advance Information

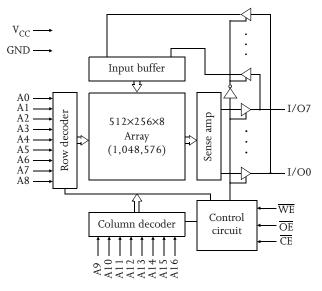


# 5V/3.3V 128K X 8 CMOS SRAM (Revolutionary pinout)

### Features

- AS7C1025A (5V version)
- AS7C31025A (3.3V version)
- Industrial and commercial temperatures
- Organization: 131,072 x 8 bits
- High speed
  - 10/10/12/15/20 ns address access time
- 3/3/4/5 ns output enable access time
- Low power consumption: ACTIVE
  - 660 mW (AS7C1025A) / max @ 10 ns (5V)
  - 324 mW (AS7C31025A) / max @ 10 ns (3.3V)
- Low power consumption: STANDBY
  - 55 mW (AS7C1025A) / max CMOS (5V)
  - 36 mW (AS7C31025A) / max CMOS (3.3V)

# Logic block diagram



### Selection guide

AS7C1025A-10 AS7C1025A-12 AS7C1025A-15 AS7C1025A-20 AS7C31025A-10 AS7C31025A-12 AS7C31025A-15 AS7C31025A-20 Unit Maximum address access time 10 12 15 20 ns Maximum output enable access 3 3 4 5 ns time Maximum AS7C1025A 120 110 100 100 mA operating 90 AS7C31025A 80 80 80 mA current Maximum AS7C1025A 10 10 10 15 mA CMOS standby AS7C31025A 10 10 10 15 mА current

2/6/01; V.0.9

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P. 1 of 8

- Latest 6T 0.25u CMOS technology
- 2.0V data retention
- Easy memory expansion with  $\overline{CE}$ ,  $\overline{OE}$  inputs
- Center power and ground
- TTL/LVTTL-compatible, three-state I/O
- JEDEC-standard packages
- 32-pin, 300 mil SOJ
- 32-pin, 400 mil SOJ
- 32-pin, TSOP II
- ESD protection  $\geq 2000$  volts
- Latch-up current  $\geq 200 \text{ mA}$

#### Pin arrangement

32-pin A0 1 A1 2 A2 3 A3 4 CE 5 I/O0 6 I/O1 7 V <sub>CC</sub> 8 GND 9 I/O2 10 I/O3 11 WE 12 A4 13 A5 14 A6 15 A7 16	Alto Alto Alto Alto Alto Alto Alto Alto	
32-pin So 32-pin So 32-pin So 32-pin So 32-pin So 33-pin So 33-pin So 33-pin So 32-pin So 33-pin So 32-pin	OJ (300 mil) OJ (400 mil) 31 A15 30 A14 29 CF 28 CF 29 CF 29 CF 29 CF 29 CF 29 CF 20	5

### Functional description

The AS7C1025A and AS7C31025A are high-performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) devices organized as 131,072 x 8 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

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Equal address access and cycle times ( $t_{AA}$ ,  $t_{RC}$ ,  $t_{WC}$ ) of 10/12/15/20 ns with output enable access times ( $t_{OE}$ ) of 3/3/4/5 ns are ideal for high-performance applications. The chip enable input  $\overline{CE}$  permits easy memory and expansion with multiple-bank memory systems.

When  $\overline{CE}$  is high the devices enter standby mode. The standard AS7C1025A is guaranteed not to exceed 55 mW power consumption in standby mode. Both devices also offer 2.0V data retention.

A write cycle is accomplished by asserting write enable ( $\overline{WE}$ ) and chip enable ( $\overline{CE}$ ). Data on the input pins I/O0-I/O7 is written on the rising edge of  $\overline{WE}$  (write cycle 1) or  $\overline{CE}$  (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ( $\overline{OE}$ ) or write enable ( $\overline{WE}$ ).

A read cycle is accomplished by asserting output enable ( $\overline{\text{OE}}$ ) and chip enable ( $\overline{\text{CE}}$ ), with write enable ( $\overline{\text{WE}}$ ) high. The chips drive I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5V supply (AS7C1025A) or 3.3V supply (AS7C31025A). The AS7C1025A and AS7C31025A are packaged in common industry standard packages.

### Absolute maximum ratings

Parameter	Device	Symbol	Min	Max	Unit
Voltage on V <sub>CC</sub> relative to GND	AS7C1025A	V <sub>t1</sub>	-0.50	+7.0	V
voltage on ver relative to Grup	AS7C31025A	V <sub>t1</sub>	-0.50	+5.0	V
Voltage on any pin relative to GND		V <sub>t2</sub>	-0.50	$V_{CC} + 0.5$	V
Power dissipation		P <sub>D</sub>	_	1.0	W
Storage temperature (plastic)	-	T <sub>stg</sub>	-65	+150	°C
Ambient temperature with V <sub>CC</sub> applied		T <sub>bias</sub>	-55	+125	°C
DC current into outputs (low)		I <sub>OUT</sub>	_	20	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### Truth table

CE	WE	ŌĒ	Data	Mode
Н	Х	Х	High Z	Standby (I <sub>SB</sub> , I <sub>SB1</sub> )
L	Н	Н	High Z	Output disable (I <sub>CC</sub> )
L	Н	L	D <sub>OUT</sub>	Read (I <sub>CC</sub> )
L	L	Х	D <sub>IN</sub>	Write (I <sub>CC</sub> )

Key: X = Don't Care, L = Low, H = High

# Recommended operating conditions

Parameter	Device	Symbol	Min	Nominal	Max	Unit
Supply voltage	AS7C1025A	V <sub>CC</sub>	4.5	5.0	5.5	V
Supply voltage	AS7C31025A	V <sub>CC</sub>	3.0	3.3	3.6	V
	AS7C1025A	V <sub>IH</sub>	2.2	_	$V_{CC} + 0.5$	V
Input voltage	AS7C31025A	V <sub>IH</sub>	2.0	-	$V_{CC} + 0.5$	V
	Both	v <sub>IL</sub> †	-0.5	-	0.8	V
Ambient operating temperature	commercial	T <sub>A</sub>	0	-	70	°C
Ambient operating temperature	industrial	T <sub>A</sub>	-40	—	85	°C

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 ${\rm \bar{t}}_{V_{IL}\,min.}$  = -3.0V for pulse width less than  $t_{RC}/2.$ 

# DC operating characteristics (over the operating range) $^{I}$

		landeteristics (over the open		-1	10	- 1	12	-1	5	-20		
Parameter	Sym	Test conditions	Device	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input leakage current	I <sub>LI</sub>	$V_{CC} = Max$ , $V_{IN} = GND$ to $V_{CC}$	Both	_	1	_	1	_	1	_	1	μА
Output leakage current	I <sub>LO</sub>	$V_{CC} = Max, \overline{CE} = V_{IH}, V_{out} = GND$ to $V_{CC}$	Both	_	1	_	1	_	1	-	1	μΑ
Operating			AS7C1025A	-	120	_	110	-	100	-	100	
power supply current	supply I <sub>CC</sub> CE	$\overline{\text{CE}} = \text{V}_{\text{IL}},  \text{f} = \text{f}_{\text{Max}},  \text{I}_{\text{OUT}} = 0   \text{mA}$	AS7C31025A	_	90	-	80	-	80	-	80	mA
Standby	т	$\overline{\text{CE}} = \text{V}_{\text{IH}}, \text{ f} = \text{f}_{\text{Max}}, \text{ f}_{\text{OUT}} = 0$	AS7C1025A	-	30	—	25	-	20	-	20	mA
power	I <sub>SB</sub>	$CE = V_{IH}, I = I_{Max}, I_{OUT} = 0$	AS7C31025A	-	30	_	25	-	20	Ι	20	IIIA
supply current <sup>1</sup>	т	$\overline{\text{CE}} \ge \text{V}_{\text{CC}}$ -0.2V, $\text{V}_{\text{IN}} \le 0.2$ V or $\text{V}_{\text{IN}}$	AS7C1025A	-	10	_	10	-	10	Ι	15	mA
current	I <sub>SB1</sub>	$\geq$ V <sub>CC</sub> –0.2V, f = 0, f <sub>OUT</sub> = 0	AS7C31025A	-	10	_	10	-	10	Ι	15	IIIA
Output	V <sub>OL</sub>	$I_{OL} = 8$ mA, $V_{CC} = Min$	AS7C1025A	-	.04	_	0.4	-	0.4	-	0.4	V
voltage	V <sub>OH</sub>	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$	AS7C31025A	2.4		2.4	-	2.4	_	2.4	-	V
		$V_{CC} = 2.0V$	AS7C1025A	-	1	—	1	_	1		5	mA
Data retention current	I <sub>CCDR</sub>	$\label{eq:VCC} \begin{split} \overline{\text{CE}} &\geq \text{V}_{\text{CC}} - 0.2 \text{V} \\ \text{V}_{\text{IN}} &\geq \text{V}_{\text{CC}} - 0.2 \text{V} \text{ or} \\ \text{V}_{\text{IN}} &\leq 0.2 \text{V} \end{split}$	AS7C31025A	_	1	_	1	_	1	_	5	mA

# Capacitance (f = 1 MHz, $T_a = 25$ °C, $V_{CC} = \text{NOMINAL})^2$

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C <sub>IN</sub>	A, $\overline{CE}$ , $\overline{WE}$ , $\overline{OE}$	$V_{IN} = 0V$	5	pF
I/O capacitance	C <sub>I/O</sub>	I/O	$V_{IN} = V_{OUT} = 0V$	7	pF

# Read cycle (over the operating range)<sup>3,9</sup>

		-10		-1	2	- 1	15	-2	-20		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t <sub>RC</sub>	10	-	12	-	15	—	20	-	ns	
Address access time	t <sub>AA</sub>	-	10	-	12	-	15	-	20	ns	3
Chip enable $(\overline{CE})$ access time	t <sub>ACE</sub>	—	10	_	12	_	15	-	20	ns	3
Output enable $(\overline{OE})$ access time	t <sub>OE</sub>	_	3	_	3	_	4	_	5	ns	
Output hold from address change	t <sub>OH</sub>	2	-	3	-	3	-	3	-	ns	5
$\overline{CE}$ Low to output in low Z	t <sub>CLZ</sub>	0	_	0	_	0	-	0	_	ns	4,5
CE Low to output in high Z	t <sub>CHZ</sub>	-	3	_	3	-	4	_	5	ns	4,5
$\overline{OE}$ Low to output in low Z	t <sub>OLZ</sub>	0	—	0	—	0	-	0	-	ns	4,5
OE High to output in high Z	t <sub>OHZ</sub>	—	3	-	3	_	4	-	5	ns	4,5
Power up time	t <sub>PU</sub>	0	-	0	-	0	_	0	_	ns	4,5
Power down time	t <sub>PD</sub>	-	10	_	12	_	15	_	20	ns	4,5
Read waveform 1 (address con Address	t <sub>AA</sub>	t <sub>RC</sub>			ta valid	t <sub>OH</sub>					
D <sub>OUT</sub> D <sub>OUT</sub> t <sub>ACE</sub> t <sub>CLZ</sub> Supply current	t <sub>OE</sub>	→ →		Data val	id +		toHz tcHz D 50%				I <sub>CC</sub> I <sub>SB</sub>

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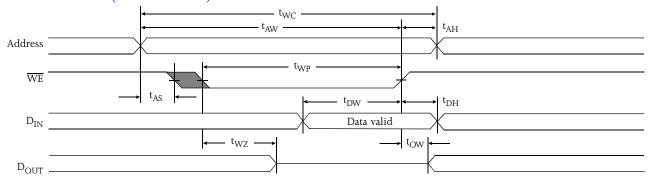
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		-1	10 -12 -15		15	-20					
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t <sub>WC</sub>	10		12	_	15	_	20	_	ns	
Chip enable $(\overline{CE})$ to write end	t <sub>CW</sub>	8		10	-	12	_	12	_	ns	
Address setup to write end	t <sub>AW</sub>	8		9	_	10	_	12	_	ns	
Address setup time	t <sub>AS</sub>	0		0	-	0	—	0	_	ns	
Write pulse width	t <sub>WP</sub>	7		8	-	9	_	12	_	ns	
Address hold from end of write	t <sub>AH</sub>	0		0	_	0	_	0	_	ns	
Data valid to write end	t <sub>DW</sub>	5		6	_	8	_	10	_	ns	
Data hold time	t <sub>DH</sub>	0		0	-	0	_	0	_	ns	4,5
Write enable to output in high Z	t <sub>WZ</sub>		6	_	6	_	6	—	8	ns	4,5
Output active from write end	t <sub>OW</sub>	1		1	—	1	—	2	—	ns	4,5

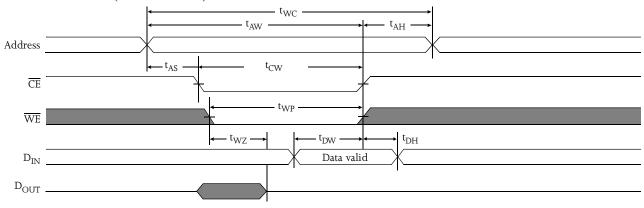
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# Write cycle (over the operating range)<sup>11</sup>

# Write waveform 1 ( $\overline{\text{WE}}$ controlled)<sup>10,11</sup>



# Write waveform 2 $(\overline{\text{CE}} \text{ controlled})^{10,11}$



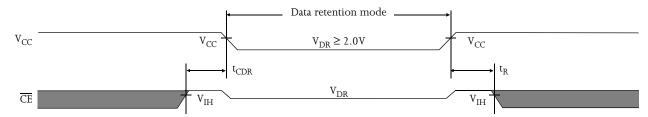
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### Data retention characteristics (over the operating range)

Parameter	Symbol	Test conditions	Min	Max	Unit
V <sub>CC</sub> for data retention	V <sub>DR</sub>	V = 2.0V	2.0	_	V
Data retention current	I <sub>CCDR</sub>	$V_{CC} = 2.0V$	_	500	μΑ
Chip enable to data retention time	t <sub>CDR</sub>	$\overline{\text{CE}} \ge \text{V}_{\text{CC}} - 0.2 \text{V}$	0	-	ns
Operation recovery time	t <sub>R</sub>	$V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$	t <sub>RC</sub>	-	ns
Input leakage current	I <sub>LI</sub>	, IN = 0.2 (	_	1	μΑ

### Data retention waveform



+ 5 V

480W

C(14)

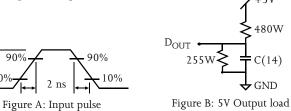
GND

## AC test conditions

+3.0V -

GND

- Output load: see Figure B or Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.



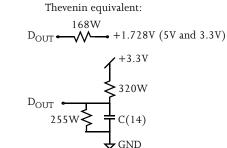


Figure C: 3.3V Output load

### Notes

- During  $V_{CC}$  power-up, a pull-up resistor to  $V_{CC}$  on  $\overline{CE}$  is required to meet  $I_{SB}$  specification. 1
- This parameter is sampled, but not 100% tested. 2

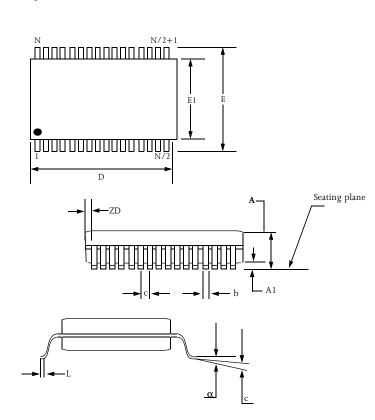
90%

- For test conditions, see AC Test Conditions, Figures A, B, and C. 3
- $t_{CLZ}$  and  $t_{CHZ}$  are specified with CL = 5pF, as in Figure C. Transition is measured  $\pm$ 500mV from steady-state voltage. 4
- 5 This parameter is guaranteed, but not 100% tested.
- $\overline{\text{WE}}$  is High for read cycle. 6
- 7  $\overline{CE}$  and  $\overline{OE}$  are Low for read cycle.
- Address valid prior to or coincident with  $\overline{\text{CE}}$  transition Low. 8
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- CE or WE must be High during address transitions. Either CE or WE asserting high terminates a write cycle. 10
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 NA.
- 13 C=30pF, except all high Z and low Z parameters, where C=5pF.

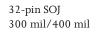
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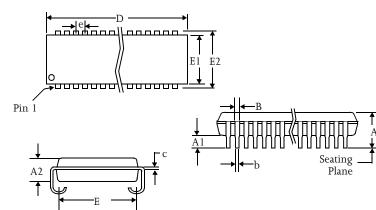
# Package dimensions

32-pin TSOP II



	32-pin TSOP II (mm)						
Symbol	Min	Max					
А	-	1.2					
A1	0.05	0.15					
b	0.3	0.52					
С	0.12	0.21					
D	20.82	21.08					
E1	10.03	10.29					
Е	11.56	11.96					
е	1.27	BSC					
L	0.40	0.60					
ZD	0.95 REF.						
α	0°	5°					





	32-pi 300	n SOJ mil	32-pin SOJ 400 mil		
Symbol	Min Max		Min	Max	
Α	-	0.145	-	0.145	
A1	0.025	-	0.025	-	
A2	0.086	0.105	0.086	0.115	
В	0.026	0.032	0.026	0.032	
b	0.014	0.020	0.015	0.020	
С	0.006	0.013	0.007	0.013	
D	0.820	0.830	0.820	0.830	
E	0.250	0.275	0.360	0.380	
E1	0.292	0.305	0.395	0.405	
E2	0.330	0.340	0.435	0.445	
e	0.050	) BSC	0.050 BSC		

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### Ordering codes

Package \ Access time	Voltage	Temperature	10 ns	12 ns	15 ns	20 ns
		Commercial	AS7C1025A-10TC	AS7C1025A-12TC	AS7C1025A-15TC	AS7C1025A-20TC
TSOD II		Industrial	AS7C1025A-10TI	AS7C1025A-12TI	AS7C1025A-15TI	AS7C1025A-20TI
150F II		Commercial	AS7C31025A-10TC	AS7C31025A-12TC	AS7C31025A-15TC	AS7C31025A-20TC
3.3 V	3.3 V	Industrial	AS7C31025A-10TI	AS7C31025A-12TI	AS7C31025A-15TI	AS7C31025A-20TI
EN	5V	Commercial	AS7C1025A-10TJC	AS7C1025A-12TJC	AS7C1025A-15TJC	AS7C1025A-20TJC
300-mil SOJ	51	Industrial	AS7C1025A-10TJI	AS7C1025A-12TJI	AS7C1025A-15TJI	AS7C1025A-20TJI
300-1111 305	3.3V	Commercial	AS7C31025A-10TJC	AS7C31025A-12TJC	AS7C31025A-15TJC	AS7C31025A-20TJC
	5.5 V	Industrial	AS7C31025A-10TJI	AS7C31025A-12TJI	AS7C31025A-15TJI	AS7C31025A-20TJI
	5V	Commercial	AS7C1025A-10JC	AS7C1025A-12JC	AS7C1025A-15JC	AS7C1025A-20JC
400-mil SOJ	51	Industrial	AS7C1025A-10JI	AS7C1025A-12JI	AS7C1025A-15JI	AS7C1025A-20JI
	3.3V	Commercial	AS7C31025A-10JC	AS7C31025A-12JC	AS7C31025A-15JC	AS7C31025A-20JC
	5.5 v	Industrial	AS7C31025A-10JI	AS7C31025A-12JI	AS7C31025A-15JI	AS7C31025A-20JI

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## Part numbering system

AS7C	X	1025	-XX	X	х
SRAM prefix	Blank=5V CMOS 3=3.3V CMOS	Device number	Access time		Temperature range C = Commercial, 0°C to 70°C I = Industrial, -40°C to 85°C

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