

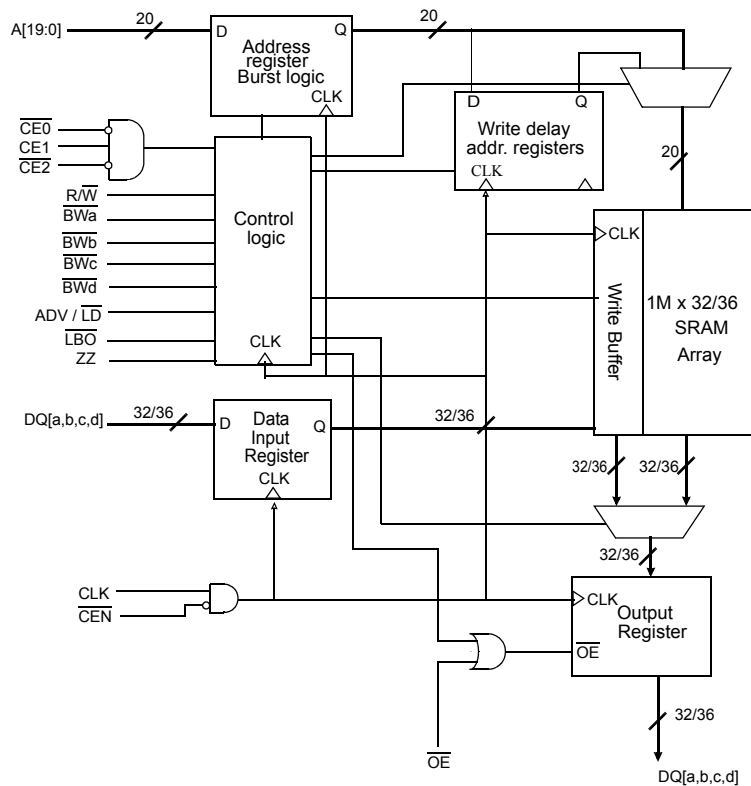


3.3V 1M × 32/36 Pipelined SRAM with NTD™

Features

- Organization: 1,048,576 words × 32 or 36 bits
- NTD™ architecture for efficient bus operation
- Fast clock speeds to 200 MHz
- Fast clock to data access: 3.2/3.5/3.8 ns
- Fast OE access time: 3.2/3.5/3.8 ns
- Fully synchronous operation
- Asynchronous output enable control
- Available in 100-pin TQFP packages
- Byte write enables
- Clock enable for operation hold
- Multiple chip enables for easy expansion
- 3.3V core power supply
- 2.5V or 3.3V I/O operation with separate V_{DDQ}
- Self-timed write cycles
- Interleaved or linear burst modes
- Snooze mode for standby operation

Logic block diagram



Selection guide

| | -200 | -166 | -133 | Units |
|-----------------------------------|------|------|------|-------|
| Minimum cycle time | 5 | 6 | 7.5 | ns |
| Maximum clock frequency | 200 | 166 | 133 | MHz |
| Maximum clock access time | 3.2 | 3.5 | 3.8 | ns |
| Maximum operating current | 450 | 400 | 350 | mA |
| Maximum standby current | 170 | 150 | 140 | mA |
| Maximum CMOS standby current (DC) | 90 | 90 | 90 | mA |



32 Mb Synchronous SRAM products list^{1,2}

| Org | Part Number | Mode | Speed |
|-------|----------------|--------|-----------------|
| 2MX18 | AS7C332MPFS18A | PL-SCD | 200/166/133 MHz |
| 1MX32 | AS7C331MPFS32A | PL-SCD | 200/166/133 MHz |
| 1MX36 | AS7C331MPFS36A | PL-SCD | 200/166/133 MHz |
| 2MX18 | AS7C332MPFD18A | PL-DCD | 200/166/133 MHz |
| 1MX32 | AS7C331MPFD32A | PL-DCD | 200/166/133 MHz |
| 1MX36 | AS7C331MPFD36A | PL-DCD | 200/166/133 MHz |
| 2MX18 | AS7C332MFT18A | FT | 7.5/8.5/10 ns |
| 1MX32 | AS7C331MFT32A | FT | 7.5/8.5/10 ns |
| 1MX36 | AS7C331MFT36A | FT | 7.5/8.5/10 ns |
| 2MX18 | AS7C332MNTD18A | NTD-PL | 200/166/133 MHz |
| 1MX32 | AS7C331MNTD32A | NTD-PL | 200/166/133 MHz |
| 1MX36 | AS7C331MNTD36A | NTD-PL | 200/166/133 MHz |
| 2MX18 | AS7C332MNTF18A | NTD-FT | 7.5/8.5/10 ns |
| 1MX32 | AS7C331MNTF32A | NTD-FT | 7.5/8.5/10 ns |
| 1MX36 | AS7C331MNTF36A | NTD-FT | 7.5/8.5/10 ns |

1 Core Power Supply: VDD = 3.3V ± 0.165V

2 I/O Supply Voltage: VDDQ = 3.3V ± 0.165V for 3.3V I/O
VDDQ = 2.5V ± 0.125V for 2.5V I/O

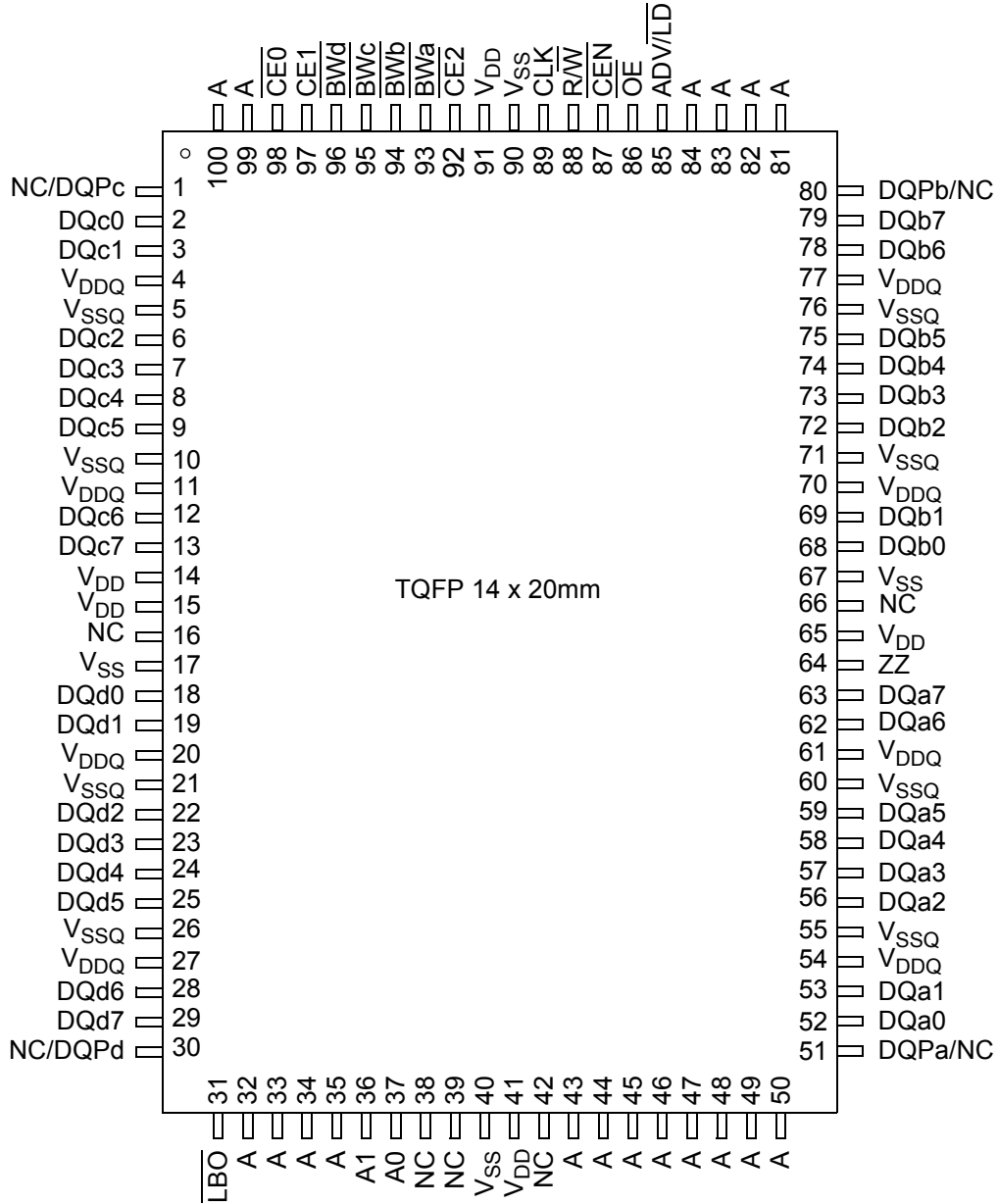
- PL-SCD : Pipelined Burst Synchronous SRAM - Single Cycle Deselect
- PL-DCD : Pipelined Burst Synchronous SRAM - Double Cycle Deselect
- FT : Flow-through Burst Synchronous SRAM
- NTD¹-PL : Pipelined Burst Synchronous SRAM with NTDTM
- NTD-FT : Flow-through Burst Synchronous SRAM with NTDTM

1. NTD: No Turnaround Delay. NTDTM is a trademark of Alliance Semiconductor Corporation. All trademarks mentioned in this document are the property of their respective owners.



Pin assignment

100-pin TQFP - top view



Note: For pins 1, 30, 51, and 80, NC applies to the x32 configuration.
DQPn applies to the x36 configuration.



Functional description

The AS7C331MNTD32A/36A family is a high performance CMOS 32 Mbit Synchronous Static Random Access Memory (SRAM) organized as 1,048,576 words \times 32 or 36 bits and incorporates a LATE LATE Write.

This variation of the 32Mb synchronous SRAM uses the No Turnaround Delay (NTD™) architecture, featuring an enhanced write operation that improves bandwidth over pipelined burst devices. In a normal pipelined burst device, the write data, command, and address are all applied to the device on the same clock edge. If a read command follows this write command, the system must wait for two 'dead' cycles for valid data to become available. These dead cycles can significantly reduce overall bandwidth for applications requiring random access or read-modify-write operations.

NTD™ devices use the memory bus more efficiently by introducing a write latency which matches the two-cycle pipelined or one-cycle flow-through read latency. Write data is applied two cycles after the write command and address, allowing the read pipeline to clear. With NTD™, write and read operations can be used in any order without producing dead bus cycles.

Assert R/\overline{W} low to perform write cycles. Byte write enable controls write access to specific bytes, or can be tied low for full 32/36 bit writes. Write enable signals, along with the write address, are registered on a rising edge of the clock. Write data is applied to the device two clock cycles later. Unlike some asynchronous SRAMs, output enable \overline{OE} does not need to be toggled for write operations; it can be tied low for normal operations. Outputs go to a high impedance state when the device is de-selected by any of the three chip enable inputs. In pipelined mode, a two cycle deselect latency allows pending read or write operations to be completed.

Use the ADV (burst advance) input to perform burst read, write and deselect operations. When ADV is high, external addresses, chip select, R/\overline{W} pins are ignored, and internal address counters increment in the count sequence specified by the \overline{LBO} control. Any device operations, including burst, can be stalled using the $\overline{CEN}=1$, the clock enable input.

The AS7C331MNTD32A/36A operates with a $3.3V \pm 5\%$ power supply for the device core (V_{DD}). DQ circuits use a separate power supply (V_{DDQ}) that operates across 3.3V or 2.5V ranges. These devices are available in a 100-pin TQFP.

TQFP Capacitance

| Parameter | Symbol | Test conditions | Min | Max | Unit |
|-------------------|-------------|-------------------------|-----|-----|------|
| Input capacitance | C_{IN}^* | $V_{in} = 0V$ | - | 5 | pF |
| I/O capacitance | $C_{I/O}^*$ | $V_{in} = V_{out} = 0V$ | - | 7 | pF |

* Guaranteed not tested

TQFP thermal resistance

| Description | Conditions | | Symbol | Typical | Units |
|---|---|---------|---------------|---------|-------|
| Thermal resistance (junction to ambient) ¹ | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51 | 1-layer | θ_{JA} | 40 | °C/W |
| | | 4-layer | θ_{JA} | 22 | °C/W |
| Thermal resistance (junction to top of case) ¹ | | | θ_{JC} | 8 | °C/W |

¹ This parameter is sampled



Signal descriptions

| Signal | I/O | Properties | Description |
|--------------------------------|-----|------------|---|
| CLK | I | CLOCK | Clock. All inputs except \overline{OE} , \overline{LBO} , and ZZ are synchronous to this clock. |
| \overline{CEN} | I | SYNC | Clock enable. When de-asserted high, the clock input signal is masked. |
| A, A0, A1 | I | SYNC | Address. Sampled when all chip enables are active and $\overline{ADV/LD}$ is asserted. |
| DQ[a,b,c,d] | I/O | SYNC | Data. Driven as output when the chip is enabled and \overline{OE} is active. |
| $\overline{CE0}$, CE1, CE2 | I | SYNC | Synchronous chip enables. Sampled at the rising edge of CLK, when $\overline{ADV/LD}$ is asserted. Are ignored when $\overline{ADV/LD}$ is high. |
| $\overline{ADV/LD}$ | I | SYNC | Advance or Load. When sampled high, the internal burst address counter will increment in the order defined by the \overline{LBO} input value. When low, a new address is loaded. |
| R/ \overline{W} | I | SYNC | A high during LOAD initiates a READ operation. A low during LOAD initiates a WRITE operation. Is ignored when $\overline{ADV/LD}$ is high. |
| $\overline{BW[a,b,c,d]}$ | I | SYNC | Byte write enables. Used to control write on individual bytes. Sampled along with WRITE command and BURST WRITE. |
| \overline{OE} | I | ASYNC | Asynchronous output enable. I/O pins are not driven when \overline{OE} is inactive. |
| \overline{LBO} | I | STATIC | Selects Burst mode. When tied to V_{DD} or left floating, device follows interleaved Burst order. When driven Low, device follows linear Burst order. <i>This signal is internally pulled High.</i> |
| ZZ | I | ASYNC | Snooze. Places device in low power mode; data is retained. Connect to GND if unused. |
| NC | - | - | No connect |

Snooze Mode

SNOOZE MODE is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2} . The duration of SNOOZE MODE is dictated by the length of time the ZZ is in a High state.

The ZZ pin is an asynchronous, active high input that causes the device to enter SNOOZE MODE.

When the ZZ pin becomes a logic High, I_{SB2} is guaranteed after the time t_{ZZI} is met. After entering SNOOZE MODE, all inputs except ZZ is disabled and all outputs go to High-Z. Any operation pending when entering SNOOZE MODE is not guaranteed to successfully complete. Therefore, SNOOZE MODE (READ or WRITE) must not be initiated until valid pending operations are completed. Similarly, when exiting SNOOZE MODE during t_{PUS} , only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SNOOZE MODE.



Burst order

| Interleaved burst order $\overline{\text{LBO}} = 1$ | | | | | Linear burst order $\overline{\text{LBO}} = 0$ | | | | |
|---|-------|-------|-------|-------|--|-------|-------|-------|-------|
| | A1 A0 | A1 A0 | A1 A0 | A1 A0 | | A1 A0 | A1 A0 | A1 A0 | A1 A0 |
| Starting address | 0 0 | 0 1 | 1 0 | 1 1 | Starting Address | 0 0 | 0 1 | 1 0 | 1 1 |
| First increment | 0 1 | 0 0 | 1 1 | 1 0 | First increment | 0 1 | 1 0 | 1 1 | 0 0 |
| Second increment | 1 0 | 1 1 | 0 0 | 0 1 | Second increment | 1 0 | 1 1 | 0 0 | 0 1 |
| Third increment | 1 1 | 1 0 | 0 1 | 0 0 | Third increment | 1 1 | 0 0 | 0 1 | 1 0 |

Synchronous truth table^[5,6,7,8,9,11]

| $\overline{\text{CE0}}$ | CE1 | $\overline{\text{CE2}}$ | $\overline{\text{ADV/LD}}$ | R/W | $\overline{\text{BWn}}$ | $\overline{\text{OE}}$ | $\overline{\text{CEN}}$ | Address source | CLK | Operation | DQ | Notes |
|-------------------------|--------------|-------------------------|----------------------------|--------------|-------------------------|------------------------|-------------------------|----------------|--------|-------------------------------|--------|----------|
| H | X | X | L | X | X | X | L | NA | L to H | DESELECT Cycle | High-Z | |
| X | X | H | L | X | X | X | L | NA | L to H | DESELECT Cycle | High-Z | |
| X | L | X | L | X | X | X | L | NA | L to H | DESELECT Cycle | High-Z | |
| X | X | X | H | X | X | X | L | NA | L to H | CONTINUE DESELECT Cycle | High-Z | 1 |
| L | H | L | L | H | X | L | L | External | L to H | READ Cycle (Begin Burst) | Q | |
| X | X | X | H | X | X | L | L | Next | L to H | READ Cycle (Continue Burst) | Q | 1,10 |
| L | H | L | L | H | X | H | L | External | L to H | NOP/DUMMY READ (Begin Burst) | High-Z | 2 |
| X | X | X | H | X | X | H | L | Next | L to H | DUMMY READ (Continue Burst) | High-Z | 1,2,10 |
| L | H | L | L | L | L | X | L | External | L to H | WRITE CYCLE (Begin Burst) | D | 3 |
| X | X | X | H | X | L | X | L | Next | L to H | WRITE CYCLE (Continue Burst) | D | 1,3,10 |
| L | H | L | L | L | H | X | L | External | L to H | NOP/WRITE ABORT (Begin Burst) | High-Z | 2,3 |
| X | X | X | H | X | H | X | L | Next | L to H | WRITE ABORT (Continue Burst) | High-Z | 1,2,3,10 |
| X | X | X | X | X | X | X | H | Current | L to H | INHIBIT CLOCK | - | 4 |

Key: X = Don't Care, H = HIGH, L = LOW. $\overline{\text{BWn}} = \text{H}$ means all byte write signals ($\overline{\text{BWa}}$, $\overline{\text{BWb}}$, $\overline{\text{BWc}}$, and $\overline{\text{BWd}}$) are HIGH. $\overline{\text{BWn}} = \text{L}$ means one or more byte write signals are LOW.

Notes:

1 CONTINUE BURST cycles, whether READ or WRITE, use the same control inputs. The type of cycle performed (READ or WRITE) is chosen in the initial BEGIN BURST cycle. A CONTINUE DESELECT cycle can only be entered if a DESELECT CYCLE is executed first.

2 DUMMY READ and WRITE ABORT cycles can be considered NOPs because the device performs no external operation. A WRITE ABORT means a WRITE command is given, but no operation is performed.

3 $\overline{\text{OE}}$ may be wired LOW to minimize the number of control signals to the SRAM. The device will automatically turn off the output drivers during a WRITE cycle. $\overline{\text{OE}}$ may be used when the bus turn-on and turn-off times do not meet an application's requirements.

4 If an INHIBIT CLOCK command occurs during a READ operation, the DQ bus will remain active (Low-Z). If it occurs during a WRITE cycle, the bus will remain in High-Z. No WRITE operations will be performed during the INHIBIT CLOCK cycle.

5 $\overline{\text{BWa}}$ enables WRITES to byte "a" (DQa pins); $\overline{\text{BWb}}$ enables WRITES to byte "b" (DQb pins); $\overline{\text{BWc}}$ enables WRITES to byte "c" (DQc pins); $\overline{\text{BWd}}$ enables WRITES to byte "d" (DQd pins).

6 All inputs except $\overline{\text{OE}}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.

7 Wait states are inserted by setting $\overline{\text{CEN}}$ HIGH.

8 This device contains circuitry that will ensure that the outputs will be in High-Z during power-up.

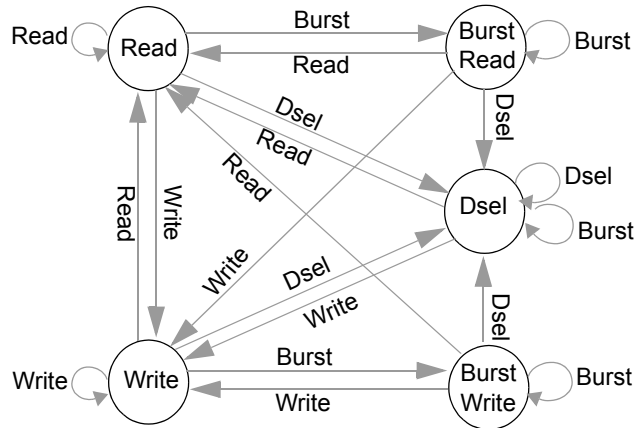
9 The device incorporates a 2-bit burst counter. Address wraps to the initial address every fourth BURST CYCLE.

10 The address counter is incremented for all CONTINUE BURST cycles.

11. ZZ pin is always Low in this truth table.



State diagram for NTD SRAM



Absolute maximum ratings

| Parameter | Symbol | Min | Max | Unit |
|--|-------------------|------|-----------------|------|
| Power supply voltage relative to GND | V_{DD}, V_{DDQ} | -0.5 | +4.6 | V |
| Input voltage relative to GND (input pins) | V_{IN} | -0.5 | $V_{DD} + 0.5$ | V |
| Input voltage relative to GND (I/O pins) | V_{IN} | -0.5 | $V_{DDQ} + 0.5$ | V |
| Power dissipation | P_d | - | 1.8 | W |
| Short circuit output current | I_{OUT} | - | 20 | mA |
| Storage temperature | T_{stg} | -65 | +150 | °C |
| Temperature under bias | T_{bias} | -65 | +135 | °C |

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.

Recommended operating conditions at 3.3V I/O

| Parameter | Symbol | Min | Nominal | Max | Unit |
|---------------------------|-----------|-------|---------|-------|------|
| Supply voltage for inputs | V_{DD} | 3.135 | 3.3 | 3.465 | V |
| Supply voltage for I/O | V_{DDQ} | 3.135 | 3.3 | 3.465 | V |
| Ground supply | V_{SS} | 0 | 0 | 0 | V |

Recommended operating conditions at 2.5V I/O

| Parameter | Symbol | Min | Nominal | Max | Unit |
|---------------------------|-----------|-------|---------|-------|------|
| Supply voltage for inputs | V_{DD} | 3.135 | 3.3 | 3.465 | V |
| Supply voltage for I/O | V_{DDQ} | 2.375 | 2.5 | 2.625 | V |
| Ground supply | V_{SS} | 0 | 0 | 0 | V |



DC electrical characteristics for 3.3V I/O operation

| Parameter | Sym | Conditions | Min | Max | Unit |
|------------------------------------|-----------------|--|--------|-----------------------|------|
| Input leakage current [†] | I _{LI} | V _{DD} = Max, 0V ≤ V _{IN} ≤ V _{DD} | -2 | 2 | μA |
| Output leakage current | I _{LO} | OE ≥ V _{IH} , V _{DD} = Max, 0V ≤ V _{OUT} ≤ V _{DDQ} | -2 | 2 | μA |
| Input high (logic 1) voltage | V _{IH} | Address and control pins | 2* | V _{DD} +0.3 | V |
| | | I/O pins | 2* | V _{DDQ} +0.3 | |
| Input low (logic 0) voltage | V _{IL} | Address and control pins | -0.3** | 0.8 | V |
| | | I/O pins | -0.5** | 0.8 | |
| Output high voltage | V _{OH} | I _{OH} = -4 mA, V _{DDQ} = 3.135V | 2.4 | - | V |
| Output low voltage | V _{OL} | I _{OL} = 8 mA, V _{DDQ} = 3.465V | - | 0.4 | V |

DC electrical characteristics for 2.5V I/O operation

| Parameter | Sym | Conditions | Min | Max | Unit |
|------------------------------------|-----------------|--|--------|-----------------------|------|
| Input leakage current [†] | I _{LI} | V _{DD} = Max, 0V ≤ V _{IN} ≤ V _{DD} | -2 | 2 | μA |
| Output leakage current | I _{LO} | OE ≥ V _{IH} , V _{DD} = Max, 0V ≤ V _{OUT} ≤ V _{DDQ} | -2 | 2 | μA |
| Input high (logic 1) voltage | V _{IH} | Address and control pins | 1.7* | V _{DD} +0.3 | V |
| | | I/O pins | 1.7* | V _{DDQ} +0.3 | V |
| Input low (logic 0) voltage | V _{IL} | Address and control pins | -0.3** | 0.7 | V |
| | | I/O pins | -0.3** | 0.7 | V |
| Output high voltage | V _{OH} | I _{OH} = -4 mA, V _{DDQ} = 2.375V | 1.7 | - | V |
| Output low voltage | V _{OL} | I _{OL} = 8 mA, V _{DDQ} = 2.625V | - | 0.7 | V |

[†] L \overline{B} O and ZZ pins have an internal pull-up or pull-down, and input leakage = ±10 μA.

*V_{IH} max < V_{DD} +1.5V for pulse width less than 0.2 X t_{CYC}

**V_{IL} min = -1.5 for pulse width less than 0.2 X t_{CYC}

I_{DD} operating conditions and maximum limits

| Parameter | Sym | Test conditions | -200 | -166 | -133 | Unit |
|---|------------------|---|------|------|------|------|
| Operating power supply current ¹ | I _{CC} | $\overline{CE0} \leq V_{IL}$, CE1 ≥ V _{IH} , $\overline{CE2} \leq V_{IL}$, f = f _{Max} , I _{OUT} = 0 mA, ZZ ≤ V _{IL} | 450 | 400 | 350 | mA |
| Standby power supply current | I _{SB} | All V _{IN} ≤ 0.2V or ≥ V _{DD} - 0.2V, Deselected, f = f _{Max} , ZZ ≤ V _{IL} | 170 | 150 | 140 | mA |
| | I _{SB1} | Deselected, f = 0, ZZ ≤ 0.2V, all V _{IN} ≤ 0.2V or ≥ V _{DD} - 0.2V | 90 | 90 | 90 | |
| | I _{SB2} | Deselected, f = f _{Max} , ZZ ≥ V _{DD} - 0.2V, all V _{IN} ≤ V _{IL} or ≥ V _{IH} | 80 | 80 | 80 | |

¹ I_{CC} given with no output loading. I_{CC} increases with faster cycle times and greater output loading.



Timing characteristics over operating range

| Parameter | Sym | -200 | | -166 | | -133 | | Unit | Notes ¹ |
|---|-------------------|------|-----|------|-----|------|-----|-------|--------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| Clock frequency | F _{MAX} | – | 200 | – | 166 | – | 133 | MHz | |
| Cycle time | t _{CYC} | 5 | – | 6 | – | 7.5 | – | ns | |
| Clock access time | t _{CD} | – | 3.2 | – | 3.5 | – | 3.8 | ns | |
| Output enable low to data valid | t _{OE} | – | 3.2 | – | 3.5 | – | 3.8 | ns | |
| Clock high to output low Z | t _{LZC} | 0 | – | 0 | – | 0 | – | ns | 2,3,4 |
| Data output invalid from clock high | t _{OH} | 1.5 | – | 1.5 | – | 1.5 | – | ns | 2 |
| Output enable low to output low Z | t _{LZOE} | 0 | – | 0 | – | 0 | – | ns | 2,3,4 |
| Output enable high to output high Z | t _{HZOE} | – | 3.0 | – | 3.4 | – | 3.8 | ns | 2,3,4 |
| Clock high to output high Z | t _{HZC} | – | 3.0 | – | 3.4 | – | 3.8 | ns | 2,3,4 |
| Output enable high to invalid output | t _{OHOE} | 0 | – | 0 | – | 0 | – | ns | |
| Clock high pulse width | t _{CH} | 2.0 | – | 2.4 | – | 2.4 | – | ns | 5 |
| Clock low pulse width | t _{CL} | 2.0 | – | 2.4 | – | 2.4 | – | ns | 5 |
| Address and Control setup to clock high | t _{AS} | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6 |
| Data setup to clock high | t _{DS} | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6 |
| Write setup to clock high | t _{WS} | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6, 7 |
| Chip select setup to clock high | t _{CSS} | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6, 8 |
| Address hold from clock high | t _{AH} | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6 |
| Data hold from clock high | t _{DH} | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6 |
| Write hold from clock high | t _{WH} | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6, 7 |
| Chip select hold from clock high | t _{CSH} | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6, 8 |
| Clock enable setup to clock high | t _{CENS} | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6 |
| Clock enable hold from clock high | t _{CENH} | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6 |
| ADV setup to clock high | t _{ADVS} | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6 |
| ADV hold from clock high | t _{ADVH} | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6 |
| ZZ High to Power down | t _{PDS} | 2 | – | 2 | – | 2 | – | cycle | |
| ZZ Low to Power up | t _{PUS} | 2 | – | 2 | – | 2 | – | cycle | |

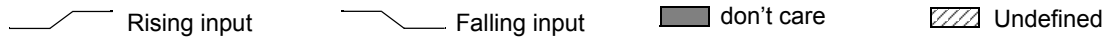
¹ See "Notes" on page 15

Snooze Mode Electrical Characteristics

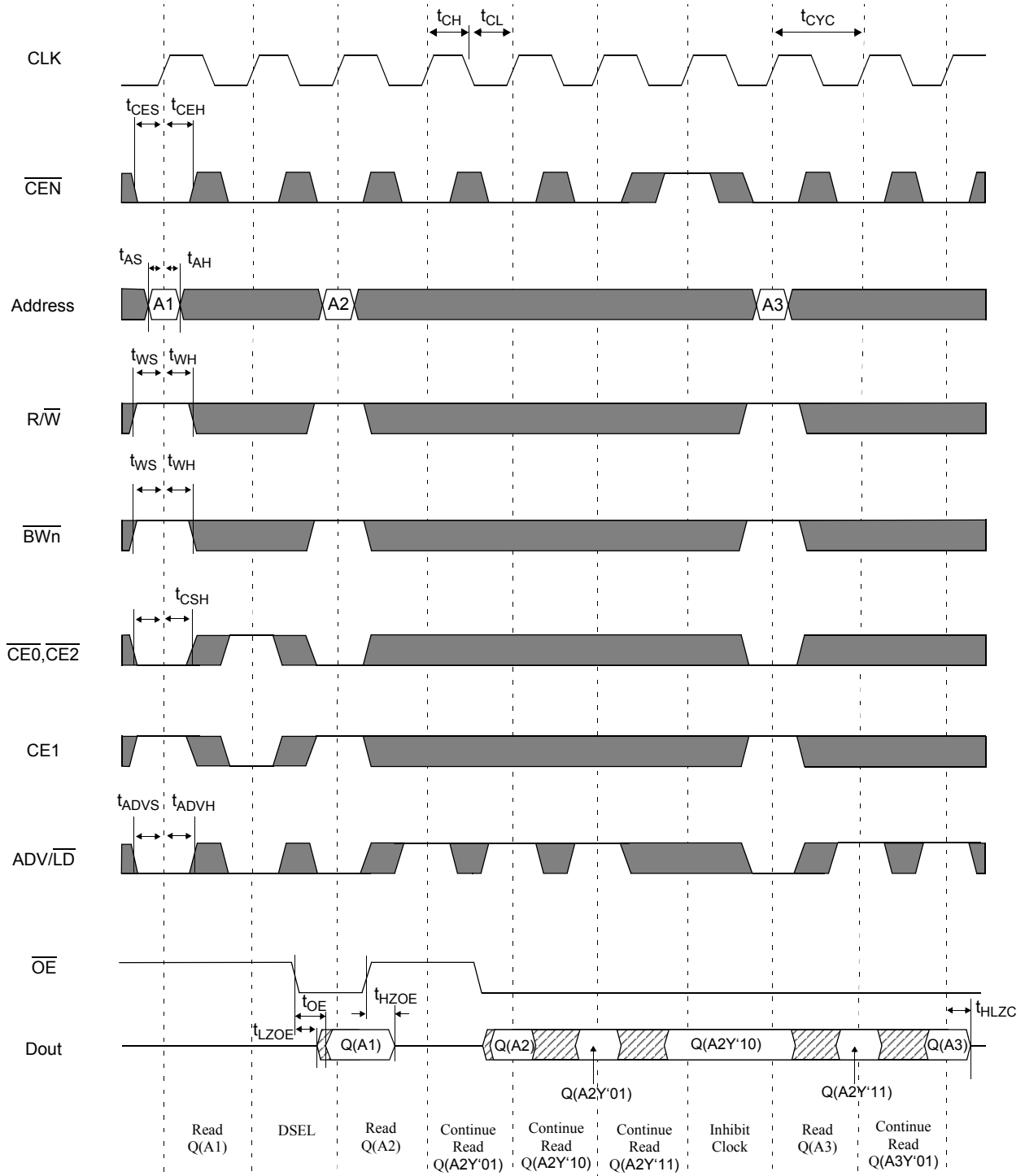
| Description | Conditions | Symbol | Min | Max | Units |
|------------------------------------|----------------------|-------------------|-----|-----|-------|
| Current during Snooze Mode | ZZ ≥ V _{IH} | I _{SB2} | | 80 | mA |
| ZZ active to input ignored | | t _{PDS} | 2 | | cycle |
| ZZ inactive to input sampled | | t _{PUS} | 2 | | cycle |
| ZZ active to SNOOZE current | | t _{ZZI} | | 2 | cycle |
| ZZ inactive to exit SNOOZE current | | t _{RZZI} | 0 | | |



Key to switching waveforms

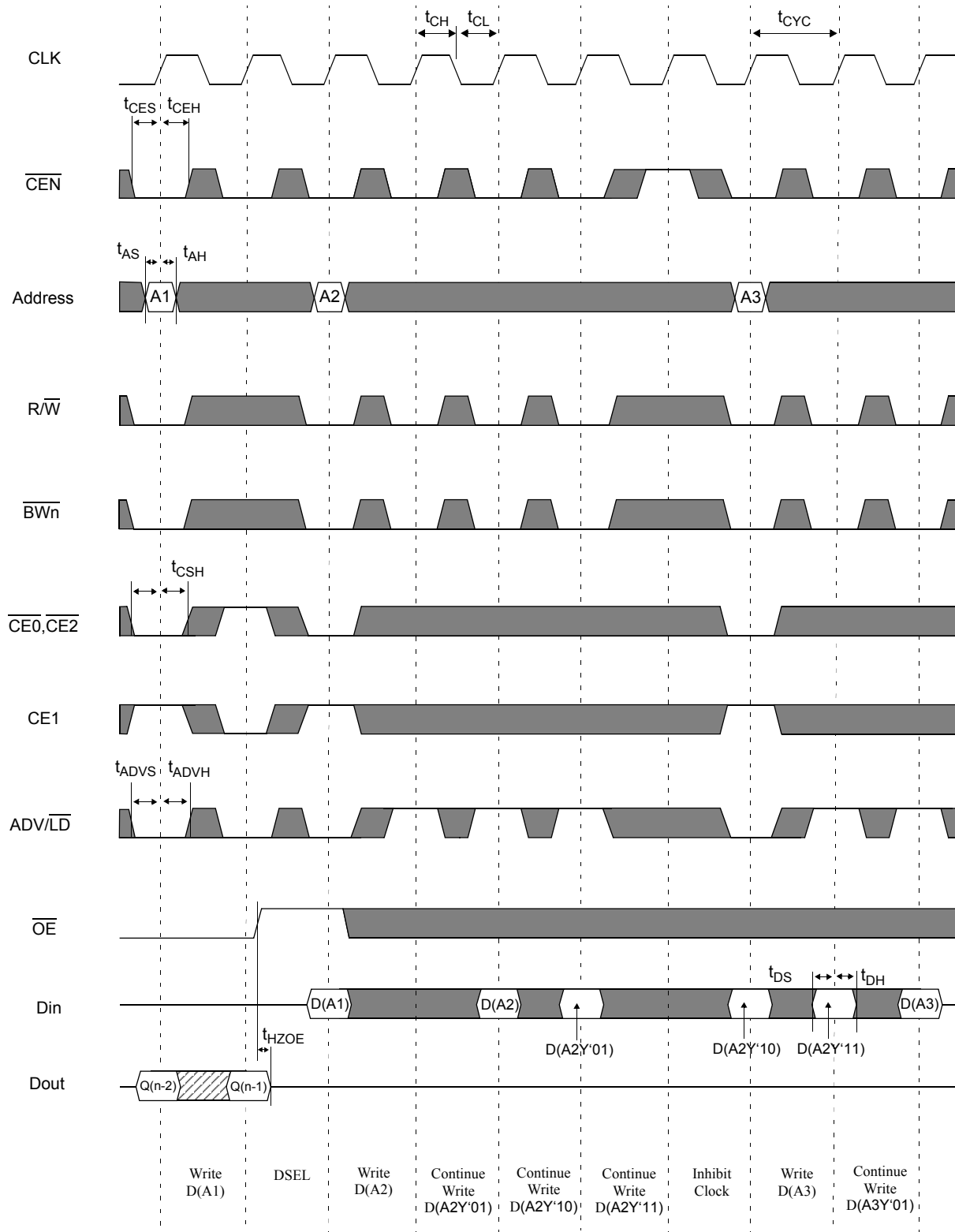


Timing waveform of read cycle



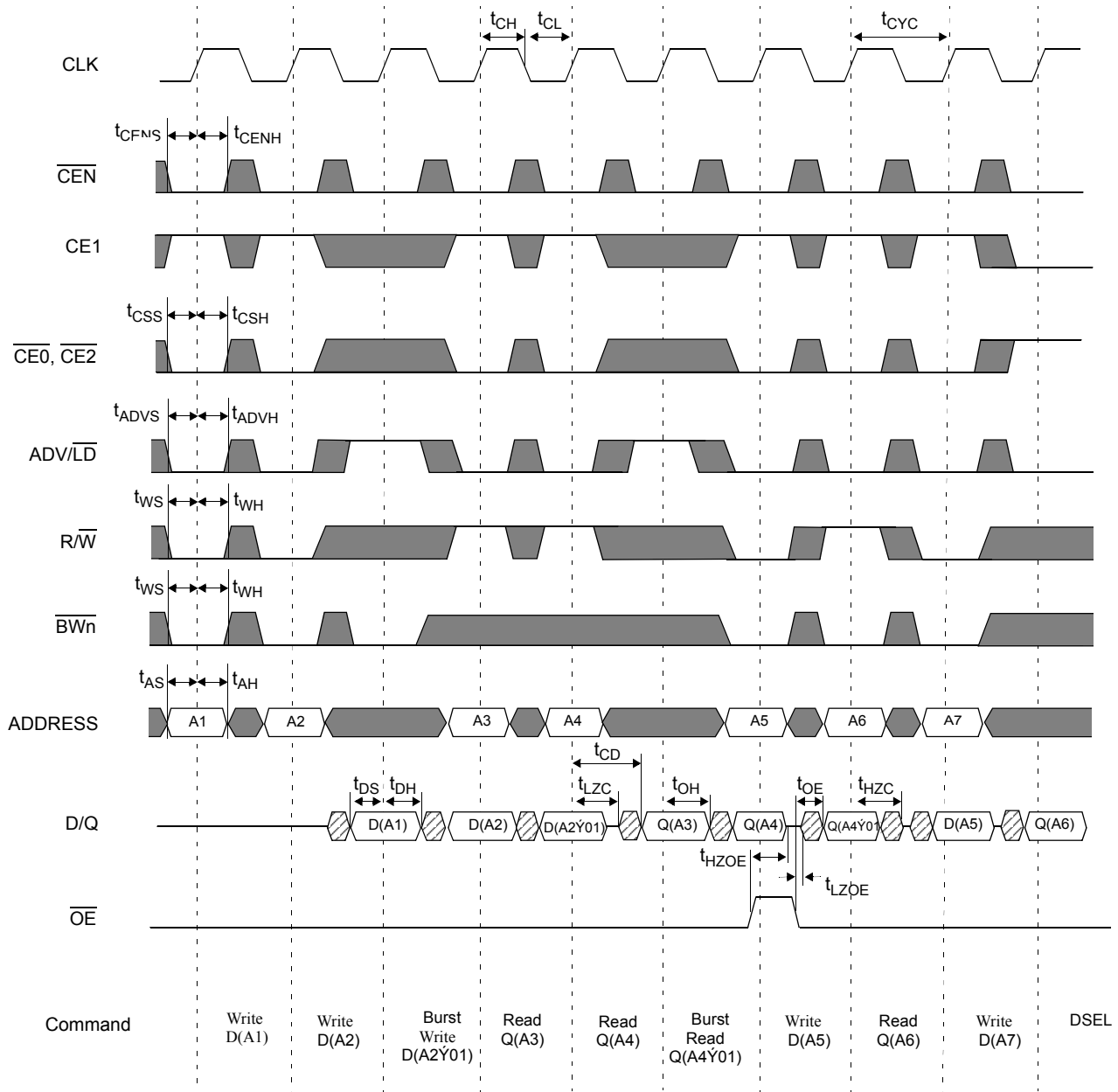


Timing waveform of write cycle





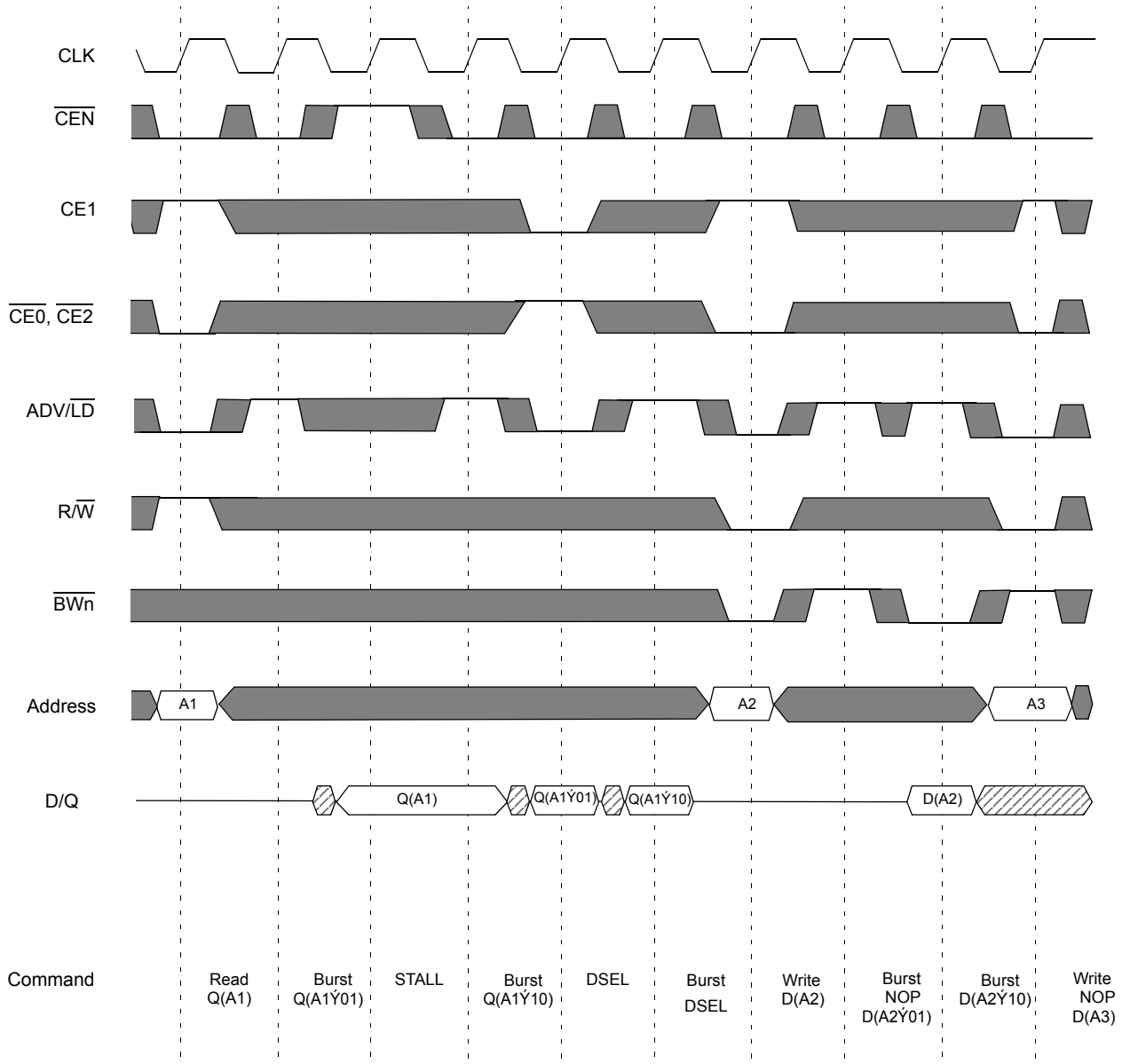
Timing waveform of read/write cycle



Note: \dot{Y} = XOR when \overline{LBO} = high/no connect. \dot{Y} = ADD when \overline{LBO} = low. $\overline{BW[a:d]}$ is don't care.



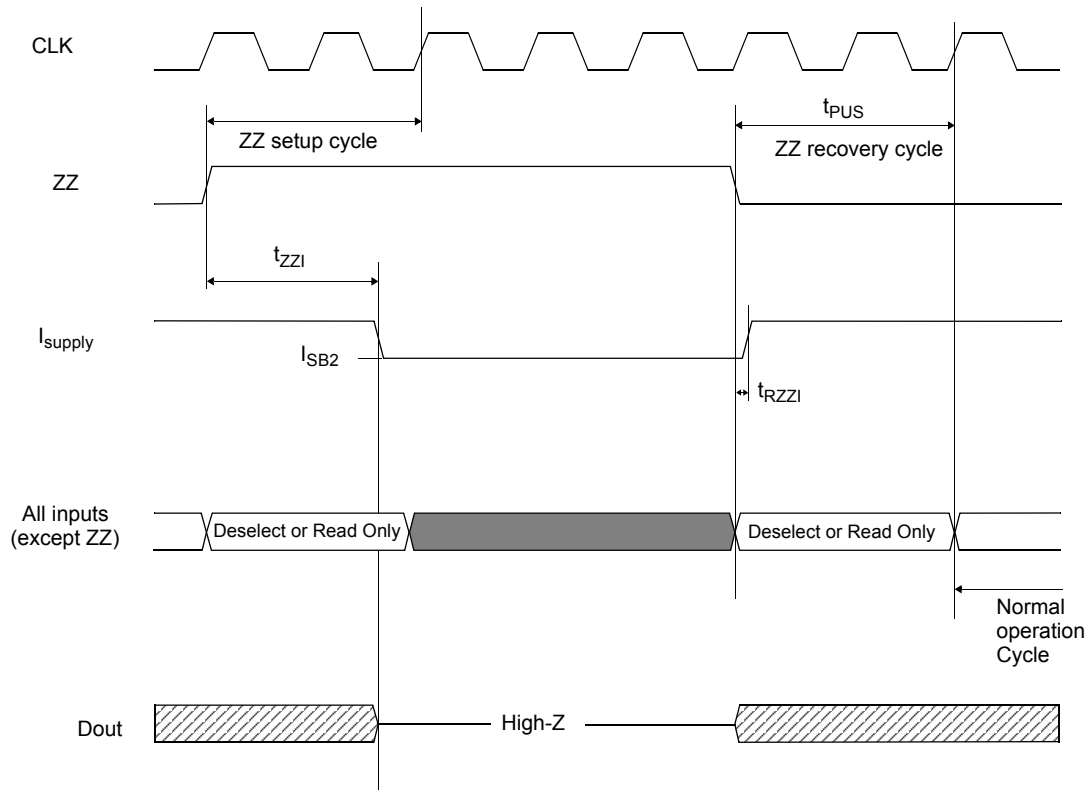
NOP, stall and deselect cycles



Note: \dot{Y} = XOR when \overline{LBO} = high/no connect; \dot{Y} = ADD when \overline{LBO} = low. \overline{OE} is low.



Timing waveform of snooze mode





AC test conditions

- Output load: For t_{LZC} , t_{LZOE} , t_{HZOE} , and t_{HZC} , see Figure C. For all others, see Figure B.
- Input pulse level: GND to 3V. See Figure A.
- Input rise and fall time (measured at 0.3V and 2.7V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

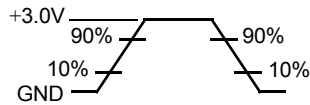


Figure A: Input waveform

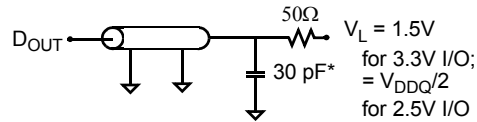


Figure B: Output load (A)

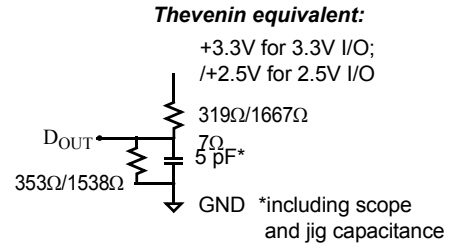


Figure C: Output load(B)

Notes

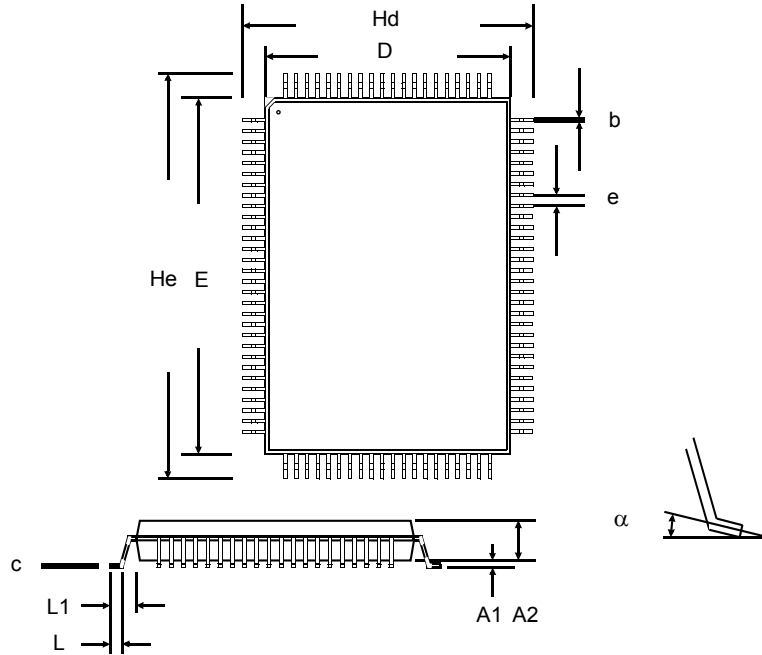
- 1) For test conditions, see “AC test conditions”, Figures A, B, and C
- 2) This parameter measured with output load condition in Figure C.
- 3) This parameter is sampled, but not 100% tested.
- 4) t_{HZOE} is less than t_{LZOE} , and t_{HZC} is less than t_{LZC} at any given temperature and voltage.
- 5) t_{CH} is measured high above V_{IH} , and t_{CL} is measured low below V_{IL}
- 6) This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of CLK when chip is enabled.
- 7) Write refers to $\overline{R/W}$ and $\overline{BW[a,b,c,d]}$.
- 8) Chip select refers to $\overline{CE0}$, CE1, and $\overline{CE2}$.



Package dimensions

100-pin quad flat pack (TQFP)

| | TQFP | |
|---------------------------|--------------|-------|
| | Min | Max |
| A1 | 0.05 | 0.15 |
| A2 | 1.35 | 1.45 |
| b | 0.22 | 0.38 |
| c | 0.09 | 0.20 |
| D | 13.90 | 14.10 |
| E | 19.90 | 20.10 |
| e | 0.65 nominal | |
| Hd | 15.90 | 16.10 |
| He | 21.90 | 22.10 |
| L | 0.45 | 0.75 |
| L1 | 1.00 nominal | |
| α | 0° | 7° |
| Dimensions in millimeters | | |





Ordering information

| Package & Width | -200 MHz | -166 MHz | -133 MHz |
|-----------------|-----------------------|-----------------------|-----------------------|
| TQFP x32 | AS7C331MNTD32A-200TQC | AS7C331MNTD32A-166TQC | AS7C331MNTD32A-133TQC |
| | AS7C331MNTD32A-200TQI | AS7C331MNTD32A-166TQI | AS7C331MNTD32A-133TQI |
| TQFP x36 | AS7C331MNTD36A-200TQC | AS7C331MNTD36A-166TQC | AS7C331MNTD36A-133TQC |
| | AS7C331MNTD36A-200TQI | AS7C331MNTD36A-166TQI | AS7C331MNTD36A-133TQI |

Note:

Add suffix 'N' to the above part number for Lead Free Parts (Ex. AS7C331MNTD32A-200TQCN)

Part numbering guide

| AS7C | 33 | 1M | NTD | 32/36 | A | -XXX | TQ | C/I | X |
|------|----|----|-----|-------|---|------|----|-----|----|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |

- Alliance Semiconductor SRAM prefix
- Operating voltage: 33 = 3.3V
- Organization: 1M = 1M
- NTD™ = No Turn-Around Delay. Pipelined mode
- Organization: 32 = x 32, 36 = x 36
- Production version: A = first production version
- Clock speed (MHz)
- Package type: TQ = TQFP
- Operating temperature: C = commercial (0° C to 70° C); I = industrial (-40° C to 85° C)
- N = Lead Free Part



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Part Number: AS7C331MNTD32A /
AS7C331MNTD36A

Document Version: V 1.6

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