RENESAS

HN58V65AI Series
HN58V66AI Series
HN58V65A-SR Series
HN58V66A-SR Series

64k EEPROM (8-kword × 8-bit)
Ready/$\overline{\text{Busy}}$ function, $\overline{\text{RES}}$ function (HN58V66A)
Wide Temperature Range version

Description

Renesas Technology's HN58V65A series and HN58V66A series are electrically erasable and programmable EEPROM's organized as 8192-word × 8-bit. They have realized high speed, low power consumption and high reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology. They also have a 64-byte page programming function to make their write operations faster.

Features

- Single supply: 2.7 to 5.5 V
- Access time:
  — 100 ns (max) at 2.7 V ≤ V_{CC} < 4.5 V
  — 70 ns (max) at 4.5 V ≤ V_{CC} ≤ 5.5 V
- Power dissipation:
  — Active: 20 mW/MHz (typ)
  — Standby: 110 μW (max)
- On-chip latches: address, data, $\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$
- Automatic byte write: 10 ms (max)
- Automatic page write (64 bytes): 10 ms (max)
- Ready/$\overline{\text{Busy}}$
- Data polling and Toggle bit
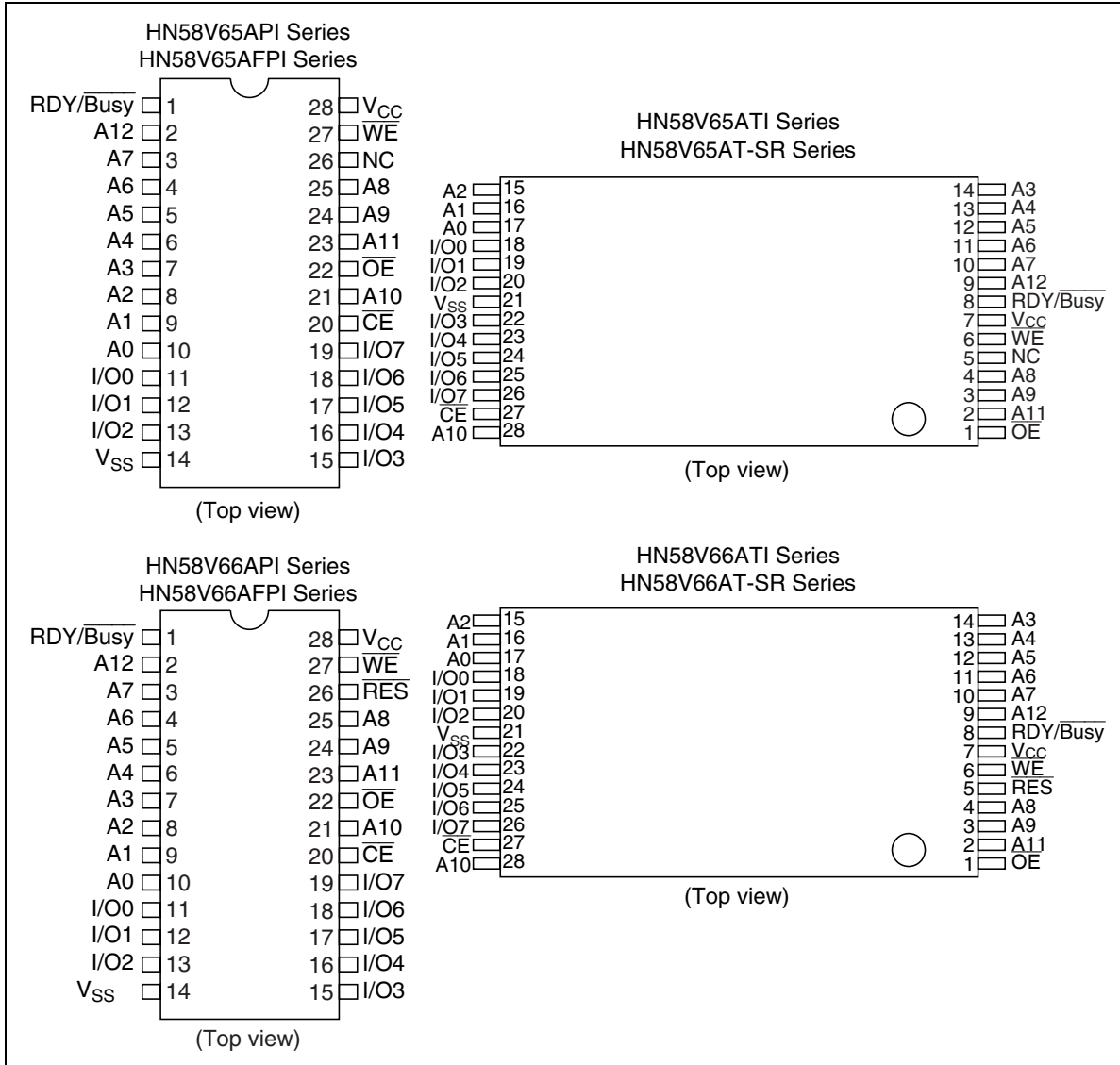- Data protection circuit on power on/off

RENESAS

Features (cont)

- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by $\overline{\text{RES}}$ pin (only the HN58V66A series)
- Operating temperature range:
    - HN58V65AI/HN58V66AI Series: −40 to +85°C
    - HN58V65A-SR/HN58V66A-SR Series: −20 to +85°C
- There are also lead free products.

Ordering Information

Type No.	Access time		Package
	2.7 V ≤ V_{CC} < 4.5 V	4.5 V ≤ V_{CC} ≤ 5.5 V	
HN58V65API-10	100 ns	70 ns	600 mil 28-pin plastic DIP (DP-28)
HN58V66API-10	100 ns	70 ns	
HN58V65AFPI-10	100 ns	70 ns	400 mil 28-pin plastic SOP (FP-28D)
HN58V66AFPI-10	100 ns	70 ns	
HN58V65ATI-10	100 ns	70 ns	28-pin plastic TSOP(TFP-28DB)
HN58V66ATI-10	100 ns	70 ns	
HN58V65AT-10SR	100 ns	70 ns	
HN58V66AT-10SR	100 ns	70 ns	
HN58V65API-10E	100 ns	70 ns	600 mil 28-pin plastic DIP (DP-28V)
HN58V66API-10E	100 ns	70 ns	Lead free
HN58V65AFPI-10E	100 ns	70 ns	400 mil 28-pin plastic SOP (FP-28DV)
HN58V66AFPI-10E	100 ns	70 ns	Lead free
HN58V65ATI-10E	100 ns	70 ns	28-pin plastic TSOP(TFP-28DBV)
HN58V66ATI-10E	100 ns	70 ns	Lead free
HN58V65AT-10SRE	100 ns	70 ns	
HN58V66AT-10SRE	100 ns	70 ns	

Pin Arrangement

HN58V65API Series
HN58V65AFPI Series

Pin		Pin	
RDY/$\overline{\text{Busy}}$	1	28	V$_{CC}$
A12	2	27	$\overline{\text{WE}}$
A7	3	26	NC
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	$\overline{\text{OE}}$
A2	8	21	A10
A1	9	20	$\overline{\text{CE}}$
A0	10	19	I/O7
I/O0	11	18	I/O6
I/O1	12	17	I/O5
I/O2	13	16	I/O4
V$_{SS}$	14	15	I/O3

(Top view)

HN58V65ATI Series
HN58V65AT-SR Series

A2	15	14	A3
A1	16	13	A4
A0	17	12	A5
I/O0	18	11	A6
I/O1	19	10	A7
I/O2	20	9	A12
V$_{SS}$	21	8	RDY/$\overline{\text{Busy}}$
I/O3	22	7	V$_{CC}$
I/O4	23	6	$\overline{\text{WE}}$
I/O5	24	5	NC
I/O6	25	4	A8
I/O7	26	3	A9
$\overline{\text{CE}}$	27	2	A11
A10	28	1	$\overline{\text{OE}}$

(Top view)

HN58V66API Series
HN58V66AFPI Series

Pin		Pin	
RDY/$\overline{\text{Busy}}$	1	28	V$_{CC}$
A12	2	27	$\overline{\text{WE}}$
A7	3	26	$\overline{\text{RES}}$
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	$\overline{\text{OE}}$
A2	8	21	A10
A1	9	20	$\overline{\text{CE}}$
A0	10	19	I/O7
I/O0	11	18	I/O6
I/O1	12	17	I/O5
I/O2	13	16	I/O4
V$_{SS}$	14	15	I/O3

(Top view)

HN58V66ATI Series
HN58V66AT-SR Series

A2	15	14	A3
A1	16	13	A4
A0	17	12	A5
I/O0	18	11	A6
I/O1	19	10	A7
I/O2	20	9	A12
V$_{SS}$	21	8	RDY/$\overline{\text{Busy}}$
I/O3	22	7	V$_{CC}$
I/O4	23	6	$\overline{\text{WE}}$
I/O5	24	5	$\overline{\text{RES}}$
I/O6	25	4	A8
I/O7	26	3	A9
$\overline{\text{CE}}$	27	2	A11
A10	28	1	$\overline{\text{OE}}$

(Top view)

RENESAS

Pin Description

Pin name	Function
A0 to A12	Address input
I/O0 to I/O7	Data input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground
RDY/$\overline{Busy}$	Ready busy
$\overline{RES}$*1	Reset
NC	No connection

Note: 1. This function is supported by only the HN58V66A series.

Block Diagram

Note: 1. This function is supported by only the HN58V66A series.
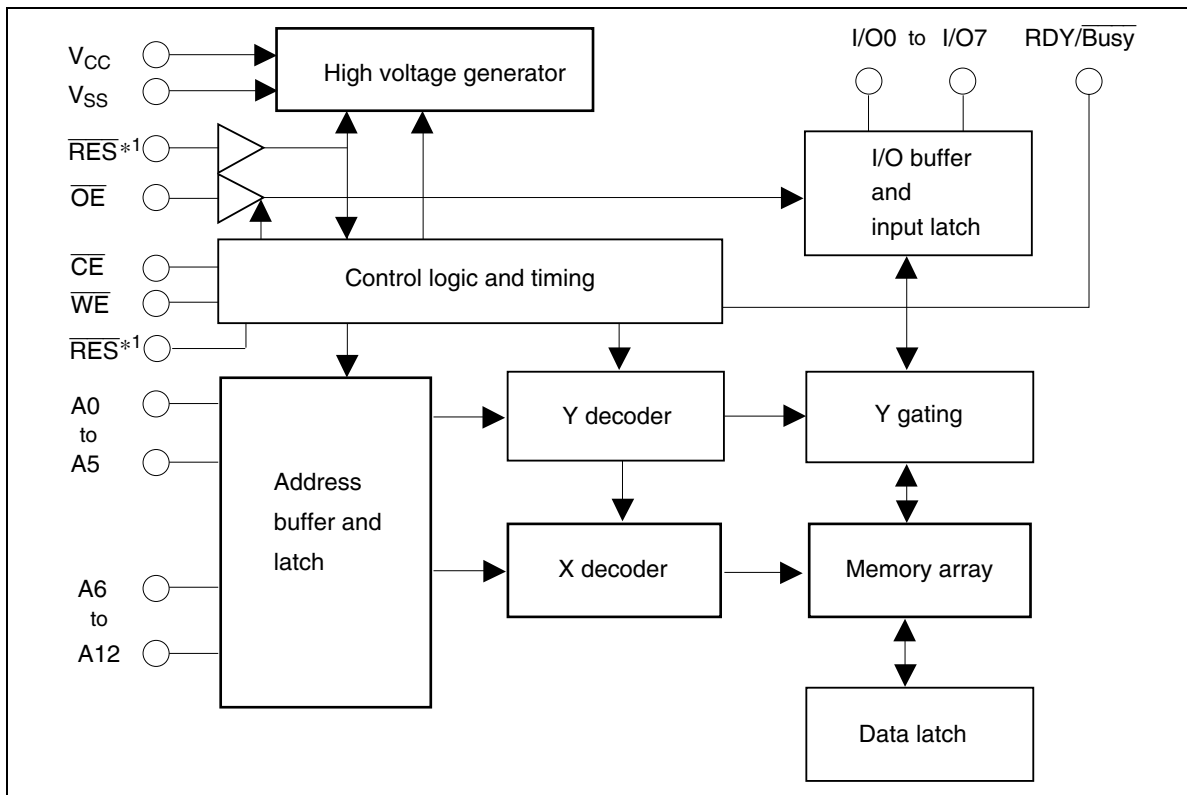
Operation Table

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$*3	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H*1	High-Z	Dout
Standby	V_{IH}	×*2	×	×	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	×	×	V_{IH}	×	—	—
	×	V_{IL}	×	×	—	—
$\overline{Data\ Polling}$	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Dout (I/O7)
Program reset	×	×	×	V_{IL}	High-Z	High-Z

Notes: 1. Refer to the recommended DC operating conditions.

2. × : Don't care

3. This function supported by only the HN58V66A series.

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Power supply voltage relative to V_{SS}		V_{CC}	−0.6 to +7.0	V
Input voltage relative to V_{SS}		Vin	−0.5*1 to +7.0*3	V
Operating temperature range *2	HN58V65AI/HN58V66AI	Topr	−40 to +85	°C
	HN58V65A-SR/HN58V66A-SR	Topr	−20 to +85	°C
Storage temperature range		Tstg	−55 to +125	°C

Notes: 1. Vin min : −3.0 V for pulse width ≤ 50 ns.

2. Including electrical characteristics and data retention.

3. Should not exceed V_{CC} + 1 V.

RENESAS

Recommended DC Operating Conditions

Parameter	Symbol		Min	Typ	Max	Unit
Supply voltage	V_{CC}		2.7	—	5.5	V
	V_{SS}		0	0	0	V
Input voltage	V_{IL}		$-0.3*^1$	—	$0.6*^5$	V
	V_{IH}		$2.4*^2$	—	$V_{CC} + 0.3*^3$	V
	V_H*^4		$V_{CC} - 0.5$	—	$V_{CC} + 1.0$	V
Operating temperature Topr		HN58V65AI/HN58V66AI	−40	—	+85	°C
		HN58V65A-SR/HN58V66A-SR	−20	—	+85	°C

Notes: 1. V_{IL} min: −1.0 V for pulse width ≤ 50 ns.
2. V_{IH} = 3.0 V for V_{CC} = 3.6 to 5.5 V.
3. V_{IH} max: V_{CC} + 1.0 V for pulse width ≤ 50 ns.
4. This function is supported by only the HN58V66A series.
5. V_{IL} = 0.8 V for V_{CC} = 3.6 V to 5.5 V

DC Characteristics

(Ta = −40 to +85°C, V_{CC} = 2.7 to 5.5 V: HN58V66AI/HN58V66AI,
Ta = −20 to +85°C, V_{CC} = 2.7 to 5.5 V: HN58V66A-SR/HN58V66A-SR)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	$2*^1$	µA	V_{CC} = 5.5 V, Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
Standby V_{CC} current	I_{CC1}	—	1 to 2	5	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} current	I_{CC3}	—	—	6	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 3.6 V
		—	—	10	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 5.5 V
		—	—	15	mA	Iout = 0 mA, Duty = 100%, Cycle = 100 ns at V_{CC} = 3.6 V
		—	—	25	mA	Iout = 0 mA, Duty = 100%, Cycle = 70 ns at V_{CC} = 5.5 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	$V_{CC} \times 0.8$	—	—	V	I_{OH} = −400 µA

Note: 1. I_{LI} on $\overline{RES}$: 100 µA max (only the HN58V66A series)

RENESAS

Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin*[1]	—	—	6	pF	Vin = 0 V
Output capacitance	Cout*[1]	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics

(Ta = −40 to +85°C, V_{CC} = 2.7 to 5.5 V: HN58V65AI/HN58V66AI,
Ta = −20 to +85°C, V_{CC} = 2.7 to 5.5 V: HN58V65A-SR/HN58V66A-SR)

Test Conditions

- Input pulse levels : 0.4 V to 2.4 V (V_{CC} = 2.7 to 3.6 V), 0.4 V to 3.0 V (V_{CC} = 3.6 to 5.5 V)
  0 V to V_{CC} ($\overline{RES}$ pin*[2])
- Input rise and fall time : ≤ 5 ns
- Input timing reference levels : 0.8, 1.8 V
- Output load : 1TTL Gate +100 pF
- Output reference levels : 1.5 V, 1.5 V

Read Cycle 1 ($2.7 \leq V_{CC} < 4.5$ V)

Parameter	Symbol	HN58V65AI/HN58V66AI HN58V65A-SR/HN58V66A-SR -10 Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	100	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{CE}$ to output delay	t_{CE}	—	100	ns	$\overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{OE}$ to output delay	t_{OE}	10	50	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$
Address to output hold	t_{OH}	0	—	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{OE}$ ($\overline{CE}$) high to output float*[1]	t_{DF}	0	40	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{RES}$ low to output float*[1, 2]	t_{DFR}	0	350	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{RES}$ to output delay*[2]	t_{RR}	0	450	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$

RENESAS

Write Cycle 1 $(2.7 \leq V_{CC} < 4.5 \text{ V})$

Parameter	Symbol	Min*3	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	50	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	50	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	200	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	200	—	—	ns	
Data latch time	t_{DL}	100	—	—	ns	
Byte load cycle	t_{BLC}	0.3	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10*4	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	0*5	—	—	ns	
Reset protect time*2	t_{RP}	100	—	—	µs	
Reset high time*2, 6	t_{RES}	1	—	—	µs	

Notes: 1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
2. This function is supported by only the HN58V66A series.
3. Use this device in longer cycle than this value.
4. t_{WC} must be longer than this value unless polling techniques or RDY/$\overline{Busy}$ are used. This device automatically completes the internal write operation within this value.
5. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/$\overline{Busy}$ are used.
6. This parameter is sampled and not 100% tested.
7. A6 through A12 are page addresses and these addresses are latched at the first falling edge of $\overline{WE}$.
8. A6 through A12 are page addresses and these addresses are latched at the first falling edge of $\overline{CE}$.
9. See AC read characteristics.

RENESAS

Read Cycle 2 ($4.5 \leq V_{CC} \leq 5.5$ V)

| Parameter | Symbol | HN58V65AI/HN58V66AI HN58V65A-SR/HN58V66A-SR | | Unit | Test conditions |
| | | -10 | | | |
		Min	Max		
Address to output delay	t_{ACC}	—	70	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{CE}$ to output delay	t_{CE}	—	70	ns	$\overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{OE}$ to output delay	t_{OE}	10	40	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$
Address to output hold	t_{OH}	0	—	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{OE}$ ($\overline{CE}$) high to output float*[1]	t_{DF}	0	30	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{RES}$ low to output float*[1, 2]	t_{DFR}	0	350	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{RES}$ to output delay*[2]	t_{RR}	0	450	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$

RENESAS

Write Cycle 2 $(4.5 \leq V_{CC} \leq 5.5 \text{ V})$

Parameter	Symbol	Min*[3]	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	50	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	50	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	100	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	100	—	—	ns	
Data latch time	t_{DL}	50	—	—	ns	
Byte load cycle	t_{BLC}	0.2	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10*[4]	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	0*[5]	—	—	ns	
Reset protect time*[2]	t_{RP}	100	—	—	µs	
Reset high time*[2, 6]	t_{RES}	1	—	—	µs	

Notes: 1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.

2. This function is supported by only the HN58V66A.

3. Use this device in longer cycle than this value.

4. t_{WC} must be longer than this value unless polling techniques or RDY/$\overline{Busy}$ are used. This device automatically completes the internal write operation within this value.

5. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/$\overline{Busy}$ are used.

6. This parameter is sampled and not 100% tested.

7. A6 through A12 are page address and these addresses are latched at the first falling edge of $\overline{WE}$.

8. A6 through A12 are page address and these addresses are latched at the first falling edge of $\overline{CE}$.

9. See AC read characteristics.
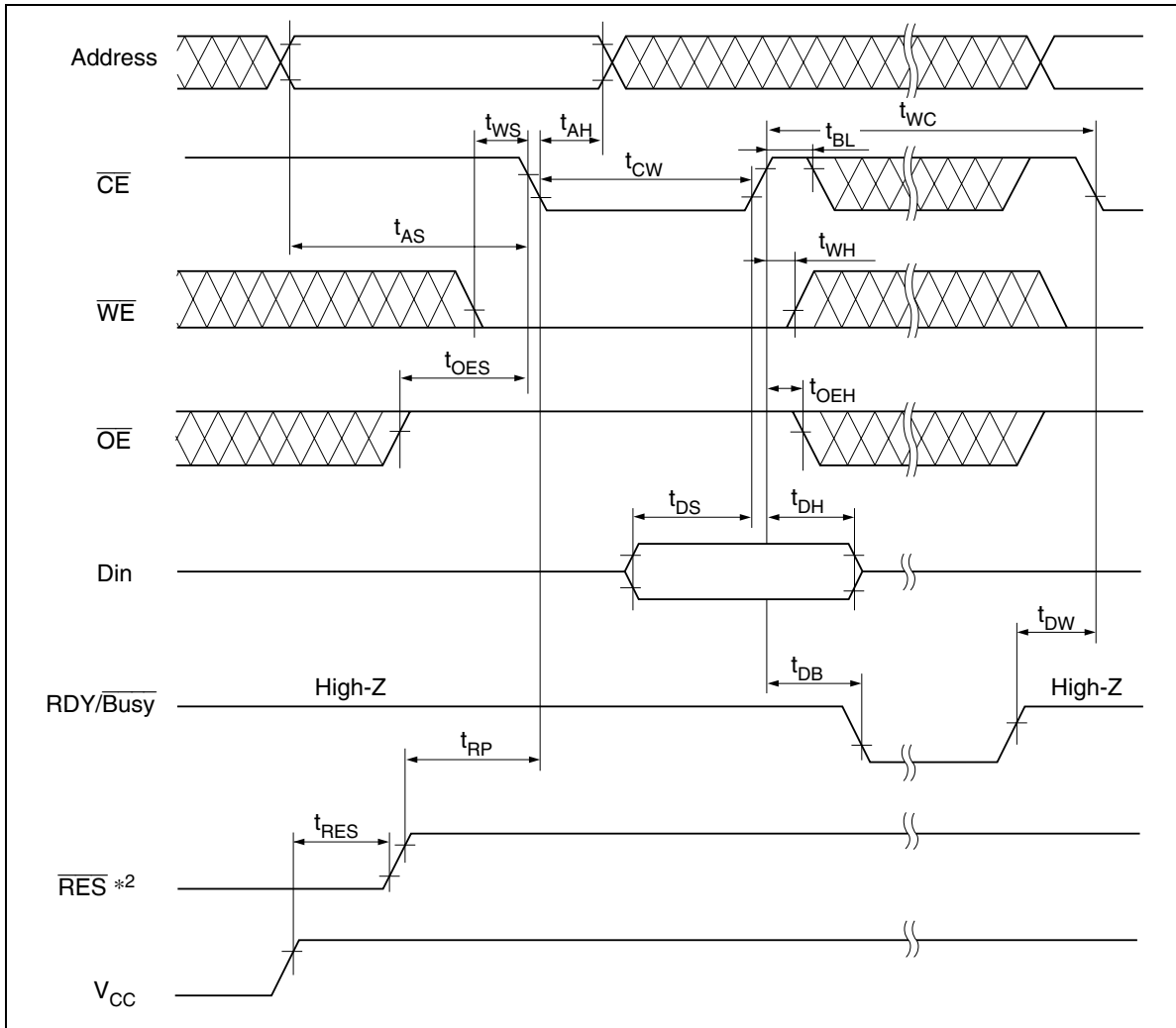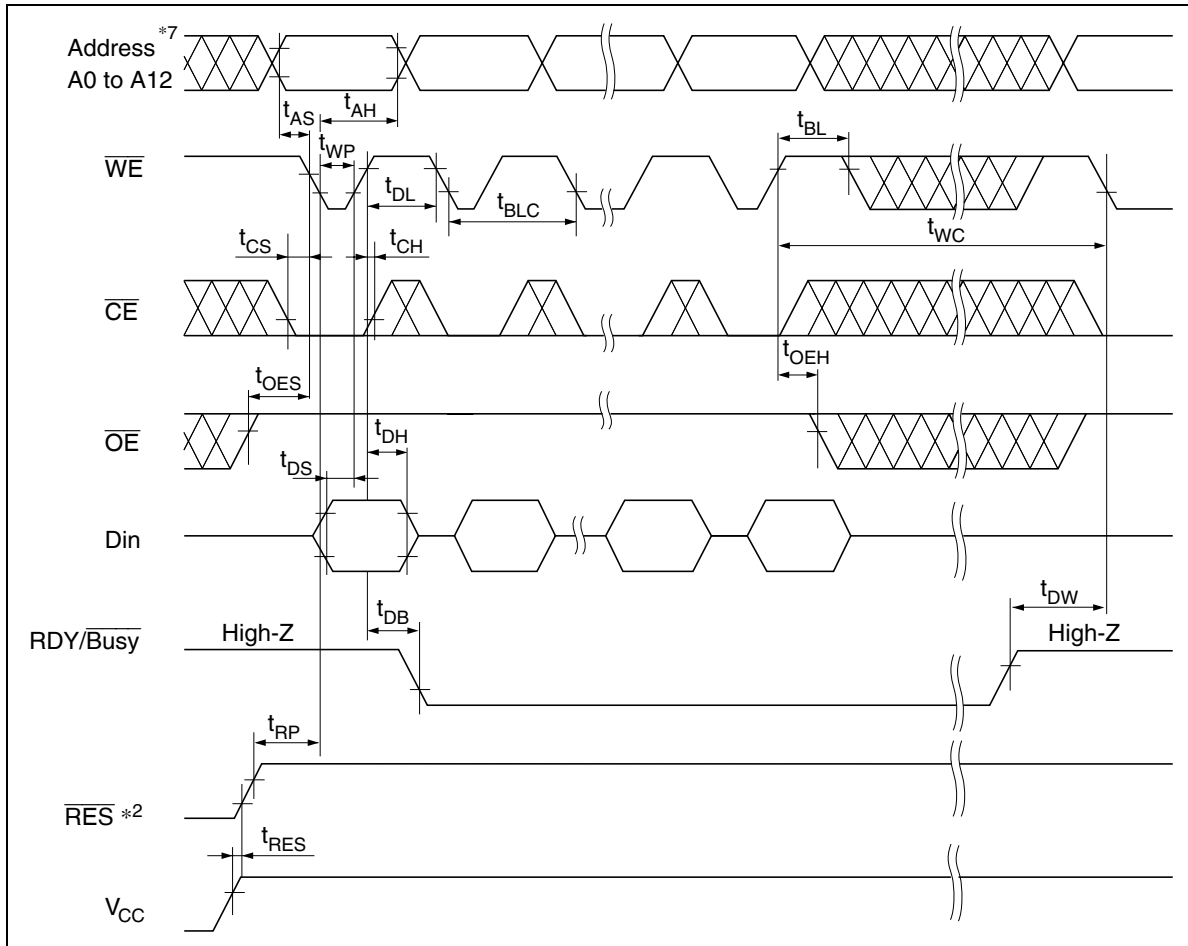
RENESAS

Timing Waveforms

Read Timing Waveform
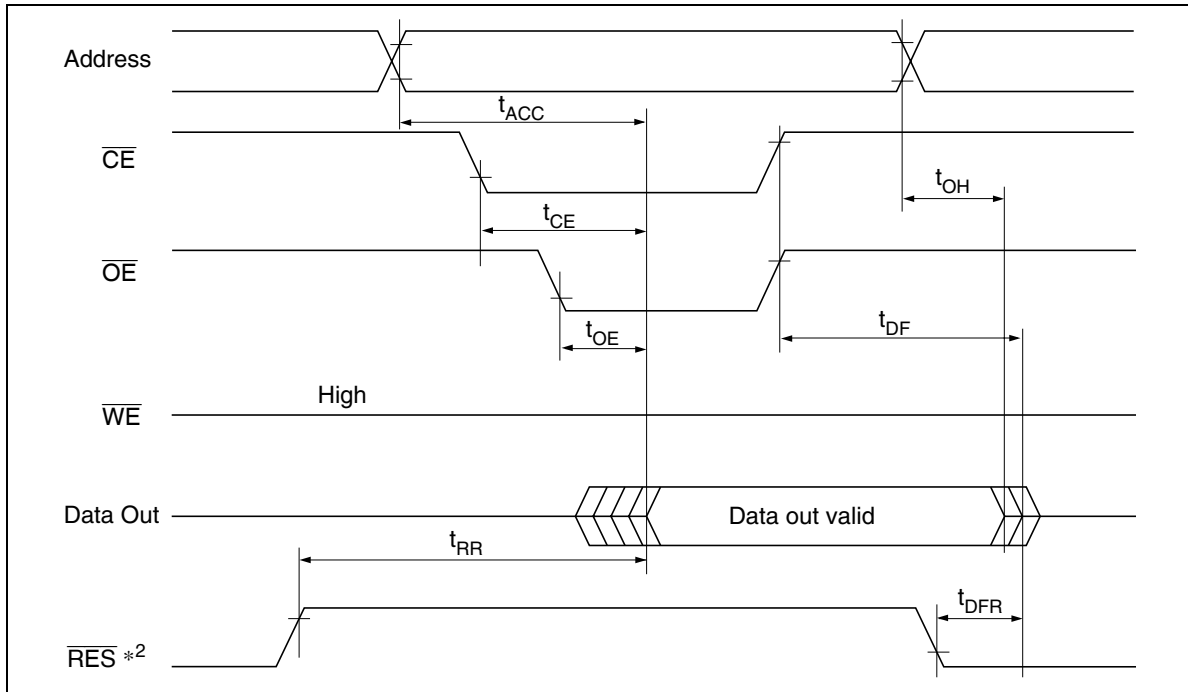
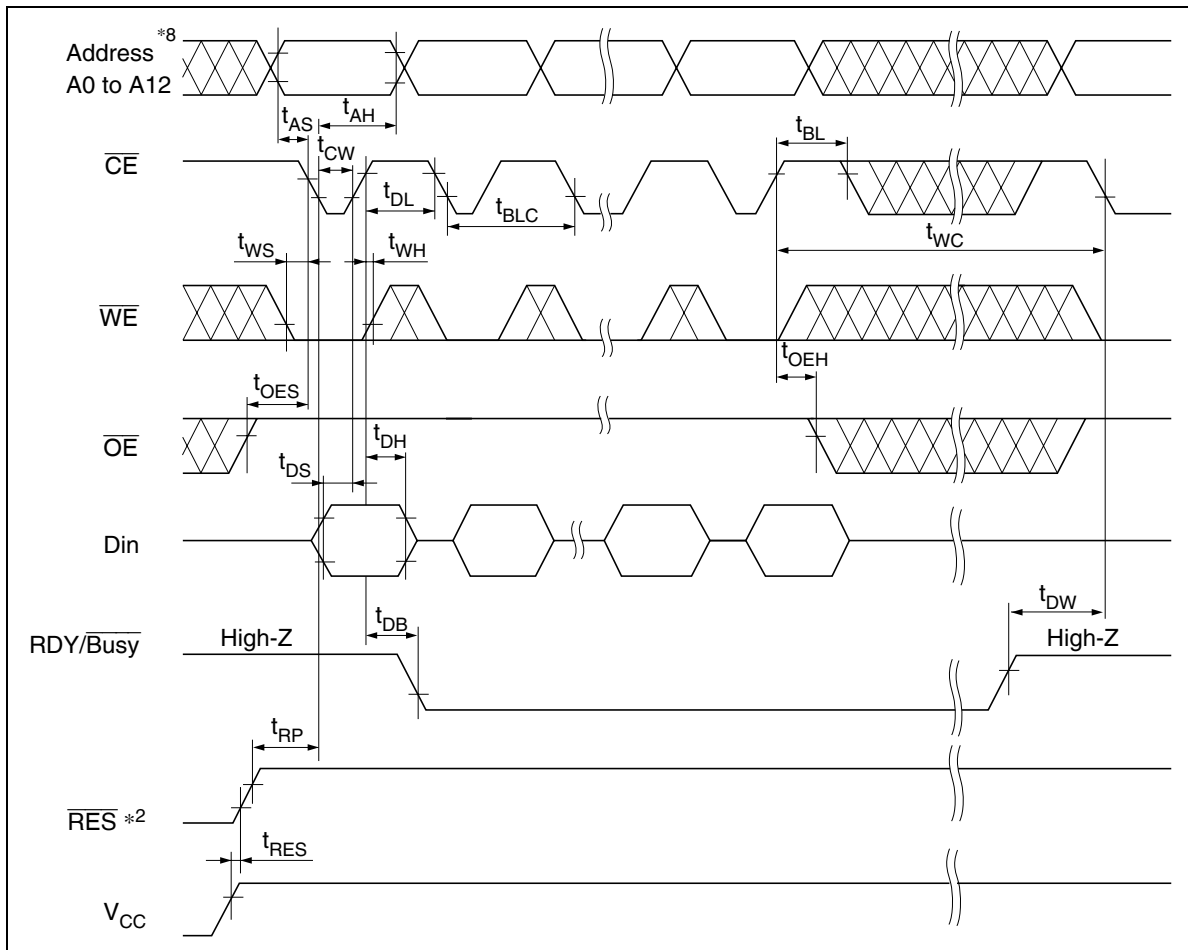## Byte Write Timing Waveform(1) ($\overline{\text{WE}}$ Controlled)
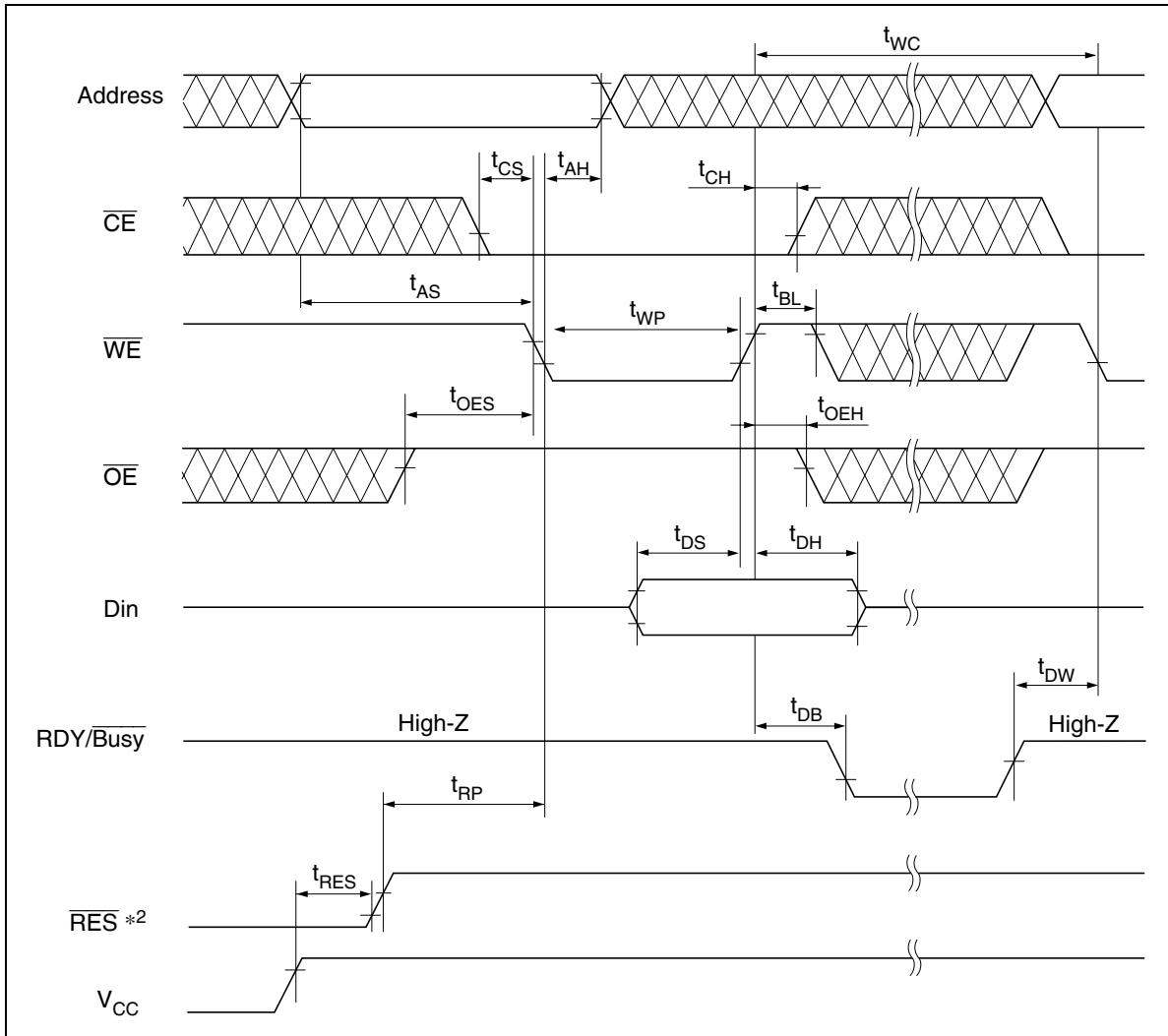
Byte Write Timing Waveform(2) ($\overline{CE}$ Controlled)

Page Write Timing Waveform(1) ($\overline{\text{WE}}$ Controlled)

Page Write Timing Waveform(2) ($\overline{CE}$ Controlled)
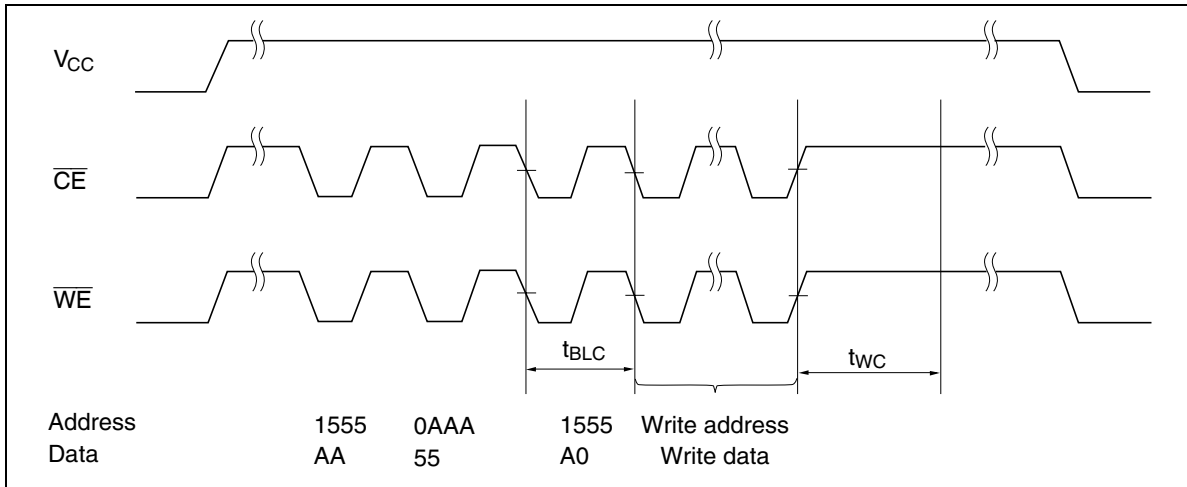
$\overline{\text{Data}}$ Polling Timing Waveform

Toggle Bit

This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from "1" to "0" (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

Toggle Bit Waveform

Notes: 1. I/O6 beginning state is "1".

2. I/O6 ending state will vary.

3. See AC read characteristics.

4. Any address location can be used, but the address must be fixed.
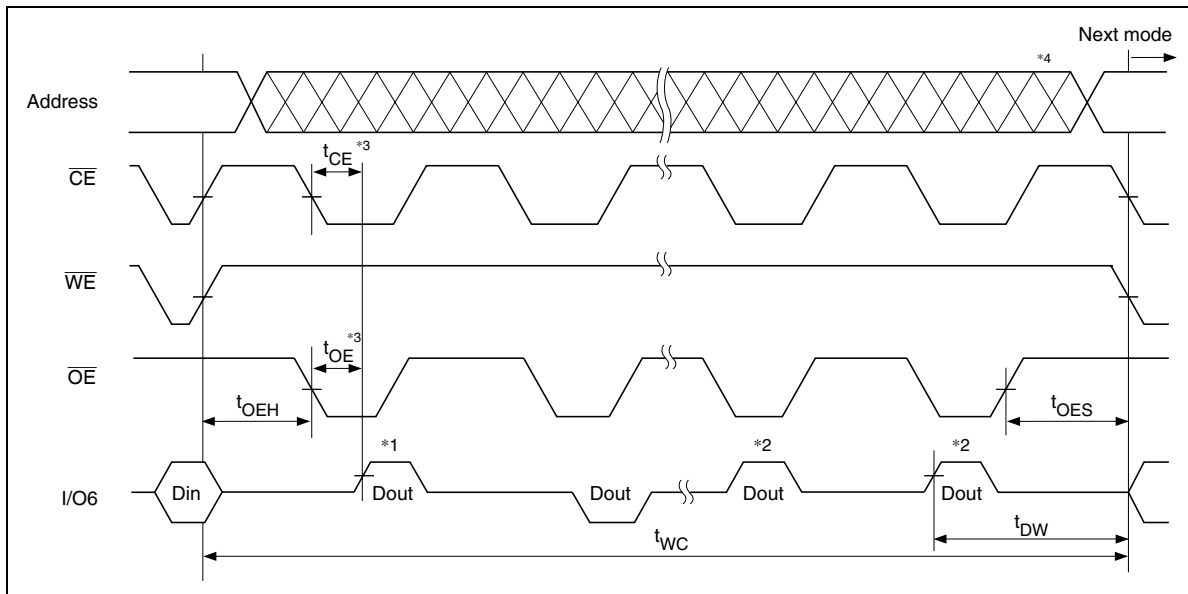
Software Data Protection Timing Waveform(1) (in protection mode)

Software Data Protection Timing Waveform(2) (in non-protection mode)
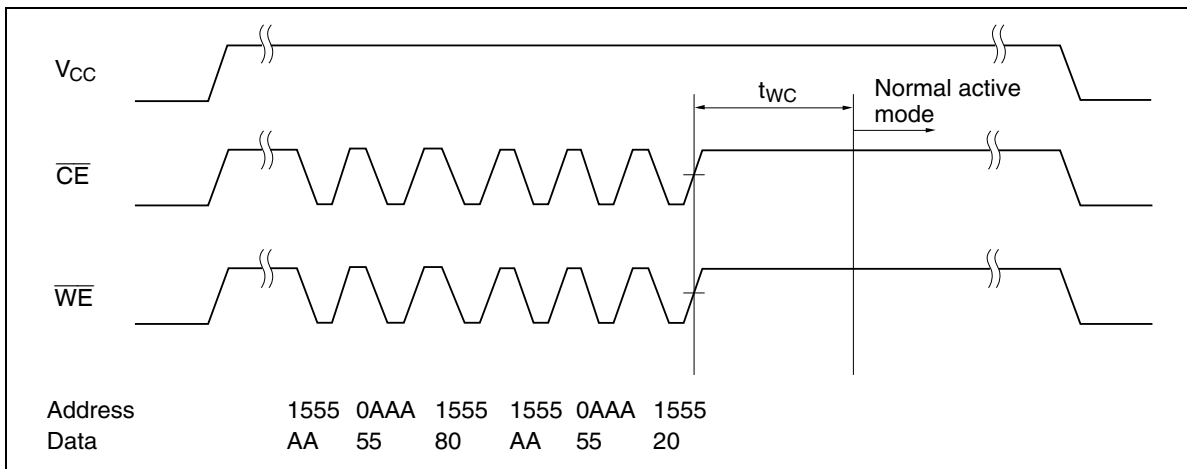
Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 μs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. When $\overline{CE}$ or $\overline{WE}$ is kept high for 100 μs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{Data}$ Polling

$\overline{Data}$ polling indicates the status that the EEPROM is in a write cycle or not. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{Busy}$ Signal

RDY/$\overline{Busy}$ signal also allows status of the EEPROM to be determined. The RDY/$\overline{Busy}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{Busy}$ signal changes state to high impedance.

$\overline{RES}$ Signal (only the HN58V66A series)

When $\overline{RES}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during read and programming because it doesn't provide a latch function.
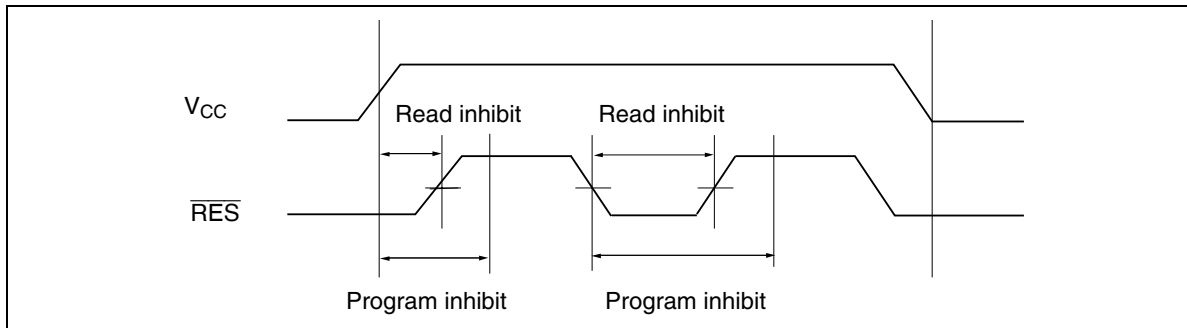
$\overline{\text{WE}}$, $\overline{\text{CE}}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, and data is latched by the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$.

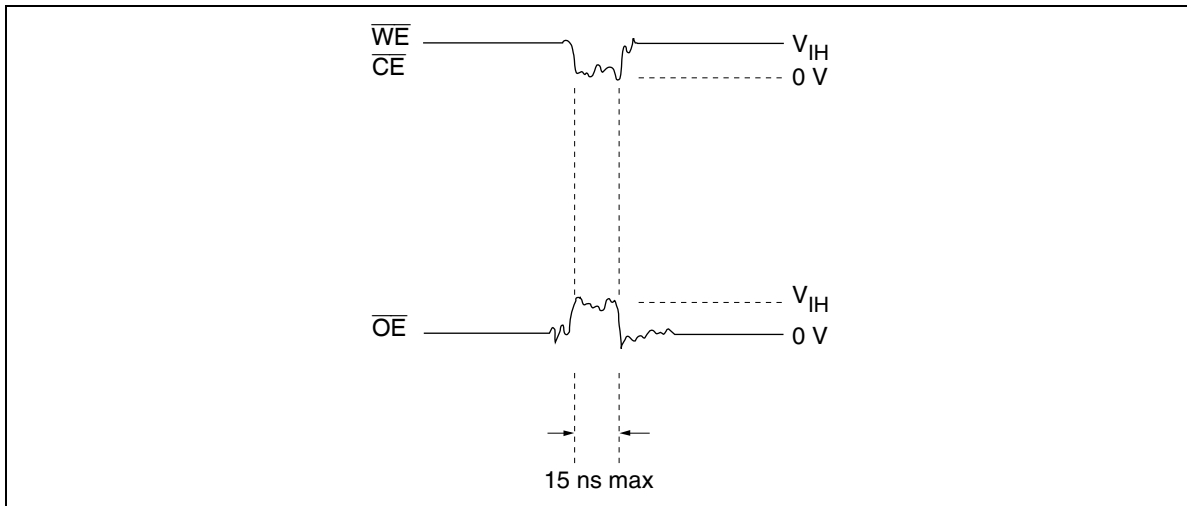### Write/Erase Endurance and Data Retention Time

The endurance is 10^5 cycles in case of the page programming and 10^4 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

Data Protection

To prevent this phenomenon, this device has a noise cancellation function that cuts noise if its width is 15 ns or less.

1. Data Protection against Noise on Control Pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$) during Operation

   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. Be careful not to allow noise of a width of more than 15 ns on the control pins.

2. Data protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

Note: The EEPROM should be kept in unprogrammable state during V_{CC} on/off by using CPU RESET signal.
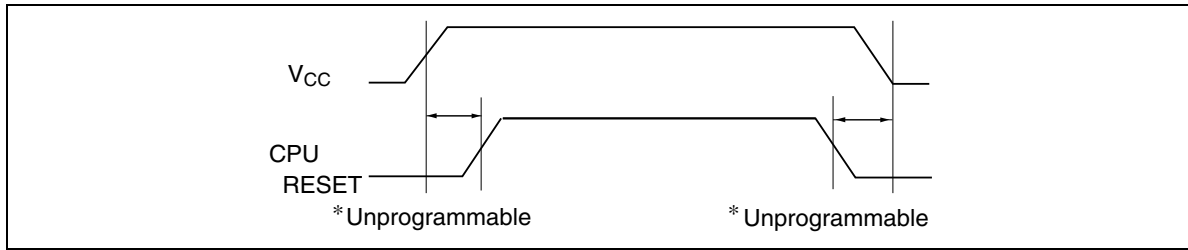
2.1 Protection by $\overline{CE}$, $\overline{OE}$, $\overline{WE}$

To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

$\overline{CE}$	V_{CC}	×	×
$\overline{OE}$	×	V_{SS}	×
$\overline{WE}$	×	×	V_{CC}

×: Don't care.

V_{CC}: Pull-up to V_{CC} level.

V_{SS}: Pull-down to V_{SS} level.

RENESAS

2.2 Protection by $\overline{\text{RES}}$ (only the HN58V66A series)

The unprogrammable state can be realized by that the CPU's reset signal inputs directly to the EEPROM's $\overline{\text{RES}}$ pin. $\overline{\text{RES}}$ should be kept V_{SS} level during V_{CC} on/off. The EEPROM breaks off programming operation when $\overline{\text{RES}}$ becomes low, programming operation doesn't finish correctly in case that $\overline{\text{RES}}$ falls low during programming operation. $\overline{\text{RES}}$ should be kept high for 10 ms after the last data input.
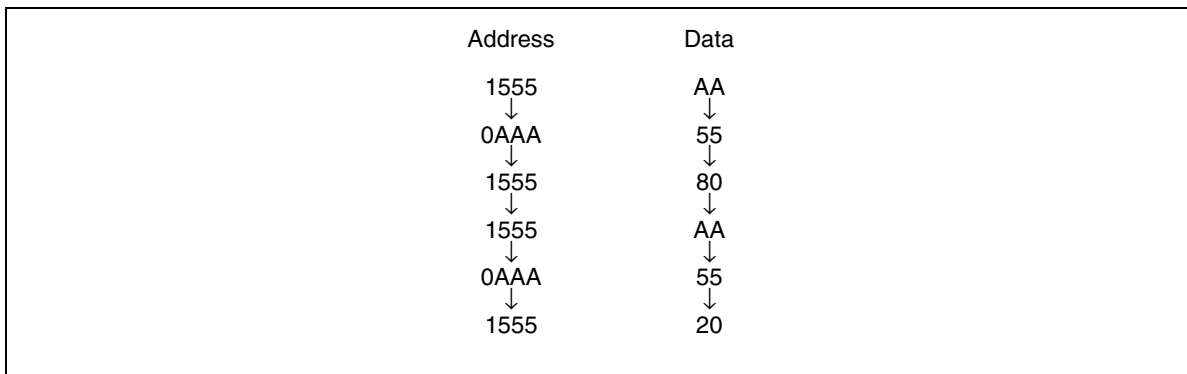
RENESAS
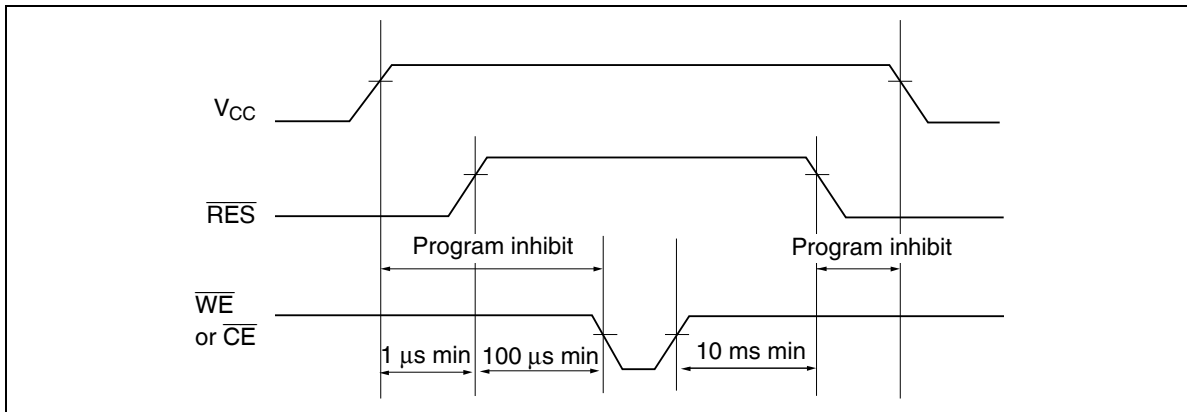
3. Software data protection

To prevent unintentional programming caused by noise generated by external circuits, this device has the software data protection function. In software data protection mode, 3 bytes of data must be input before write data as follows. And these bytes can switch the non-protection mode to the protection mode. SDP is enabled if only the 3 byte code is input.

Address	Data
1555	AA
↓	↓
0AAA	55
↓	↓
1555	A0
↓	↓
Write address	Write data } Normal data input
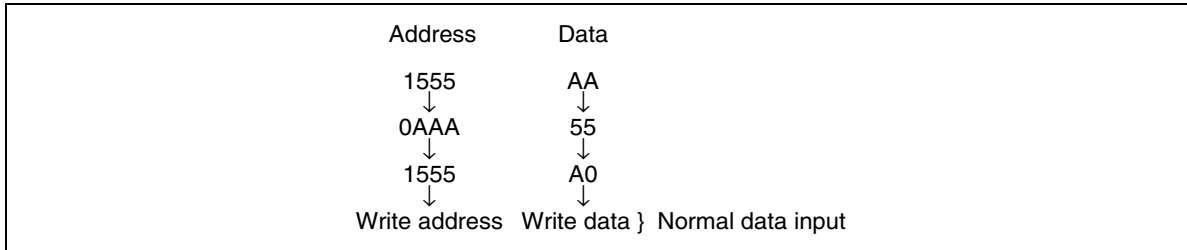
Software data protection mode can be canceled by inputting the following 6 bytes. After that, this device turns to the non-protection mode and can write data normally. But when the data is input in the canceling cycle, the data cannot be written.

Address	Data
1555	AA
↓	↓
0AAA	55
↓	↓
1555	80
↓	↓
1555	AA
↓	↓
0AAA	55
↓	↓
1555	20

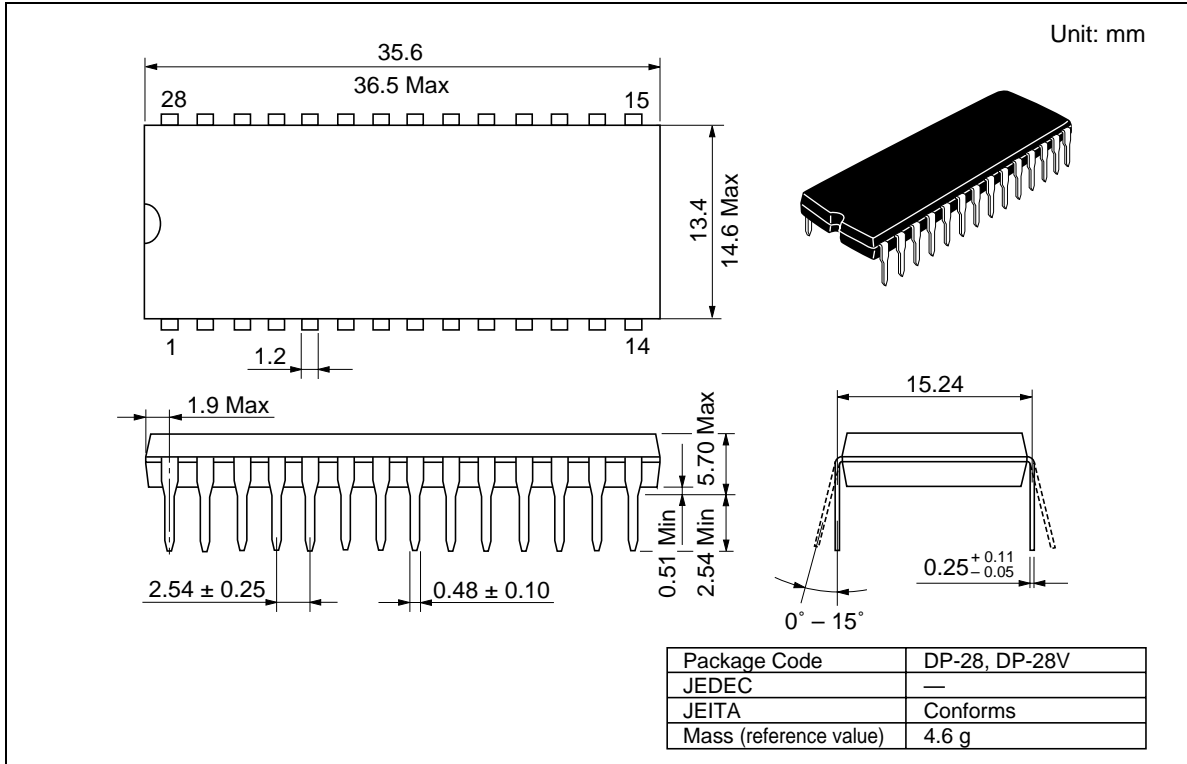The software data protection is not enabled at the shipment.

Note: There are some differences between Renesas Technology's and other company's for enable/disable sequence of software data protection. If there are any questions, please contact with Renesas Technology's sales offices.

RENESAS

Package Dimensions

HN58V65API Series
HN58V66API Series (DP-28, DP-28V)

Unit: mm

35.6
36.5 Max

28   15

13.4
14.6 Max

1   14

1.2

1.9 Max

5.70 Max
0.51 Min
2.54 Min

2.54 ± 0.25   0.48 ± 0.10

15.24

$0.25^{+\,0.11}_{-\,0.05}$

0° − 15°

Package Code	DP-28, DP-28V
JEDEC	—
JEITA	Conforms
Mass (reference value)	4.6 g

RENESAS

Package Dimensions (cont)

HN58V65AFPI Series
HN58V66AFPI Series (FP-28D, FP-28DV)

Unit: mm

Package Code	FP-28D, FP-28DV
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.7 g

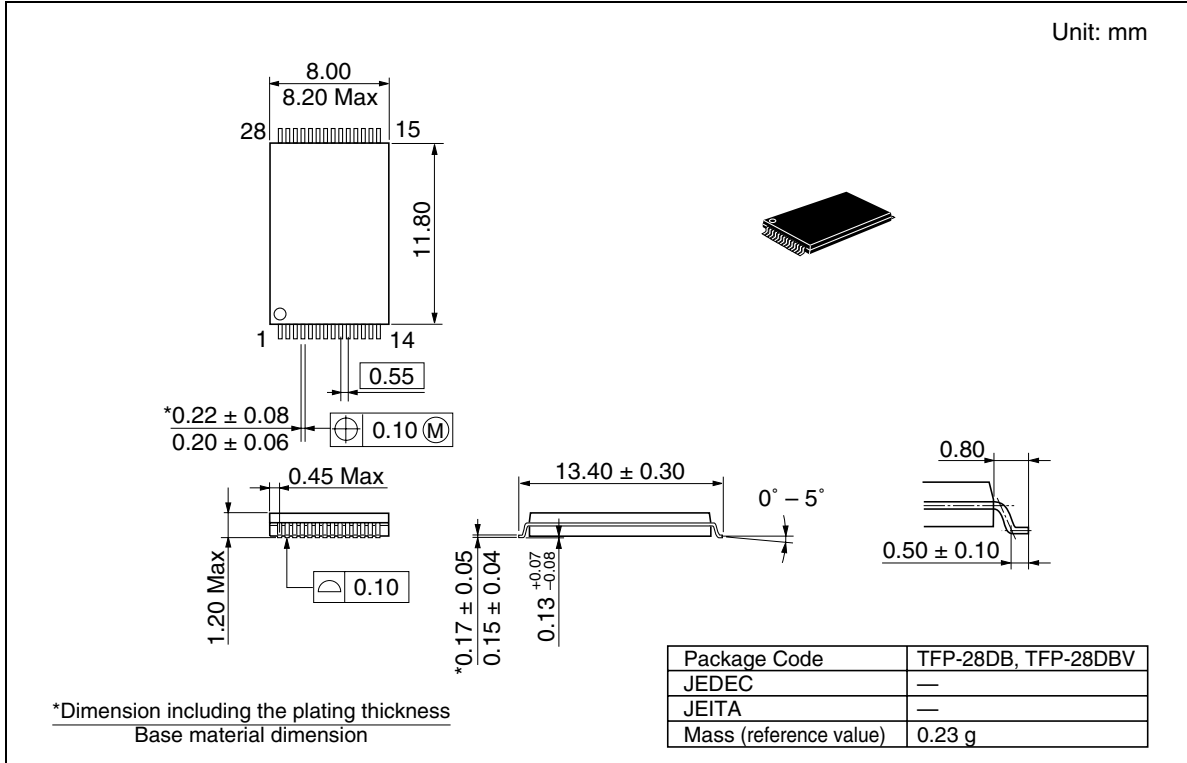*Dimension including the plating thickness
Base material dimension
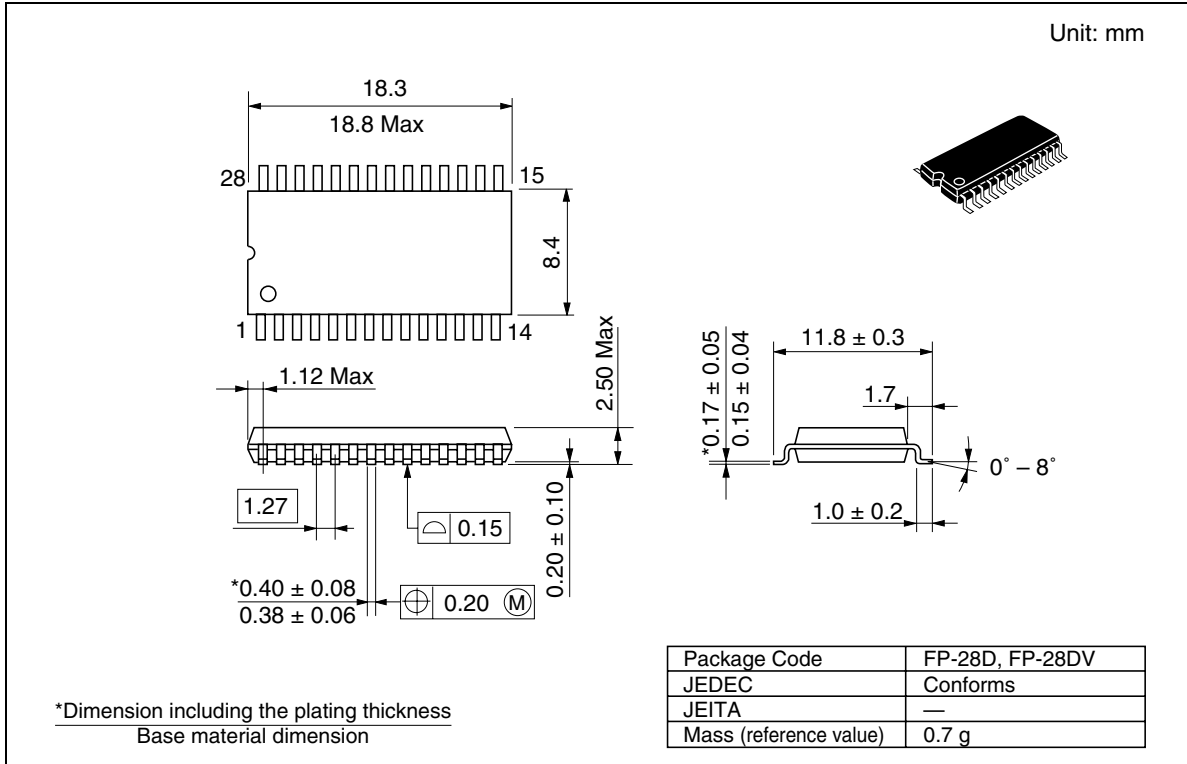
Package Dimensions (cont)

HN58V65ATI Series
HN58V66ATI Series
HN58V65AT-SR Series
HN58V66AT-SR Series (TFP-28DB, TFP-28DBV)

Unit: mm

8.00
8.20 Max

28   15

11.80

1   14

0.55

*0.22 ± 0.08
0.20 ± 0.06

⊕ 0.10 Ⓜ

0.80

0.45 Max

13.40 ± 0.30

0˚ − 5˚

0.50 ± 0.10

1.20 Max

⌒ 0.10

*0.17 ± 0.05
0.15 ± 0.04

0.13 $^{+0.07}_{-0.08}$

Package Code	TFP-28DB, TFP-28DBV
JEDEC	—
JEITA	—
Mass (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension

Rev.3.00, Feb.02.2004, page 26 of 26

RENESAS

Revision History
HN58V65AI/HN58V66AI/HN58V65A-SR/HN58V66A-SR Series Data Sheet

Rev.	Date	Contents of Modification	
		Page	**Description**
0.0	Mar. 12, 1997	—	Initial issue
1.0	Aug. 29, 1997	—	Addition of HN58V65A-SR/HN58V66A-SR
		7	AC Characteristics
			Input pulse level: 0.4 V to V_{CC} to 0 V to V_{CC}
		11	Timing Waveform
			Read Timing Waveform: Correct error
		19	Functional Description
			Data Protection 3.: Addition of description
2.0	Oct. 31, 1997	6	DC Characteristics
			I_{CC3} (max): 6/10/12/25 mA to 6/10/15/25 mA
3.00	Feb. 02, 2004	2	Ordering Information
			Addition of HN58V65API-10E, HN58V66API-10E, HN58V65AFPI-10E, HN58V66AFPI-10E, HN58V65ATI-10E, HN58V66ATI-10E, HN58V65AT-10SRE, HN58V66AT-10SRE
		24-26	Package Dimensions
			DP-28 to DP-28, DP-28V
			FP-28D to FP-28D, FP-28DV
			TFP-28DB to TFP-28DB, TFP-28DBV

RenesasTechnology Corp. Sales Strategic Planning Div.   Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!
1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials
1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.

RENESAS

RENESAS SALES OFFICES

http://www.renesas.com

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH
Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001